LPC47N217

64-Pin Super I/O with LPC Interface

Product Features

- 3.3 Volt Operation (5V tolerant)
- Programmable Wakeup Event Interface (IO_PME# Pin)
- SMI Support (IO_SMI# Pin)
- GPIOs (14)
- Two IRQ Input Pins
- XNOR Chain
- PC99a, PC2001
- ACPI 2.0 Compliant
- 64-pin STQFP RoHS Compliant Package
- Intelligent Auto Power Management
- Serial Ports
  - One Full Function Serial Port
  - High Speed 16C550A Compatible UART with Send/Receive 16-Byte FIFO
  - Supports 230k and 460k Baud
  - Programmable Baud Rate Generator
  - Modem Control Circuitry
- Infrared Communications Controller
  - IrDA v1.2 (4Mbps), HPSIR, ASKIR, Consumer IR Support
  - 1 IR Port
  - 96 Base I/O Address, 15 IRQ Options and 3 DMA Options
- Multi-Mode Parallel Port with ChiProtect™
  - Standard Mode IBM PC/XT, PC/AT, and PS/2 Compatible Bidirectional Parallel Port
  - Enhanced Parallel Port (EPP) Compatible - EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
  - IEEE 1284 Compliant Enhanced Capabilities Port (ECP)
  - ChiProtect Circuitry for Protection Against Damage Due to Printer Power-On
  - 192 Base I/O Address, 15 IRQ and 3 DMA Options
- LPC Bus Host Interface
  - Supports LPC Bus frequencies of 19.2 MHz to 33 MHz
  - Multiplexed Command, Address and Data Bus
  - 8-Bit I/O Transfers
  - 8-Bit DMA Transfers
  - 16-Bit Address Qualification
  - Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
  - PCI CLKRUN# Support
  - Power Management Event (IO_PME#) Interface Pin

Description

The Microchip LPC47N217 is a 3.3V PC 99, PC2001, and ACPI 2.0 compliant Super I/O Controller. The LPC47N217 implements the LPC interface, a pin reduced ISA interface which provides the same or better performance as the ISA/X-bus with a substantial savings in pins used. The part also includes 14 GPIO pins.

The LPC47N217 incorporates a 16C550A compatible UART and one Multi-Mode parallel port with ChiProtect circuitry plus EPP and ECP support. This device also offers a full 16-bit internally decoded address bus, a Serial IRQ interface with PCI CLKRUN# support, relocatable configuration ports, and three DMA channel options.

The on-chip UART is compatible with the 16C550A. There is a dedicated Serial Infrared interface UART, which complies with IrDA v1.2 (Fast IR), HPSIR, and ASKIR formats (used by Sharp and other PDAs), as well as Consumer IR.

The parallel port is compatible with IBM PC/AT architectures, as well as IEEE 1284 EPP and ECP. The parallel port ChiProtect circuitry prevents damage caused by an attached powered printer when the LPC47N217 is not powered.

The LPC47N217 features Software Configurable Logic (SCL) for ease of use. SCL allows programmable system configuration of key functions such as the parallel port and UART.

The LPC47N217 supports the ISA Plug-and-Play Standard register set (Version 1.0a) and provides the recommended functionality to support Windows operating systems, PC99, and PC2001. The I/O Address, DMA Channel, and Hardware IRQ of each device in the LPC47N217 may be reprogrammed through the internal configuration registers. There are multiple I/O address location options, a Serialized IRQ interface, and three DMA channels.

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An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

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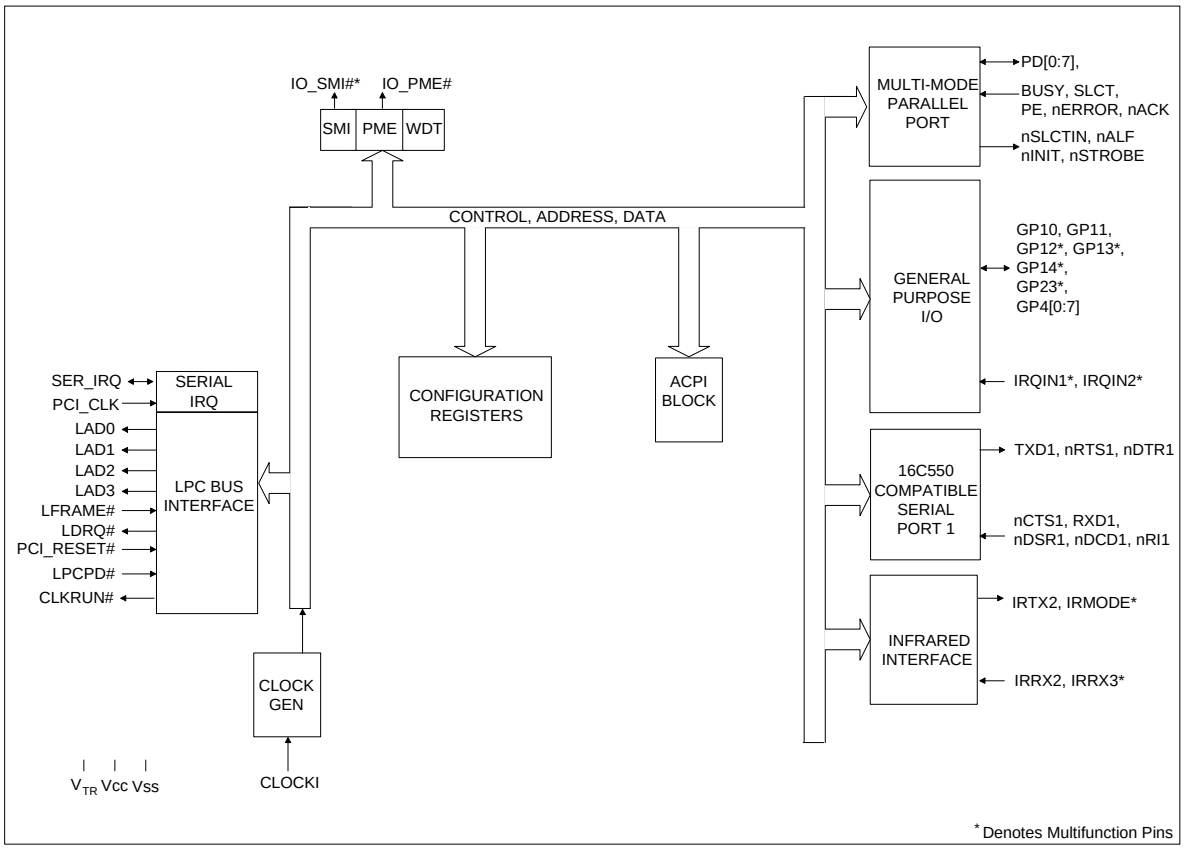
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BLOCK DIAGRAM

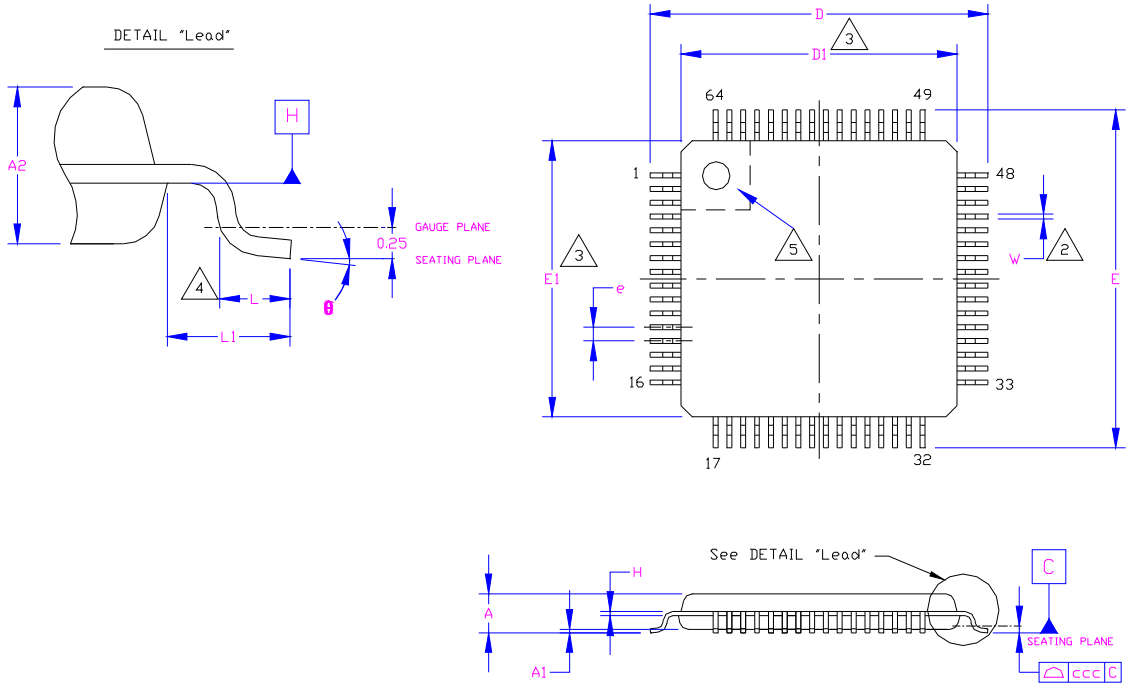
FIGURE 1: LPC47N217 BLOCK DIAGRAM



PACKAGE OUTLINE

Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging.

FIGURE 2: 64-PIN STQFP PACKAGE, 7 X 7 X 1.4 BODY, 2 MM FOOTPRINT



	Min	Nominal	Max	Remarks
A	~	~	1.60	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	1.35	1.40	1.45	Body Thickness
D	8.80	9.00	9.20	X Span
D1	6.80	7.00	7.20	X body Size
E	8.80	9.00	9.20	Y Span
E1	6.80	7.00	7.20	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00 REF.	~	Lead Length
e		0.40 Basic		Lead Pitch
θ	0^o	~	7^o	Lead Foot Angle
W	0.13	0.18	0.23	Lead Width
ccc	~	~	0.08	Coplanarity

Note 1: Controlling Unit: millimeter.

2: Tolerance on the true position of the leads is ± 0.035 mm maximum.

3: Package body dimensions D1 and E1 do not include the mold protrusion.
Maximum mold protrusion is 0.25 mm per side. D1 and E1 dimensions determined at datum plane H.

4: Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.

5: Details of pin 1 identifier are optional but must be located within the zone indicated.

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APPENDIX A: PRODUCT BRIEF REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00001810A (08-07-14)	Replaces previous SMSC version Rev.0.2 (09-21-06)	

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PART NO.[1]	-	XXX[2]	-	[X][3]
Device		Package		Tape and Reel Option

Device:	LPC47N217 [1]		
Package:	JV	=	64-pin STQFP [2]
Tape and Reel Option:	Blank	=	Tray packaging
	TR	=	Tape and Reel [3]

Example:

LPC47N217-JV = 64-pin STQFP

Note 1: These products meet the halogen maximum concentration values per IEC61249-2-21.

Note 2: All package options are RoHS compliant. For RoHS compliance and environmental information, please visit http://www.microchip.com/pagehandler/en-us/aboutus/ehs.html .

Note 3: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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