USB2250/50i/51/51i

Ultra Fast USB 2.0 Multi-Slot Flash Media Controller

General Description

The Microchip USB2250/50i/51/51i is a USB 2.0 compliant, Hi-Speed mass storage class peripheral controller intended for reading and writing to more than 24 popular flash media formats from the CompactFlash® (CF), SmartMedia™ (SM), xD-Picture Card™ (xD)[1], Memory Stick® (MS), Secure Digital (SD), and MultiMediaCard™ (MMC) families.

The USB2250/50i/51/51i is a fully integrated, single chip solution capable of ultra high performance operation. Average sustained transfer rates exceeding 35 MB/s are possible if the media and host can support those rates.

Highlights

- 128-pin VTQFP (14x14 mm) RoHS compliant package
- Targeted for applications in which single or "combo" media sockets are used
- Supports multiple simultaneous card insertions
- Flexible assignment of number of LUNs and how card types are associated with the LUNs
- Hardware-controlled data flow architecture for all self-mapped media
- Pipelined hardware support for access to non-self-mapped media
- Order number with “i” denotes the version that supports the industrial temperature range of -40ºC to 85ºC

Hardware Features

- Single chip flash media controller with non-multiplexed interface for independent card sockets
- Flash Media Specification Revision Compliance
  - CompactFlash 4.1
  - Secure Digital 2.0
  - MultiMediaCard 4.2
- MMC Streaming Mode support
  - Memory Stick 1.43
  - Memory Stick Pro Format 1.02
  - Memory Stick Duo Format 1.10
  - Memory Stick Pro-HG Duo Format 1.01
  - xD-Picture Card 1.2
  - SmartMedia 1.3
- Extended configuration options
  - xD player mode operation
  - Socket switch polarities, etc.
- Media Activity LED
- On board 24 MHz crystal driver circuit
- Optional external 24 MHz clock input
  - 4 Independent internal card power FETs
  - 200 mA each
  - "Fold-back" short circuit protection
- 8051 8-bit microprocessor
  - 60 MHz - single cycle execution
  - 64 KB ROM | 14 KB RAM
- Internal regulator for 1.8 V core operation
- Optimized pinout improves signal routing which eases implementation for improved signal integrity

OEM Selectable

- Vendor, product, and language IDs
- Manufacturer ID and product strings (28 character)
- Serial number string (12h digit max)
- Customizable vendor specific data by optional use of external serial EEPROM
- Bus- or self-powered selection
- LED blink interval or duration
- Internal power FET configuration

Software Features

- Optimized for low latency interrupt handling
- Reduced memory footprint
- Device Firmware Upgrade (DFU) support of external EEPROM or External Flash
  - Assembly line support
  - End user field upgrade support
  - DFU Package consists of driver, firmware, sample DFU application and source code, DFU driver API
- Optional custom firmware with up to 128 KB external ROM

Applications

- Flash Media Card Reader/Writer
- Printers
- Desktop and Mobile PCs
- Consumer A/V
- Media Players/Viewers
- Vista ReadyBoost™

1.) xD-Picture Card not applicable to USB2251.

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1.0 INTRODUCTION

The Microchip USB2250/50i/51/51i is a flash media card reader solution fully compliant with the USB 2.0 specification. All required resistors on the USB ports are integrated into the device. This includes all series termination resistors on D+ and D– pins and all required pull-down and pull-up resistors. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

Hardware Features

- Single chip flash media controller
- USB2250/USB2251 supports the commercial temperature range of 0°C to +70°C
- USB2250i/USB2251i supports the industrial temperature range of -40°C to +85°C
- 8051 8-bit microprocessor
  - 60 MHz - single cycle execution
  - 64 KB ROM |14 KB RAM
- Integrated regulator for 1.8 V core operation
- **Flash Media Card Specification Revision Compliance**
- Compact Flash 4.1
  - CF UDMA Modes 0-4
  - CF PIO Modes 0-6
- Secure Digital 2.0
  - HS-SD and HC-SD
  - TransFlash™ and reduced form factor media
- MultiMediaCard 4.2
  - 1/4/8 bit MMC
- Memory Stick 1.43
- Memory Stick Pro Format 1.02
- Memory Stick Pro-HG Duo Format 1.01
  - Memory Stick, MS Duo, HS-MS, MS Pro-HG, MS Pro
- Memory Stick Duo 1.10
- Smart Media 1.3
- xD-Picture Card 1.2

Software Features

- If the OEM is using an external EEPROM, the following features are available:
  - Customizable vendor, product, and device ID’s
  - 12-hex digits maximum for the serial number string
  - 28-character manufacturer ID and product strings for the flash media reader/writer

1.1 Acronyms

ATA: Advanced Technology Attachment

CFC: Compact Flash Controller

FET: Field Effect Transistor

LUN: Logical Unit Number

MMC: MultiMediaCard

MSC: Memory Stick Controller

PLL: Phase-Locked Loop

RoHS: Restriction of Hazardous Substances Directive

RXD: Received eXchange Data

SDC: Secure Digital Controller

SIE: Serial Interface Engine

SMC: SmartMedia Controller

True IDE Mode: True Integrated Drive Electronics Mode

TXD: Transmit eXchange Data

UART: Universal Asynchronous Receiver-Transmitter

UCHAR: Unsigned Character

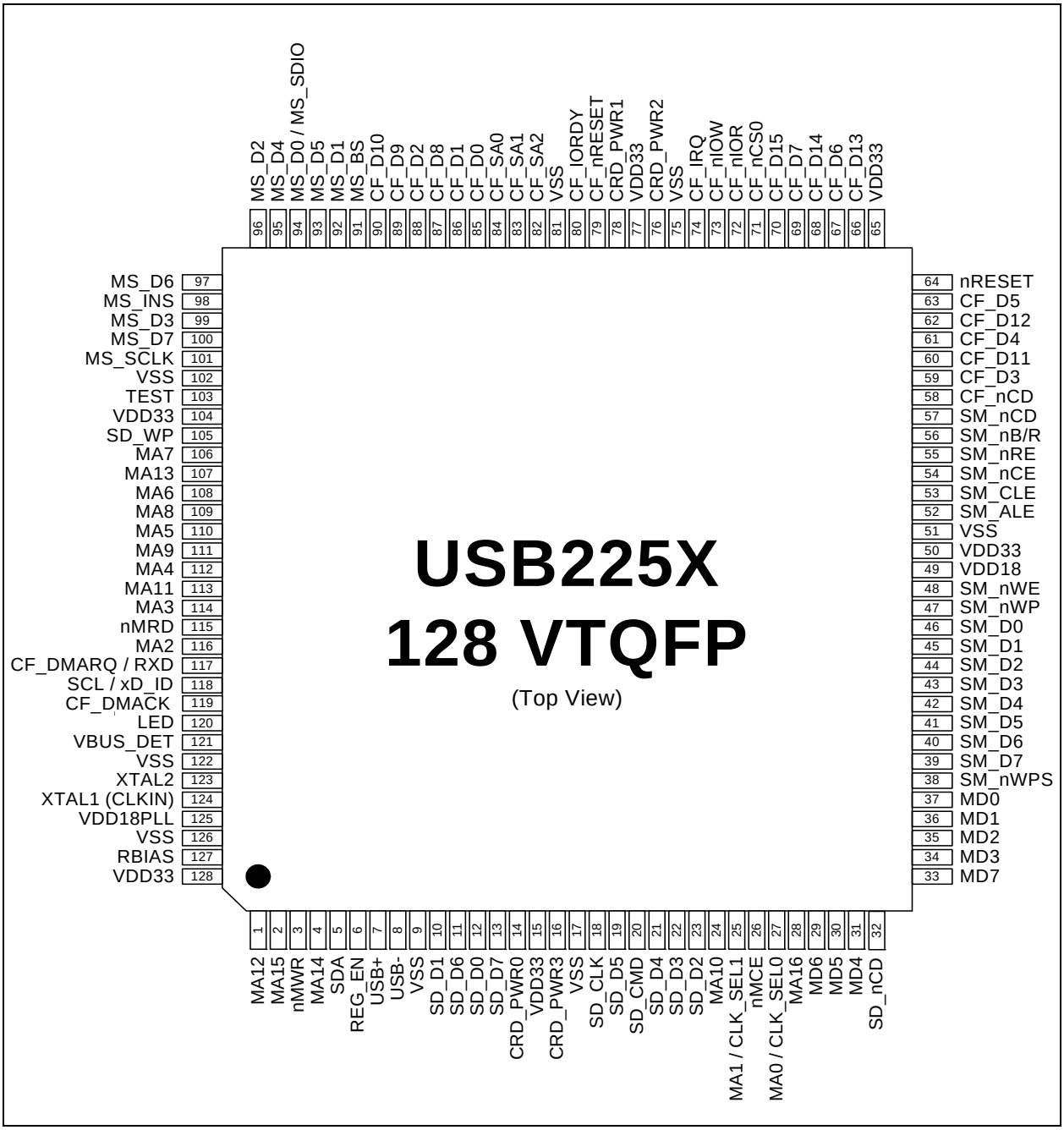
UINT: Unsigned Integer

VTQFP: Very Thin Quad Flat Package

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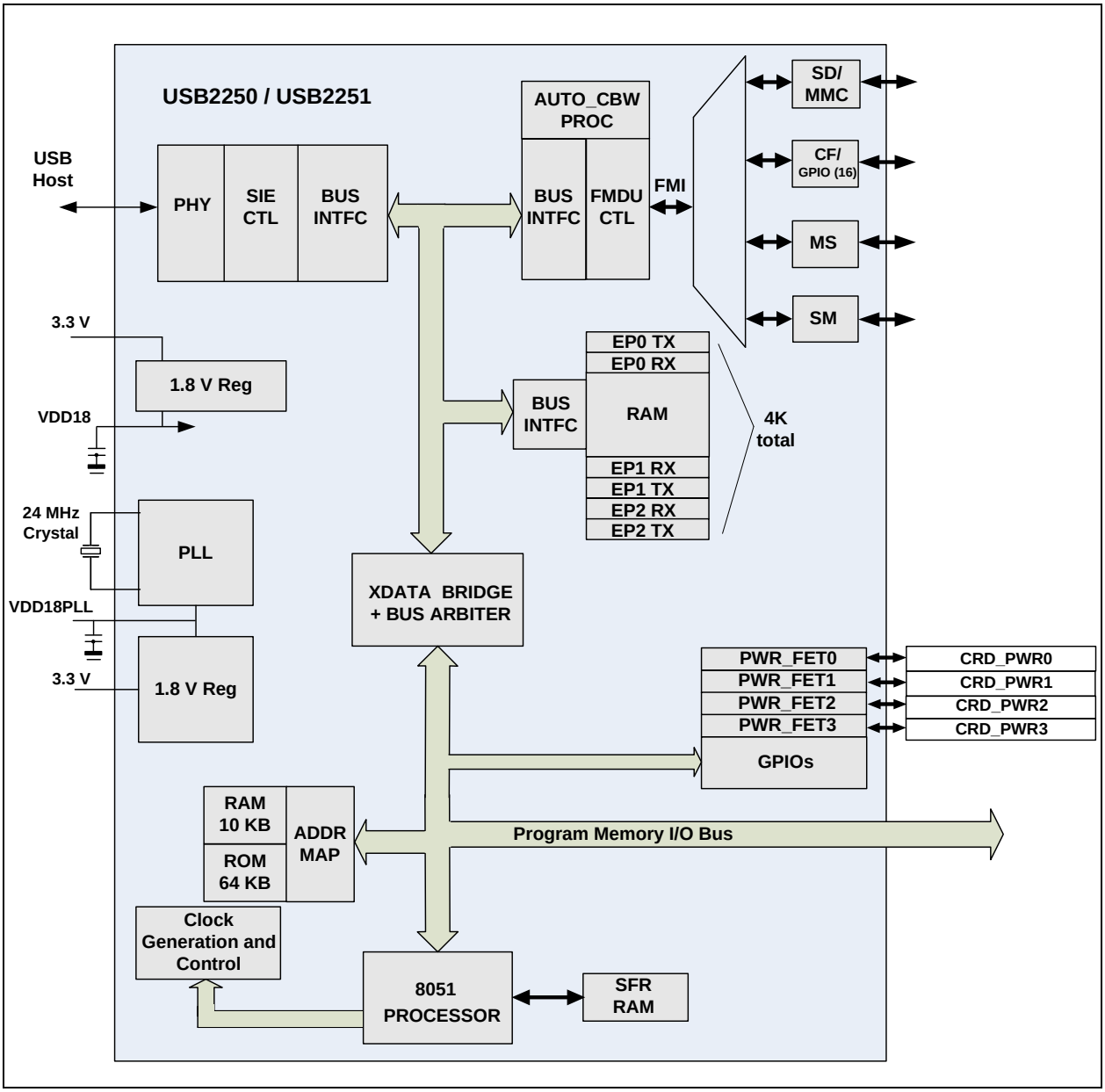
2.0 PIN CONFIGURATION

FIGURE 2-1: 128-PIN VTQFP DIAGRAM



3.0 BLOCK DIAGRAM

FIGURE 3-1: USB2250/50I/51/51I BLOCK DIAGRAM



4.0 PIN TABLE

4.1 128-Pin Package

TABLE 4-1: 128-PIN VTQFP PACKAGE

COMPACT FLASH INTERFACE (28 PINS)			
CF_D0	CF_D1	CF_D2	CF_D3
CF_D4	CF_D5	CF_D6	CF_D7
CF_D8	CF_D9	CF_D10	CF_D11
CF_D12	CF_D13	CF_D14	CF_D15
CF_nIOR	CF_nIOW	CF_IRQ	CF_nRESET
CF_IORDY	CF_nCS0	CF_DMACK	CF_SA0
CF_SA1	CF_SA2	CF_nCD	CF_DMARQ
SMARTMEDIA INTERFACE (17 PINS)			
SM_D0	SM_D1	SM_D2	SM_D3
SM_D4	SM_D5	SM_D6	SM_D7
SM_ALE	SM_CLE	SM_nRE	SM_nWE
SM_nWP	SM_nB/R	SM_nCE	SM_nCD
SM_nWPS			
MEMORY STICK INTERFACE (11 PINS)			
MS_BS	MS_D0 / MS_SDIO	MS_SCLK	MS_INS
MS_D1	MS_D2	MS_D3	MS_D4
MS_D5	MS_D6	MS_D7	
SECURE DIGITAL / MULTIMEDIACARD INTERFACE (12 PINS)			
SD_CMD	SD_CLK	SD_D0	SD_D1
SD_D2	SD_D3	SD_WP	SD_nCD
SD_D4	SD_D5	SD_D6	SD_D7
USB INTERFACE (6 PINS)			
USB+	USB-	RBIAS	
XTAL2	XTAL1 (CLKIN)	REG_EN	

TABLE 4-1: 128-PIN VTQFP PACKAGE (CONTINUED)

MEMORY/IO INTERFACE (28 PINS)			
MA0 / CLK_SEL0	MA1 / CLK_SEL1	MA2	MA3
MA4	MA5	MA6	MA7
MA8	MA9	MA10	MA11
MA12	MA13	MA14	MA15
MA16	MD0	MD1	MD2
MD3	MD4	MD5	MD6
MD7	nMRD	nMWR	nMCE
MISC (10 PINS)			
nRESET	VBUS_DET	SCL / xD_ID	SDA
LED	CRD_PWR0	CRD_PWR1	CRD_PWR2
CRD_PWR3	TEST		
DIGITAL, POWER (16 PINS)			
(6) VDD33	(8) VSS	VDD18	VDD18PLL
TOTAL 128			

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5.0 PIN DESCRIPTIONS

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface. The pin descriptions are applied when using the internal default firmware and can be referenced in Section 7.0, "Configuration Options," on page 21. Please reference Section 1.1, "Acronyms," on page 5 for a list of the acronyms used.

The “n” symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. When “n” is not present in the signal name, the signal is asserted at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

5.1 128-Pin VTQFP Pin Descriptions

TABLE 5-1: USB2250/50I/51/51I 128-PIN VTQFP PIN DESCRIPTIONS

Name	Symbol	128-Pin VTQFP	Buffer Type	Description
COMPACT FLASH (CF) INTERFACE				
CF Chip Select 0	CF_nCS0	71	O12PU	This pin is the active low chip select 0 signal for the task file registers of the CF ATA device in True IDE mode. This pin has a weak internal pull-up resistor.
CF Register Address	CF_SA[2:0]	82 83 84	I/O12	These pins are the register select address bits for the CF ATA device.
CF Interrupt	CF_IRQ	74	IPD	This is the active high interrupt request signal from the CF device. This pin has a weak internal pull-down resistor.
CF Data 15-8	CF_D[15:8] /	70 68 66 62 60 90 89 87	I/O12PD	CF_D[15:8]: These pins are the bi-directional data signals CF_D15 - CF_D8 in True IDE mode data transfer. In True IDE mode, all task file register operations occur on CF_D[7:0], while data transfer occurs on CF_D[15:0]. These bi-directional data signals have weak internal pull-down resistors.
CF Data 7-0	CF_D[7:0]	69 67 63 61 59 88 86 85	I/O12PD	CF_D[7:0]: These pins are the bi-directional data signals CF_D7 - CF_D0 in True IDE mode data transfer. In True IDE mode, all of the task file register operations occur on CF_D[7:0], while data transfer occurs on CF_D[15:0]. These bi-directional data signals have weak internal pull-down resistors.
IO Ready	CF_IORDY	80	IPU	This pin is the active high input signal for IORDY. This pin has a weak internal pull-up resistor.
CF Card Detection1	CF_nCD	58	I/O12	Designates as the Compact Flash card detection pin.
CF Hardware Reset	CF_RESET_N	79	O12	This pin is an active low hardware reset signal to the CF device.
CF IO Read	CF_nIOR	72	O12	This pin is an active low read strobe signal for the CF device.
CF IO Write Strobe	CF_nIOW	73	O12	This pin is an active low write strobe signal for the CF device.

TABLE 5-1: USB2250/50I/51/51I 128-PIN VTQFP PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	128-Pin VTQFP	Buffer Type	Description
CF DMA request	CF_DMARQ /	117	I	CF_DMARQ: This pin is the DMA request from the device to the CF controller.
	RXD			RXD: The signal can be used as input to the RXD of UART in the device. Custom firmware is required to activate this function.
CF DMA acknowledge	CF_DMACK	119	O12	CF_nDMACK: This pin is an active low DMA acknowledge signal for the CF device.
SMARTMEDIA (SM) INTERFACE				
SM Write Protect	SM_nWP	47	O12PD	This pin is an active low write protect signal for the SM device and has a weak pull-down resistor that is permanently enabled.
SM Address Strobe	SM_ALE	52	O12PD	This pin is an active high Address Latch Enable signal for the SM device and has a weak pull-down resistor that is permanently enabled.
SM Command Strobe	SM_CLE	53	O12PD	This pin is an active high Command Latch Enable signal for the SM device and has a weak pull-down resistor that is permanently enabled.
SM Data 7-0	SM_D[7:0]	39 40 41 42 43 44 45 46	I/O12PD	These pins are the bi-directional data signals SM_D7-SM_D0 and have weak internal pull-down resistors.
SM Read Enable	SM_nRE	55	O12PU	This pin is an active low read strobe signal for the SM device. When using the internal FET, this pin has a weak internal pull-up resistor that is tied to the output of the internal power FET. If an external FET is used (internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used).
SM Write Enable	SM_nWE	48	O12PU	This pin is an active low write strobe signal for the SM device. When using the internal FET, this pin has a weak internal pull-up resistor that is tied to the output of the internal power FET. If an external FET is used (internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used).
SM Write Protect Switch	SM_nWPS	38	IPU	A write-protect seal is detected when this pin is low. This pin has a weak internal pull-up resistor.
SM Busy or Data Ready	SM_nB/R	56	IPU	This pin is connected to the BSY/RDY pin of the SM device. When using the internal FET, this pin has a weak internal pull-up resistor that is tied to the output of the internal power FET. If an external FET is used (internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used).

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TABLE 5-1: USB2250/50I/51/51I 128-PIN VTQFP PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	128-Pin VTQFP	Buffer Type	Description
SM Chip Enable	SM_nCE	54	O12PU	This pin is the active low chip enable signal to the SM device. When using the internal FET, this pin has a weak internal pull-up resistor that is tied to the output of the internal power FET. If an external FET is used (internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used).
SM Card Detection	SM_nCD	57	I/O12	Designates as the Smart Media card detection pin.
MEMORY STICK (MS) INTERFACE				
MS Bus State	MS_BS	91	O12	This pin is connected to the bus state pin of the MS device. It is used to control the bus states 0, 1, 2 and 3 (BS0, BS1, BS2 and BS3) of the MS device.
MS Card Insertion	MS_INS	98	IPU	Designates as the Memory Stick card detection pin.
MS System CLK	MS_SCLK	101	O12	This pin is an output clock signal to the MS device. The clock frequency is software configurable.
MS System Data In/Out	MS_D[7:1]	100 97 93 95 99 96 92	I/O12PD	MS_D[7:1]: These pins are the bi-directional data signals for the MS device. MS_D2 and MS_D3 have weak pull-down resistors. MS_D1 has a pull-down resistor if it is in parallel mode, otherwise it is disabled. In 4- or 8-bit parallel mode, each MS_D7:1 signal has a weak pull-down resistor.
MS System Data In/Out	MS_D0 /	94	I/O12PD	MS_D0: This pin is one of the bi-directional data signals for the MS device. In serial mode, the most significant bit (MSB) of each byte is transmitted first by either MSC or the MS device on MS_D0, MS_D2, and MS_D3 (which have weak pull-down resistors). If MS_D1 is in parallel mode, it has a pull-down resistor; Otherwise, it is disabled. In 4- or 8-bit parallel mode, the MS_D0 signal has a weak pull-down resistor.
SECURE DIGITAL (SD) / MULTIMEDIACARD (MMC) INTERFACE				
SD Data 7-0	SD_D[7:0]	13 11 19 21 22 23 10 12	I/O12PU	These pins are bi-directional data signals SD_D0 - SD_D7 and have weak pull-up resistors.
SD Clock	SD_CLK	18	O12	This is an output clock signal to the SD/MMC device. The clock frequency is software configurable.

TABLE 5-1: USB2250/50I/51/51I 128-PIN VTQFP PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	128-Pin VTQFP	Buffer Type	Description
SD Command	SD_CMD	20	I/O12PU	This is a bi-directional signal that connects to the CMD signal of the SD/MMC device and has a weak internal pull-up resistor.
SD Write Protected	SD_WP	105	I/O12	Designates as the Secure Digital card mechanical write detect pin.
SD Card Detect	SD_nCD	32	I/O12	Designates as the Secure Digital card detection pin.
USB INTERFACE				
USB Bus Data	USB+ USB-	7 8	I/O-U	These pins connect to the USB bus data signals.
USB Transceiver Bias	RBIAS	127	I-R	A 12.0 kΩ, ±1.0% resistor is attached from VSS to this pin in order to set the transceiver's internal bias currents.
24 MHz Crystal Input (External Clock Input)	XTAL1 (CLKIN)	124	ICLKx	This pin can be connected to one terminal of the crystal or it can be connected to an external 24/48 MHz clock when a crystal is not used. The MA[1:0] pins will be sampled while RESET_N is asserted, and the value will be latched upon RESET_N negation. This will determine the clock source and value.
24 MHz Crystal Output	XTAL2	123	OCLKx	This is the other terminal of the crystal, or it is left open when an external clock source is used to drive XTAL1(CLKIN). It may not be used to drive any external circuitry other than the crystal circuit.
MEMORY / IO INTERFACE				
Memory Data Bus	MD[7:0]	33 29 30 31 34 35 36 37	I/O12PU	These signals are used to transfer data between the internal CPU and the external program memory and have weak internal pull-up resistors.

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TABLE 5-1: USB2250/50I/51/51I 128-PIN VTQFP PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	128-Pin VTQFP	Buffer Type	Description
Memory Address Bus	MA16	28	O12	These signals address memory locations within the external memory.
	MA[15:2]	2 4 107 1 113 24 111 109 106 108 110 112 114 116	O12	These signals address memory locations within the external memory.
	MA[1:0] /	25	O12	MA[1:0]: These signals address memory locations within the external memory.
	CLK_ SEL[1:0]	27	I/O12PD	CLK_SEL[1:0]: During RESET_N assertion, these pins will select the operating frequency of the external clock, and the corresponding weak pull-down resistors are enabled. When RESET_N is negated, the value on these pins will be latched internally and these pins will revert to MA[1:0] functionality; the internal pull-downs will be disabled. CLK_SEL[1:0] = '00'. 24 MHz CLK_SEL[1:0] = '01'. RESERVED CLK_SEL[1:0] = '10'. RESERVED CLK_SEL[1:0] = '11'. 48 MHz If the latched value is '1', the corresponding MA pin is tri-stated when the chip is in power down state. If the latched value is '0', the corresponding MA pin will function identically to MA[15:3] pins at all times (other than during RESET_N assertion).
Memory Write Strobe	nMWR	3	O12	This pin is the active low program Memory Write strobe signal.
Memory Read Strobe	nMRD	115	O12	This pin is the active low program Memory Read strobe signal.
Memory Chip Enable	nMCE	26	O12	This pin is the active low program Memory Chip Enable strobe signal. This signal is asserted when any external access is being done by the processor. This signal is held to the logic 'high' while RESET_N is asserted.

TABLE 5-1: USB2250/50I/51/51I 128-PIN VTQFP PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	128-Pin VTQFP	Buffer Type	Description
MISC				
General Purpose Input/Output	LED	120	I/O12	LED: It can be used as an LED output.
	VBUS_DET	121	I/O12	VBUS is a 3.3 volt input. A resistor divider must be used if connecting to 5 volts of USB power.
	SCL /	118	O12	SCL: This is the clock output when used with an external EEPROM.
	xD_ID		I/O12	xD_ID: This is the xD-Picture Card detection pin only applicable to USB2250/USB2250i.
	SDA	5	I/O12	SDA: This is the data pin when used with an external serial EEPROM.
	CRD_PWR0	14	I/O12	CRD_PWR: Card power drive of 3.3 V at either 100 mA or 200 mA.
			I/O200	
	CRD_PWR1	78	I/O12	CRD_PWR: Card power drive of 3.3 V at either 100 mA or 200 mA.
			I/O200	
	CRD_PWR2	76	I/O200	CRD_PWR: Card power drive of 3.3 V at either 100 mA or 200 mA. Requirement: This must be the only FET used to power SM devices. Failure to do this will violate SM voltage specification on SM device pins.
	CRD_PWR3	16	I/O200	CRD_PWR: Card power drive of 3.3 V at either 100 mA or 200 mA. Requirement: This must be the only FET used to power SM devices. Failure to do this will violate SM voltage specification on SM device pins.
RESET Input	RESET_N	64	IS	This active low signal is used by the system to reset the chip. The active low pulse should be at least 1μs wide.
TEST Input	TEST	103	I	Tie this pin to ground for normal operation.
Regulator Enable	REG_EN	6	IPU	This signal is used to enable the internal 1.8 V regulator.
DIGITAL POWER, and GROUND				
1.8 V Digital Core Power	VDD18	49		If the internal regulator is enabled, then this pin must have a 1.0 μF (or greater) ±20% (ESR <0.1 Ω) capacitor to VSS.
1.8 V PLL Power	VDD18PLL	125		If the internal regulator is enabled, then this pin must have a 1.0 μF (or greater) ±20% (ESR <0.1 Ω) capacitor to VSS.
3.3 V Power and Voltage Regulator Input	VDD33	15 50 65 77 104 128		If the internal regulator is enabled, pins 50 and 128 each require an external bypass capacitor of 4.7 μF minimum.

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TABLE 5-1: USB2250/50I/51/51I 128-PIN VTQFP PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	128-Pin VTQFP	Buffer Type	Description
Ground	VSS	9 17 51 75 81 102 122 126		Ground Reference

Note 5-1 Hot-insertion capable card connectors are required for all flash media. It is required for the SD connector to have a Write Protect switch. This allows the chip to detect the MMC card.

Note 5-2 nMCE is normally asserted except when the 8051 is in standby mode.

5.2 Buffer Type Descriptions

TABLE 5-2: BUFFER TYPE DESCRIPTIONS

BUFFER	DESCRIPTION
I	Input.
IPU	Input with internal weak pull-up resistor.
IPD	Input with internal weak pull-down resistor.
IS	Input with Schmitt trigger.
I/O12	Input/Output buffer with 12 mA sink and 12 mA source.
I/O200	Input/Output buffer 12 mA with FET disabled, 100/200 mA source only when the FET is enabled.
I/O12PD	Input/Output buffer with 12 mA sink and 12 mA source with an internal weak pull-down resistor.
I/O12PU	Input/Output buffer with 12 mA sink and 12 mA source with a pull-up resistor.
O12	Output buffer with 12 mA source.
O12PU	Output buffer with 12 mA sink and 12 mA source, with a pull-up resistor.
O12PD	Output buffer with 12 mA sink and 12 mA source, with a pull-down resistor.
ICLKx	XTAL clock input.
OCLKx	XTAL clock output.
I/O-U	Analog Input/Output as defined in the USB 2.0 Specification.
I-R	RBIAS.

6.0 PIN RESET STATE TABLE

FIGURE 6-1: PIN RESET STATES

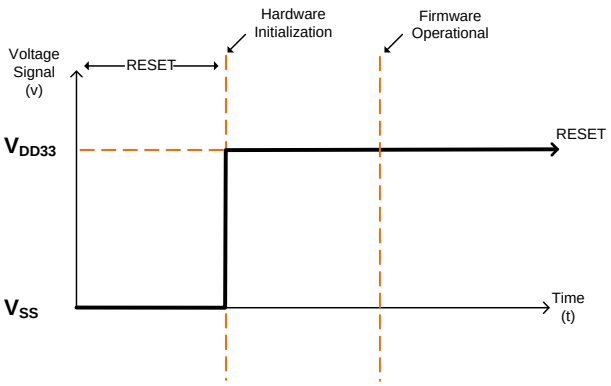


TABLE 6-1: LEGEND FOR PIN RESET STATES TABLE

Symbol	Description
0	Output driven low
1	Output driven high
IP	Input enabled
PU	Hardware enables pull-up
PD	Hardware enables pull-down
--	Hardware disables function
Z	Hardware disables pad. Both output driver and input buffers are disabled.

6.1 128-Pin Reset States

6.2 128-Pin Reset States

TABLE 6-2: USB2250/50I/51/51I 128-PIN RESET STATES

		Reset State					Reset State		
Pin	Pin Name	Function	Input/ Out-put	PU/ PD	Pin	Pin Name	Function	Input/ Out-put	PU/ PD
85	CF_D0	None	z	--	58	CF_nCD	None	IP	pu
86	CF_D1	None	z	--	46	SM_D0	SM	z	pd
88	CF_D2	None	z	--	45	SM_D1	SM	z	pd
59	CF_D3	None	z	--	44	SM_D2	SM	z	pd
61	CF_D4	None	z	--	43	SM_D3	SM	z	pd
63	CF_D5	None	z	--	42	SM_D4	SM	z	pd
67	CF_D6	None	z	--	41	SM_D5	SM	z	pd
69	CF_D7	None	z	--	40	SM_D6	SM	z	pd
87	CF_D8	None	z	--	39	SM_D7	SM	z	pd
89	CF_D9	None	z	--	52	SM_ALE	SM	z	pd
90	CF_D10	None	z	--	53	SM_CLE	SM	z	pd
60	CF_D11	None	z	--	47	SM_nWP	SM	z	pd
62	CF_D12	None	z	--	38	SM_nWPS	SM	z	--
66	CF_D13	None	z	--	57	SM_nCD	None	IP	pu
68	CF_D14	None	z	--	91	MS_BS	MS	z	pd
70	CF_D15	None	z	--	101	MS_SCLK	MS	z	pd
72	CF_nIOR	CF	z	--	94	MS_D0 / MS_SDIO	MS	z	pd
73	CF_nIOW	CF	z	--	92	MS_D1	MS	z	pd
74	CF_nIRQ	CF	z	--	96	MS_D2	MS	z	pd
79	CF_nRESET	CF	z	--	99	MS_D3	MS	z	pd
80	CF_IORDY	CF	z	--	95	MS_D4	MS	z	pd
71	CF_nCS0	CF	z	--	93	MS_D5	MS	z	pd
84	CF_SA0	CF	z	--	97	MS_D6	MS	z	pd
83	CF_SA1	CF	z	--	100	MS_D7	MS	z	pd
82	CF_SA2	CF	z	--	98	MS_INS	None	IP	pu

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TABLE 6-2: USB2250/50I/51/51I 128-PIN RESET STATES (CONTINUED)

		Reset State		
Pin	Pin Name	Function	Input/ Out-put	PU/ PD
119	CF_DMACK	None	0	--
117	CF_DMARQ	None	0	--
12	SD_D0	SD	z	--
10	SD_D1	SD	z	--
23	SD_D2	SD	z	--
22	SD_D3	SD	z	--
21	SD_D4	SD	z	--
19	SD_D5	SD	z	--
11	SD_D6	SD	z	--
13	SD_D7	SD	z	--
105	SD_WP	None	0	--
32	SD_nCD	None	IP	pu
27	MA0 / CLK_SEL0	MA	IP	pd
25	MA1 / CLK_SEL1	MA	IP	pd
116	MA2	MA	IP	pd
114	MA3	MA	IP	pd
112	MA4	MA	0	--
110	MA5	MA	0	--
108	MA6	MA	0	--
106	MA7	MA	0	--
109	MA8	MA	0	--
111	MA9	MA	0	--
24	MA10	MA	0	--
113	MA11	MA	0	--
107	MA13	MA	0	--
28	MA16	MA	0	--
37	MD0	MA	z	pu

		Reset State		
Pin	Pin Name	Function	Input/ Out-put	PU/ PD
20	SD_CMD	SD	z	--
34	MD3	MA	z	pu
18	SD_CLK	SD	z	--
31	MD4	MA	z	pu
30	MD5	MA	z	pu
29	MD6	MA	z	pu
33	MD7	MA	z	pu
115	nMRD	MA	1	--
26	nMCE	MA	1	--
120	LED	None	0	--
118	SCL / xD_ID	None	0	--
14	CRD_PWR0	None	z	--
78	CRD_PWR1	None	z	--
76	CRD_PWR2	None	z	--
16	CRD_PWR3	None	z	--
103	TEST	TEST	IP	--
64	nRESET	nRESET	IP	--
1	MA12	MA	0	--
4	MA14	MA	0	--
2	MA15	MA	0	--
3	nMWR	MA	1	--
121	VBUS_DET	None	IP	--
5	SDA	None	0	pu
55	SM_nRE	SM	z	--
48	SM_nWE	SM	z	--
56	SM_nB/R	SM	z	--
54	SM_nCE	SM	z	--

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TABLE 6-2: USB2250/50I/51/51I 128-PIN RESET STATES (CONTINUED)

		Reset State						Reset State		
Pin	Pin Name	Function	Input/ Out-put	PU/ PD		Pin	Pin Name	Function	Input/ Out-put	PU/ PD
36	MD1	MA	z	pu		7	USB+	USB+	z	--
35	MD2	MA	z	pu		8	USB-	USB-	z	--

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7.0 CONFIGURATION OPTIONS

7.1 Card Reader

The Microchip USB2250/50i/51/51i is fully compliant with the following flash media card reader specifications:

- Compact Flash 4.1
  - CF UDMA Modes 0-4
  - CF PIO Modes 0-6
- Secure Digital 2.0
  - HS-SD and HC-SD
  - TransFlash™ and reduced form factor media
- MultiMediaCard 4.2
  - 1/4/8 bit MMC
- Memory Stick 1.43
- Memory Stick Pro Format 1.02
- Memory Stick Pro-HG Duo Format 1.01
  - Memory Stick, MS Duo, HS-MS, MS Pro-HG, MS Pro
- Memory Stick Duo 1.10
- Smart Media 1.3
- xD-Picture Card 1.2

7.1.1 VBUS DETECT

According to Section 7.2.1 of the USB 2.0 Specification, a device cannot provide power to its D+ or D- pull-up resistors unless the upstream port's VBUS is in the asserted (powered) state. The VBUS_DET pin on the device monitors the state of the upstream VBUS signal and will not pull-up the D+ resistor if VBUS is not active. If VBUS goes from an active to an inactive state (not powered), the device will remove power from the D+ pull-up resistor within 10 seconds.

7.2 System Configurations

7.2.1 EEPROM

The USB2250/50i/51/51i can be configured via a 2-wire (I^2C) EEPROM (512x8) flash device containing the options for the USB2250/50i/51/51i. If an external configuration device does not exist the internal default values will be used. If one of the external devices is used for configuration, the OEM can update the values through the USB interface. The device will then "attach" to the upstream USB host.

The USBDM tool set is available in the USB225x Card Reader software release package. To download the software package from Microchip's website, please visit:

http://www.microchip.com/SWLibraryWeb/producttc.aspx?product=OBJ%20files%20for%20USB2250

to go to the OBJ Card Reader Software Download Agreement. Review the license, and if you agree, check the "I agree" box and then select "Confirm". You will then be able to download the USB225x Card reader combo release package zip files containing the USBDM tool set. Please note that the following applies to the system values and descriptions when used:

- N/A = Not applicable to this part
- Reserved = For internal use

7.2.2 EEPROM DATA DESCRIPTOR

TABLE 7-1: INTERNAL FLASH MEDIA CONTROLLER CONFIGURATIONS

Address	Register Name	Description	Internal Default Value
00h	USB_SER_LEN	USB Serial String Descriptor Length	1Ah
01h	USB_SER_TYP	USB Serial String Descriptor Type	03h
02h-19h	USB_SER_NUM	USB Serial Number	"000000225001" (See Note 7-1)
1Ah-1Bh	USB_VID	USB Vendor Identifier	0424
1Ch-1Dh	USB_PID	USB Product Identifier	2250
1Eh	USB_LANG_LEN	USB Language String Descriptor Length	04h
1Fh	USB_LANG_TYP	USB Language String Descriptor Type	03h
20h	USB_LANG_ID_LSB	USB Language Identifier Least Significant Byte	09h (See Note 7-2)
21h	USB_LANG_ID_MSB	USB Language Identifier Most Significant Byte	04h (See Note 7-2)
22h	USB_MFR_STR_LEN	USB Manufacturer String Descriptor Length	10h
23h	USB_MFR_STR_TYP	USB Manufacturer String Descriptor Type	03h
24h-31h	USB_MFR_STR	USB Manufacturer String	“Generic” (See Note 7-1)
32h-5Dh	Reserved	-	00h
5Eh	USB_PRD_STR_LEN	USB Product String Descriptor Length	24h
5Fh	USB_PRD_STR_TYP	USB Product String Descriptor Type	03h
60h-99h	USB_PRD_STR	USB Product String	"Flash Card Reader" (See Note 7-1)
9Ah	USB_BM_ATT	USB BmAttribute	80h
9Bh	USB_MAX_PWR	USB Max Power	30h (96 mA)
9Ch	ATT_LB	Attribute Lo byte	40h (Reverse SD_WP only)
9Dh	ATT_HLB	Attribute Hi Lo byte	00h
9Eh	ATT_LHB	Attribute Lo Hi byte	00h
9Fh	ATT_HB	Attribute Hi byte	00h
A0h	MS_PWR_LB	Memory Stick Device Power Lo byte	08h
A1h	MS_PWR_HB	Memory Stick Device Power Hi byte	00h
A2h	CF_PWR_LB	Compact Flash Device Power Lo byte	80h
A3h	CF_PWR_HB	Compact Flash Device Power Hi byte	00h
A4h	SM_PWR_LB	Smart Media Device Power Lo byte	00h
A5h	SM_PWR_HB	Smart Media Device Power Hi byte	08h
A6h	SD_PWR_LB	Secure Digital Device Power Lo byte	00h

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TABLE 7-1: INTERNAL FLASH MEDIA CONTROLLER CONFIGURATIONS (CONTINUED)

Address	Register Name	Description	Internal Default Value
A7h	SD_PWR_HB	Secure Digital Device Power Hi byte	80h
A8h	LED_BLK_INT	LED Blink Interval	02h
A9h	LED_BLK_DUR	LED Blink After Access	28h
AAh - B0h	DEV0_ID_STR	Device 0 Identifier String	“CF”
B1h - B7h	DEV1_ID_STR	Device 1 Identifier String	“MS”
B8h - BEh	DEV2_ID_STR	Device 2 Identifier String	“SM”
BFh - C5h	DEV3_ID_STR	Device 3 Identifier String	“SD/MMC”
C6h - CDh	INQ_VEN_STR	Inquiry Vendor String	“Generic”
CEh-D2h	INQ_PRD_STR	Inquiry Product String	2250
D3h	DYN_NUM_LUN	Dynamic Number of LUNs	FFh
D4h - D7h	DEV_LUN_MAP	Device to LUN Mapping	FFh, FFh, FFh, FFh
D8h - DAh	MS_BUS_TIMINGReserved	-	00h, 03h, 07h
DBh - DDh	MS_BUS_TIMINGReserved	-	5Ch, 56h, 97h
DEh-FBh	Not Applicable	-	00h
FCh-FFh	NVSTORE_SIG	Non-Volatile Storage Signature	“ATA2”

Note 7-1 This value is a UNICODE UTF-16LE encoded string value that meets the USB 2.0 specification (Revision 2.0, 2000). Values in double quotations without this note are ASCII values.

Note 7-2 For a list of the most current 16-bit language ID’s defined by the USB-IF, please visit http://www.unicode.org or consult *The Unicode Standard, Worldwide Character Encoding*, (Version 4.0), The Unicode Consortium, Addison-Wesley Publishing Company, Reading, Massachusetts.

7.2.3 EEPROM DATA DESCRIPTOR REGISTER DESCRIPTIONS

7.2.3.1 00h: USB Serial String Descriptor Length

Byte	Name	Description
0	USB_SER_LEN	USB serial string descriptor length as defined by Section 9.6.7 “String” of the USB 2.0 Specification (Revision 2.0, 2000). This field is the “bLength” which describes the size of the string descriptor (in bytes).

7.2.3.2 01h: USB Serial String Descriptor Type

Byte	Name	Description
1	USB_SER_TYP	USB serial string descriptor type as defined by Section 9.6.7 “String” of the USB 2.0 Specification (Revision 2.0, 2000). This field is the “bDescriptorType” which is a constant value associated with a string descriptor type.

7.2.3.3 02h-19h: USB Serial Number Option

Byte	Name	Description
25:2	USB_SER_NUM	Maximum string length is 12 hex digits. Must be unique to each device.

7.2.3.4 1Ah-1Bh: USB Vendor ID Option

Byte	Name	Description
1:0	USB_VID	This ID is unique for every vendor. The vendor ID is assigned by the USB Implementer’s Forum.

7.2.3.5 1Ch-1Dh: USB Product ID Option

Byte	Name	Description
1:0	USB_PID	This ID is unique for every product. The product ID is assigned by the vendor.

7.2.3.6 1Eh: USB Language Identifier Descriptor Length

Byte	Name	Description
0	USB_LANG_LEN	USB language ID string descriptor length as defined by Section 9.6.7 “String” of the USB 2.0 Specification (Revision 2.0, 2000). This field is the “bLength” which describes the size of the string descriptor (in bytes).

7.2.3.7 1Fh: USB Language Identifier Descriptor Type

Byte	Name	Description
1	USB_LANG_TYP	USB language ID string descriptor type as defined by Section 9.6.7 “String” of the USB 2.0 Specification (Revision 2.0, 2000). This field is the “bDescriptorType” which is a constant value associated with a string descriptor type.

7.2.3.8 20h: USB Language Identifier Least Significant Byte

Byte	Name	Description
2	USB_LANG_ID _LSB	English language code = ‘0409’. See Note 7-2 to reference additional language ID’s defined by the USB-IF.

7.2.3.9 21h: USB Language Identifier Most Significant Byte

Byte	Name	Description
3	USB_LANG_ID _MSB	English language code = ‘0409’. See Note 7-2 to reference additional language ID’s defined by the USB-IF.

7.2.3.10 22h: USB Manufacturer String Descriptor Length

Byte	Name	Description
0	USB_MFR_STR _LEN	USB manufacturer string descriptor length as defined by Section 9.6.7 “String” of the USB 2.0 Specification (Revision 2.0, 2000). This field is the “bLength” which describes the size of the string descriptor (in bytes).

7.2.3.11 23h: USB Manufacturer String Descriptor Type

Byte	Name	Description
1	USB_MFR_STR _TYP	USB manufacturer string descriptor type as defined by Section 9.6.7 “String” of the USB 2.0 Specification (Revision 2.0, 2000). This field is the “bDescriptorType” which is a constant value associated with a string descriptor type.

7.2.3.12 24h-31h: USB Manufacturer String Option

Byte	Name	Description
15:2	USB_MFR_STR	Maximum string length is 29 characters.

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7.2.3.13 32h-5Dh: Reserved

Byte	Name	Description
59:16	Reserved	Reserved.

7.2.3.14 5Eh: USB Product String Descriptor Length

Byte	Name	Description
0	USB_PRD_STR _LEN	USB product string descriptor length as defined by Section 9.6.7 “String” of the USB 2.0 Specification (Revision 2.0, 2000). This field is the “bLength” which describes the size of the string descriptor (in bytes). Maximum string length is 29 characters

7.2.3.15 5Fh: USB Product String Descriptor Type

Byte	Name	Description
1	USB_PRD_STR _TYP	USB product string descriptor type as defined by Section 9.6.7 “String” of the USB 2.0 Specification (Revision 2.0, 2000). This field is the “bDescriptorType” which is a constant value associated with a string descriptor type.

7.2.3.16 60h-99h: USB Product String Option

Byte	Name	Description
59:2	USB_PRD_STR	This string will be used during the USB enumeration process in the Windows® operating system. Maximum string length is 29 characters.

7.2.3.17 9Ah: USB BmAttribute (1 byte)

Byte	Name	Description
7:0	USB_BM_ATT	Self- or Bus-Power: Selects between self- and bus-powered operation. The hub is either self-powered (draws less than 2 mA) or bus-powered (limited to 100 mA maximum power prior to being configured by the host controller). When configured as a bus-powered device, the Microchip device consumes less than 100 mA of current prior to being configured. After configuration, the bus-powered Microchip device (along with all associated device circuitry, any embedded devices if part of a compound device, and 100 mA per externally available downstream port) must consume no more than 500 mA of current. The current consumption is system dependent, and the OEM must ensure that the USB 2.0 Specification is not violated. When configured as a self-powered device, <1 mA of current is consumed and all ports are available, with each port being capable of sourcing 500 mA of current. **80 = Bus-powered operation (default)** C0 = Self-powered operation A0 = Bus-powered operation with remote wake-up E0 = Self-powered operation with remote wake-up

7.2.3.18 9Bh: USB MaxPower (1 byte)

Byte	Name	Description
7:0	USB_MAX_PWR	USB Max Power per the USB 2.0 Specification. Do NOT set this value greater than 100 mA.

7.2.3.19 9Ch-9Fh: Attribute Byte Descriptions

Byte	Byte Name	Bit	Description
0	ATT_LB	3:0	Always reads ‘0’.
		4	Inquire Manufacturer and Product ID Strings ‘1’ - Use the Inquiry Manufacturer and Product ID Strings. ‘0’ (default) - Use the USB Descriptor Manufacturer and Product ID Strings.
		5	Always reads ‘0’.
		6	Reverse SD Card Write Protect Sense ‘1’ (default) - SD cards will be write protected when SW_nWP is high, and writable when SW_nWP is low. ‘0’ - SD cards will be write protected when SW_nWP is low, and writable when SW_nWP is high.
		7	Reserved.
1	ATT_HLB	3:0	Always reads ‘0’.
		4	Activity LED True Polarity ‘1’ - Activity LED to Low True. ‘0’ (default) - Activity LED polarity to High True.
		5	Common Media Insert / Media Activity LED ‘1’ - The activity LED will function as a common media inserted/media access LED. ‘0’ (default) - The activity LED will remain in its idle state until media is accessed.
		6	Always reads ‘0’.
		7	Reserved.
2	ATT_LHB	0	Attach on Card Insert / Detach on Card Removal ‘1’ - Attach on Insert is enabled. ‘0’ (default) - Attach on Insert is disabled.
		1	Always reads ‘0’.
		2	Enable Device Power Configuration ‘1’ - Custom Device Power Configuration stored in the NVSTORE is used. ‘0’ (default) - Default Device Power Configuration is used.
		7:3	Always reads ‘0’.
3	ATT_HB	6:0	Always reads ‘0’.
		7	xD Player Mode

7.2.4 A0H-A7H: DEVICE POWER CONFIGURATION

The USB2250/50i/51/51i has four internal FETs which can be utilized for card power. This section describes the default internal configuration. The settings are stored in NVSTORE and provide the following features:

1. A card can be powered by an external FET or by an internal FET.
2. The power limit can be set to 100 mA or 200 mA (Default) for the internal FET.

Each media uses two bytes to store its device power configuration. Bit 3 selects between internal or external card power FET options. For internal FET card power control, bits 0 through 2 are used to set the power limit. The “Device Power Configuration” bits are ignored unless the “Enable Device Power Configuration” bit is set. See Section 7.2.3.19, "9Ch-9Fh: Attribute Byte Descriptions," on page 26.

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7.2.4.1 A0h-A1h: Memory Stick Device Power Configuration

FET	Type	Bits	Bit Type	Description
0	FET Lo Byte MS_PWR_LB	3:0	Low Nibble	0000b Disabled
1		7:4	High Nibble	
2	**FET Hi Byte** MS_PWR_HB	**3:0**	**Low Nibble**	0000b Disabled 0001b External FET enabled 1000b Internal FET with 100 mA power limit **1010b Internal FET with 200 mA power limit**
3		7:4	High Nibble	0000b Disabled

7.2.4.2 A2h-A3h: Compact Flash Device Power Configuration

FET	Type	Bits	Bit Type	Description
0	FET Lo Byte CF_PWR_LB	3:0	Low Nibble	0000b Disabled
1		7:4	High Nibble	
2	**FET Hi Byte** CF_PWR_HB	**3:0**	**Low Nibble**	0000b Disabled 0001b External FET enabled 1000b Internal FET with 100 mA power limit **1010b Internal FET with 200 mA power limit**
3		7:4	High Nibble	0000b Disabled

7.2.4.3 A4h-A5h: Smart Media Device Power Configuration

FET	Type	Bits	Bit Type	Description
0	FET Lo Byte SM_PWR_LB	3:0	Low Nibble	0000b Disabled
1		7:4	High Nibble	
2	**FET Hi Byte** SM_PWR_HB	**3:0**	**Low Nibble**	0000b Disabled 0001b External FET enabled 1000b Internal FET with 100 mA power limit **1010b Internal FET with 200 mA power limit**
3		7:4	High Nibble	0000b Disabled

7.2.4.4 A6h-A7h: Secure Digital Device Power Configuration

FET	Type	Bits	Bit Type	Description
0	FET Lo Byte SD_PWR_LB	3:0	Low Nibble	0000b Disabled
1		7:4	High Nibble	
2	**FET Hi Byte** SD_PWR_HB	**3:0**	**Low Nibble**	0000b Disabled 0001b External FET enabled 1000b Internal FET with 100 mA power limit **1010b Internal FET with 200 mA power limit**
3		7:4	High Nibble	0000b Disabled

7.2.4.5 A8h: LED Blink Interval

Byte	Name	Description
0	LED_BLK_INT	The blink rate is programmable in 50 ms intervals. The high bit (7) indicates an idle state: ‘0’ - Off ‘1’ - On The remaining bits (6:0) are used to determine the blink interval up to a max of 63 x 50 ms.

7.2.4.6 A9h: LED Blink Duration

Byte	Name	Description
1	LED_BLK_DUR	LED Blink After Access. This byte is used to designate the number of seconds that the LED will continue to blink after a drive access. Setting this byte to "05" will cause the LED to blink for 5 seconds after a drive access.

7.2.5 DEVICE ID STRINGS

These bytes are used to specify the LUN descriptor returned by the device. These bytes are used in combination with the device to LUN mapping bytes in applications where the OEM wishes to reorder and rename the LUNs. If multiple devices are mapped to the same LUN (a COMBO LUN), then the CLUN#_ID_STR will be used to name the COMBO LUN instead of the individual device strings. When applicable, the "SM" value will be overridden with xD once an xD-Picture Card has been identified.

7.2.5.1 AAh-B0h: Device 0 Identifier String

Byte	Name	Description
6:0	DEV0_ID_STR	Not applicable.

7.2.5.2 B1h-B7h: Device 1 Identifier String

Byte	Name	Description
6:0	DEV1_ID_STR	This ID string is associated with the Memory Stick device.

7.2.5.3 B8h-BEh: Device 2 Identifier String

Byte	Name	Description
6:0	DEV2_ID_STR	This ID string is associated with the Smart Media device.

7.2.5.4 BFh-C5h: Device 3 Identifier String

Byte	Name	Description
6:0	DEV3_ID_STR	This ID string is associated with the Secure Digital / MultiMediaCard device.

7.2.5.5 C6h-CDh: Inquiry Vendor String

Byte	Name	Description
7:0	INQ_VEN_STR	If bit 4 of the 1st attribute byte is set, the device will use these strings in response to a USB inquiry command, instead of the USB descriptor manufacturer and product ID strings.

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7.2.5.6 CEh-D2h: Inquiry Product String

Byte	Name	Description
4:0	INQ_PRD_STR	If bit 4 of the 1st attribute byte is set, the device will use these strings in response to a USB inquiry command, instead of the USB descriptor manufacturer and product ID strings.

7.2.5.7 D3h: Dynamic Number of LUNs

Byte	Name	Description
7:0	DYN_NUM_LUN	These bytes are used to specify the number of LUNs the device exposes to the host. These bytes are also used for icon sharing by assigning more than one LUN to a single icon. This is used in applications where the device utilizes a combo socket and the OEM wishes to have only a single icon displayed for one or more interfaces. If this field is set to "FF", the program assumes that you are using the default value and icons will be configured per the default configuration.

7.2.5.8 D4h-D7h: Device to LUN Mapping

Byte	Name	Description
3:0	DEV_LUN_MAP	These registers map a device controller (SD/MMC, SM, and MS) to a Logical Unit Number (LUN). The device reports the mapped LUNs to the USB host in the USB descriptor during enumeration. The icon installer associates custom icons with the LUNs specified in these fields. Setting a register to "FF" indicates that the device is not mapped. Setting all of the DEV_LUN_MAP registers for all devices to "FF" forces the use of the default mapping configuration. Not all configurations are valid. Valid configurations depend on the hardware, packaging, and OEM board layout. The number of unique LUNs mapped must match the value in the Section 7.2.5.7, "D3h: Dynamic Number of LUNs," on page 29.

7.2.5.9 D8h-FBh: Not Applicable

Byte	Name	Description
35:0	Not Applicable	Not Applicable.

7.2.5.10 FCh-FFh: **Non-Volatile Storage Signature**

Byte	Name	Description
3:0	NVSTORE_SIG	This signature is used to verify the validity of the data in the first 256 bytes of the configuration area. The signature must be set to ‘ATA2’ for USB2250/50i/51/51i.

7.3 Default Configuration Option

The Microchip device can be configured via its internal default configuration. Please see Section 7.2.2, "EEPROM Data Descriptor" for specific details on how to enable default configuration. Please refer to Table 7-1 for the internal default values that are loaded when this option is selected.

7.3.1 EXTERNAL HARDWARE NRESET

A valid hardware reset is defined as assertion of nRESET for a minimum of 1 µs after all power supplies are within operating range. While reset is asserted, the device (and its associated external circuitry) consumes less than 500 µA of current.

Assertion of nRESET (external pin) causes the following:

1. The PHY is disabled and the differential pair will be in a high-impedance state.
2. All transactions immediately terminate; no states are saved.
3. All internal registers return to the default state.
4. The external crystal oscillator is halted.
5. The PLL is halted.
6. The processor is reset.
7. All media interfaces are reset.

7.3.1.1 nRESET for EEPROM Configuration

FIGURE 7-1: NRESET TIMING FOR EEPROM MODE

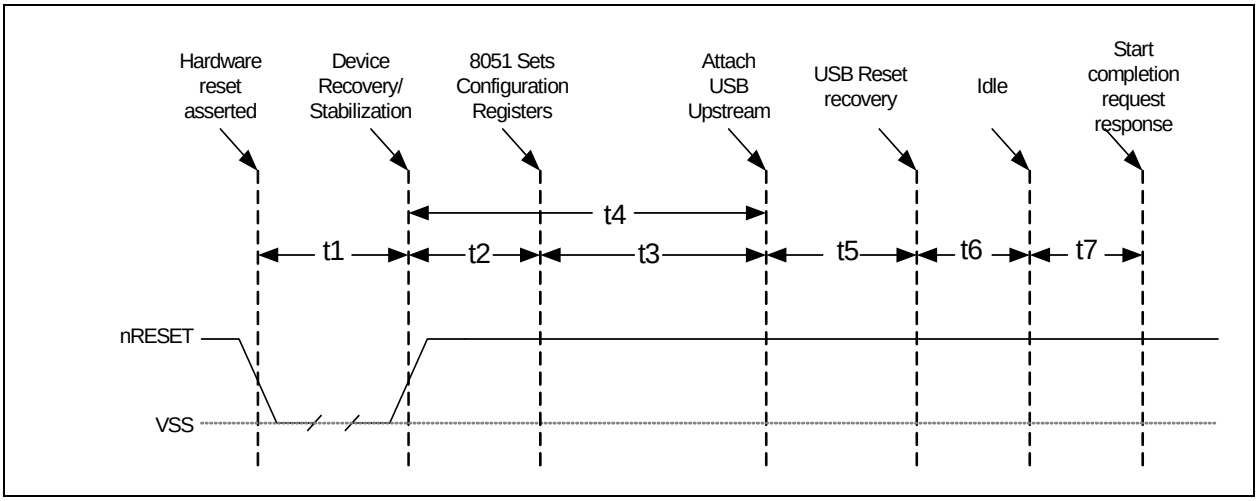


TABLE 7-2: NRESET TIMING FOR EEPROM MODE

Name	Description	MIN	TYP	MAX	Units
t1	nRESET asserted	1			µsec
t2	Device recovery/stabilization			500	µsec
t3	8051 programs device configuration		20	50	msec
t4	USB attach			100	msec
t5	Host acknowledges attach and signals USB reset	100			msec
t6	USB idle		Undefined		msec
t7	Ready to handle requests (with or without data)			5	msec

Note: All power supplies must have reached the operating levels mandated in Section 9.0, "DC Parameters", prior to (or coincident with) the assertion of nRESET.

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7.3.2 USB BUS RESET

In response to the upstream port signaling a reset to the device, the device does the following:

1. Sets default address to ‘0’.
2. Sets configuration to: Unconfigured.
3. All transactions are stopped.
4. Processor reinitializes and restarts.
5. All media interfaces are disabled.

8.0 AC SPECIFICATIONS

8.1 Oscillator/Crystal

Parallel Resonant, Fundamental Mode, 24 MHz ± 350 ppm.

FIGURE 8-1: TYPICAL CRYSTAL CIRCUIT

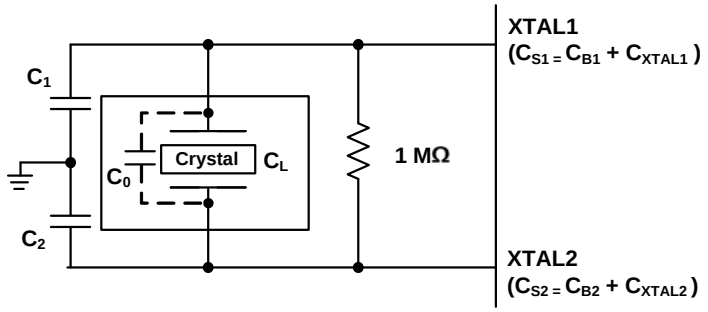


TABLE 8-1: CRYSTAL CIRCUIT LEGEND

Symbol	Description	In Accordance With
C_0	Crystal shunt capacitance	Crystal manufacturer's specification (See Note 8-1)
C_L	Crystal load capacitance	
C_B	Total board or trace capacitance	OEM board design
C_S	Stray capacitance	Microchip IC and OEM board design
C_{XTAL}	XTAL pin input capacitance	Microchip IC
C_1	Load capacitors installed on OEM board	Calculated values based on Figure 8-2, "Capacitance Formulas" (See Note 8-2)
C_2		

FIGURE 8-2: CAPACITANCE FORMULAS

$$C_1 = 2 \times (C_L - C_0) - C_{S1}$$

$$C_2 = 2 \times (C_L - C_0) - C_{S2}$$

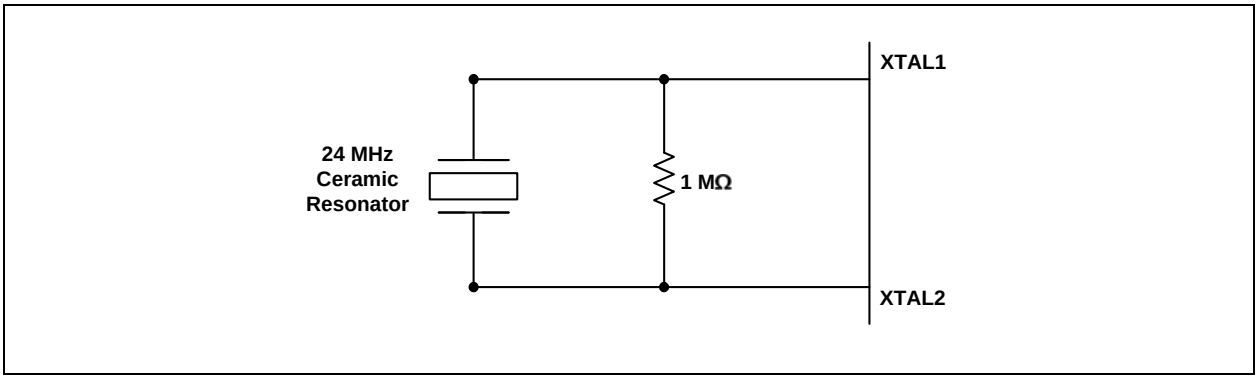
Note 8-1 C_0 is usually included (subtracted by the crystal manufacturer) in the specification for C_L and should be set to '0' for use in the calculation of the capacitance formulas in Figure 8-2, "Capacitance Formulas". However, the OEM PCB itself may present a parasitic capacitance between XTAL1 and XTAL2. For an accurate calculation of C_1 and C_2, take the parasitic capacitance between traces XTAL1 and XTAL2 into account.

Note 8-2 Each of these capacitance values is typically approximately 18 pF.

8.2 Ceramic Resonator

24 MHz ± 350 ppm

FIGURE 8-3: CERAMIC RESONATOR USAGE WITH MICROCHIP IC



8.3 External Clock

50% Duty cycle ± 10%, 24/48 MHz ± 350 ppm, Jitter < 100 ps rms.

The external clock is recommended to conform to the signaling level designated in the JESD76-2 specification on 1.8 V CMOS Logic. XTAL2 should be treated as a no connect.

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9.0 DC PARAMETERS

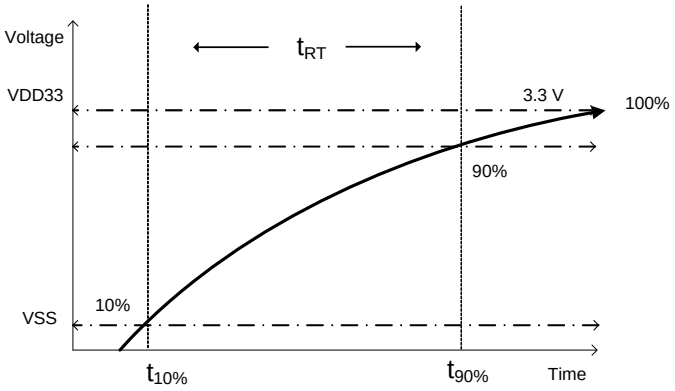
9.1 Maximum Ratings

Parameter	Symbol	MIN	MAX	Units	Comments
Storage Temperature	T_A	-55	150	°C	
Lead Temperature				°C	Please refer to JEDEC specification J-STD-020D.
3.3 V supply voltage	V_{DD33}	-0.5	4.0	V	
Voltage on USB+ and USB- pins		-0.5	(3.3 V supply voltage + 2) ≤ 6	V	
Voltage on CRD_PWR0, CRD_PWR1, CRD_PWR2 and CRD_PWR3		-0.5	V_{DD33} + 0.3	V	When internal power FET operation of these pins are enabled, these pins may be simultaneously shorted to ground or any voltage up to 3.63 V indefinitely, without damage to the device as long as V_{DD33} is less than 3.63 V and T_A is less than 70^oC.
Voltage on any signal pin		-0.5	V_{DD33} + 0.3	V	
Voltage on XTAL1		-0.5	3.6	V	
Voltage on XTAL2		-0.5	V_{DD18} + 0.3	V	

Note 9-1 Stresses above the specified parameters may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any condition above those indicated in the operation sections of this specification is not implied.

Note 9-2 When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.

FIGURE 9-1: SUPPLY RISE TIME MODEL



Note 9-3 When powering the device, the maximum power supply ramp time should be set at a rate faster than 400 µs. This speed is important to ensure that the device resets properly. Measure rise time at 10% and 90%.

9.2 Operating Conditions

Parameter	Symbol	MIN	MAX	Units	Comments
Operating Temperature					Ambient temperature in still air.
Commercial Part	T_A	0	70	°C	
Industrial Part	T_A	-40	85	°C	
3.3 V supply voltage	V_{DD33}	3.0	3.6	V	(Note 9-4)
3.3 V supply rise time	t_{RT}	0	400	µs	(See Figure 9-1 and Note 9-3)
Voltage on USB+ and USB- pins		-0.3	5.5	V	If any 3.3 V supply voltage drops below 3.0 V, then the MAX becomes: (3.3 V supply voltage) + 0.5 ≤ 5.5
Voltage on any signal pin		-0.3	V_{DD33}	V	
Voltage on XTAL1		-0.3	V_{DD33}	V	
Voltage on XTAL2		-0.3	V_{DD18}	V	

Note 9-4 A 3.3 V regulator with an output tolerance of 1% must be used if the output of the internal power FET's must support a 5% tolerance.

9.3 DC Electrical Characteristics

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
I, IPU, IPD Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Pull Down	PD		72		µA	
Pull Up	PU		58		µA	
IS Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Hysteresis	V_{HYSI}		420		mV	
ICLK Input Buffer						
Low Input Level	V_{ILCK}			0.5	V	
High Input Level	V_{IHCK}	1.4			V	
Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0 to V_{DD33}

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Parameter	Symbol	MIN	TYP	MAX	Units	Comments
Input Leakage						
(All I and IS buffers)						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	µA	V_{IN} = V_{DD33}
O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA @ V_{DD33}= 3.3 V
High Output Level	V_{OH}	V_{DD33} - 0.4			V	I_{OH} = -12 mA @ V_{DD33}= 3.3 V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DD33} (Note 9-5)
I/O12, I/O12PU & I/O12PD Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA @ V_{DD33}= 3.3 V
High Output Level	V_{OH}	V_{DD33} - 0.4			V	I_{OH} = -12 mA @ V_{DD33}= 3.3 V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DD33} (Note 9-5)
Pull Down	PD		72		µA	
Pull Up	PU		58		µA	
IO-U (Note 9-6)						
I-R (Note 9-7)						
I/O200 Integrated Power FET for CRD_PWR0, CRD_PWR1, CRD_PWR2 and CRD_PWR3						
High Output Current Mode	I_{OUT}	200			mA	$Vdrop_{FET}$ = 0.46 V
Low Output Current Mode (Note 9-8)	I_{OUT}	100			mA	$Vdrop_{FET}$ = 0.23 V
On Resistance (Note 9-8)	R_{DSON}			2.1	Ω	I_{FET} = 70 mA
Output Voltage Rise Time	t_{DSON}			800	µs	C_{LOAD} = 10 µF
Supply Current Unconfigured	I_{CCINIT}		80	90	mA	

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
Supply Current Active Full Speed	I_{CC}		110	140	mA	V_{DD33} = 3.3 V
High Speed	I_{CC}		135	165	mA	
Supply Current Suspend	I_{CSBY}		350	750	µA	V_{DD33}, V = 3.3 V
Industrial Temperature Suspend	I_{CSBYI}		350	950	µA	

Note 9-5 Output leakage is measured with the current pins in high impedance.

Note 9-6 See The USB 2.0 Specification, Chapter 7, for USB DC electrical characteristics

Note 9-7 RBIAS is a 3.3 V tolerant analog pin.

Note 9-8 Output current range is controlled by program software, software disables FET during short circuit condition.

9.4 Capacitance

T_A = 25°C; fc = 1 MHz; V_{DD}, V_{DDP} = 1.8 V

Parameter	Symbol	Limits			Unit	Test Condition
		MIN	TYP	MAX		
Clock Input Capacitance	C_{XTAL}			2	pF	All pins (except USB pins and pins under test) are tied to AC ground.
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

9.5 Package Thermal Specification

TABLE 9-1: 128-PIN VTQFP PACKAGE THERMAL PARAMETERS

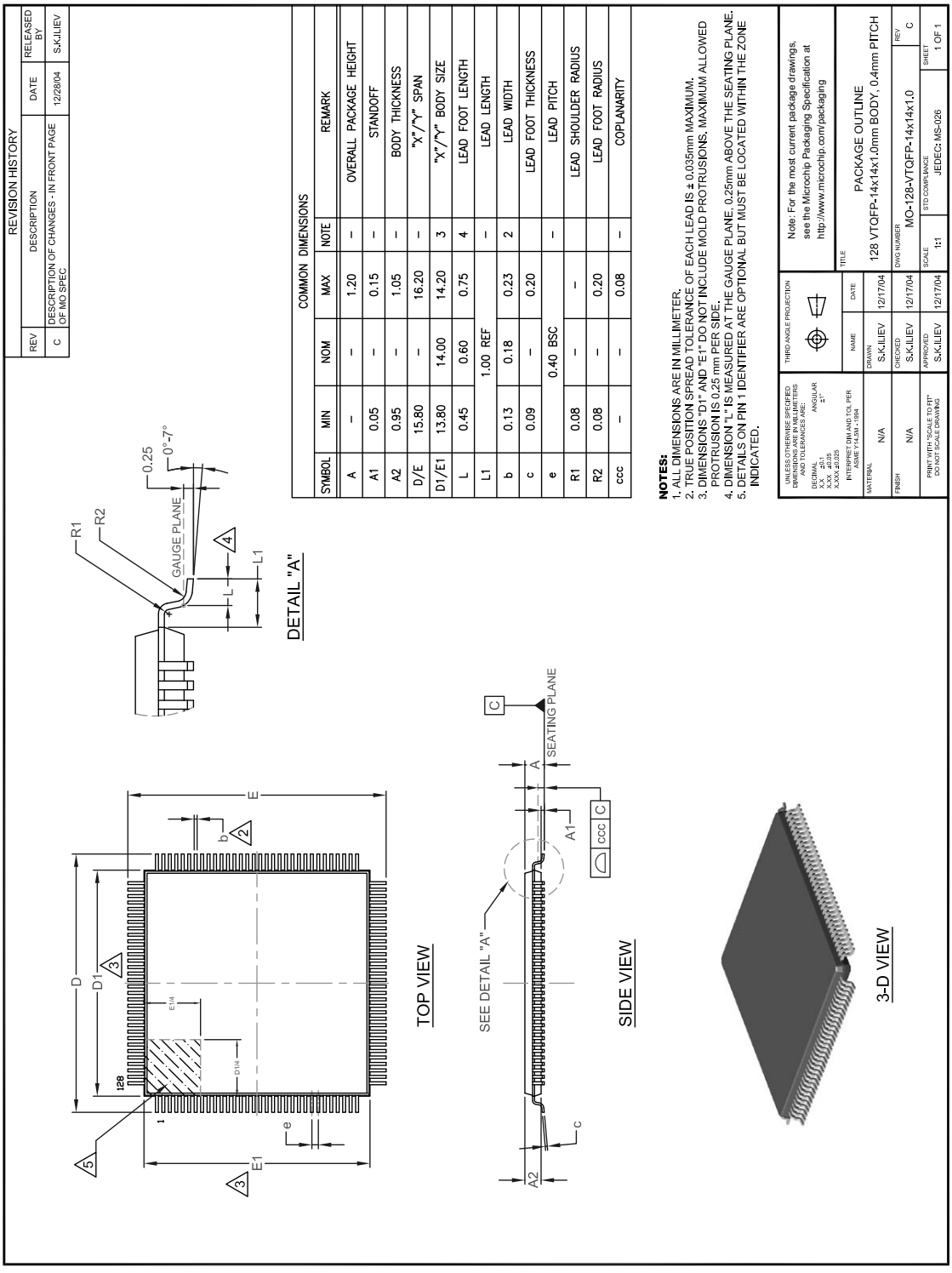
Parameter	Velocity (meters/sec)	Symbol	Value	Unit
Thermal Resistance	0	Θ_{JA}	55	°C/W
	1		48	
	2		45	
Junction-to-Top-of-Package	0	Ψ_{JT}	18	°C/W
	1		18	
	2		18	

Note 9-9 Thermal parameters are measured or estimated for devices with the exposed pad soldered to thermal vias in a multilayer 2S2P PCB per JESD51. Thermal resistance is measured from the die to the ambient air.

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10.0 PACKAGE OUTLINE

FIGURE 10-1: 128-PIN VTQFP, 14X14X1.0 MM BODY, 2.0 MM PITCH



APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
DS00002005A (10-22-15)	Replaces previous SMSC version Rev. 2.0 (09-29-09)	

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X]	-	XXX	-	[X]
Device	Temperature Range		Package		Internal Microchip Code

Device:	USB2250, USB2250i, USB2251, USB2251i	
Temperature Range:	Blank	= 0°C to +70°C (Commercial)
	i	= -40°C to+85°C (Industrial)
Package:	NU	= 128-pin VTQFN

Examples:

1. **USB2250-NU-06**
   128-pin VTQFN RoHS Compliant package, Commercial Temp, Tray
2. **USB2250-NU-05**
   128-pin VTQFN RoHS Compliant package, Commercial Temp, Tray
3. **USB2251-NU-06**
   128-pin VTQFN RoHS Compliant package, Commercial Temp, Tray
4. **USB2251-NU-05**
   128-pin VTQFN RoHS Compliant package, Commercial Temp, Tray
5. **USB2250i-NU-06**
   128-pin VTQFN RoHS Compliant package, Industrial Temp, Tray

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