DAC Programmable CCFL Switching Regulator (Bits-to-Nits™)

FEATURES

- Wide Battery Input Range: 4.5V to 30V
- **Grounded Lamp or Floating Lamp Configurations**
- Open Lamp Protection
- **Precision 50μA Full-Scale DAC Programming Current**
- Standard SPI Mode or Pulse Mode
- **DAC Setting Is Retained in Shutdown**

APPLICATIONS

- Notebook and Palmtop Computers
- Portable Instruments
- Retail Terminals

DESCRIPTION

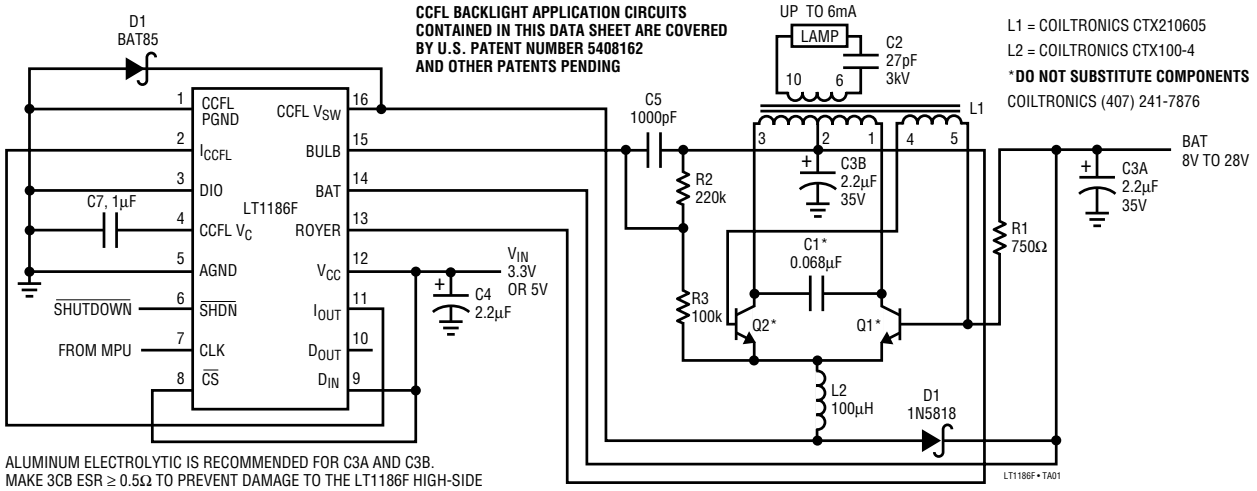
The LT®1186F is a fixed frequency, current mode, switching regulator that provides the control function for Cold Cathode Fluorescent Lighting (CCFL). The IC includes an efficient high current switch, an oscillator, output drive logic, control circuitry and a micropower 8-bit 50μA full-scale current output DAC. The DAC provides simple "bits-to-lamp current control" and communicates in two interface modes including standard SPI mode and pulse mode. On power-up, the DAC counter resets to half-scale and the DAC configures to SPI or pulse mode depending on the $\overline{CS}$ signal level. In SPI mode, the system microprocessor serially transfers the present 8-bit data and reads back the previous 8-bit data. In pulse mode, the upper six bits of the DAC configure as increment-only (1-wire interface) or increment/decrement (2-wire interface) operation depending on the D_{IN} signal level.

The LT1186F control circuitry operates from a logic supply voltage of 3.3V or 5V. The IC also has a battery supply voltage pin that operates from 4.5V to 30V. The LT1186F draws 6mA typical quiescent current. An active low shutdown pin reduces total supply current to 35μA for standby operation and the DAC retains its last setting. A 200kHz switching frequency minimizes magnetic component size. Current mode switching techniques with cycle-by-cycle limiting gives high reliability and simple loop frequency compensation. The LT1186F is available in a 16-pin narrow SO package.

LT, LTC and LT are registered trademarks of Linear Technology Corporation.
Bits-to-Nits is a trademark of Linear Technology Corporation. 1 Nit = 1 Candela/meter^2

TYPICAL APPLICATION

90% Efficient Floating CCFL with 1-Wire (Increment Only) Pulse Mode Control of Lamp Current



ALUMINUM ELECTROLYTIC IS RECOMMENDED FOR C3A AND C3B.
MAKE 3CB ESR ≥ 0.5Ω TO PREVENT DAMAGE TO THE LT1186F HIGH-SIDE SENSE RESISTOR DUE TO SURGE CURRENTS AT TURN-ON

C1 MUST BE A LOW LOSS CAPACITOR, C1 = WIMA MKP-20

Q1, Q2 = ZETEX ZTX849 OR ROHM 2SC5001

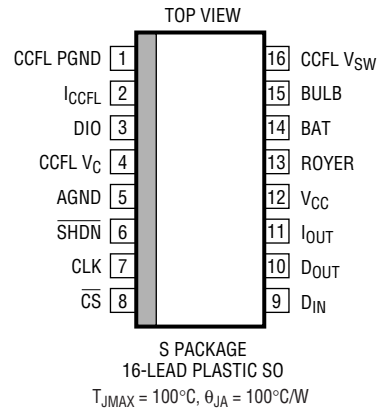
0μA TO 50μA I_{CCFL} CURRENT GIVES 0mA TO 6mA LAMP CURRENT FOR A TYPICAL DISPLAY.

FOR ADDITIONAL CCFL/LCD CONTRAST APPLICATION CIRCUITS, REFER TO THE LT1182/83/84/84F DATA SHEET

ABSOLUTE MAXIMUM RATINGS

V_{CC} 7V
BAT, Royer, BULB 30V
CCFL V_{SW} 60V
Shutdown 6V
I_{CCFL} Input Current 10mA
DIO Input Current (Peak, <100ms) 100mA
Digital Inputs ..... –0.3V to V_{CC} + 0.3V
Digital Outputs ..... –0.3V to V_{CC} + 0.3V
DAC Output Voltage ..... –20V to V_{CC} + 0.3V
Junction Temperature (Note 1) ..... 100°C
Operating Ambient Temperature Range
LT1186FC ..... 0°C to 100°C
LT1186FI ..... –40°C to 100°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S PACKAGE
16-LEAD PLASTIC SO
T_{JMAX} = 100°C, θ_{JA} = 100°C/W

ORDER PART NUMBER

LT1186FCS
LT1186FIS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = $\overline{SHUTDOWN}$ = D_{IN} = $\overline{CS}$ = 3.3V, BAT = Royer = BULB = 12V, I_{CCFL} = CCFL V_{SW} = Open, D_{OUT} = Three-State, DIO = I_{OUT} = CLK = GND, CCFL V_C = 0.5V, unless otherwise specified.

xSYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Supply Current	3V ≤ V_{CC} ≤ 6.5V, 1/2 Full-Scale DAC Output Current	●		6	9.5	mA
$I_{\overline{SHDN}}$	$\overline{SHUTDOWN}$ Supply Current	$\overline{SHUTDOWN}$ = 0V, CCFL V_C Open (Note 2)			35	70	µA
	$\overline{SHUTDOWN}$ Input Bias Current	$\overline{SHUTDOWN}$ = 0V, CCFL V_C = Open			5	10	µA
	$\overline{SHUTDOWN}$ Threshold Voltage		●	0.45	0.85	1.2	V
f	Switching Frequency	Measured at CCFL V_{SW}, I_{SW} = 50mA, I_{CCFL} = 100µA, CCFL V_C = Open	 ●	175 160	200 200	225 240	kHz kHz
DC(MAX)	Maximum Switch Duty Cycle	Measured at CCFL V_{SW}	 ●	80 75	85 85		% %
BV	Switch Breakdown Voltage	Measured at CCFL V_{SW}		60	70		V
	Switch Leakage Current	V_{SW} = 12V, Measured at CCFL V_{SW} V_{SW} = 30V, Measured at CCFL V_{SW}				20 40	µA µA
	I_{CCFL} Summing Voltage	3V ≤ V_{CC} ≤ 6.5V	 ●	0.425 0.385	0.465 0.465	0.505 0.555	V V
	ΔI_{CCFL} Summing Voltage for ΔInput Programming Current	I_{CCFL} = 0µA to 100µA			5	15	mV
	CCFL V_C Offset Sink Current	CCFL V_C = 1.5V, Positive Current Measured into Pin		–5	5	15	µA
	ΔCCFL V_C Source Current for ΔI_{CCFL} Programming Current	I_{CCFL} = 25µA, 50µA, 75µA, 100µA, CCFL V_C = 1.5V T_J < 0°C	● ●	4.70 4.60	4.95 4.95	5.20 5.20	µA/µA µA/µA
	CCFL V_C to DIO Current Servo Ratio	DIO = 5mA out of Pin, Measure I(V_C) at CCFL V_C = 1.5V	●	94	99	104	µA/mA
	CCFL V_C Low Clamp Voltage	V_{BAT} – V_{BULB} = BULB Protect Servo Voltage	●		0.1	0.3	V
	CCFL V_C High Clamp Voltage	I_{CCFL} = 100µA	●	1.7	2.1	2.4	V
	CCFL V_C Switching Threshold	CCFL V_{SW} DC = 0%	●	0.6	0.95	1.3	V

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
	CCFL High-Side Sense Servo Current	I_{CCFL} = 100µA, I(V_C) = 0µA at CCFL V_C = 1.5V T_J < 0°C	● ●	0.93 0.91	1.00 1.00	1.07 1.07	A A
	CCFL High-Side Sense Servo Current Line Regulation	BAT = 5V to 30V, I_{CCFL} = 100µA, I(V_C) = 0µA at CCFL V_C = 1.5V			0.1	0.16	%/V
	CCFL High-Side Sense Supply Current	Current Measured into BAT and Royer Pins	●	50	100	150	µA
	BULB Protect Servo Voltage	I_{CCFL} = 100µA, I(V_C) = 0µA at CCFL V_C = 1.5V, Servo Voltage Measured between BAT and BULB Pins	●	6.5	7.0	7.5	V
	BULB Input Bias Current	I_{CCFL} = 100µA, I(V_C) = 0µA at CCFL V_C = 1.5V			5	9	µA
I_{LIM}	CCFL Switch Current Limit	Duty Cycle = 50% Duty Cycle = 75% (Note 3)	● ●	1.25 0.9	1.9 1.6	3.0 2.6	A A
V_{SAT}	CCFL Switch On Resistance	CCFL I_{SW} = 1A	●		0.6	1.0	Ω
$\frac{\Delta I_Q}{\Delta I_{SW}}$	Supply Current Increase During CCFL Switch On Time	CCFL I_{SW} = 1A			20	30	mA/A
	DAC Resolution				8		Bits
	DAC Full-Scale Current	V(I_{OUT}) = 0.465V, Measured in SPI Mode	 ●	48.5 47.0	50 50	51.5 53.0	µA µA
	DAC Zero Scale Current	V(I_{OUT}) = 0.465V, Measured in SPI Mode				200	nA
	DAC Differential Nonlinearity		●			±2.0	LSB
	DAC Supply Voltage Rejection	3V ≤ V_{CC} ≤ 6.5V, I_{OUT} = Full Scale, V(I_{OUT}) = 0.465V	●		2	4	LSB
	Logic Input Current	0V ≤ V_{IN} ≤ V_{CC}	●			±1	µA
V_{IH}	High Level Input Voltage	V_{CC} = 3.3V V_{CC} = 5V	● ●	1.9 2			V V
V_{IL}	Low Level Input Voltage	V_{CC} = 3.3V V_{CC} = 5V	● ●			0.45 0.80	V V
V_{OH}	High Level Output Voltage	V_{CC} = 3.3V, I_O = 400µA V_{CC} = 5V, I_O = 400µA	● ●	2.1 2.4			V V
V_{OL}	Low Level Output Voltage	V_{CC} = 3.3V, I_O = 1mA V_{CC} = 5V, I_O = 2mA	● ●			0.4 0.4	V V
I_{OZ}	Three-State Output Leakage	$V_{\overline{CS}}$ = V_{CC}	●			±5	µA
SERIAL INTERFACE (Notes 4, 5)							
f_{CLK}	Clock Frequency		●			2	MHz
t_{CKS}	Setup Time, CLK↓ Before $\overline{CS}$↓		●	150			ns
t_{CSS}	Setup Time, $\overline{CS}$↓ Before CLK↑		●	400			ns
t_{DV}	$\overline{CS}$↓ to D_{OUT} Valid	See Test Circuits	●	150			ns
t_{DS}	Data in Setup Time Before CLK↑		●	150			ns
t_{DH}	Data in Hold Time After CLK↑		●	150			ns
t_{DO}	CLK↓ to D_{OUT} Valid	See Test Circuits	●	150			ns
t_{CKHI}	CLK High Time		●	200			ns
t_{CKLO}	CLK Low Time		●	250			ns
t_{CSH}	CLK↓ Before $\overline{CS}$↑		●	150			ns
t_{DZ}	$\overline{CS}$↑ to D_{OUT} In Hi-Z	See Test Circuits	●			400	ns
t_{CKH}	$\overline{CS}$↑ Before CLK↑		●			400	ns

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = $\overline{SHUTDOWN}$ = D_{IN} = $\overline{CS}$ = 3.3V, BAT = Royer = BULB = 12V, I_{CCFL} = CCFL V_{SW} = Open, D_{OUT} = Three-State, DIO = I_{OUT} = CLK = GND, CCFL V_C = 0.5V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
SERIAL INTERFACE (Notes 4, 5)							
t_{CSLO}	$\overline{CS}$ Low Time	f_{CLK} = 2MHz	●	4550			ns
t_{CSHI}	$\overline{CS}$ High Time		●	400			ns

The ● denotes specifications which apply over the specified operating temperature range.

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

LT1186FCS: $T_J = T_A + (P_D)(100°C/W)$

Note 2: Does not include switch leakage.

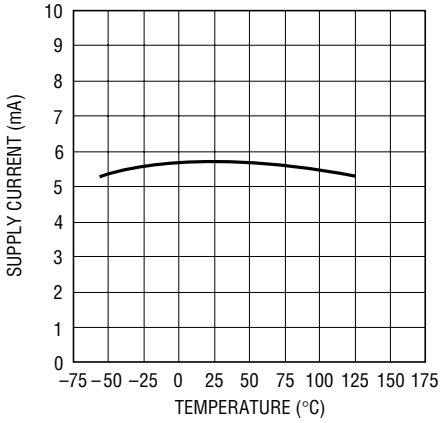
Note 3: For duty cycles (DC) between 50% and 80%, minimum guaranteed switch current is given by I_{LIM} = 1.4(1.393 – DC) for the LT1186F due to internal slope compensation circuitry.

Note 4: Timings for all input signals are measured at 0.8V for a High-to-Low transition and 2.0V for a Low-to-High transition.

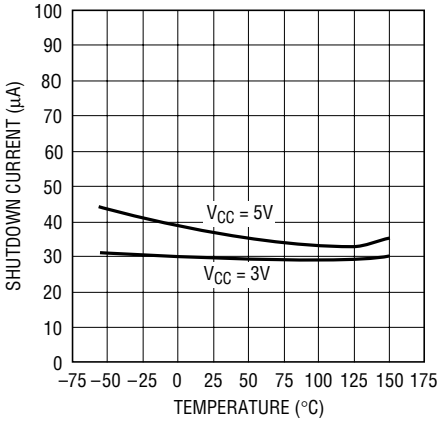
Note 5: Timings are guaranteed but not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

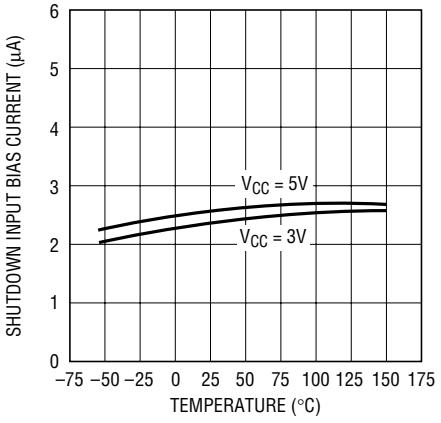
Supply Current vs Temperature



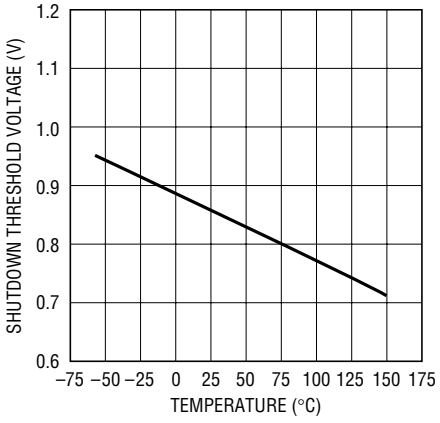
Shutdown Current vs Temperature



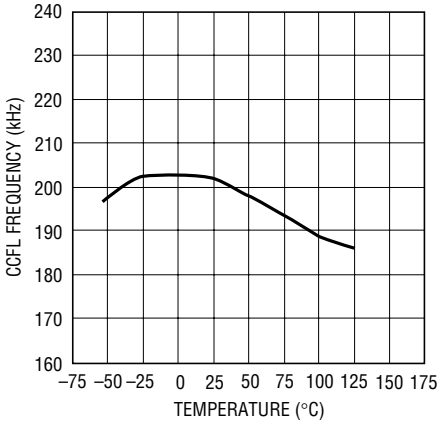
Shutdown Input Bias Current vs Temperature



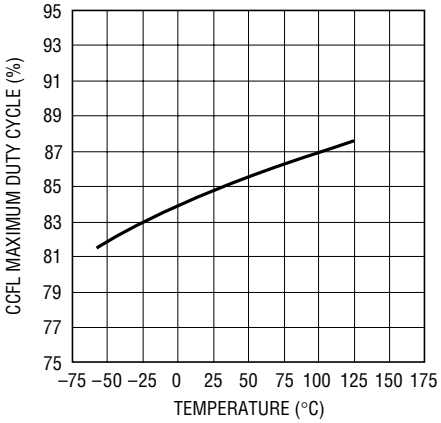
Shutdown Threshold Voltage vs Temperature



Frequency vs Temperature

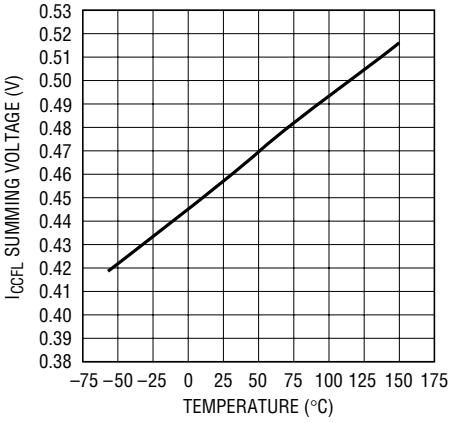


Maximum Duty Cycle vs Temperature



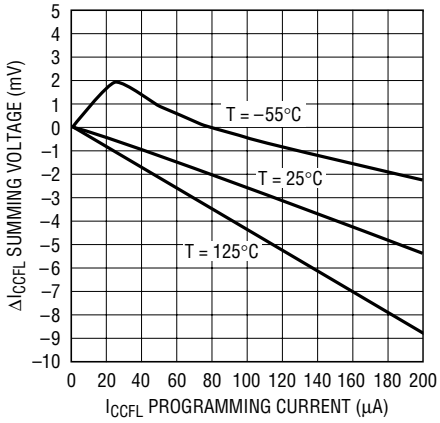
TYPICAL PERFORMANCE CHARACTERISTICS

I_{CCFL} Summing Voltage vs Temperature



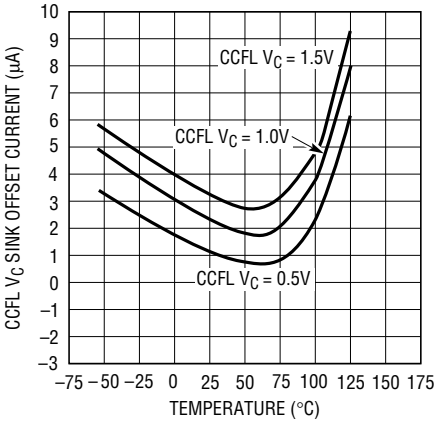
LT1186F • G07

I_{CCFL} Summing Voltage Load Regulation



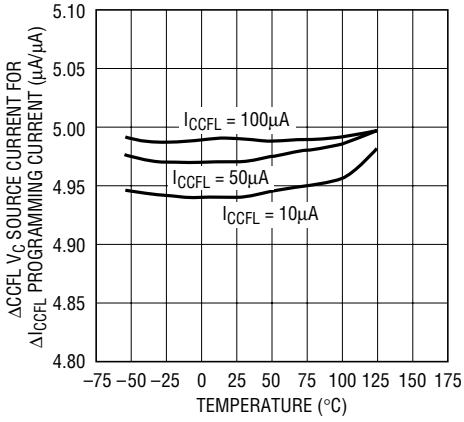
LT1186F • G08

V_C Sink Offset Current vs Temperature



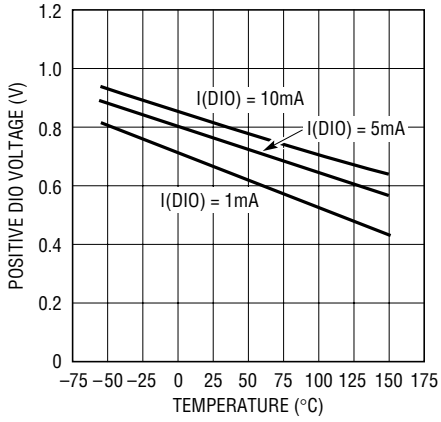
LT1186F • G09

ΔCCFL V_C Source Current for ΔI_{CCFL} Programming Current vs Temperature



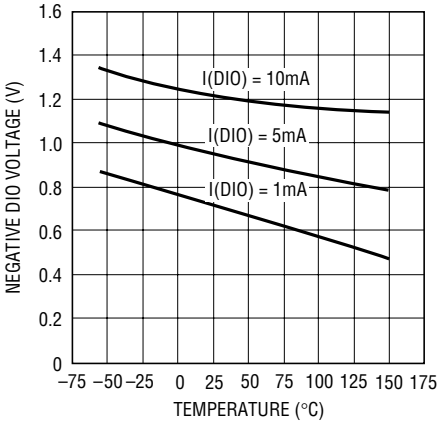
LT1186F • G10

Positive DIO Voltage vs Temperature



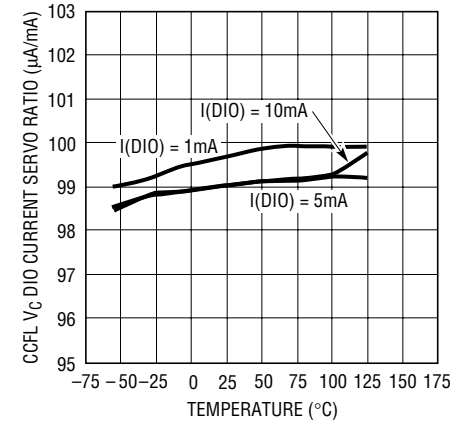
LT1186F • G11

Negative DIO Voltage vs Temperature



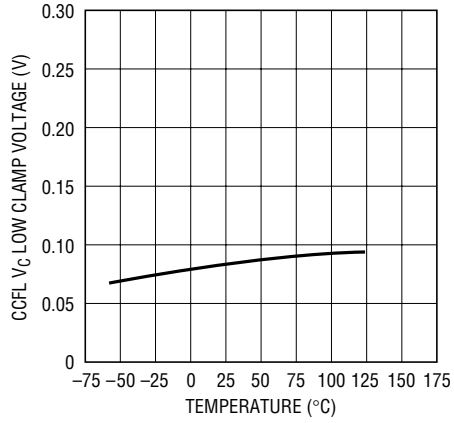
LT1186F • G12

V_C to DIO Current Servo Ratio vs Temperature



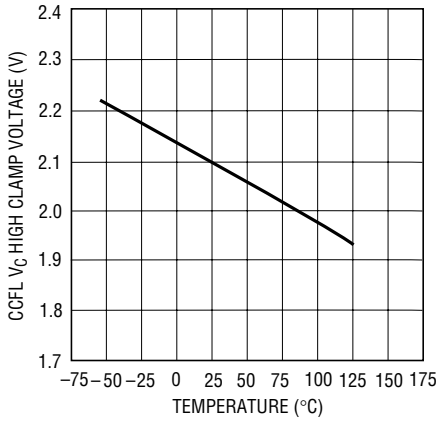
LT1186F • G13

V_C Low Clamp Voltage vs Temperature



LT1186F • G14

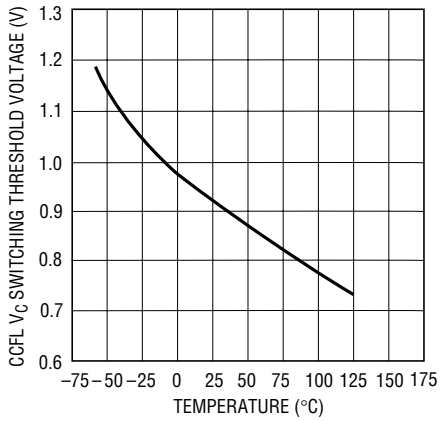
V_C High Clamp Voltage vs Temperature



LT1186F • G15

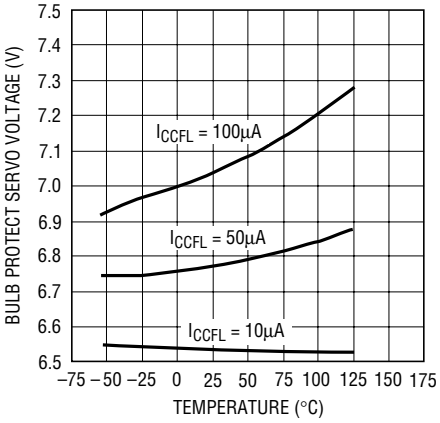
TYPICAL PERFORMANCE CHARACTERISTICS

V_C Switching Threshold vs Temperature



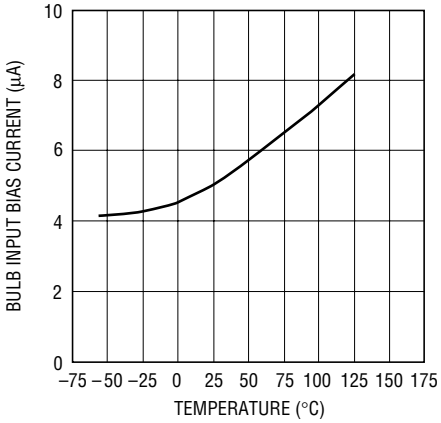
LT1186F • G16

BULB Protect Servo Voltage vs Temperature



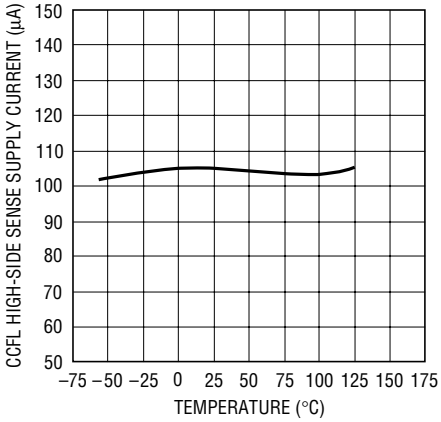
LT1186F • G17

BULB Input Bias Current vs Temperature



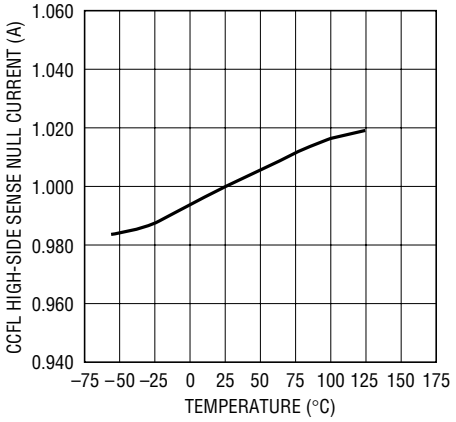
LT1186F • G18

High-Side Sense Supply Current vs Temperature



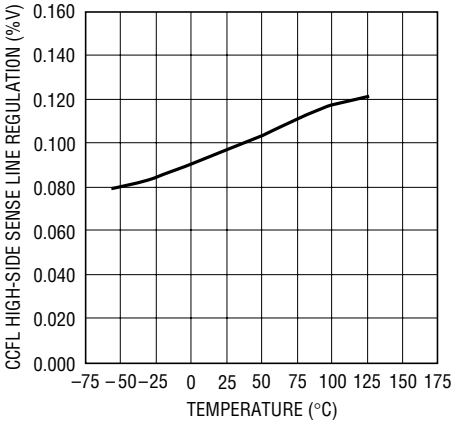
LT1186F • G19

High-Side Sense Null Current vs Temperature



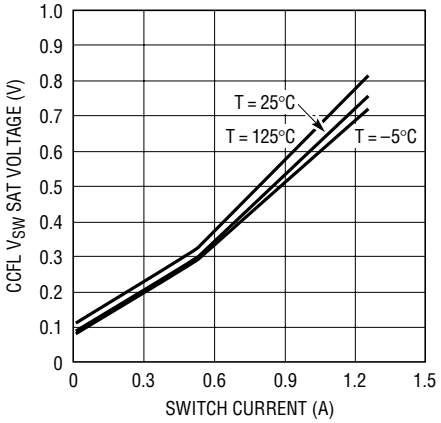
LT1186F • G20

High-Side Sense Null Current Line Regulation vs Temperature



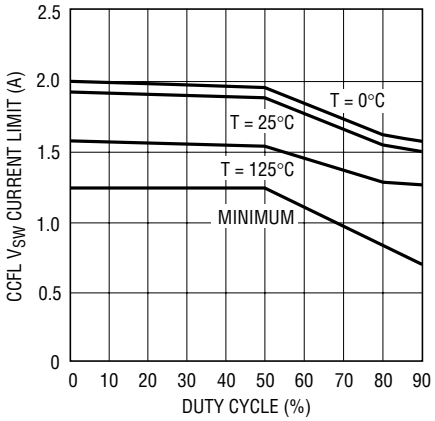
LT1186F • G21

V_{SW} Sat Voltage vs Switch Current



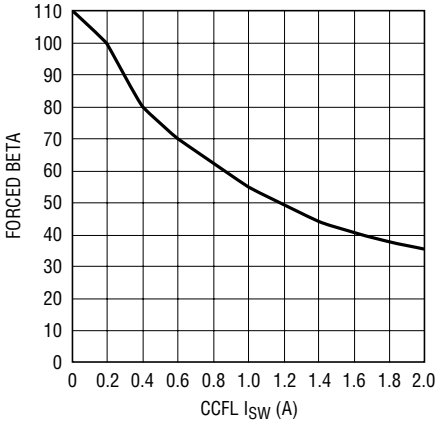
LT1186F • G22

V_{SW} Current Limit vs Duty Cycle



LT1186F • G23

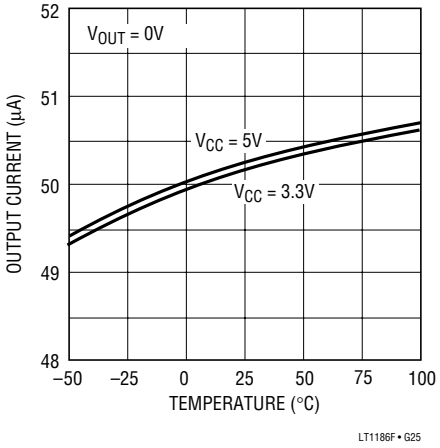
Forced Beta vs I_{SW} on V_{SW}



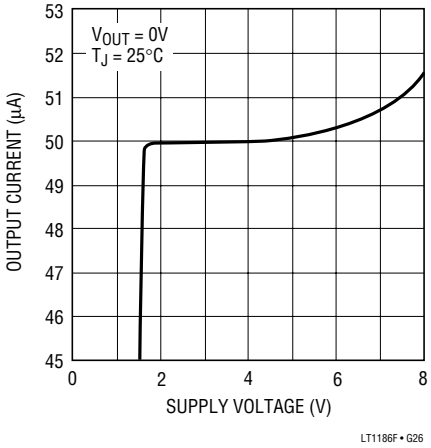
LT1186F • G24

TYPICAL PERFORMANCE CHARACTERISTICS

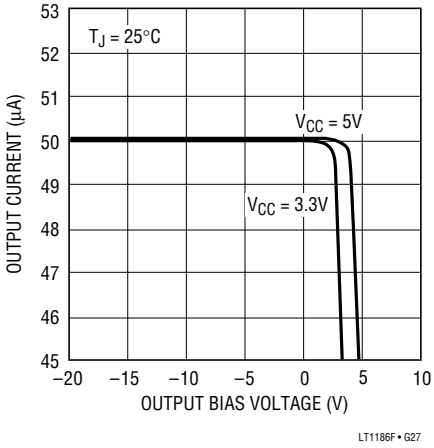
DAC I_{OUT} vs Temperature



DAC I_{OUT} vs Supply Voltage



DAC I_{OUT} vs I_{OUT} Bias Voltage



PIN FUNCTIONS

CCFL PGND (Pin 1): This pin is the emitter of an internal NPN power switch. CCFL switch current flows through this pin and permits internal, switch-current sensing. The regulator provides a separate analog ground and power ground to isolate high current ground paths from low current signal paths. Linear Technology recommends the use of star-ground layout techniques.

I_{CCFL} (Pin 2): This pin is the input to the CCFL lamp current programming circuit. This pin internally regulates to 465mV. The pin accepts a DC input current signal of 0µA to 50µA full scale from the DAC. This input signal is converted to a 0µA to 250µA source current at the CCFL V_C pin. As input programming current increases, the regulated lamp current increases. For a typical 6mA lamp, the range of input programming current is about 0µA to 50µA.

DIO (Pin 3): This pin is the common connection between the cathode and anode of two internal diodes. The remaining terminals of the two diodes connect to ground. In a grounded-lamp configuration, DIO connects to the low voltage side of the lamp. Bidirectional lamp current flows in the DIO pin and thus the diodes conduct alternately on half cycles. Lamp current is controlled by monitoring one-half of the average lamp current. The diode conducting on negative half cycles has one-tenth of its current diverted to the CCFL V_C pin. This current nulls against the source current provided by the lamp-current programmer circuit. A single capacitor on the CCFL V_C pin provides both stable loop compensation and an averaging function to the half-wave-rectified sinusoidal lamp current. Therefore, input programming current relates to one-half of average lamp current. This scheme reduces the number of loop compensation components and permits faster loop transient response in comparison to previously published circuits. If a floating lamp configuration is used, ground the DIO pin.

CCFL V_C (Pin 4): This pin is the output of the lamp current programmer circuit and the input of the current comparator for the CCFL regulator. Its uses include frequency compensation, lamp-current averaging for grounded-lamp circuits and current limiting. The voltage on the CCFL V_C pin determines the current trip level for switch turn-off. During normal operation this pin sits at a voltage between 0.95V (zero switch current) and 2.0V (maximum switch current) with respect to analog ground (AGND). This pin has a high impedance output and permits external voltage clamping to adjust current limit. A single capacitor to ground provides stable loop compensation. This simplified loop compensation method permits the CCFL regulator to exhibit single-pole transient response behavior and virtually eliminates transformer output overshoot.

PIN FUNCTIONS

AGND (Pin 5): This is the low current analog ground. It is the negative sense terminal for the internal 1.24V reference and the I_{CCFL} summing voltage in the LT1186F. Connect low current signal paths that terminate to ground and frequency compensation components that terminate to ground directly to this pin for best regulation and performance.

$\overline{\text{SHDN}}$ (Pin 6): Pulling this pin low causes complete regulator shutdown with quiescent current typically reduced to 35μA. If the pin is not used, use a pull-up resistor to force a logic high level (maximum of 6V) or tie directly to V_{CC}. In a shutdown condition, the DAC retains its last output current setting and returns to this level when the logic-low signal at the shutdown pin is removed.

CLK (Pin 7): This pin is the shift clock for the DAC. This clock synchronizes the serial data and is a Schmitt trigger input. In standard SPI mode, the clock shifts data into D_{IN} and out of D_{OUT} on the rising and falling edges of the clock respectively. In pulse mode, the rising edge of the clock either increments or decrements the counter. This action depends on the choice of a 1-wire interface (increment only) or a 2-wire interface (increment/decrement).

$\overline{\text{CS}}$ (Pin 8): This pin is the chip select input for the DAC. In SPI mode, a logic low on the $\overline{\text{CS}}$ pin enables the DAC to receive and transfer 8-bit serial data. After the serial input data is shifted in, a rising edge of $\overline{\text{CS}}$ transfers the data into the counter, the DAC assumes the new I_{OUT} value and the D_{OUT} pin returns to the high impedance state. On power up, a logic high places the DAC into pulse mode. Pulling $\overline{\text{CS}}$ low after this places the DAC into SPI mode until V_{CC} resets.

D_{IN} or UP/$\overline{\text{DN}}$ (Pin 9): This pin is the digital input for the DAC. In SPI mode, the 8-bit serial data is shifted into the D_{IN} input on each rising edge of the clock signal. In pulse mode, on power up, a logic high at D_{IN} transfers the pin function from D_{IN} to UP/$\overline{\text{DN}}$, puts the counter into increment-only mode and the pin function shifts to up or down increment control of DAC output current. If UP/$\overline{\text{DN}}$ receives a logic-low signal, the counter configures to increment/decrement mode until V_{CC} resets.

D_{OUT} (Pin 10): This pin is the digital output for the DAC. In SPI mode, D_{OUT} is in three-state until $\overline{\text{CS}}$ falls low. The D_{OUT} pin then serially transfers the previous 8-bit data on every falling edge of the clock. When $\overline{\text{CS}}$ rises high again, D_{OUT} returns to a three-state condition. In pulse mode, D_{OUT} is always three-stated.

I_{OUT} (Pin 11): This pin is the analog current output for the DAC and provides an output current of 50 ±3μA over temperature. This pin can be biased from –20V to 2V for a 3.3V V_{CC} supply voltage or from –20V to 2.5V for a 5V V_{CC} supply voltage. However, this pin is tied to the I_{CCFL} pin and provides the programming current which sets operating lamp current. The I_{OUT} pin has very little bias voltage change when it is tied to the I_{CCFL} pin as I_{CCFL} is regulated. The programming current is sourced from the I_{OUT} pin and sunk by the I_{CCFL} pin.

V_{CC} (Pin 12): This is the supply pin for the LT1186F. The IC accepts an input voltage range of 3V minimum to 6.5V maximum with little change in quiescent current (zero switch current). An internal, low-dropout regulator provides a 2.4V supply for most of the internal circuitry. Supply current increases as switch current increases at a rate approximately 1/50 of switch current. This corresponds to a forced Beta of 50 for the power switch. The IC incorporates undervoltage lockout by sensing regulator dropout and locking out switching for input voltages below 2.5V. Hysteresis is not used to maximize the useful range of input voltage. The typical input voltage is a 3.3V or 5V logic supply.

ROYER (Pin 13): This pin connects to the center-tapped primary of the Royer converter and is used with the BAT pin in a floating-lamp configuration where lamp current is controlled by sensing Royer primary-side converter current. This pin is the inverting terminal of a high-side current sense amplifier. The typical quiescent current is 50μA into the pin. If the CCFL regulator is not used in a floating-lamp configuration, tie the Royer and BAT pins together.

PIN FUNCTIONS

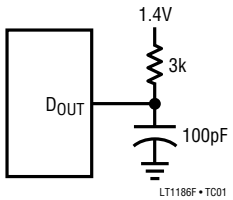
BAT (Pin 14): This pin connects to the battery or AC wall adapter voltage from which the CCFL Royer converter operates. This voltage is typically higher than the V_{CC} supply voltage but can equal V_{CC} if V_{CC} is a 5V logic supply. The BAT voltage must be at least 2.1V greater than the internal 2.4V regulator or 4.5V. This pin provides biasing for the lamp-current programming block, is used with the Royer pin for floating-lamp configurations and connects to one input for the open-lamp protection circuitry. For floating-lamp configurations, this pin is the noninverting terminal of a high-side current sense amplifier. The typical quiescent current is 50μA into the pin. The BAT and Royer pins monitor the primary-side Royer converter current through an internal 0.1Ω topside current sense resistor. A 0A to1A primary-side, center tap converter current is translated to an input signal range of 0mV to 100mV for the current sense amplifier. This input range translates to a 0μA to 500μA sink current at the CCFL V_C pin that nulls against the source current provided by the programmer circuit. The BAT pin also connects to the topside of the internal clamp between the BAT and BULB pins that is used for open-lamp protection.

BULB (Pin 15): This pin connects to the low side of a 7V threshold comparator between the BAT and BULB pins. This circuit sets the maximum voltage level across the primary side of the Royer converter under all operating conditions and limits the maximum secondary output under start-up conditions or open-lamp conditions. This eases transformer voltage rating requirements. Set the voltage limit to ensure lamp start-up with worst-case, lamp start voltages and cold temperature, system operating conditions. The BULB pin connects to the junction of an external divider network. The divider network connects from the center tap of the Royer transformer or the actual battery supply voltage to the topside of the current source "tail inductor." A capacitor across the top of the divider network filters switching ripple and sets a time constant that determines how quickly the clamp activates. When the comparator activates, sink current is generated to pull the CCFL V_C pin down. This action transfers the entire regulator loop from current mode operation into voltage mode operation.

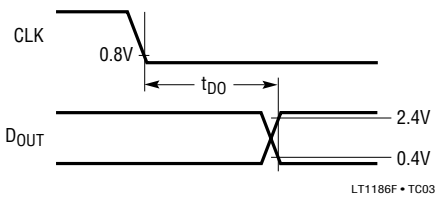
CCFL V_{SW} (Pin 16): This pin is the collector of the internal NPN power switch for the CCFL regulator. The power switch provides a minimum of 1.25A. Maximum switch current is a function of duty cycle as internal slope compensation ensures stability with duty cycles greater than 50%. Using a driver loop to automatically adapt base drive current to the minimum required to keep the switch in a quasi-saturation state yields fast switching times and high efficiency operation. The ratio of switch current to driver current is about 50:1.

TEST CIRCUITS

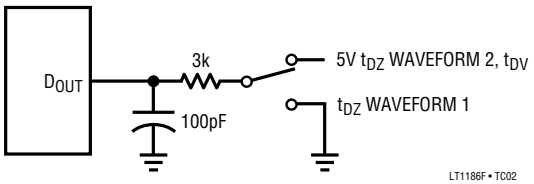
Load Circuit for t_{DO}



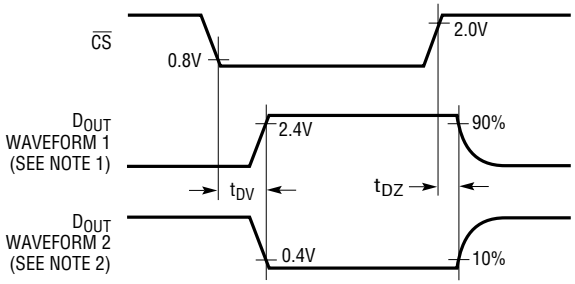
Voltage Waveforms for t_{DO}



Load Circuit for t_{DZ}, t_{DV}



Voltage Waveforms for t_{DZ}, t_{DV}



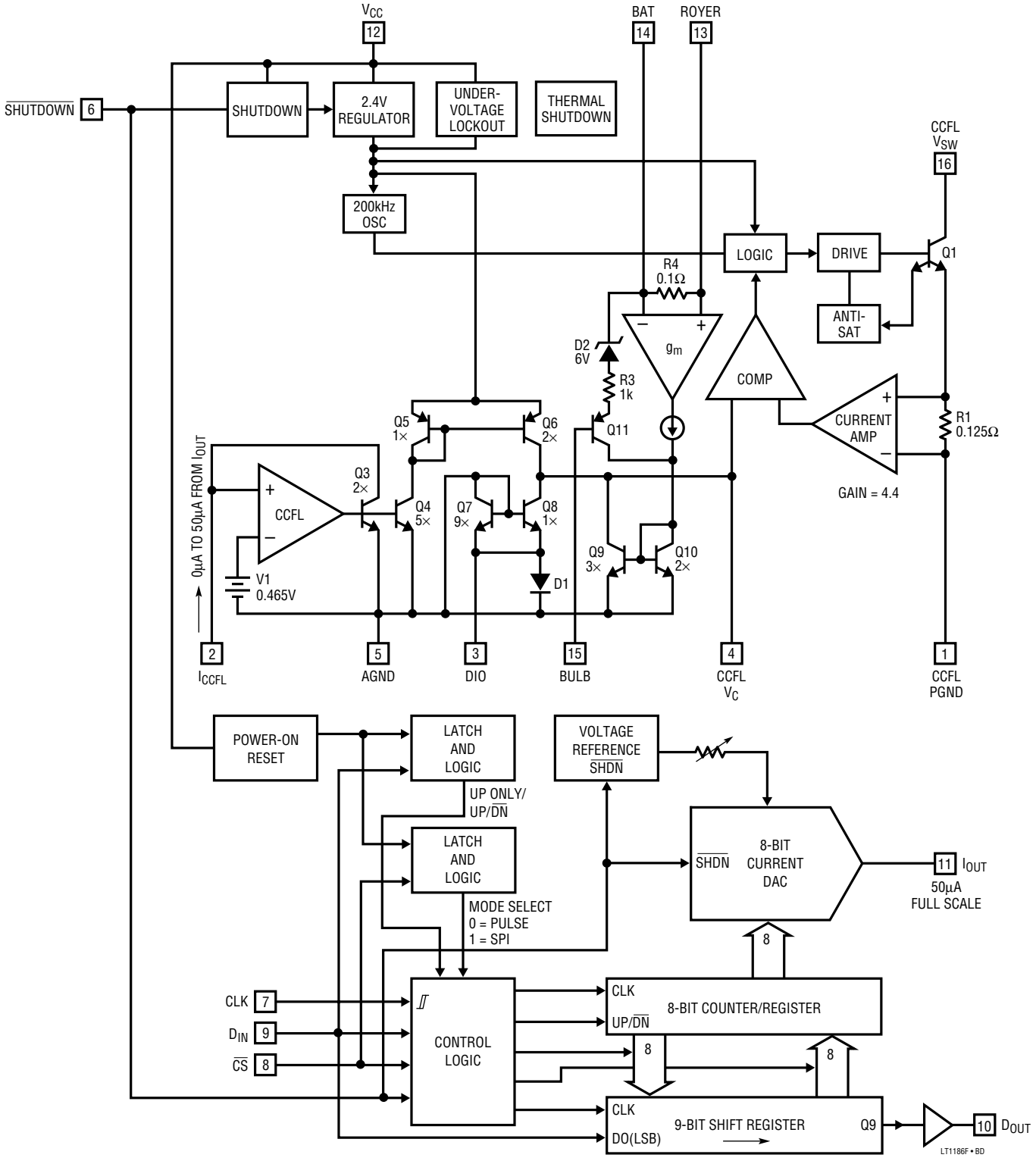
NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY $\overline{CS}$

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY $\overline{CS}$

LT1186F • TC04

BLOCK DIAGRAM

LT1186F DAC Programmable CCFL Switching Regulator



APPLICATIONS INFORMATION

Introduction

Current generation portable computers and instruments use backlit Liquid Crystal Displays (LCDs). Cold Cathode Fluorescent Lamps (CCFLs) provide the highest available efficiency in back lighting the display. Providing the most light out for the least amount of input power is the most important goal. These lamps require high voltage AC to operate, mandating an efficient high voltage DC/AC converter. The lamps operate from DC, but migration effects damage the lamp and shorten its lifetime. Lamp drive should contain zero DC component. In addition to good efficiency, the converter should deliver the lamp drive in the form of a sine wave. This minimizes EMI and RF emissions. Such emissions can interfere with other devices and can also degrade overall operating efficiency. Sinusoidal CCFL drive maximizes current-to-light conversion in the lamp. The circuit should also permit lamp intensity control from zero to full brightness with no hysteresis or "pop-on."

The small size and battery-powered operation associated with LCD equipped apparatus dictate low component count and high efficiency for these circuits. Size constraints place severe limitations on circuit architecture and long battery life is a priority. Laptop and handheld portable computers offer an excellent example. The CCFL and its power supply are responsible for almost 50% of the battery drain. Additionally, all components, including PC board and hardware, usually must fit within the LCD enclosure with a height restriction of 5mm to 10mm.

The CCFL regulator drives an inductor that acts as a switched-mode current source for a current-driven Royer-class converter with efficiencies as high as 90%. The control loop forces the CCFL PWM to modulate the average inductor current to maintain constant current in the lamp. The constant current value, and thus lamp intensity, is programmable. This drive technique provides a wide range of intensity control. A unique lamp-current programming block permits either grounded lamp or floating lamp configurations. Grounded lamp circuits directly sense one-half of average lamp current. Floating lamp circuits directly sense the Royer's primary-side converter current. Floating-lamp circuits provide symmetric differential drive to the lamp and reduce the parasitic loss from stray lamp-to-frame capacitance, extending illumination range.

Block Diagram Operation

The LT1186F is a fixed frequency, current mode switching regulator. A fixed frequency, current mode switcher controls switch duty cycle directly by switch current rather than by output voltage. Referring to the block diagram for the LT1186F, the switch turns ON at the start of each oscillator cycle. The switch turns OFF when switch current reaches a predetermined level. The control of output lamp current is obtained by using the output of a unique programming block to set current trip level. The current mode switching technique has several advantages. First, it provides excellent rejection of input voltage variations. Second, it reduces the 90° phase shift at mid-frequencies in the energy storage inductor. This simplifies closed-loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short-circuit conditions.

The LT1186F incorporates a low dropout internal regulator that provides a 2.4V supply for most of the internal circuitry. This low dropout design allows input voltage to vary from 3V to 6.5V with little change in quiescent current. An active low shutdown pin typically reduces total supply current to 35μA by shutting off the 2.4V regulator and locks out switching action for standby operation. The IC incorporates undervoltage lockout by sensing regulator dropout and locking out switching below about 2.5V. The regulator also provides thermal shutdown protection that locks out switching in the presence of excessive junction temperatures.

A 200kHz oscillator is the basic clock for all internal timing. The oscillator turns on the output switch via its own logic and driver circuitry. Adaptive anti-sat circuitry detects the onset of saturation in the power switch and adjusts base drive current instantaneously to limit switch saturation. This minimizes driver dissipation and provides rapid turn-off of the switch. The CCFL power switch is guaranteed to provide a minimum of 1.25A in the LT1186F. The anti-sat

APPLICATIONS INFORMATION

circuitry provides a ratio of switch current to driver current of about 50:1.

8-Bit Current Output DAC

The 8-bit current output DAC is guaranteed monotonic and is digitally adjustable by the 8-bit counter in 256 equal steps. On power up, the counter resets to 80H and the DAC assumes its mid-range value. The current output I_{OUT} drives the I_{CCFL} pin and sets control current for the lamp current programming block. The DAC has its own 1.24V bandgap reference and a voltage to current converter that is trimmed at wafer sort to provide the precision full-scale current reference. Over temperature, the current output of the DAC is 50µA ±6%.

Digital Interface

On power-up, a logic high at $\overline{CS}$ configures the DAC into pulse mode. If $\overline{CS}$ is ever pulled low, the chip configures into SPI mode until V_{CC} resets. On power-up in pulse mode, a logic high at D_{IN} puts the counter into increment-only mode. If UP/$\overline{DN}$ (D_{IN}) is ever pulled low, the counter configures into increment/decrement mode until V_{CC} resets. These modes are illustrated in Figure 1.

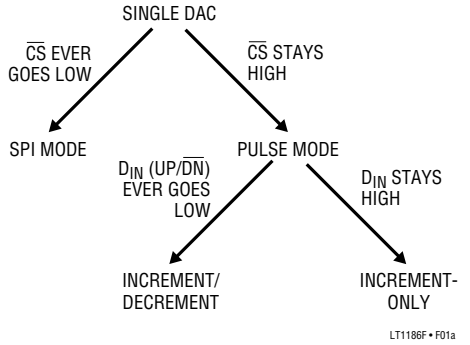


Figure 1a. Tree Diagram (LT1186F DAC Operating Modes)

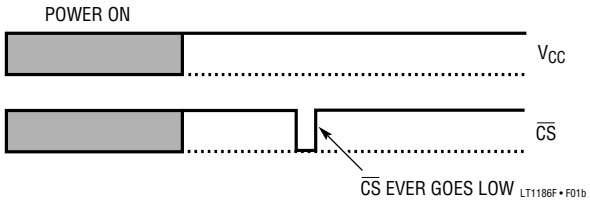


Figure 1b. SPI Mode Setup

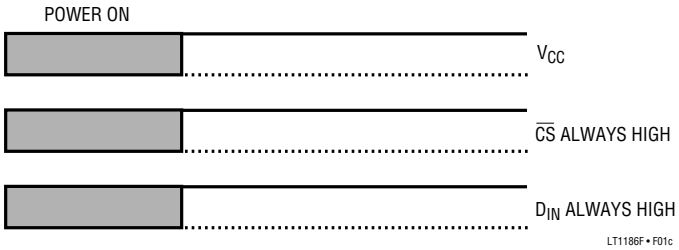


Figure 1c. Pulse Mode Setup (Increment Only)

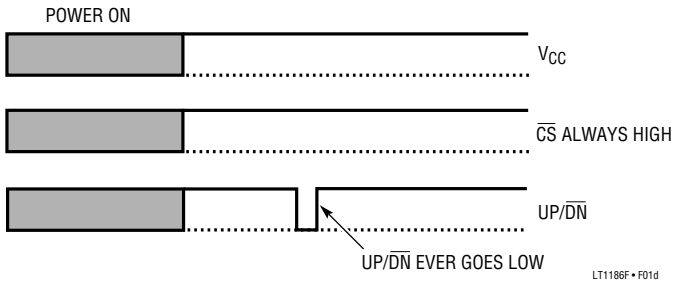


Figure 1d. Pulse Mode Setup (Increment/Decrement)

Standard SPI Mode

Refer to the serial interface operating sequence in Figure 2. A falling edge at $\overline{CS}$ initiates the data transfer. After the falling $\overline{CS}$ is recognized, D_{OUT} comes out of three-state. The clock (CLK) synchronizes the data transfer. Each input bit shifts into D_{IN} beginning with the MSB on the rising CLK edge and each previous data bit shifts out of D_{OUT} beginning with the MSB on the falling CLK edge. After the 8-bit serial input data is shifted in, a rising edge at $\overline{CS}$ transfers the data into the counter, the DAC assumes the new value I_{OUT} = (8-bit serial input data)(50µA)/255 and the D_{OUT} pin returns to a high impedance state.

1-Wire Interface (Pulse Mode)

In increment-only pulse mode, each rising edge of CLK increments the upper six bits of the counter by one count. When incremented beyond 11111100B, the counter rolls over and sets the DAC to the minimum value 00000000B. Therefore, a single pulse applied to CLK increases the upper 6-bit counter by one-step, and 63 pulse applied to CLK decreases the counter by one-step. The last two LSBs are always zero in this mode. $I_{OUT} = (B_7B_6B_5B_4B_3B_2B_1B_0)$ (50µA)/255. The upper 6-bit counter = $B_7B_6B_5B_4B_3B_2$ and $B_1 = B_0 = 0$. To configure the LT1186F into increment-only mode, tie $\overline{CS}$ and D_{IN} to V_{CC}.

APPLICATIONS INFORMATION

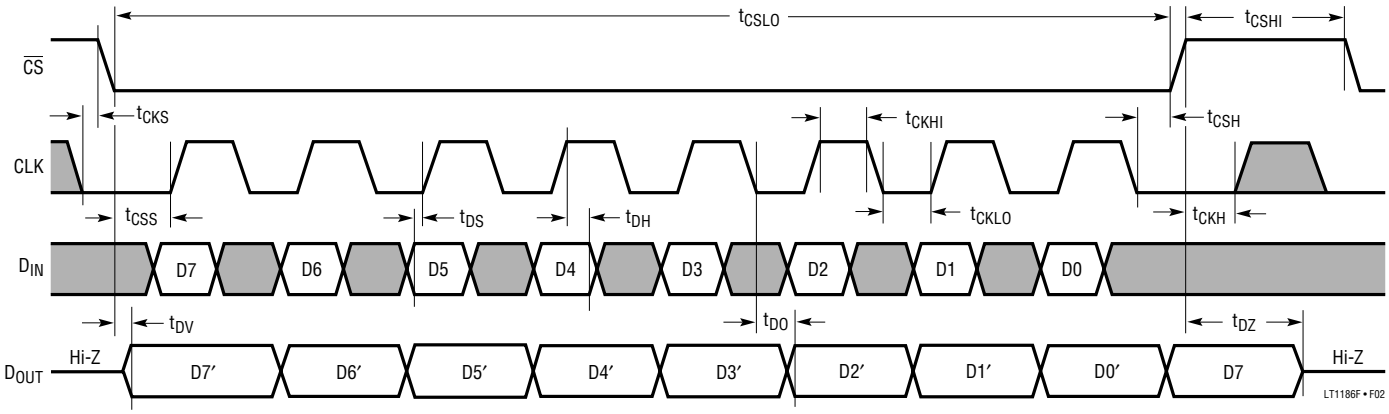


Figure 2. SPI Interface Timing Specification

2-Wire Interface (Pulse Mode)

In increment/decrement pulse mode, a logic high at UP/$\overline{DN}$ programs the counter into increment mode and each rising edge of CLK increments the upper six bits of the counter by one. The counter stops incrementing at 11111100B. A logic low at UP/$\overline{DN}$ programs the counter into decrement mode and each rising edge of CLK decrements the upper six bits of the counter by one. The counter stops decrementing at 00000000B. The last two LSBs are always zero in this mode. I_{OUT} = ($B_7B_6B_5B_4B_3B_2B_1B_0$) (50μA)/255. The upper 6-bit counter = $B_7B_6B_5B_4B_3B_2$ and $B_1 = B_0 = 0$. To configure the LT1186F into increment/decrement mode, tie $\overline{CS}$ to V_{CC} and pulse the UP/$\overline{DN}$ pin once on power-up.

Simplified Lamp Current Programming

A programming block in the LT1186F controls lamp current, permitting either grounded lamp or floating lamp configurations. Grounded configurations control lamp current by directly controlling one-half of actual lamp current and converting it to a feedback signal to close a control loop. Floating configurations control lamp current by directly controlling the Royer's primary-side converter current and generating a feedback signal to close a control loop.

Previous backlighting solutions have used a traditional error amplifier in the control loop to regulate lamp current. This approach converted an RMS current into a DC voltage for the input of the error amplifier. This approach used several time constants in order to provide stable loop frequency compensation. This compensation scheme meant that the loop had to be fairly slow and that output overshoot with start-up or overload conditions had to be carefully evaluated in terms of transformer stress and breakdown voltage requirements.

The LT1186F eliminates the error amplifier concept entirely and replaces it with a lamp current programming block. This block provides an easy-to-use interface to program lamp current. The programmer circuit also reduces the number of time constants in the control loop by combining the error signal conversion scheme and frequency compensation into a single capacitor. The control loop thus exhibits the response of a single pole system, allows for faster loop transient response and virtually eliminates overshoot under start-up or overload conditions.

Lamp current is programmed at the input of the programmer block, the I_{CCFL} pin. This pin is the input of a shunt regulator and accepts a DC input current signal of 0μA to 50μA from the DAC. This input signal is converted to a 0μA to 250μA source current at the CCFL V_C pin. The programmer circuit is simply a current-to-current converter with a gain of five. The typical input current programming range for 0mA to 6mA lamp current is 0μA to 50μA.

The I_{CCFL} pin is sensitive to capacitive loading and will oscillate with capacitance greater than 10pF. For example, loading the I_{CCFL} pin with a 1× or 10× scope probe causes oscillation and erratic CCFL regulator operation because of the probe's respective input capacitance. A current meter in series with the I_{CCFL} pin will also produce oscil-

APPLICATIONS INFORMATION

lation due to its shunt capacitance. Use a decoupling resistor of several kilohms between the I_{CCFL} pin and the I_{OUT} pin if excessive trace stray capacitance exists. Normally, this resistor is not required.

In some applications, the maximum programming current required at the I_{CCFL} pin for a maximum lamp current will be less than the full-scale output current of the DAC, which is 50μA. The system designer can either limit the maximum programming current through software built into the system, or use a current splitter which shunts a percentage of the full-scale current from the I_{CCFL} pin. A splitter circuit is illustrated in Figure 3. A divider string is used from a reference voltage to set up a voltage level equal to the I_{CCFL} summing voltage, or 465mV. The main current flowing in the divider string should be chosen to swamp out the effects of the shunted current into the divider string.

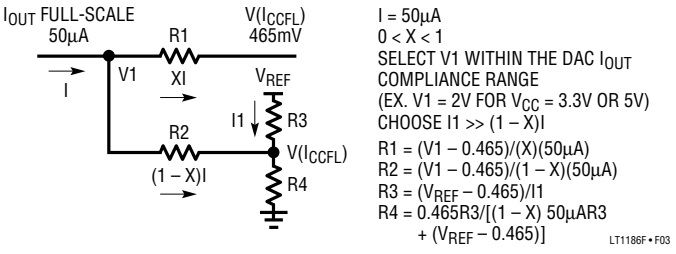


Figure 3

Grounded Lamp Configuration

In a grounded lamp configuration, the low voltage side of the lamp connects directly to the LT1186F DIO pin. This pin is the common connection between the cathode and anode of two internal diodes. In previous grounded lamp solutions, these diodes were discrete units and are now integrated onto the IC, saving cost and board space. Bidirectional lamp current flows in the DIO pin and thus, the diodes conduct alternately on half cycles. Lamp current is controlled by monitoring one-half of the average lamp current. The diode conducting on negative half cycles has one-tenth of its current diverted to the CCFL pin and nulls against the source current provided by the lamp current programmer circuit. The compensation capacitor on the CCFL V_C pin provides stable loop compensation and an averaging function to the rectified sinusoidal lamp current. Therefore, input programming current relates to one-half of average lamp current.

The transfer function between lamp current and input programming current must be empirically determined and is dependent on the particular lamp/display housing combination used. The lamp and display housing are a distributed loss structure due to parasitic lamp-to-frame capacitance. This means that the current flowing at the high-voltage side of the lamp is higher than what is flowing at the DIO pin side of the lamp. The input programming current is set to control lamp current at the high-voltage side of the lamp, even though the feedback signal is the lamp current at the bottom of the lamp. This ensures that the lamp is not overdriven which can degrade the lamp's operating lifetime. Therefore, the full scale current of the DAC does not necessarily correspond to the current required to set maximum lamp current.

Floating Lamp Configuration

In a floating lamp configuration, the lamp is fully floating with no galvanic connection to ground. This allows the transformer to provide symmetric differential drive to the lamp. Balanced drive eliminates the field imbalance associated with parasitic lamp-to-frame capacitance and reduces "thermometering" (uneven lamp intensity along the lamp length) at low lamp currents.

Carefully evaluate display designs in relation to the physical layout of the lamp, its leads and the construction of the display housing. Parasitic capacitance from any high voltage point to DC or AC ground creates paths for unwanted current flow. This parasitic current flow degrades electrical efficiency and losses up to 25% have been observed in practice. As an example, at a Royer operating frequency of 60kHz, 1pF of stray capacitance represents an impedance of 2.65MΩ. With an operating lamp voltage of 400V and an operating lamp current of 6mA, the parasitic current is 150μA. This additional current must be supplied by the transformer secondary. Layout techniques that increase parasitic capacitance include long high voltage lamp leads, reflective metal foil around the lamp and displays supplied in metal enclosures. Losses for a good display are under 5%, whereas, losses for a bad display range from 5% to 25%. Lossy displays are the primary reason to use a floating lamp configuration. Providing symmetric, differential drive to the lamp reduces the total parasitic loss by one-half.

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Maintaining closed-loop control of lamp current in a floating lamp configuration necessitates deriving a feedback signal from the primary side of the Royer transformer. Previous solutions have used an external precision shunt and high-side sense amplifier configuration. This approach has been integrated onto the LT1186F for simplicity of design and ease of use. An internal 0.1Ω resistor monitors the Royer converter current and connects between the input terminals of a high-side sense amplifier. A 0 – 1 Amp Royer primary-side, center-tap current is translated to a 0μA to 500μA sink current at the CCFL V_C pin to null against the source current provided by the lamp current programmer circuit. The compensation capacitor on the CCFL V_C pin provides stable loop compensation and an averaging function to the error sink current. Therefore, input programming current is related to average Royer converter current. Floating lamp circuits operate similarly to grounded lamp circuits except for the derivation of the feedback signal.

The transfer function between lamp current and input programming current must be empirically determined and is dependent upon a myriad of factors including lamp characteristics, display construction, transformer turns ratio and the tuning of the Royer oscillator. Once again, lamp current will be slightly higher at one end of the lamp and input programming current should be set for this higher level to ensure that the lamp is not overdriven.

The internal 0.1Ω high-side sense resistor on the LT1186F is rated for a maximum DC current of 1A. This resistor can be damaged by extremely high surge currents at start-up. The Royer converter typically uses a few microfarads of bypass capacitance at the center tap of the transformer. This capacitor charges up when the system is first powered by the battery pack or an AC wall adapter. The amount of current delivered at start-up can be very large if the total impedance in this path is small and the voltage source has high current capability. Linear Technology recommends the use of an aluminum electrolytic for the transformer center-tap bypass capacitor with an ESR greater than or equal to 0.5Ω. This lowers the peak surge currents to an acceptable level. In general, the wire and trace inductance in this path also help reduce the di/dt of the surge current. This issue only exists with floating lamp circuits as grounded lamp circuits do not make use of the high-side sense resistor.

Input Capacitor Type

Caution must be used in selecting the input capacitor type for switching regulators. Aluminum electrolytics are electrically rugged and the lowest cost, but are physically large to meet required ripple current ratings, and size constraints (especially height) may preclude their use. Ceramic capacitors are now available in larger values and their high ripple current and voltage rating make them ideal for input bypassing. Cost is fairly high and footprint can be large.

Solid tantalum capacitors would be a good choice except for a history of occasional failure when subjected to large current surges during start-up. The input bypass capacitor of regulators can see these high surges when a battery or high capacitance source is connected. Some manufacturers have developed tantalum capacitor lines specially tested for surge capability (AVX TPS series for instance), but even these units may fail if the input voltage surge approaches the capacitor's maximum voltage rating. AVX recommends derating the capacitor voltage by 2:1 for high surge applications.

Applications Support

Linear Technology invests an enormous amount of time, resources and technical expertise in understanding, designing and evaluating backlight/LCD contrast solutions for system designers. The design of an efficient and compact LCD backlight system is a study of compromise in a transduced electronic system. Every aspect of the design is interrelated and any design change requires complete re-evaluation for all other critical design parameters. Linear Technology has engineered one of the most complete test and evaluation setups for backlight designs and understands the issues and tradeoffs in achieving a compact, efficient and economical customer solution. Linear Technology welcomes the opportunity to discuss, design, evaluate and optimize any backlight/LCD contrast system with a customer. For further information on backlight/LCD contrast designs, consult the References.

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

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2. Williams, Jim. August 1993. *Techniques for 92% Efficient LCD Illumination*. Linear Technology Corporation, Application Note 55.

3. Bonte, Anthony. March 1995. *LT1182 Floating CCFL with Dual Polarity Contrast*. Linear Technology Corporation, Design Note 99.

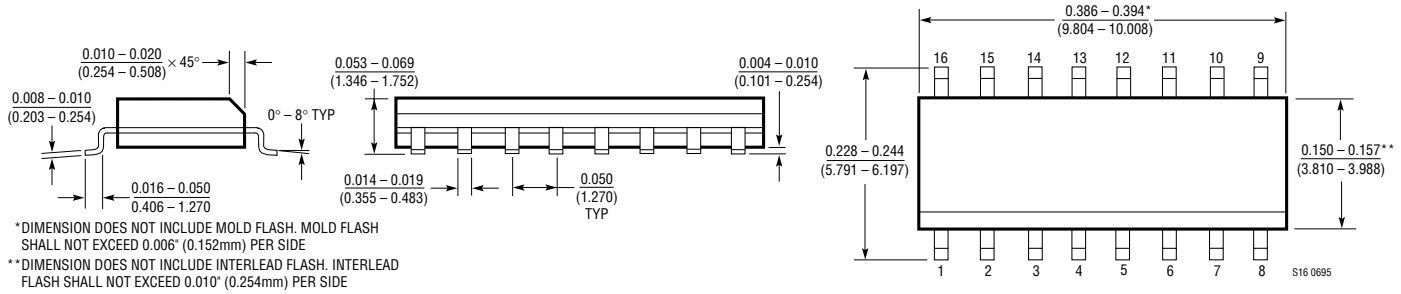
4. Williams, Jim. April 1995. *A Precision Wideband Current Probe for LCD Backlight Measurement*. Linear Technology Corporation, Design Note 101.

5. LT1182/LT1183/LT1184/LT1184F Data Sheet. *CCFL/LCD Contrast Switching Regulators*. April 1995. Linear Technology Corporation.

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S Package
16-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1107	Micropower DC/DC Converter for LCD Contrast Control	1A, 63kHz, Hysteretic
LT1172	Current Mode Switching Regulator for CCFL or LCD Contrast Control	1.25A, 100kHz
LT1173	Micropower DC/DC Converter for LCD Contrast Control	1A, 24kHz, Hysteretic
LT1182	Dual Current Mode Switching Regulator for CCFL and LCD Contrast Control	1.25A, 0.625A, 200kHz
LT1183	Dual Current Mode Switching Regulator for CCFL and LCD Contrast Control	1.25A, 0.625A, 200kHz
LT1184	Current Mode Switching Regulator for CCFL Control	1.25A, 200kHz
LT1184F	Current Mode Switching Regulator for CCFL Control	1.25A, 200kHz
LT1372	Current Mode Switching Regulator for CCFL or LCD Contrast Contol	1.5A, 500kHz

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