12-Bit, 800ksps Sampling A/D Converter with Shutdown

FEATURES

- **Sample Rate: 800ksps**
- **Power Dissipation: 80mW**
- **72.5dB S/(N + D) and 86dB THD at Nyquist**
- **No Pipeline Delay**
- Nap (4mW) and Sleep (10µW) Shutdown Modes
- Operates with Internal 15ppm/°C Reference or External Reference
- True Differential Inputs Reject Common Mode Noise
- 20MHz Full Power Bandwidth Sampling
- ±2.5V Bipolar Input Range
- 28-Pin SO Wide and SSOP Package

APPLICATIONS

- Telecommunications
- Digital Signal Processing
- Multiplexed Data Acquisition Systems
- High Speed Data Acquisition
- Spectrum Analysis
- Imaging Systems

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DESCRIPTION

The LTC®1409 is a 1µs, 800ksps, sampling 12-bit A/D converter that draws only 80mW from ±5V supplies. This easy-to-use device includes a high dynamic range sample-and-hold and a precision reference. Two digitally selectable power Shutdown modes provide flexibility for low power systems.

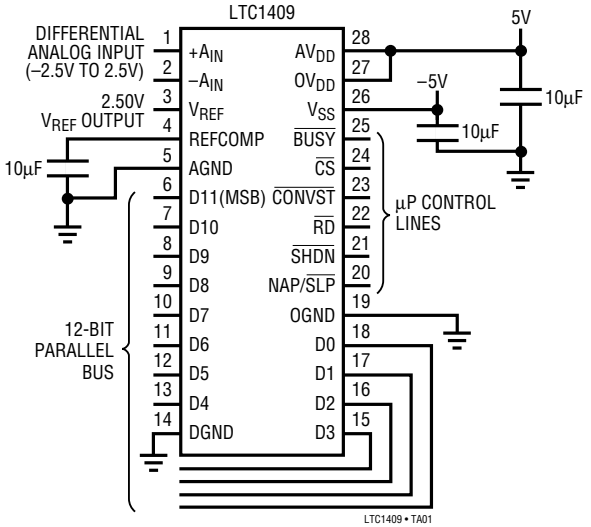
The LTC1409 full-scale input range is ±2.5V. Maximum DC specs include ±1LSB INL and ±1LSB DNL over temperature. Outstanding AC performance includes 72.5dB S/(N + D) at the Nyquist input frequency of 400kHz.

The unique differential input sample-and-hold can acquire single-ended or differential input signals up to its 20MHz bandwidth. The 60dB common mode rejection allows users to eliminate ground loops and common mode noise by measuring signals differentially from the source.

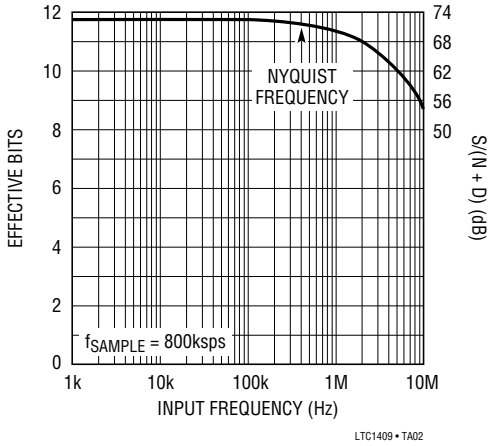
The ADC has a µP compatible, 12-bit parallel output port. There is no pipeline delay in the conversion results. A separate convert start input and a data ready signal ($\overline{BUSY}$) ease connections to FIFOs, DSPs and microprocessors. A digital output driver power supply pin allows direct connection to 3V logic.

TYPICAL APPLICATION

800kHz, 12-Bit Sampling A/D Converter



Effective Bits and Signal-to-(Noise + Distortion) vs Input Frequency

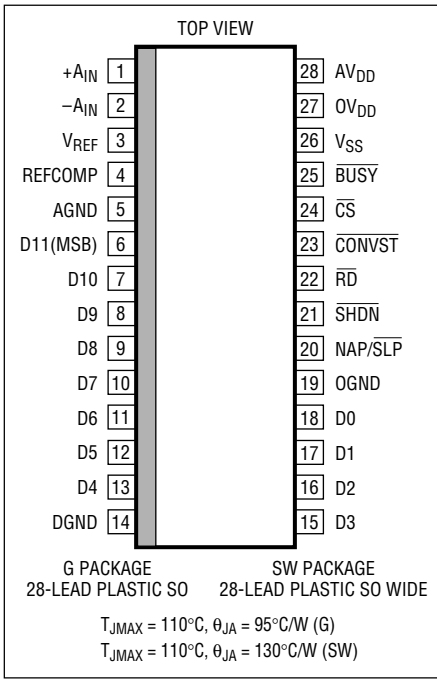


ABSOLUTE MAXIMUM RATINGS

AV_{DD} = OV_{DD} = V_{DD} (Notes 1, 2)

Supply Voltage (V_{DD}) 6V
Negative Supply Voltage (V_{SS}) ..... –6V
Total Supply Voltage (V_{DD} to V_{SS}) 12V
Analog Input Voltage
(Note 3) ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Digital Input Voltage (Note 4) ..... V_{SS} – 0.3V to 10V
Digital Output Voltage ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Power Dissipation 500mW
Operating Temperature Range
LTC1409C ..... 0°C to 70°C
LTC1409I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
28-LEAD PLASTIC SO

SW PACKAGE
28-LEAD PLASTIC SO WIDE

T_{JMAX} = 110°C, θ_{JA} = 95°C/W (G)
T_{JMAX} = 110°C, θ_{JA} = 130°C/W (SW)

ORDER PART NUMBER
LTC1409CG
LTC1409CSW
LTC1409IG
LTC1409ISW

Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS

With Internal Reference (Notes 5, 6)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			Bits
Integral Linearity Error	(Note 7)	●		±0.3	±1	LSB
Differential Linearity Error		●		±0.3	±1	LSB
Offset Error	(Note 8)	 ●		±2	±6 ±8	LSB LSB
Full-Scale Error					±15	LSB
Full-Scale Tempco	$I_{OUT(REF)}$ = 0	●		±15		ppm/°C

ANALOG INPUT

(Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 9)	4.75V ≤ V_{DD} ≤ 5.25V, –5.25V ≤ V_{SS} ≤ –4.75V	●		±2.5		V
I_{IN}	Analog Input Leakage Current	$\overline{CS}$ = High	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions During Conversions			17 5		pF pF
t_{ACQ}	Sample-and-Hold Acquisition Time		●		50	150	ns
t_{AP}	Sample-and-Hold Aperture Delay Time				–1.5		ns
t_{jitter}	Sample-and-Hold Aperture Delay Time Jitter				5		ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio	–2.5V < (–A_{IN} = +A_{IN}) < 2.5V			60		dB

DYNAMIC ACCURACY (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	100kHz Input Signal (Note 12) 400kHz Input Signal (Note 12)	● ●	70 68	73.0 72.5		dB dB
THD	Total Harmonic Distortion	100kHz Input Signal, First Five Harmonics 400kHz Input Signal, First Five Harmonics	 ●		–90 –86	 –74	dB dB
	Peak Harmonic or Spurious Noise	400kHz Input Signal	●		–90	–74	dB
IMD	Intermodulation Distortion	f_{IN1} = 29.37kHz, f_{IN2} = 32.446kHz			–84		dB
	Full Power Bandwidth				15		MHz
	Full Linear Bandwidth	S/(N + D) ≥ 68dB			1.6		MHz

INTERNAL REFERENCE CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		2.480	2.500	2.520	V
V_{REF} Output Tempco	I_{OUT} = 0			±15		ppm/°C
V_{REF} Line Regulation	4.75V ≤ V_{DD} ≤ 5.25V –5.25V ≤ V_{SS} ≤ –4.75V			0.01 0.01		LSB/V LSB/V
V_{REF} Output Resistance	–0.1mA ≤ I_{OUT} ≤ 0.1mA			4		kΩ
REFCOMP Output Voltage	I_{OUT} = 0			4.06		V

DIGITAL INPUTS AND DIGITAL OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{DD} = 4.75V I_O = –10µA I_O = –200µA	 ●	 4.0	 4.5	 	 V V
V_{OL}	Low Level Output Voltage	V_{DD} = 4.75V I_O = 160µA I_O = 1.6mA	 ●		 0.05 0.10	 0.4	 V V
I_{OZ}	High-Z Output Leakage D11 to D0	V_{OUT} = 0V to V_{DD}, $\overline{CS}$ High	●			±10	µA
C_{OZ}	High-Z Output Capacitance D11 to D0	$\overline{CS}$ High (Note 9)	●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			10		mA

POWER REQUIREMENTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage	(Notes 10, 11)		4.75		5.25	V
V_{SS}	Negative Supply Voltage	(Note 10)		–4.75		–5.25	V
I_{DD}	Positive Supply Current Nap Mode Sleep Mode	$\overline{CS}$ High $\overline{CONVST}$ = $\overline{CS}$ = $\overline{RD}$ = $\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 5V $\overline{CONVST}$ = $\overline{CS}$ = $\overline{RD}$ = $\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 0V	●		6.0 0.8 1.0	9.0 1.2	mA mA µA

POWER REQUIREMENTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SS}	Negative Supply Current	$\overline{CS}$ High	●		10	15	mA
	Nap Mode	$\overline{CONVST}$ = $\overline{CS}$ = $\overline{RD}$ = $\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 5V			10		µA
	Sleep Mode	$\overline{CONVST}$ = $\overline{CS}$ = $\overline{RD}$ = $\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 0V			1		µA
P_{DISS}	Power Dissipation		●		80	120	mW
	Nap Mode	$\overline{CONVST}$ = $\overline{CS}$ = $\overline{RD}$ = $\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 5V			3.8	6	mW
	Sleep Mode	$\overline{CONVST}$ = $\overline{CS}$ = $\overline{RD}$ = $\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 0V			0.01		mW

TIMING CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency		●	800			kHz
t_{CONV}	Conversion Time		●		900	1250	ns
t_{ACQ}	Acquisition Time		●			150	ns
t_1	$\overline{CS}$ to $\overline{RD}$ Setup Time	(Notes 9, 10)	●	0			ns
t_2	$\overline{CS}\downarrow$ to $\overline{CONVST}\downarrow$ Setup Time	(Notes 9, 10)	●	10			ns
t_3	NAP/$\overline{SLP}\downarrow$ to $\overline{SHDN}\downarrow$ Setup Time	(Notes 9, 10)	●	10			ns
t_4	$\overline{SHDN}\uparrow$ to $\overline{CONVST}\downarrow$ Wake-Up Time	(Note 10)			200		ns
t_5	$\overline{CONVST}$ Low Time	(Notes 10, 11)	●	50			ns
t_6	$\overline{CONVST}$ to $\overline{BUSY}$ Delay	C_L = 25pF			10		ns
			●			60	ns
t_7	Data Ready Before $\overline{BUSY}\uparrow$			20	35		ns
			●	15			ns
t_8	Delay Between Conversions	(Note 10)	●	40			ns
t_9	Wait Time $\overline{RD}\downarrow$ After $\overline{BUSY}\uparrow$		●	–5			ns
t_{10}	Data Access Time After $\overline{RD}\downarrow$	C_L = 25pF			15	35	ns
			●			45	ns
		C_L = 100pF			20	45	ns
			●			60	ns
t_{11}	Bus Relinquish Time				8	30	ns
		0°C ≤ T_A ≤ 70°C	●			35	ns
		–40°C ≤ T_A ≤ 85°C	●			40	ns
t_{12}	$\overline{RD}$ Low Time		●	t_{10}			ns
t_{13}	$\overline{CONVST}$ High Time		●	50			ns
t_{14}	Aperture Delay of Sample-and-Hold				–1.5		ns

The ● indicates specifications which apply over the full operating temperature range; all other limits and typicals T_A = 25°C.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND and AGND wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below V_{SS} or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} or above V_{DD} without latch-up.

Note 4: When these pin voltages are taken below V_{SS} they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} without latchup. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 5V, f_{SAMPLE} = 800kHz, t_r = t_f = 5ns unless otherwise specified.

Note 6: Linearity, offset and full-scale specifications apply for a single-ended +A_{IN} input with –A_{IN} grounded.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Bipolar offset is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111.

Note 9: Guaranteed by design, not subject to test.

Note 10: Recommended operating conditions.

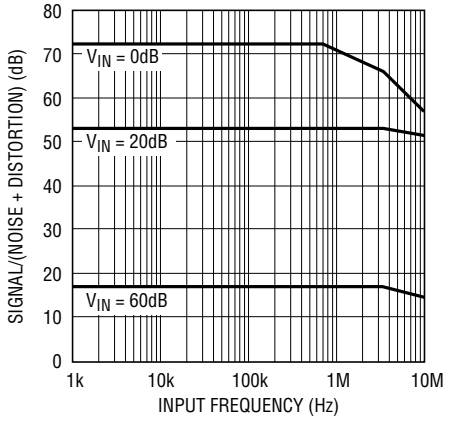
TIMING CHARACTERISTICS

Note 11: The falling $\overline{\text{CONVST}}$ edge starts a conversion. If $\overline{\text{CONVST}}$ returns high at a critical point during the conversion it can create small errors. For best results ensure that $\overline{\text{CONVST}}$ returns high either within 650ns after conversion start or after $\overline{\text{BUSY}}$ rises.

Note 12: Signal-to-noise ratio (SNR) is measured at 100kHz and distortion is measured at 400kHz. These results are used to calculate signal-to-noise plus distortion (SINAD).

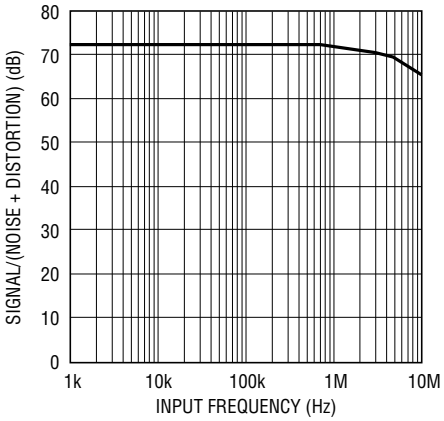
TYPICAL PERFORMANCE CHARACTERISTICS

S/(N + D) vs Input Frequency and Amplitude



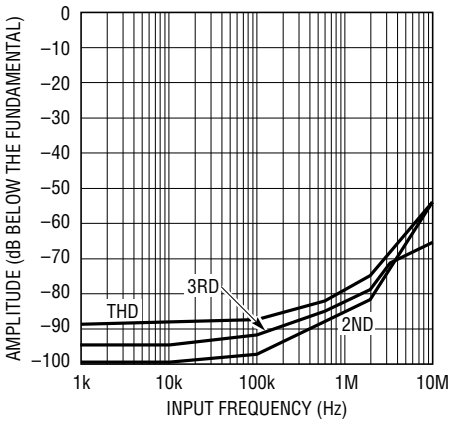
LTC1409 • TPC01

Signal-to-Noise Ratio vs Input Frequency



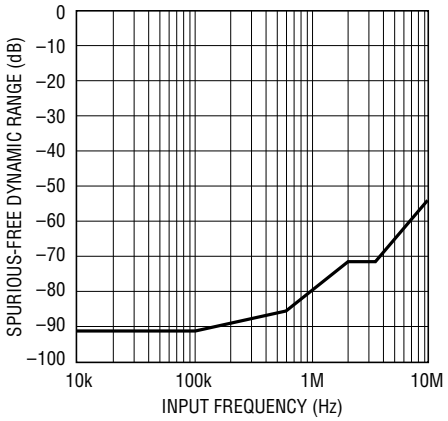
LTC1409 • TPC02

Distortion vs Input Frequency



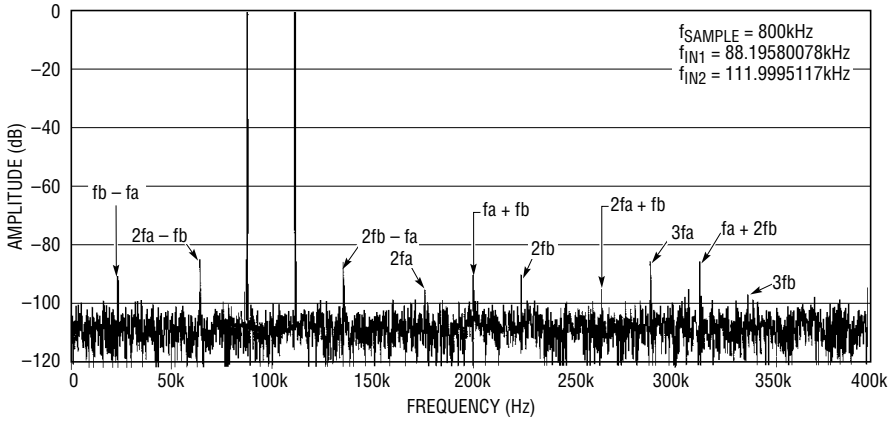
LTC1409 • TPC03

Spurious-Free Dynamic Range vs Input Frequency



LTC1409 • TPC04

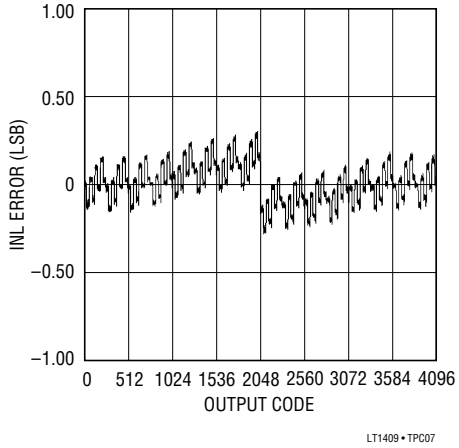
Intermodulation Distortion Plot



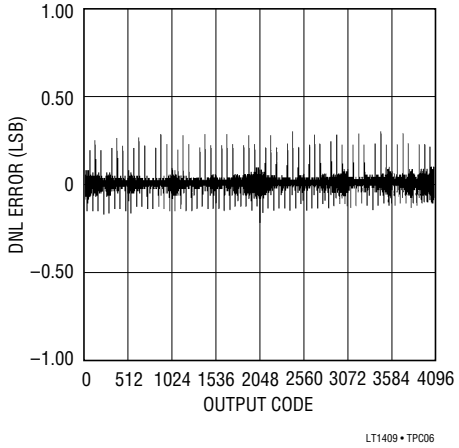
LTC1409 • TPC05

TYPICAL PERFORMANCE CHARACTERISTICS

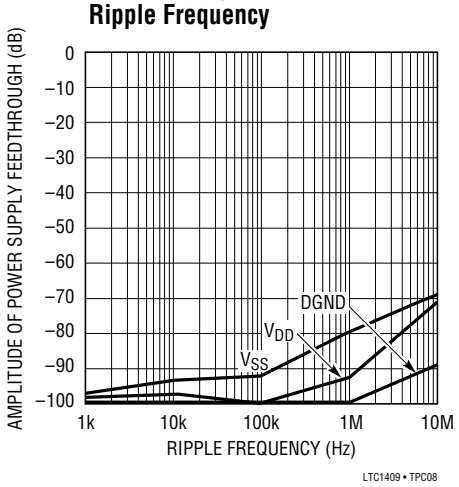
Integral Nonlinearity vs Output Code



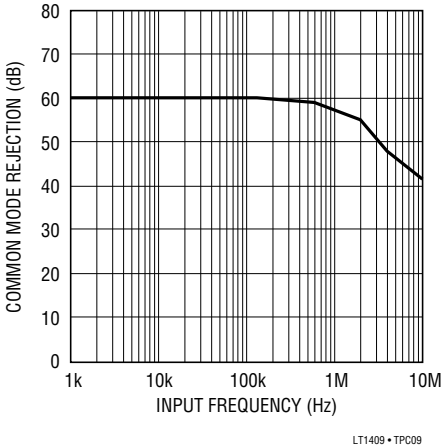
Differential Nonlinearity vs Output Code



Power Supply Feedthrough vs Ripple Frequency



Input Common Mode Rejection vs Input Frequency



PIN FUNCTIONS

+A_{IN} (Pin 1): Positive Analog Input, ±2.5V.

–A_{IN} (Pin 2): Negative Analog Input, ±2.5V.

V_{REF} (Pin 3): 2.50V Reference Output.

REFCOMP (Pin 4): 4.06V Reference Output. Bypass to AGND using 10µF tantalum in parallel with 0.1µF or 10µF ceramic.

AGND (Pin 5): Analog Ground.

D11 to D4 (Pins 6 to 13): Three-State Data Outputs.

DGND (Pin 14): Digital Ground for Internal Logic. Tie to AGND.

D3 to D0 (Pins 15 to 18): Three-State Data Outputs.

OGND (Pin 19): Digital Ground for Output Drivers. Tie to AGND.

NAP/$\overline{SLP}$ (Pin 20): Power Shutdown Mode. Selects the mode invoked by the $\overline{SHDN}$ pin. Low selects Sleep mode and high selects quick wake-up Nap mode.

$\overline{SHDN}$ (Pin 21): Power Shutdown Input. A low logic level will invoke the Shutdown mode selected by the NAP/$\overline{SLP}$ pin.

$\overline{RD}$ (Pin 22): Read Input. This enables the output drivers when $\overline{CS}$ is low.

PIN FUNCTIONS

$\overline{\text{CONVST}}$ (Pin 23): Conversion Start Signal. This active low signal starts a conversion on its falling edge.

$\overline{\text{CS}}$ (Pin 24): Chip Select. The input must be low for the ADC to recognize $\overline{\text{CONVST}}$ and $\overline{\text{RD}}$ inputs.

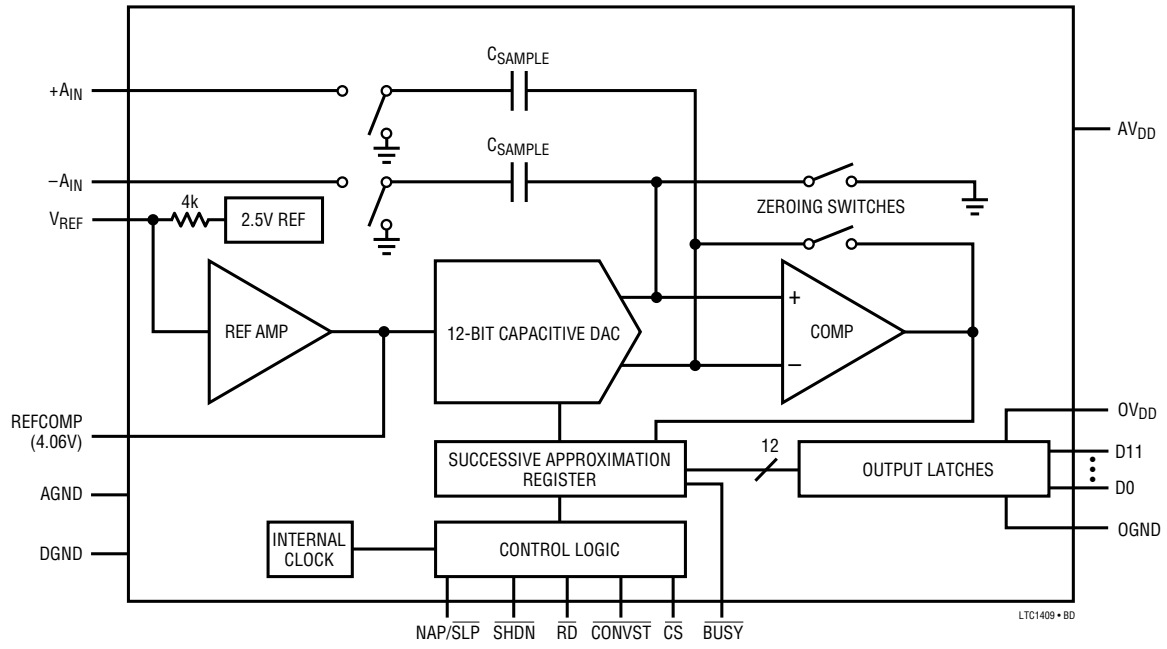
$\overline{\text{BUSY}}$ (Pin 25): The $\overline{\text{BUSY}}$ output shows the converter status. It is low when a conversion is in progress. Data valid on the rising edge of $\overline{\text{BUSY}}$.

V_{SS} (Pin 26): –5V Negative Supply. Bypass to AGND using 10µF tantalum in parallel 0.1µF or 10µF ceramic.

OV_{DD} (Pin 27): Positive Supply for Output Drivers. For 5V logic, short to Pin 28. For 3V logic, short to supply of the logic being driven.

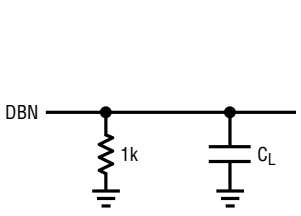
AV_{DD} (Pin 28): 5V Positive Supply. Bypass to AGND 10µF tantalum in parallel with 0.1µF or 10µF ceramic.

FUNCTIONAL BLOCK DIAGRAM

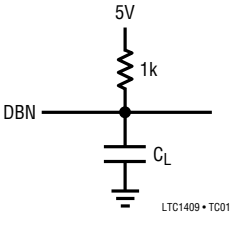


TEST CIRCUITS

Load Circuits for Access Timing

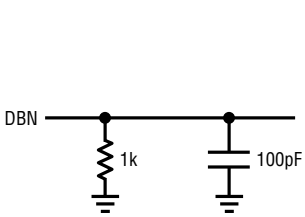


(a) Hi-Z to V_{OH} and V_{OL} to V_{OH}

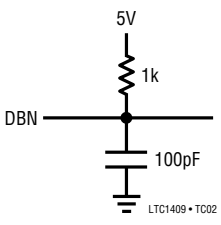


(b) Hi-Z to V_{OL} and V_{OH} to V_{OL}

Load Circuits for Bus Relinquish Time



(a) V_{OH} to Hi-Z



(b) V_{OL} to Hi-Z

APPLICATIONS INFORMATION

CONVERSION DETAILS

The LTC1409 uses a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 12-bit parallel output. The ADC is complete with a precision reference and an internal clock. The control logic provides easy interface to microprocessors and DSPs. (Please refer to the Digital Interface section for the data format.)

Conversion start is controlled by the $\overline{CS}$ and $\overline{CONVST}$ inputs. At the start of the conversion the successive approximation register (SAR) is reset. Once a conversion cycle has begun it cannot be restarted.

During the conversion, the internal differential 12-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, the $+A_{IN}$ and $-A_{IN}$ inputs are connected to the sample-and-hold capacitors (C_{SAMPLE}) during the acquire phase and the comparator offset is nulled by the zeroing switches. In this acquire phase, a minimum delay of 150ns will provide enough time for the sample-and-hold capacitors to acquire the analog signal. During the convert phase the comparator zeroing switches open, putting the comparator into compare mode. The input switches connect the C_{SAMPLE} capacitors to ground, transferring the differential analog input charge onto the summing junction. This input charge is successively compared with the binary-weighted charges supplied by the differential capacitive DAC. Bit decisions are made by the high speed comparator. At the end of a conversion, the differential DACs output balances the $+A_{IN}$ and $-A_{IN}$ input charges. The SAR contents (a 12-bit data word) which represents the difference of $+A_{IN}$ and $-A_{IN}$ are loaded into the 12-bit output latches.

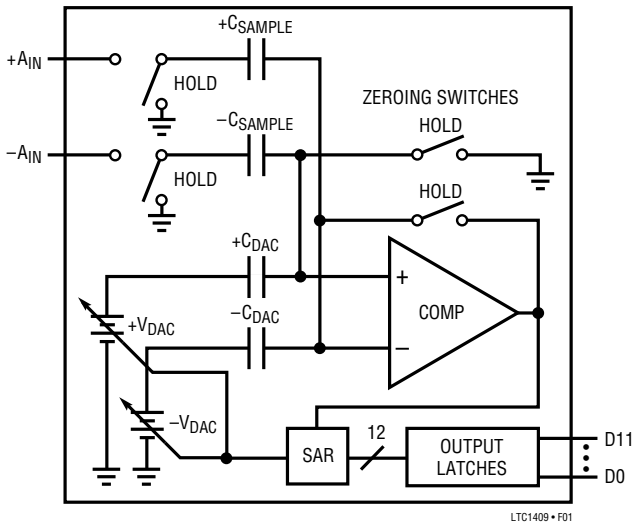


Figure 1. Simplified Block Diagram

DYNAMIC PERFORMANCE

The LTC1409 has excellent high speed sampling capability. FFT (Fast Four Transform) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 2 shows typical LTC1409 plots.

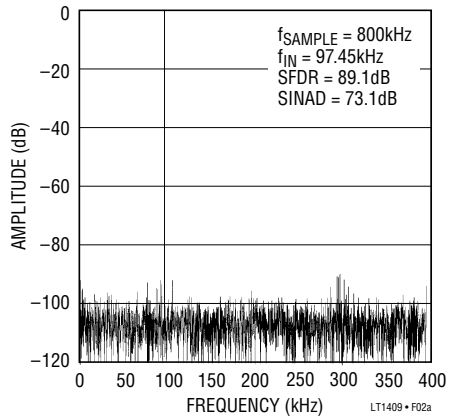


Figure 2a. LTC1409 Nonaveraged, 4096 Point FFT, Input Frequency = 100kHz

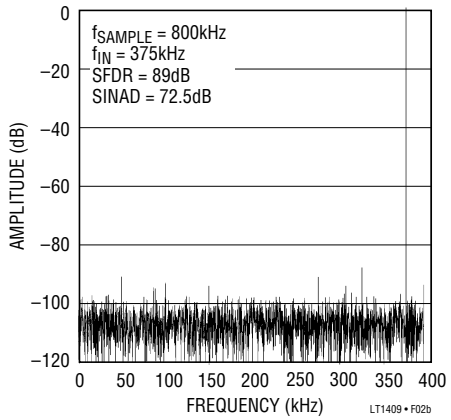


Figure 2b. LTC1409 Nonaveraged, 4096 Point FFT, Input Frequency = 375kHz

APPLICATIONS INFORMATION

Signal-to-Noise Ratio

The signal-to-noise plus distortion ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from above DC and below half the sampling frequency. Figure 2 shows a typical spectral content with an 800kHz sampling rate and a 100kHz input. The dynamic performance is excellent for input frequencies up to and beyond the Nyquist limit of 400kHz.

Effective Number of Bits

The Effective Number of Bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to the S/(N + D) by the equation:

$$N = [S/(N + D) - 1.76]/6.02$$

where N is the effective number of bits of resolution and S/(N + D) is expressed in dB. At the maximum sampling rate of 800kHz the LTC1409 maintains near ideal ENOBs up to the Nyquist input frequency of 400kHz. Refer to Figure 3.

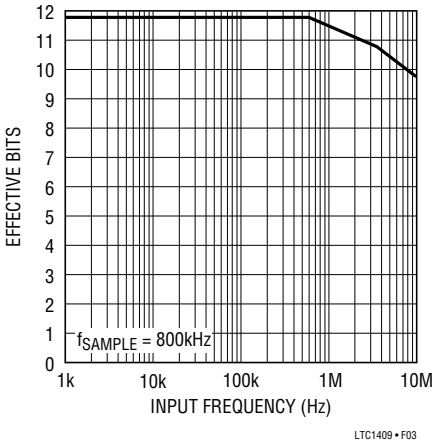


Figure 3. Effective Bits and Signal/(Noise + Distortion) vs Input Frequency

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20\ Log \frac{\sqrt{V2^2 + V3^2 + V4^2 + \ldots Vn^2}}{V1}$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through Vn are the amplitudes of the second through Nth harmonics. THD vs input frequency is shown in Figure 4. The LTC1409 has good distortion performance up to the Nyquist frequency and beyond.

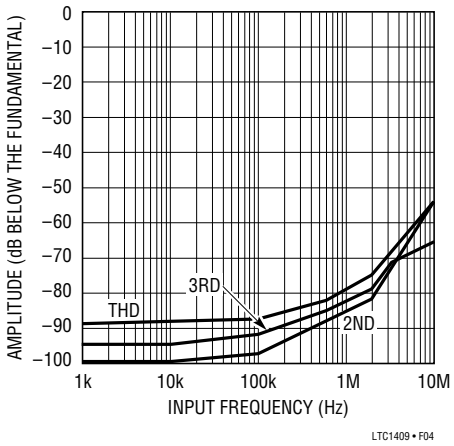


Figure 4. Distortion vs Input Frequency

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the DC transfer function can create distortion products at the sum and difference frequencies of mfa + –nfb, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include (fa + fb). If the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd order IMD products can be expressed by the following formula:

$$IMD(fa + fb) = 20\ Log \frac{\text{Amplitude at (fa + fb)}}{\text{Amplitude at fa}}$$

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This

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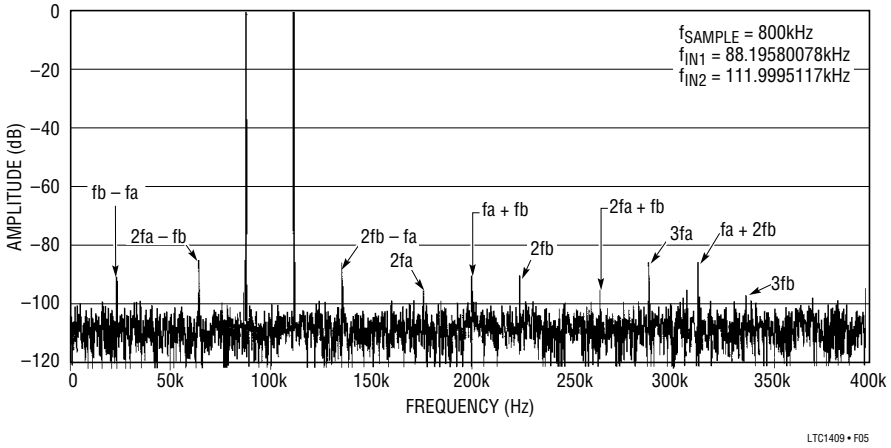


Figure 5. Intermodulation Distortion Plot

value is expressed in decibels relative to the RMS value of a full-scale input signal.

Full Power and Full Linear Bandwidth

The full power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input signal.

The full linear bandwidth is the input frequency at which the S/(N + D) has dropped to 68dB (11 effective bits). The LTC1409 has been designed to optimize input bandwidth, allowing the ADC to undersample input signals with frequencies above the converter's Nyquist Frequency. The noise floor stays very low at high frequencies; S/(N + D) becomes dominated by distortion at frequencies far beyond Nyquist.

Driving the Analog Input

The differential analog inputs of the LTC1409 are easy to drive. The inputs may be driven differentially or as a single-ended input (i.e., the $–A_{IN}$ input is grounded). The $+A_{IN}$ and $–A_{IN}$ inputs are sampled at the same instant. Any unwanted signal that is common mode to both inputs will be reduced by the common mode rejection of the sample-and-hold circuit. The inputs draw only one small current spike while charging the sample-and-hold capacitors at the end of conversion. During conversion the analog inputs draw only a small leakage current. If the source impedance of the driving circuit is low then the LTC1409 inputs can be driven directly. As source impedance increases so will acquisition time (see Figure 6). For minimum acquisition time, with high source impedance, a buffer amplifier should be used. The only requirement is that the amplifier driving the analog input(s) must settle after the small current spike before the next conversion starts (settling time must be 150ns for full throughput rate).

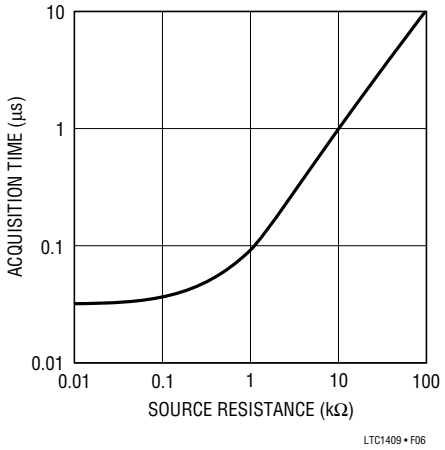


Figure 6. Acquisition Time vs Source Resistance

Choosing an Input Amplifier

Choosing an input amplifier is easy if a few requirements are taken into consideration. First, to limit the magnitude of the voltage spike seen by the amplifier from charging the sampling capacitor, choose an amplifier that has a low output impedance (<100Ω) at the closed-loop bandwidth frequency. For example, if an amplifier is used in a gain of 1 and has a unity-gain bandwidth of 50MHz, then the output impedance at 50MHz should be less than 100Ω. The second requirement is that the closed-loop

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bandwidth must be greater than 20MHz to ensure adequate small-signal settling for full throughput rate. If slower op amps are used, more settling time can be provided by increasing the time between conversions.

The best choice for an op amp to drive the LTC1409 will depend on the application. Generally applications fall into two categories: AC applications where dynamic specifications are most critical, and time domain applications where DC accuracy and settling time are most critical. The following list is a summary of the op amps that are suitable for driving the LTC1409, more detailed information is available in the Linear Technology databooks and the LinearView™ CD-ROM.

LT®1220: 30MHz unity-gain bandwidth voltage feedback amplifier. ±5V to ±15V supplies. Excellent DC specifications, 90ns settling to 0.5LSB.

LT1223: 100MHz video current feedback amplifier. 6mA supply current. ±5V to ±15V supplies. Low distortion up to and above 400kHz. Low noise. Good for AC applications.

LT1227: 140MHz video current feedback amplifier. 10mA supply current ±5V to ±15V supplies. Lowest distortion at frequencies above 400kHz. Low noise. Best for AC applications.

LT1229/LT1230: Dual and quad 100MHz current feedback amplifiers. ±2V to ±15V supplies. Low noise. Good AC specs. 6mA supply current for each amplifier.

LT1360: 37MHz voltage feedback amplifier. 3.8mA supply current. Good AC/DC specs. ±5V to ±15V supplies. 70ns settling to 0.5LSB.

LT1363: 50MHz, 450V/µs op amps. 6.3mA supply current. Good AC/DC specs. 60ns settling to 0.5LSB.

LT1364/LT1365: Dual and quad 50MHz, 450V/µs op amps. 6.3mA supply current per amplifier. 60ns settling to 0.5LSB.

Input Filtering

The noise and the distortion of the input amplifier and other circuitry must be considered since they will add to the LTC1409 noise and distortion. The small-signal bandwidth of the sample-and-hold circuit is 20MHz. Any noise or distortion products that are present at the analog inputs will be summed over this entire bandwidth. Noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for many applications. For example, Figure 7 shows a 1000pF capacitor from $+A_{IN}$ to ground and a 100Ω source resistor to limit the input bandwidth to 1.6MHz. The 1000pF capacitor also acts as a charge reservoir for the input sample-and-hold and isolates the ADC input from sampling glitch sensitive circuitry. High quality capacitors and resistors should be used since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can also generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

When high amplitude unwanted signals are close in frequency to the desired signal frequency, a multiple pole filter

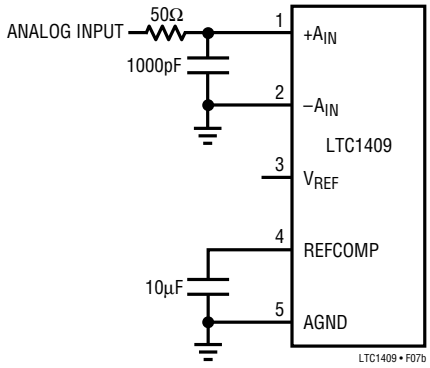


Figure 7a. RC Input Filter

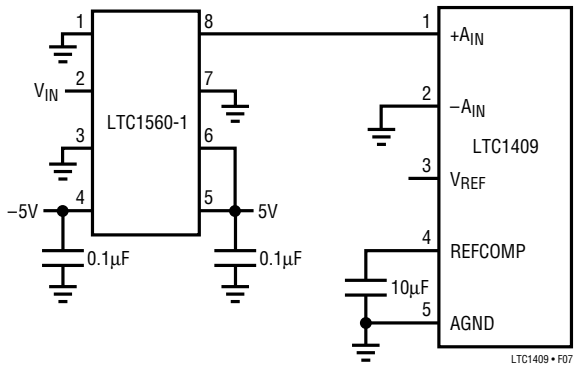


Figure 7b. 500kHz 5th Order Elliptic Lowpass Filter

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is required. Figure 7b shows a simple implementation using a LTC1560 5th order elliptic continuous time filter.

Input Range

The ±2.5V input range of the LTC1409 is optimized for low noise and low distortion. Most op amps also perform best over this same range, allowing direct coupling to the analog inputs and eliminating the need for special translation circuitry.

Some applications may require other input ranges. The LTC1409 differential inputs and reference circuitry can accommodate other input ranges often with little or no additional circuitry. The following sections describe the reference and input circuitry and how they affect the input range.

Internal Reference

The LTC1409 has an on-chip, temperature compensated, curvature corrected, bandgap reference that is factory trimmed to 2.500V. It is connected internally to a reference amplifier and is available at V_{REF} (Pin 3) see Figure 8a. A 4k resistor is in series with the output so that it can be easily overdriven by an external reference or other circuitry. The reference amplifier gains the voltage at the V_{REF} pin by 1.625 to create the required internal reference voltage. This provides buffering between the V_{REF} pin and the high speed capacitive DAC. The reference amplifier compensation pin, REFCOMP (Pin 4), must be bypassed with a capacitor to ground. The reference amplifier is stable with capacitors of 1µF or greater. For the best noise performance, a 10µF ceramic or 10µF tantalum in parallel with 0.1µF ceramic is recommended (see Figure 8b).

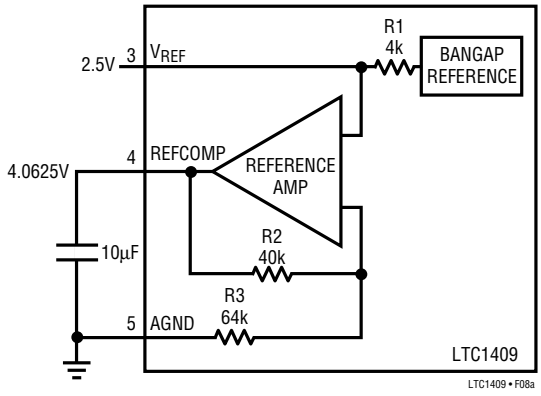


Figure 8a. LTC1409 Reference Circuit

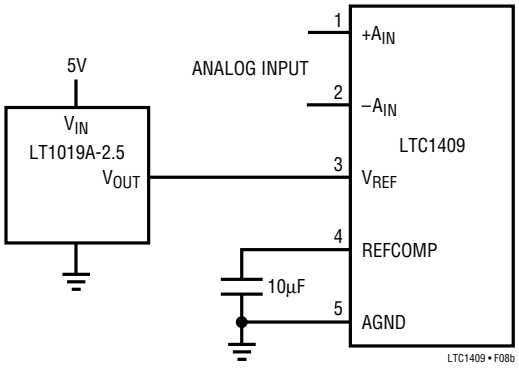


Figure 8b. Using the LT1019-2.5 as an External Reference

The V_{REF} pin can be driven with a DAC or other means shown in Figure 9. This is useful in applications where the peak input signal amplitude may vary. The input span of the ADC can then be adjusted to match the peak input signal, maximizing the signal-to-noise ratio. The filtering of the internal LTC1409 reference amplifier will limit the bandwidth and settling time of this circuit. A settling time of 5ms should be allowed for, after a reference adjustment.

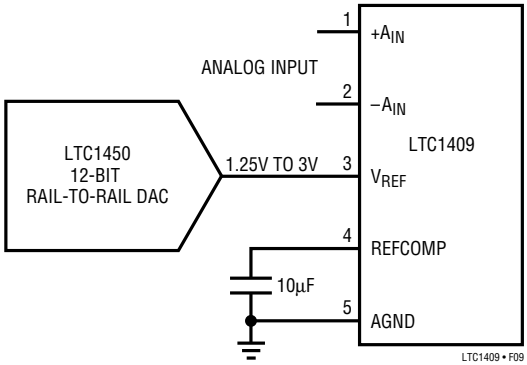


Figure 9.Driving V_{REF} with a DAC

Differential Inputs

The LTC1409 has a unique differential sample-and-hold circuit that allows rail-to-rail inputs. The ADC will always convert the difference of $+A_{IN} – (–A_{IN})$ independent of the common mode voltage. The common mode rejection holds up to extremely high frequencies, see Figure 10a. The only requirement is that both inputs can not exceed the AV_{DD} or AV_{SS} power supply voltages. Integral nonlinearity errors (INL) and differential nonlinearity errors (DNL) are independent of the common mode voltage,

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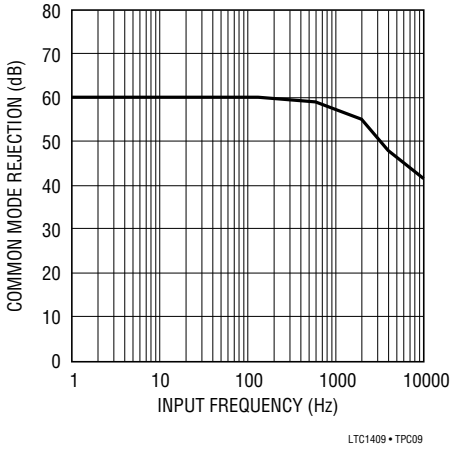


Figure 10a. CMRR vs Input Frequency

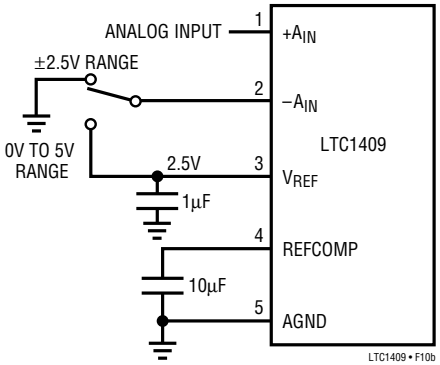


Figure 10b. Selectable 0V to 5V or ±2.5V Input Range

however, the bipolar zero error (BZE) will vary. The change in BZE is typically less than 0.1% of the common mode voltage. Dynamic performance is also affected by the common mode voltage. THD will degrade as the inputs approach either power supply rail, from 86dB with a common mode of 0V to 75dB with a common mode of 2.5V or –2.5V.

Differential inputs allow greater flexibility for accepting different input ranges. Figure 10b shows a circuit that converts a 0V to 5V analog input signal with no additional translation circuitry.

Full-Scale and Offset Adjustment

Figure 11a shows the ideal input/output characteristics for the LTC1409. The code transitions occur midway between successive integer LSB values (i.e., –FS + 0.5LSB, –FS + 1.5LSB, –FS + 2.5LSB,. FS – 1.5LSB, FS – 0.5LSB). The output is two's complement binary with 1LSB = FS – (–FS)/4096 = 5V/4096 = 1.22mV.

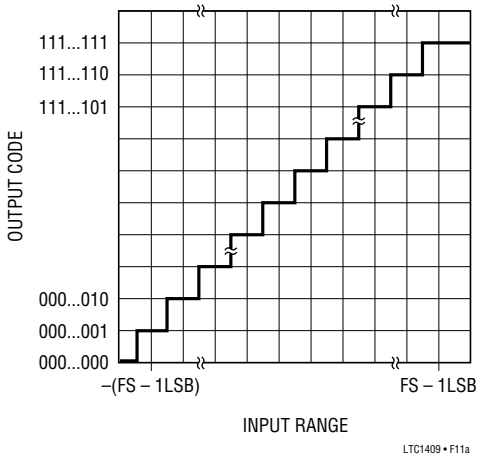


Figure 11a. LTC1409 Transfer Characteristics

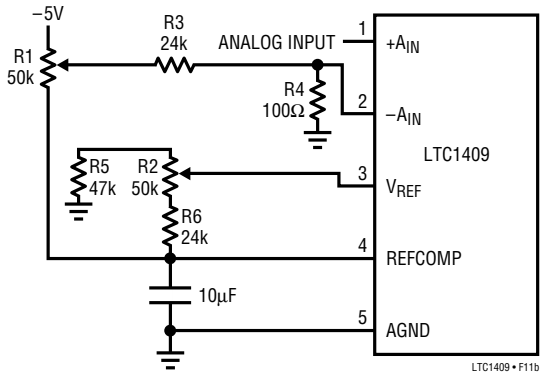


Figure 11b. Offset and Full-Scale Adjust Circuit

In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 11b shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset applied to the $-A_{IN}$ input. For zero offset error apply –0.61mV (i.e., –0.5LSB) at $+A_{IN}$ and adjust the offset at the $-A_{IN}$ input until the output code flickers between 0000 0000 0000 and 1111 1111 1111. For full-scale adjustment, an input voltage of 2.49817V (FS/2 – 1.5LSBs) is applied to A_{IN} and R2 is adjusted until the output code flickers between 0111 1111 1110 and 0111 1111 1111.

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BOARD LAYOUT AND BYPASSING

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1409, a printed circuit board with ground plane is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track.

An analog ground plane separate from the logic system ground should be established under and around the ADC. Pin 5 (AGND), Pin 14 and Pin 19 (ADC's DGND) and all other analog grounds should be connected to this single analog ground point. The REFCOMP bypass capacitor and the OV_{DD} bypass capacitor should also be connected to this analog ground plane. No other digital grounds should be connected to this analog ground plane. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible. In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in the conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a WAIT state during conversion or by using three-state buffers to isolate the ADC data bus. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The LTC1409 has differential inputs to minimize noise coupling. Common mode noise on the $+A_{IN}$ and $-A_{IN}$ leads will be rejected by the input CMRR. The $-A_{IN}$ input can be used as a ground sense for the $+A_{IN}$ input; the LTC1409 will hold and convert the difference voltage between $+A_{IN}$ and $-A_{IN}$. The leads to $+A_{IN}$ (Pin 1) and $-A_{IN}$ (Pin 2) should be kept as short as possible. In applications where this is not possible, the $+A_{IN}$ and $-A_{IN}$ traces should be run side-by-side to equalize coupling.

SUPPLY BYPASSING

High quality, low series resistance ceramic, 10µF bypass capacitors should be used at the V_{DD} and REFCOMP pins as shown in the Typical Application on the first page of this data sheet. Surface mount ceramic capacitors such as Murata GRM235Y5V106Z016 provide excellent bypassing in a small board space. Alternatively 10µF tantalum capacitors in parallel with 0.1µF ceramic capacitors can be used. Bypass capacitors must be located as close to the pins as possible. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

Example Layout

Figure 13a, 13b, 13c and 13d show the schematic and layout of a suggested evaluation board. The layout demonstrates the proper use of decoupling capacitors and ground plane with a two layer printed circuit board.

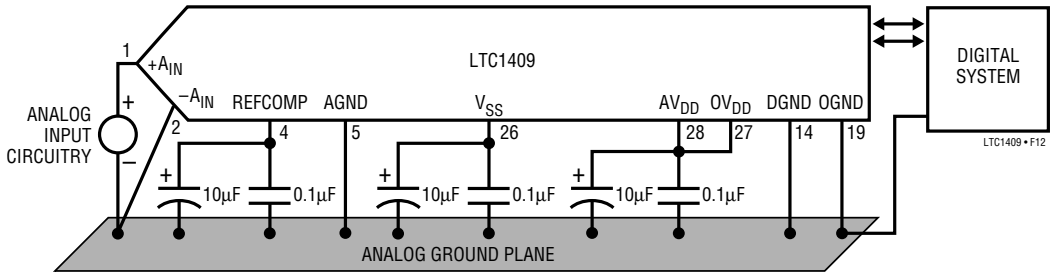


Figure 12. Power Supply Grounding Practice

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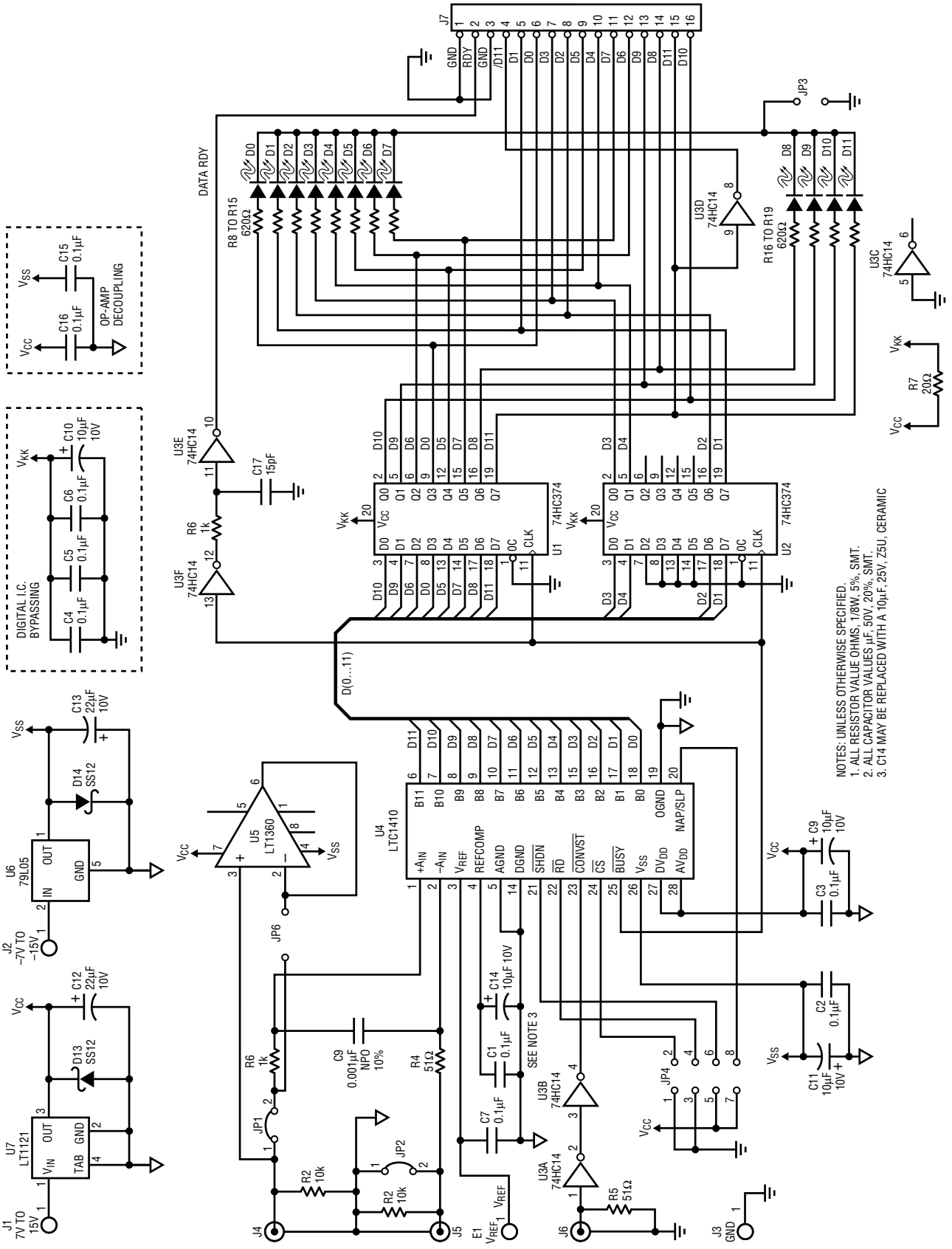


Figure 13a. Suggested Evaluation Circuit Schematic

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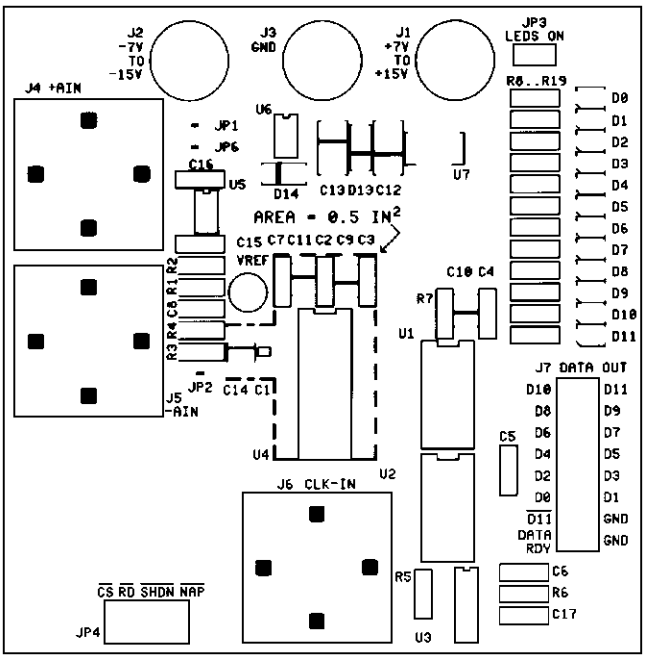


Figure 13b. Suggested Evaluation Circuit Board Component Side Silkscreen

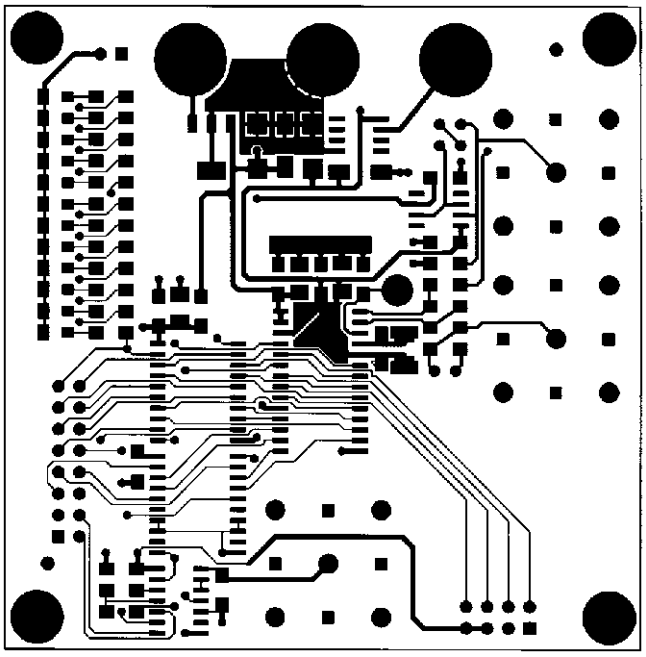


Figure 13c. Suggested Evaluation Circuit Board Component Side Layout

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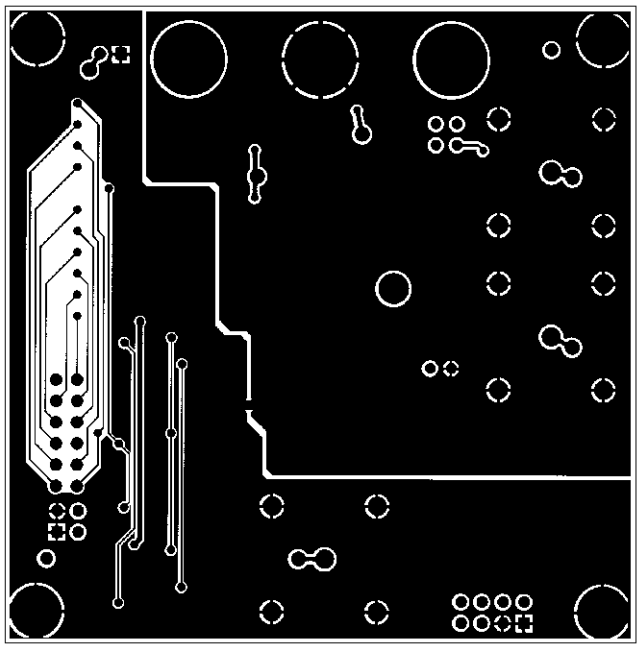


Figure 13d. Suggested Evaluation Circuit Board Solder Side Layout

Digital Interface

The A/D converter is designed to interface with microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ control inputs are common to all peripheral memory interfacing. A separate $\overline{CONVST}$ is used to initiate a conversion.

Internal Clock

The A/D converter has an internal clock that eliminates the need of synchronization between the external clock and the $\overline{CS}$ and $\overline{RD}$ signals found in other ADCs. The internal clock is factory trimmed to achieve a typical conversion time of 0.9µs, and a maximum conversion time over the full operating temperature range of 1.15µs. No external adjustments are required. The guaranteed maximum acquisition time is 150ns. In addition, a throughput time of 1250ns and a minimum sample rate of 800ksps is guaranteed.

Power Shutdown

The LTC1409 provides two power Shutdown modes, Nap and Sleep, to save power during inactive periods. The Nap mode reduces the power by 95% and leaves only the digital logic and reference powered up. The wake-up time from Nap to active is 200ns. In Sleep mode all bias currents are shut down and only leakage current remains, about 1µA. Wake-up time from Sleep mode is much slower since the reference circuit must power up and settle to 0.01% for full 12-bit accuracy. Sleep mode wake-up time is dependent on the value of the capacitor connected to the REFCOMP (Pin 4). The wake-up time is 10ms with the recommended 10µF capacitor.

Shutdown is controlled by Pin 21 ($\overline{SHDN}$). The ADC is in shutdown when it is low. The Shutdown mode is selected with Pin 20 (NAP/$\overline{SLP}$); high selects Nap.

Timing and Control

Conversion start and data read operations are controlled by three digital inputs: $\overline{CONVST}$, $\overline{CS}$ and $\overline{RD}$. A logic "0" applied to the $\overline{CONVST}$ pin will start a conversion after the ADC has been selected (i.e., $\overline{CS}$ is low). Once initiated, it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output. $\overline{BUSY}$ is low during a conversion.

Figures 16 through 20 show several different modes of operation. In modes 1a and 1b (Figures 16 and 17) $\overline{CS}$ and $\overline{RD}$ are both tied low. The falling edge of $\overline{CONVST}$ starts the conversion. The data outputs are always enabled and data

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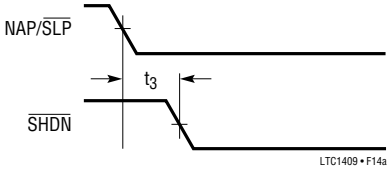


Figure 14a. NAP/SLP to SHDN Timing

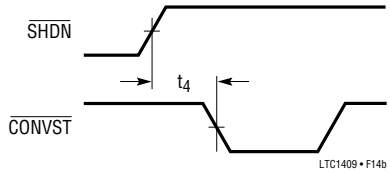


Figure 14b. SHDN to CONVST Wake-Up Timing

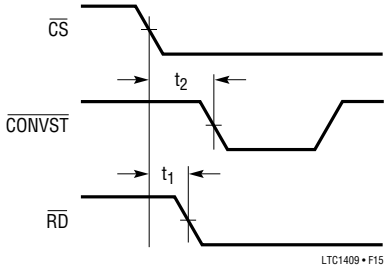


Figure 15. CS to CONVST Setup Timing

can be latched with the BUSY rising edge. Mode 1a shows operation with a narrow logic low CONVST pulse. Mode 1b shows a narrow logic high CONVST pulse.

In mode 2 (Figure 18) CS is tied low. The falling edge of CONVST signal again starts the conversion. Data outputs are in three-state until read by the MPU with the RD signal. Mode 2 can be used for operation with a shared MPU databus.

In slow memory and ROM modes (Figures 19 and 20) CS is tied low and CONVST and RD are tied together. The MPU starts the conversion and reads the output with the RD signal. Conversions are started by the MPU or DSP (no external sample clock).

In slow memory mode the processor applies a logic low to RD (= CONVST) starting the conversion. BUSY goes low forcing the processor into a WAIT state. The previous conversion result appears on the data outputs. When the conversion is complete, the new conversion results appear on the data outputs; BUSY goes high releasing the processor, and the processor takes RD (= CONVST) back high and reads the new conversion data.

In ROM mode, the processor takes RD (= CONVST) low, starting a conversion and reading the previous conversion result. After the conversion is complete, the processor can read the new result and initiate another conversion.

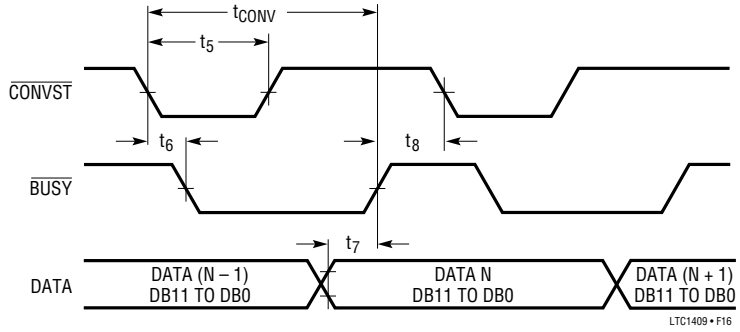


Figure 16. Mode 1a. CONVST Starts a Conversion. Data Outputs Always Enabled (CONVST = ⊓⊓⊓)

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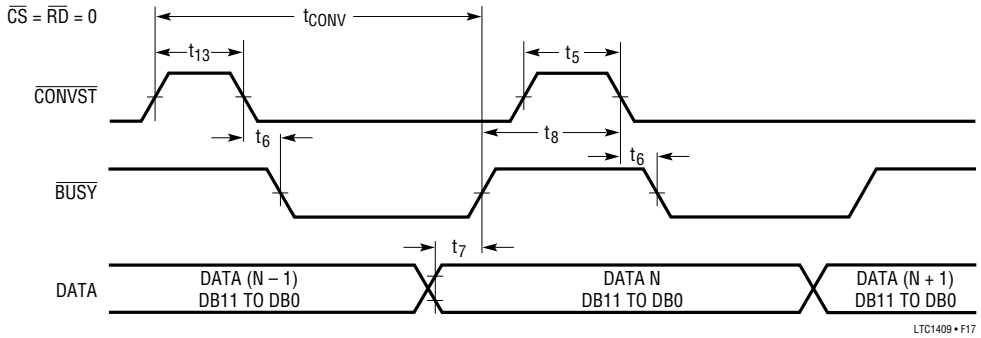


Figure 17. Mode 1b. $\overline{\text{CONVST}}$ Starts a Conversion. Data Outputs Always Enabled

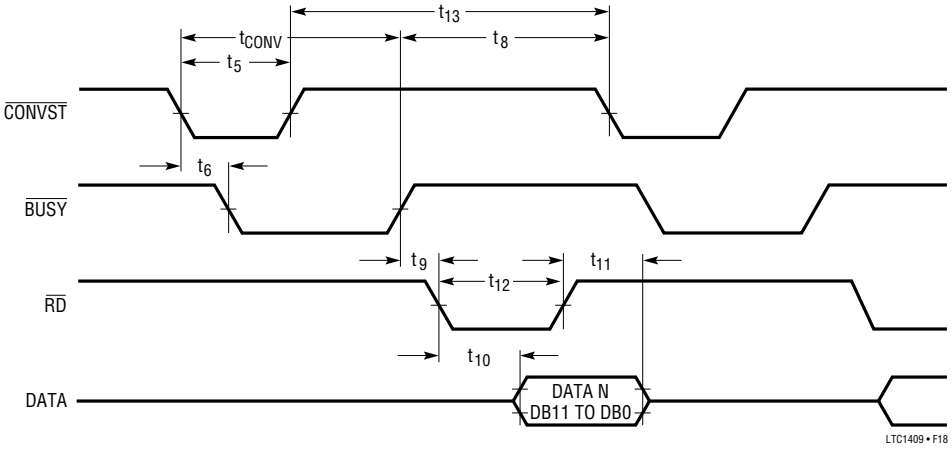


Figure 18. Mode 2. $\overline{\text{CONVST}}$ Starts a Conversion. Data is Read by $\overline{\text{RD}}$

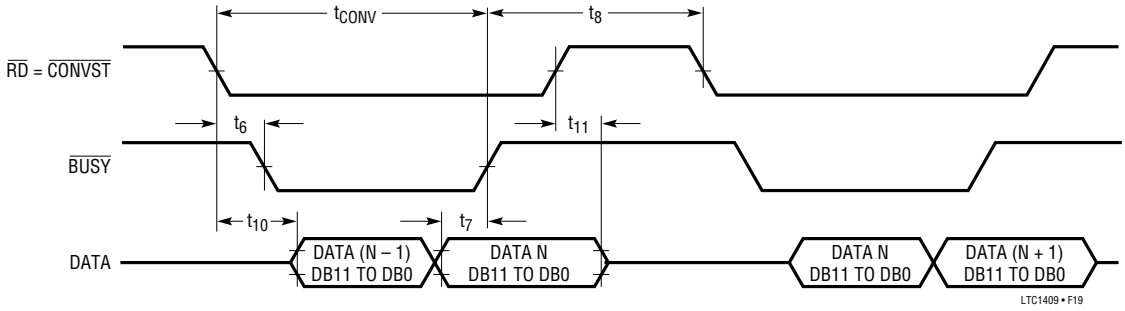


Figure 19. Slow Memory Mode Timing

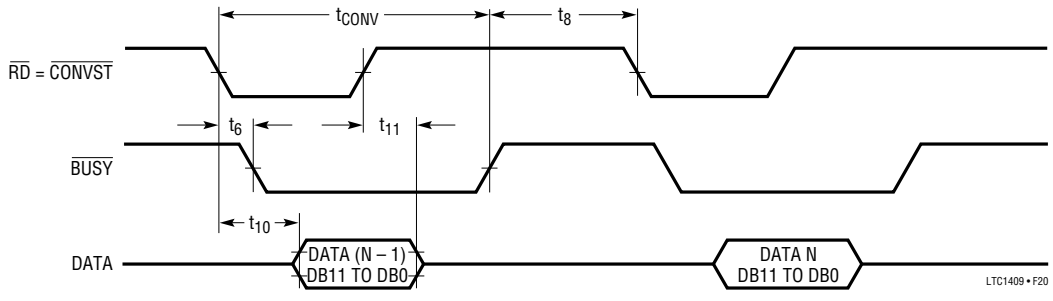
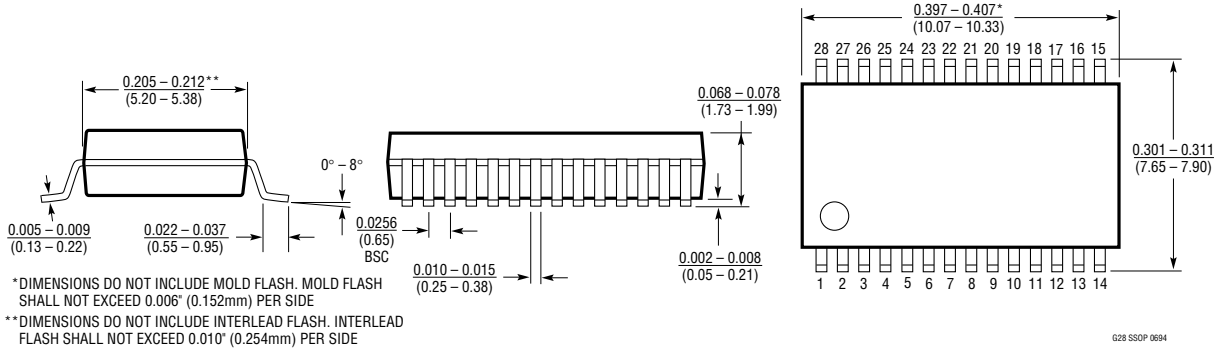


Figure 20. ROM Mode Timing

PACKAGE DESCRIPTION

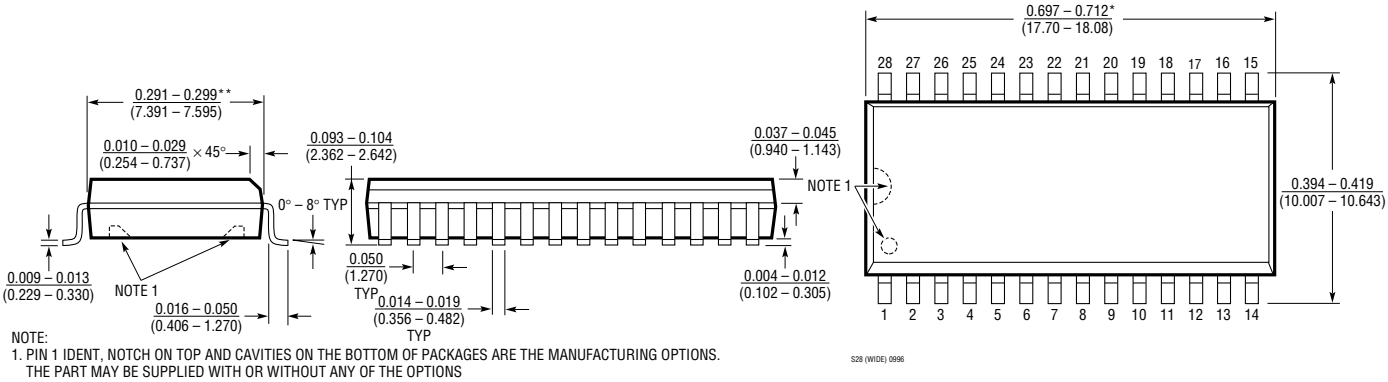
Dimensions in inches (millimeters) unless otherwise noted.

G Package
28-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

SW Package
28-Lead Plastic Small Outline (Wide 0.300)
(LTC DWG # 05-08-1620)



NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PRODUCTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1273/75/76	Complete 5V Sampling 12-Bit ADCs with 70dB SINAD at Nyquist	300ksps, Single or Dual Supplies
LTC1274/77	Low Power 12-Bit ADCs with Nap and Sleep Mode Shutdown	100ksps, 8-Bit or 12-Bit Digital I/O
LTC1278/79	High Speed Sampling 12-Bit ADCs with Shutdown	500ksps/600ksps, Single or Dual Supplies
LTC1282	Complete 3V 12-Bit ADC with 12mW Power Dissipation	Fully Specified for 3V/±3V Supply
LTC1410	High Speed Sampling 12-Bit ADC	1.25Msps, 71dB SINAD at Nyquist, Low Power
LTC1415	High Speed Sampling 12-Bit ADC	1.25Msps, Single 5V Supply, Lowest Power
LTC1419	14-Bit, 800ksps Sampling ADC	81.5dB SINAD, 150mW from ±5V Supplies
LTC1605	16-Bit, 100ksps Sampling ADC	Single Supply, ±10V Input Range, Low Power

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