High Power Step-Down Switching Regulator Controller

FEATURES

- **High Power 5V to 1.xV-3.xV Switching Controller: Can Exceed 10A Output**
- **Maximum Duty Cycle > 90% Permits 3.3V to 2.xV Conversion Using a Low Power 5V Supply**
- **All N-Channel External MOSFETs**
- Fixed Frequency Operation—Small L
- **Excellent Output Regulation: ±1% Over Line, Load and Temperature Variations**
- High Efficiency: Over 95% Possible
- No Low Value Sense Resistor Needed
- Outputs Can Drive External FETs with Up to 10,000pF Gate Capacitance
- Quiescent Current: 350µA Typ, 1µA in Shutdown
- Fast Transient Response
- Adjustable or Fixed 3.3V Output
- Available in 8-Lead SO and 16-Lead GN and SO Packages

APPLICATIONS

- Power Supply for Pentium® II and AMD-K6® Microprocessors
- High Power 5V to 3.xV Regulators
- Local Regulation for Dual Voltage Logic Boards
- Low Voltage, High Current Battery Regulation

DESCRIPTION

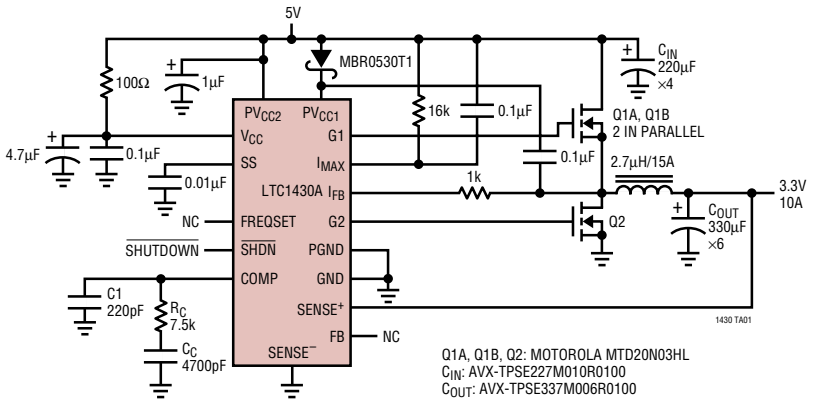
The LTC®1430A is a high power, high efficiency switching regulator controller optimized for 5V to 1.xV-3.xV applications. It includes a precision internal reference and an internal feedback system that can provide output regulation of ±1% over temperature, load current and line voltage shifts. The LTC1430A uses a synchronous switching architecture with two N-channel output devices, eliminating the need for a high power, high cost P-channel device. Additionally, it senses output current across the drain-source resistance of the upper N-channel FET, providing an adjustable current limit without an external low value sense resistor.

The LTC1430A includes a fixed frequency PWM oscillator for low output ripple under virtually all operating conditions. The 200kHz free-running clock frequency can be externally adjusted from 100kHz to above 500kHz. The LTC1430A's maximum duty cycle is typically 93.5% compared to 88% for the LTC1430. This permits 3.3V to 2.xV conversion using a low power 5V supply. The LTC1430A features low 350µA quiescent current, allowing greater than 90% efficiency operation in converter designs from 1A to greater than 50A output current. Shutdown mode drops the LTC1430A supply current to 1µA. **For new designs, refer to the LTC3830**.

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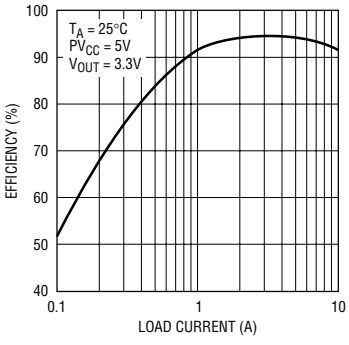
TYPICAL APPLICATION

Typical 5V to 3.3V, 10A Application



Q1A, Q1B, Q2: MOTOROLA MTD20N03HL
C_{IN}: AVX-TPSE227M010R0100
C_{OUT}: AVX-TPSE337M006R0100

Efficiency



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage
- V_{CC} 9V
- $PV_{CC1, 2}$ 13V

Input Voltage
- I_{FB} ..... −0.3V to 18V
- All Other Inputs ..... −0.3V to (V_{CC} + 0.3V)

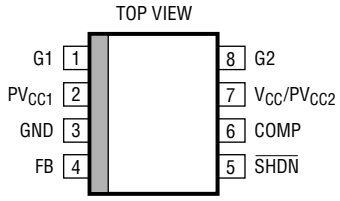
Junction Temperature ..... 150°C

Operating Temperature Range
- LTC1430AC ..... 0°C to 70°C
- LTC1430AI ..... −40°C to 85°C

Storage Temperature Range ..... −65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

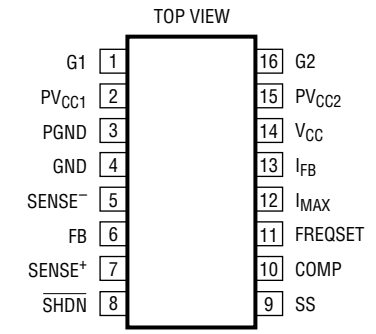
PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LTC1430ACS8
S8 PART MARKING
1430A



GN PACKAGE
16-LEAD PLASTIC SSOP

S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 130°C/W (GN)
T_{JMAX} = 150°C, θ_{JA} = 110°C/W (S)

ORDER PART NUMBER
LTC1430ACGN
LTC1430AIGN
LTC1430ACS

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, T_A = 25°C (Note 2) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1430AC MIN	LTC1430AC TYP	LTC1430AC MAX	LTC1430AI MIN	LTC1430AI TYP	LTC1430AI MAX	UNITS
V_{CC}	Supply Voltage		●	4		8	4		8	V
PV_{CC}	PV_{CC1}, PV_{CC2} Voltage		●	3		13	3		13	V
V_{OUT}	Output Voltage	Figure 1			3.30			3.30		V
V_{FB}	Feedback Voltage	SENSE+ and SENSE− Floating, V_{COMP} = 2.5V	●	1.25	1.265	1.28	1.23	1.265	1.29	V
ΔV_{OUT}	Output Load Regulation Output Line Regulation	Figure 1, I_{OUT} = 0A to 10A Figure 1, V_{CC} = 4.75V to 5.25V			5 1			5 1		mV mV
I_{VCC}	Supply Current (V_{CC} Only)	Figure 2, $V_{\overline{SHDN}} = V_{CC}$ $V_{\overline{SHDN}}$ = 0V	●		350 1	700 10		350 1	700 10	µA µA
I_{PVCC}	Supply Current (PV_{CC})	Figure 2, PV_{CC} = 5V, $V_{\overline{SHDN}} = V_{CC}$ (Note 3) $V_{\overline{SHDN}}$ = 0V			1.5 0.1			1.5 0.1		mA µA
f_{OSC}	Internal Oscillator Frequency	FREQSET Floating	●	140	200	260	130	200	300	kHz

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, T_A = 25°C (Note 2) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1430AC MIN	LTC1430AC TYP	LTC1430AC MAX	LTC1430AI MIN	LTC1430AI TYP	LTC1430AI MAX	UNITS
V_{IH}	$\overline{SHDN}$ Input High Voltage		●	2.4			2.4			V
V_{IL}	$\overline{SHDN}$ Input Low Voltage		●			0.8			0.8	V
I_{IN}	$\overline{SHDN}$ Input Current		●		±0.1	±1		±0.1	±1	µA
g_{mV}	Error Amplifier Transconductance		●	350	650	1100	300	650	1200	µmho
g_{mI}	I_{LIM} Amplifier Transconductance	(Note 4)			2400			2400		µmho
A_V	Error Amplifier Open-Loop Gain	(Note 5)	●	40	48		40	48		dB
I_{MAX}	I_{MAX} Sink Current	$V_{I(MAX)} = V_{CC}$	●	8	12	16	8	12	17	µA
I_{SS}	Soft Start Source Current	V_{SS} = 0V	●	–8	–12	–16	–8	–12	–17	µA
t_r, t_s	Driver Rise/Fall Time	Figure 3, $PV_{CC1} = PV_{CC2}$ = 5V			80	250		80	250	ns
t_{NOV}	Driver Non-Overlap Time	Figure 3, $PV_{CC1} = PV_{CC2}$ = 5V		25	130	250	25	130	250	ns
DC_{MAX}	Maximum Duty Cycle	Figure 3, $V_{COMP} = V_{CC}$, V_{FB} = 1.265V	●	90	93.5		89	93.5		%

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

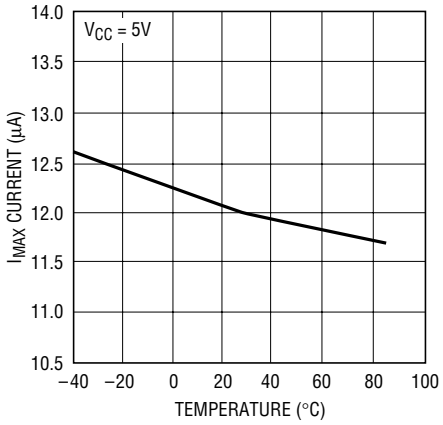
Note 3: Supply current in normal operation is dominated by the current needed to charge and discharge the external FET gates. This will vary with the LTC1430A operating frequency, operating voltage and the external FETs used.

Note 4: The I_{LIM} amplifier can sink but cannot source current. Under normal (not current limited) operation, the I_{LIM} output current will be zero.

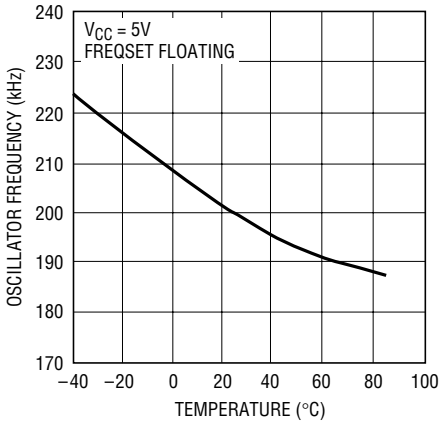
Note 5: The open-loop DC gain and transconductance from the FB pin ($SENSE^+$ and $SENSE^-$ floating) to COMP pin will be A_V and gm_V respectively.

TYPICAL PERFORMANCE CHARACTERISTICS

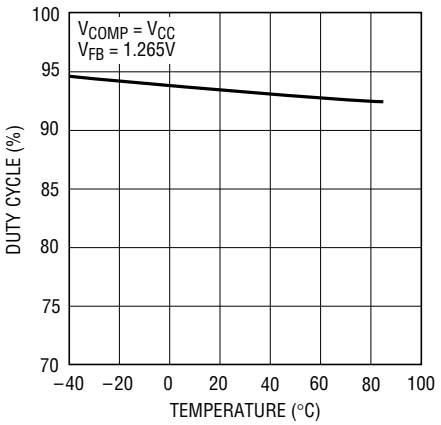
I_{MAX} Pin Sink Current vs Temperature



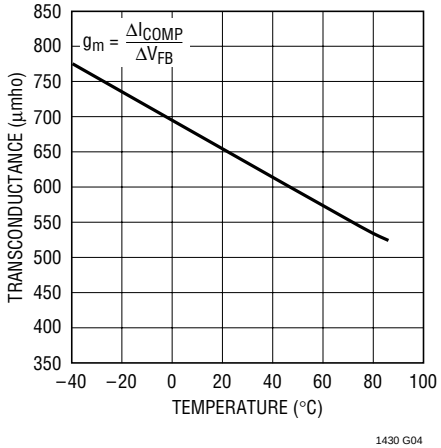
Oscillator Frequency vs Temperature



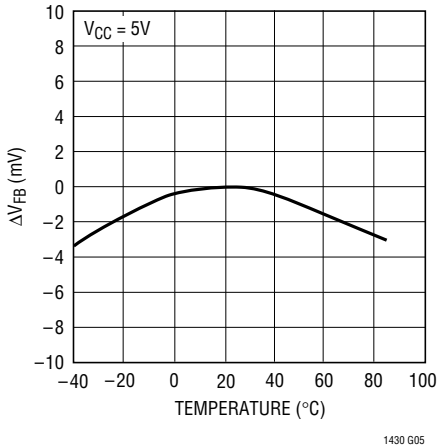
Maximum Duty Cycle vs Temperature



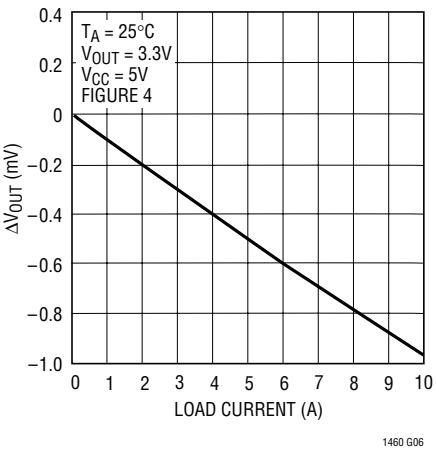
Error Amplifier Transconductance vs Temperature



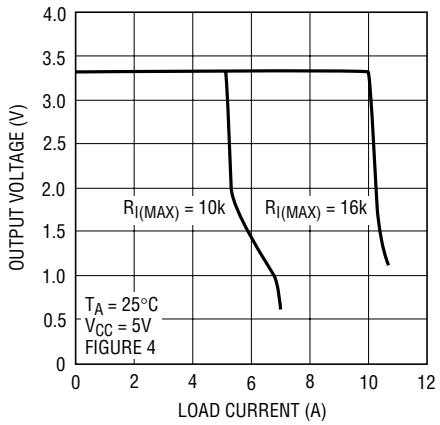
ΔV_{FB} vs Temperature



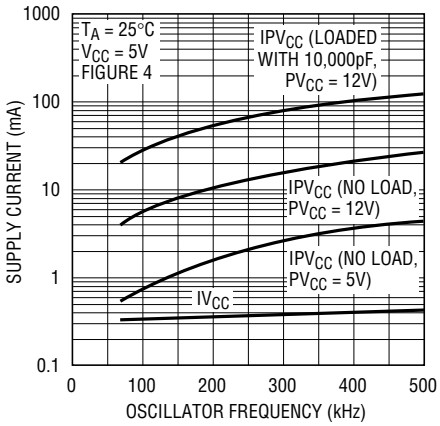
Load Regulation



Output Voltage vs Load Current with Current Limit



Supply Current vs Oscillator Frequency



PIN FUNCTIONS (16-Lead Package/8-Lead Package)

G1 (Pin 1/Pin 1): Driver Output 1. Connect this pin to the gate of the upper N-channel MOSFET, Q1. This output will swing from PV_{CC1} to PGND. It will always be low when G2 is high.

PV_{CC1} (Pin 2/Pin 2): Power V_{CC} for Driver 1. This is the power supply input for G1. G1 will swing from PGND to PV_{CC1}. PV_{CC1} must be connected to a potential of at least $PV_{CC} + V_{GS(ON)}$(Q1). This potential can be generated using an external supply or a simple charge pump connected to the switching node between the upper MOSFET and the lower MOSFET; see Applications Information for details.

PGND (Pin 3/Pin 3): Power Ground. Both drivers return to this pin. It should be connected to a low impedance ground in close proximity to the source of Q2. 8-lead parts have PGND and GND tied together at Pin 3.

GND (Pin 4/Pin 3): Signal Ground. All low power internal circuitry returns to this pin. To minimize regulation errors due to ground currents, GND should be connected to PGND right at the LTC1430A. 8-lead parts have PGND and GND tied together internally at Pin 3.

$SENSE^-$, FB, $SENSE^+$ (Pins 5, 6, 7/Pin 4): These three pins connect to the internal resistor divider and to the internal feedback node. To use the internal divider to set the output voltage to 3.3V, connect $SENSE^+$ to the positive terminal of the output capacitor and $SENSE^-$ to GND. FB should be left floating in applications that use the internal divider. To use an external resistor divider to set the output voltage, float $SENSE^+$ and $SENSE^-$ and connect the external resistor divider to FB.

$\overline{SHDN}$ (Pin 8/Pin 5): Shutdown. A TTL compatible low level at $\overline{SHDN}$ for longer than 50μs puts the LTC1430A into shutdown mode. In shutdown, G1 and G2 go low, all internal circuits are disabled and the quiescent current drops to 10μA max. A TTL compatible high level at $\overline{SHDN}$ allows the part to operate normally.

SS (Pin 9/NA): Soft Start. The SS pin allows an external capacitor to be connected to implement a soft start function. An external capacitor from SS to ground controls the start-up time and also compensates the current limit loop, allowing the LTC1430A to enter and exit current limit cleanly. See Applications Information for more details.

COMP (Pin 10/Pin 6): External Compensation. The COMP pin is connected directly to the output of the error amplifier and the input of the PWM. An RC network is used at this node to compensate the feedback loop to provide optimum transient response. See Applications Information for compensation details.

FREQSET (Pin 11/NA): Frequency Set. This pin is used to set the free running frequency of the internal oscillator. With the pin floating, the oscillator runs at about 200kHz. A resistor from FREQSET to ground will speed up the oscillator; a resistor to V_{CC} will slow it down. See Applications Information for resistor selection details.

I_{MAX} (Pin 12/NA): Current Limit Set. I_{MAX} sets the threshold for the internal current limit comparator. If I_{FB} drops below I_{MAX} with G1 on, the LTC1430A will go into current limit. I_{MAX} has a 12μA pull-down to GND. It can be adjusted with an external resistor to PV_{CC} or an external voltage source.

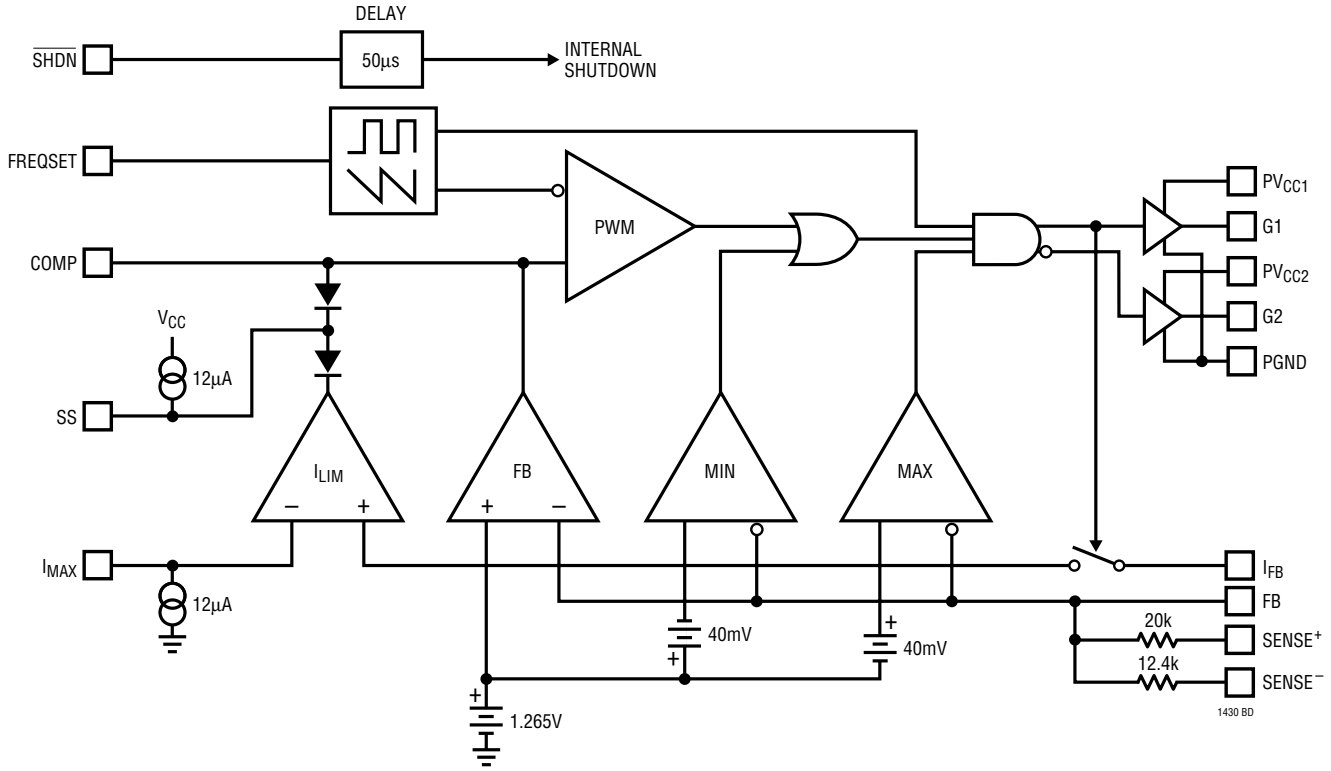
I_{FB} (Pin 13/NA): Current Limit Sense. Connect to the switched node at the source of Q1 and the drain of Q2 through a 1k resistor. The 1k resistor is required to prevent voltage transients from damaging I_{FB}. This pin can be taken up to 18V above GND without damage.

V_{CC} (Pin 14/Pin 7): Power Supply. All low power internal circuits draw their supply from this pin. Connect to a clean power supply, separate from the main PV_{CC} supply at the drain of Q1. This pin requires a 4.7μF or greater bypass capacitor. 8-lead parts have V_{CC} and PV_{CC2} tied together at Pin 7 and require at least a 10μF bypass to GND.

PV_{CC2} (Pin 15/Pin 7): Power V_{CC} for Driver 2. This is the power supply input for G2. G2 will swing from GND to PV_{CC2}. PV_{CC2} is usually connected to the main high power supply. 8-lead parts have V_{CC} and PV_{CC2} tied together at Pin 7 and require at least a 10μF bypass to GND.

G2 (Pin 16/Pin 8): Driver Output 2. Connect this pin to the gate of the lower N-channel MOSFET, Q2. This output will swing from PV_{CC2} to PGND. It will always be low when G1 is high.

BLOCK DIAGRAM



TEST CIRCUITS

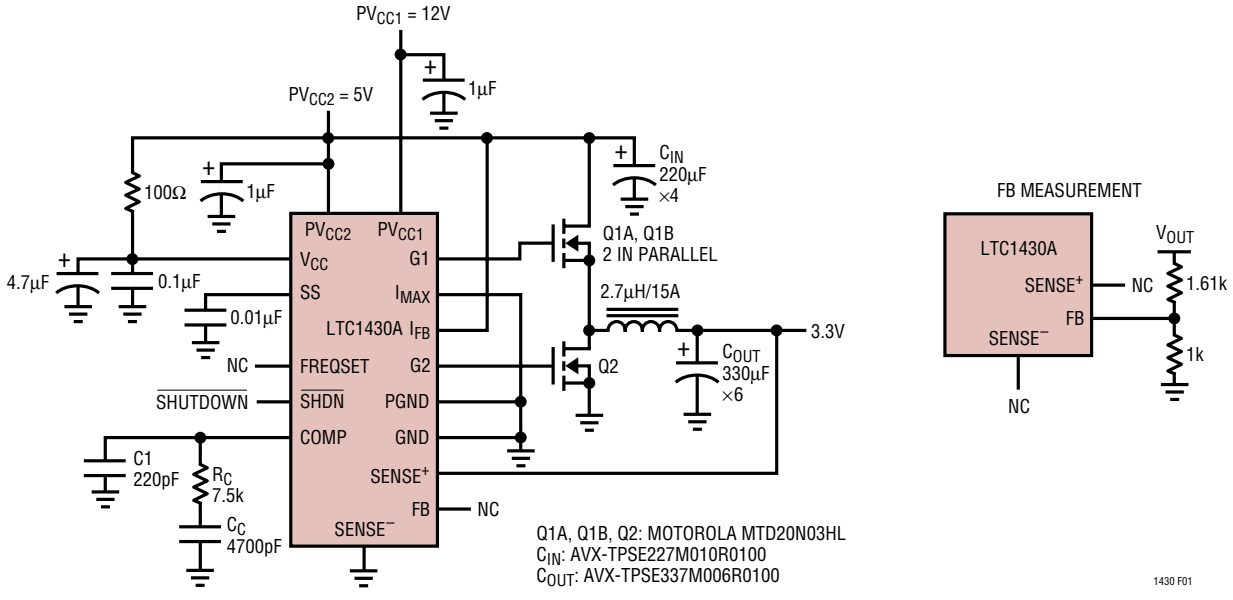


Figure 1

TEST CIRCUITS

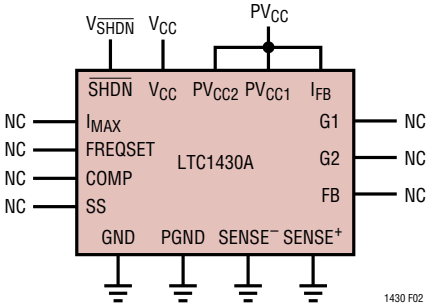


Figure 2

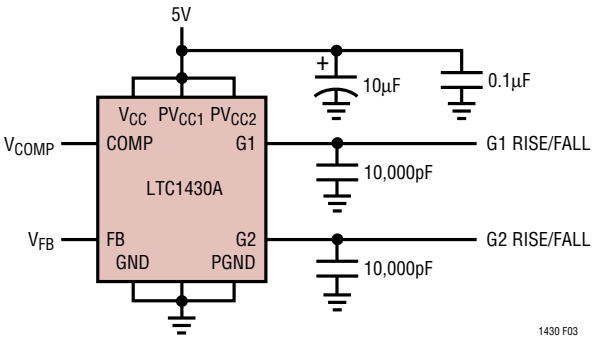


Figure 3

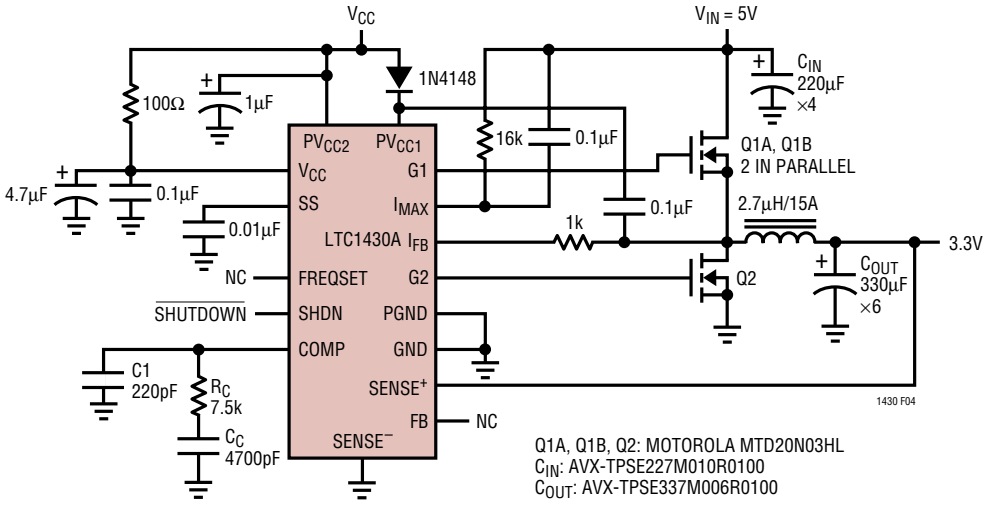


Figure 4

APPLICATIONS INFORMATION

OVERVIEW

The LTC1430A is a voltage feedback PWM switching regulator controller (see Block Diagram) designed for use in high power, low voltage step-down (buck) converters. It includes an onboard PWM generator, a precision reference trimmed to ±0.5%, two high power MOSFET gate drivers and all necessary feedback and control circuitry to form a complete switching regulator circuit. The PWM loop nominally runs at 200kHz.

The 16-lead versions of the LTC1430A include a current limit sensing circuit that uses the upper external power MOSFET as a current sensing element, eliminating the need for an external sense resistor.

Also included in the 16-lead version is an internal soft start feature that requires only a single external capacitor to operate. In addition, 16-lead parts feature an adjustable oscillator which can run at frequencies from 50kHz to 500kHz, allowing added flexibility in external component selection. The 8-lead version does not include current limit, internal soft start or frequency adjustability.

THEORY OF OPERATION

Primary Feedback Loop

The LTC1430A senses the output voltage of the circuit at the output capacitor with the $SENSE^+$ and $SENSE^-$ pins and feeds this voltage back to the internal transconductance amplifier FB. FB compares the resistor-divided output voltage to the internal 1.265V reference and outputs an error signal to the PWM comparator. This is then compared to a fixed frequency sawtooth waveform generated by the internal oscillator to generate a pulse width modulated signal. This PWM signal is fed back to the external MOSFETs through G1 and G2, closing the loop. Loop compensation is achieved with an external compensation network at COMP, the output node of the FB transconductance amplifier.

MIN, MAX Feedback Loops

Two additional comparators in the feedback loop provide high speed fault correction in situations where the FB amplifier may not respond quickly enough. MIN compares the feedback signal to a voltage 40mV (3%) below the internal reference. At this point, the MIN comparator overrides the FB amplifier and forces the loop to full duty cycle, set by the internal oscillator at about 93.5%. Similarly, the MAX comparator monitors the output voltage at 3% above the internal reference and forces the output to 0% duty cycle when tripped. These two comparators prevent extreme output perturbations with fast output transients, while allowing the main feedback loop to be optimally compensated for stability.

Current Limit Loop

The 16-lead LTC1430A devices include yet another feedback loop to control operation in current limit. The current limit loop is disabled in the 8-lead device. The I_{LIM} amplifier monitors the voltage drop across external MOSFET Q1 with the I_{FB} pin during the portion of the cycle when G1 is high. It compares this voltage to the voltage at the I_{MAX} pin. As the peak current rises, the drop across Q1 due to its $R_{DS(ON)}$ increases. When I_{FB} drops below I_{MAX}, indicating that Q1's drain current has exceeded the maximum level, I_{LIM} starts to pull current out of the external soft start capacitor, cutting the duty cycle and controlling the output current level. At the same time, the I_{LIM} comparator generates a signal to disable the MIN comparator to prevent it from conflicting with the current limit circuit. If the internal feedback node drops below about 0.8V, indicating a severe output overload, the circuitry will force the internal oscillator to slow down by a factor of as much as 100. If desired, the turn on time of the current limit loop can be controlled by adjusting the size of the soft start capacitor, allowing the LTC1430A to withstand short overcurrent conditions without limiting.

By using the $R_{DS(ON)}$ of Q1 to measure the output current, the current limit circuit eliminates the sense resistor that would otherwise be required and minimizes the number of components in the external high current path. Because power MOSFET $R_{DS(ON)}$ is not tightly controlled and varies with temperature, the LTC1430A current limit is not designed to be accurate; it is meant to prevent damage to the power supply circuitry during fault conditions. The actual current level where the limiting circuit begins to take effect may vary from unit to unit, depending on the power MOSFETs used. See Soft Start and Current Limit for more details on current limit operation.

APPLICATIONS INFORMATION

MOSFET Gate Drive

Gate drive for the top N-channel MOSFET Q1 is supplied from PV_{CC1}. This supply must be above PV_{CC} (the main power supply input) by at least one power MOSFET $V_{GS(ON)}$ for efficient operation. An internal level shifter allows PV_{CC1} to operate at voltages above V_{CC} and PV_{CC}, up to 13V maximum. This higher voltage can be supplied with a separate supply, or it can be generated using a simple charge pump as shown in Figure 5. When using a separate PV_{CC1} supply, the PV_{CC} input may exhibit a large inrush current if PV_{CC1} is present during power up. The 93.5% maximum duty cycle ensures that the charge pump will always provide sufficient gate drive to Q1. Gate drive for the bottom MOSFET Q2 is provided through PV_{CC2} for 16-lead devices or V_{CC}/PV_{CC2} for the 8-lead device. PV_{CC2} can usually be driven directly from PV_{CC} with 16-lead parts, although it can also be charge pumped or connected to an alternate supply if desired. 3.3V input applications use 3.3V at PV_{CC} and 5V at V_{CC} and PV_{CC1}. See 3.3V Input Supply Operation for more details. The 8-lead part requires an RC filter from PV_{CC} to V_{CC} to ensure proper operation; see Input Supply Considerations.

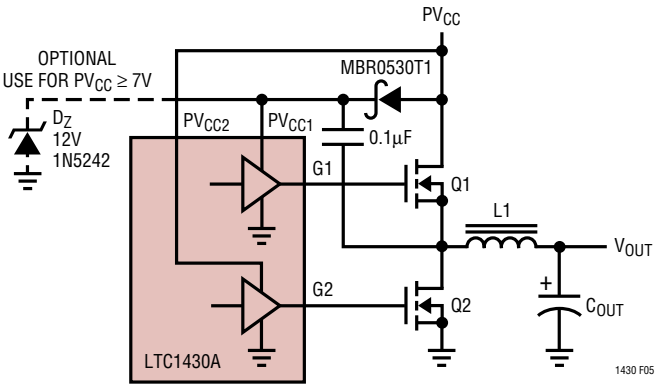


Figure 5. Doubling Charge Pump

Synchronous Operation

The LTC1430A uses a synchronous switching architecture, with MOSFET Q2 taking the place of the diode in a classical buck circuit (Figure 6). This improves efficiency by reducing the voltage drop and the resultant power dissipation across Q2 to $V_{ON} = (I)(R_{DSON(Q2)})$, usually much lower than the V_F of the diode in the classical circuit. This more than offsets the additional gate drive required by the second MOSFET, allowing the LTC1430A to achieve efficiencies in the mid-90% range for a wide range of load currents.

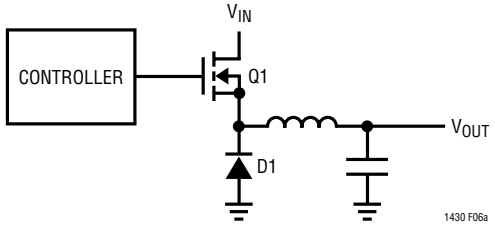


Figure 6a. Classical Buck Architecture

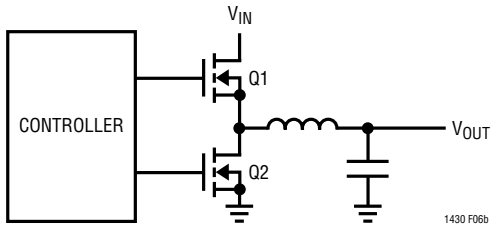


Figure 6b. Synchronous Buck Architecture

Another feature of the synchronous architecture is that unlike a diode, Q2 can conduct current in either direction. This allows the output of a typical LTC1430A circuit to sink current as well as sourcing it while remaining in regulation. The ability to sink current at the output allows the LTC1430A to be used with reactive or other nonconventional loads that may supply current to the regulator as well as drawing current from it. An example is a high current logic termination supply, such as the GTL terminator shown in the Typical Applications section.

EXTERNAL COMPONENT SELECTION

Power MOSFETs

Two N-channel power MOSFETs are required for most LTC1430A circuits. These should be selected based primarily on threshold and on-resistance considerations; thermal dissipation is often a secondary concern in high efficiency designs. Required MOSFET threshold should be determined based on the available power supply voltages and/or the complexity of the gate drive charge pump

APPLICATIONS INFORMATION

scheme. In 5V input designs where an auxiliary 12V supply is available to power PV_{CC1} and PV_{CC2}, standard MOSFETs with $R_{DS(ON)}$ specified at V_{GS} = 5V or 6V can be used with good results. The current drawn from this supply varies with the MOSFETs used and the LTC1430A's operating frequency, but is generally less than 50mA.

LTC1430A designs that use a doubler charge pump to generate gate drive for Q1 and run from PV_{CC} voltages below 7V cannot provide enough gate drive voltage to fully enhance standard power MOSFETs. When run from 5V, a doubler circuit may work with standard MOSFETs, but the MOSFET R_{ON} may be quite high, raising the dissipation in the FETs and costing efficiency. Logic level FETs are a better choice for 5V PV_{CC} systems; they can be fully enhanced with a doubler charge pump and will operate at maximum efficiency. Doubler designs running from PV_{CC} voltages near 4V will begin to run into efficiency problems even with logic level FETs; such designs should be built with tripler charge pumps (see Figure 7) or with newer, super low threshold MOSFETs. Note that doubler charge pump designs running from more than 7V and all tripler charge pump designs should include a zener clamp diode D_Z at PV_{CC1} to prevent transients from exceeding the absolute maximum rating at that pin.

Once the threshold voltage has been selected, R_{ON} should be chosen based on input and output voltage, allowable power dissipation and maximum required output current. In a typical LTC1430A buck converter circuit operating in continuous mode, the average inductor current is equal to the output load current. This current is always flowing through either Q1 or Q2 with the power dissipation split up according to the duty cycle:

$$DC\ (Q1) = \frac{V_{OUT}}{V_{IN}}$$

$$DC\ (Q2) = 1 - \frac{V_{OUT}}{V_{IN}} = \frac{(V_{IN} - V_{OUT})}{V_{IN}}$$

The R_{ON} required for a given conduction loss can now be calculated by rearranging the relation $P = I^2R$:

$$R_{ON}\ (Q1) = \frac{P_{MAX}(Q1)}{DC(Q1)(I_{MAX}^2)} = \frac{V_{IN}(P_{MAX})(Q1)}{V_{OUT}(I_{MAX}^2)}$$

$$R_{ON}\ (Q2) = \frac{P_{MAX}(Q2)}{DC(Q2)(I_{MAX}^2)} = \frac{V_{IN}(P_{MAX})(Q2)}{(V_{IN} - V_{OUT})(I_{MAX}^2)}$$

P_{MAX} should be calculated based primarily on required efficiency. A typical high efficiency circuit designed for 5V in, 3.3V at 10A out might require no more than 3% efficiency loss at full load for each MOSFET. Assuming roughly 90% efficiency at this current level, this gives a P_{MAX} value of (3.3V)(10A/0.9)(0.03) = 1.1W per FET and a required R_{ON} of:

$$R_{ON}\ (Q1) = \frac{(5V)(1.1W)}{(3.3V)(10A^2)} = 0.017\Omega$$

$$R_{ON}\ (Q2) = \frac{(5V)(1.1W)}{(5V - 3.3V)(10A^2)} = 0.032\Omega$$

Note that the required R_{ON} for Q2 is roughly twice that of Q1 in this example. This application might specify a single 0.03Ω device for Q2 and parallel two more of the same devices to form Q1. Note also that while the required R_{ON} values suggest large MOSFETs, the dissipation numbers

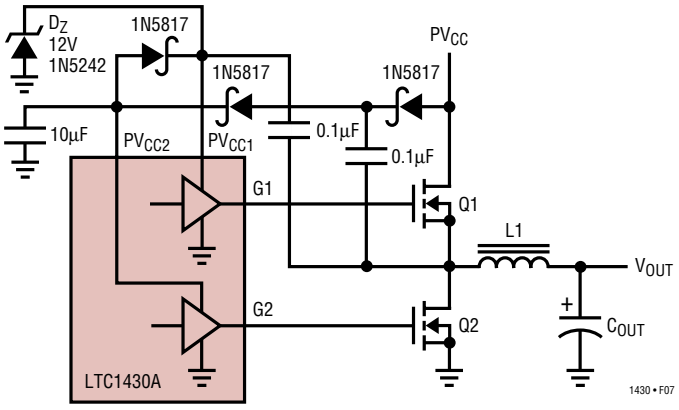


Figure 7. Tripling Charge Pump

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are only 1.1W per device or less — large TO-220 packages and heat sinks are not necessarily required in high efficiency applications. Siliconix Si4410DY (in SO-8) and Motorola MTD20N03HL (in DPAK) are two small, surface mount devices with R_{ON} values of 0.03Ω or below with 5V of gate drive; both work well in LTC1430A circuits with up to 10A output current. A higher P_{MAX} value will generally decrease MOSFET cost and circuit efficiency and increase MOSFET heat sink requirements.

Inductor

The inductor is often the largest component in an LTC1430A design and should be chosen carefully. Inductor value and type should be chosen based on output slew rate requirements and expected peak current. Inductor value is primarily controlled by the required current slew rate. The maximum rate of rise of the current in the inductor is set by its value, the input-to-output voltage differential and the maximum duty cycle of the LTC1430A. In a typical 5V to 3.3V application, the maximum rise time will be:

$$90\% \frac{(V_{IN} - V_{OUT})}{L} \frac{AMPS}{SECOND} = \frac{1.53A}{\mu s} \frac{I}{L}$$

where L is the inductor value in μH. A 2μH inductor would have a 0.76A/μs rise time in this application, resulting in a 6.5μs delay in responding to a 5A load current step. During this 6.5μs, the difference between the inductor current and the output current must be made up by the output capacitor, causing a temporary droop at the output. To minimize this effect, the inductor value should usually be in the 1μH to 5μH range for most typical 5V to 2.xV-3.xV LTC1430A circuits. Different combinations of input and output voltages and expected loads may require different values.

Once the required value is known, the inductor core type can be chosen based on peak current and efficiency requirements. Peak current in the inductor will be equal to the maximum output load current added to half the peak-to- peak inductor ripple current. Ripple current is set by the inductor value, the input and output voltage and the operating frequency. If the efficiency is high and can be approximately equal to 1, the ripple current is approximately equal to:

$$\Delta I = \frac{(V_{IN} - V_{OUT})}{(f_{OSC})(L)} DC$$

$$DC = \frac{V_{OUT}}{V_{IN}}$$

f_{OSC} = LTC1430A oscillator frequency
L = inductor value

Solving this equation with our typical 5V to 3.3V application, we get:

$$\frac{(1.7)(0.66)}{(200kHz)(2\mu H)} = 2.8A_{P-P}$$

Peak inductor current at 10A load:

$$10A + \frac{2.8A}{2} = 11.4A$$

The inductor core must be adequate to withstand this peak current without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss. Note that the current may rise above this maximum level in circuits under current limit or under fault conditions in unlimited circuits; the inductor should be sized to withstand this additional current.

Input and Output Capacitors

A typical LTC1430A design puts significant demands on both the input and output capacitors. Under normal steady load operation, a buck converter like the LTC1430A draws square waves of current from the input supply at the switching frequency, with the peak value equal to the output current and the minimum value near zero. Most of this current must come from the input bypass capacitor, since few raw supplies can provide the current slew rate to feed such a load directly. The resulting RMS current flow in the input capacitor will heat it up, causing premature capacitor failure in extreme cases. Maximum RMS current occurs with 50% PWM duty cycle, giving an RMS current value equal to $I_{OUT}/2$. A low ESR input capacitor with an adequate ripple current rating must be used to ensure reliable operation. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours (3 months) lifetime; further derating of the input capacitor ripple current beyond the manufacturer's specification is recommended to extend the useful life of the circuit.

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The output capacitor in a buck converter sees much less ripple current under steady-state conditions than the input capacitor. Peak-to-peak current is equal to that in the inductor, usually a fraction of the total load current. Output capacitor duty places a premium not on power dissipation but on low ESR. During an output load transient, the output capacitor must supply all of the additional load current demanded by the load until the LTC1430A can adjust the inductor current to the new value. ESR in the output capacitor results in a step in the output voltage equal to the ESR value multiplied by the change in load current. A 5A load step with a 0.05Ω ESR output capacitor will result in a 250mV output voltage shift; this is a 7.6% output voltage shift for a 3.3V supply! Because of the strong relationship between output capacitor ESR and output load transient response, the output capacitor is usually chosen for ESR, not for capacitance value; a capacitor with suitable ESR will usually have a larger capacitance value than is needed to control steady-state output ripple.

Electrolytic capacitors rated for use in switching power supplies with specified ripple current ratings and ESR can be used effectively in LTC1430A applications. OS-CON electrolytic capacitors from Sanyo give excellent performance and have a very high performance/size ratio for an electrolytic capacitor. Surface mount applications can use either electrolytic or dry tantalum capacitors. Tantalum capacitors must be surge tested and specified for use in switching power supplies; low cost, generic tantalums are known to have very short lives followed by explosive deaths in switching power supply applications. AVX TPS series surface mount devices are popular tantalum capacitors that work well in LTC1430A applications. A common way to lower ESR and raise ripple current capability is to parallel several capacitors. A typical LTC1430A application might require an input capacitor with a 5A ripple current capacity and 2% output shift with a 10A output load step, which requires a 0.007Ω output capacitor ESR. Sanyo OS-CON part number 10SA220M (220µF/10V) capacitors feature 2.3A allowable ripple current at 85°C and 0.035Ω ESR; three in parallel at the input and six at the output will meet the above requirements.

Input Supply Considerations/Charge Pump

The 16-lead LTC1430A requires four supply voltages to operate: PV_{CC} for the main power input, PV_{CC1} and PV_{CC2} for MOSFET gate drive and a clean, low ripple V_{CC} for the LTC1430A internal circuitry (Figure 8). In many applications, PV_{CC} and PV_{CC2} can be tied together and fed from a common high power supply, provided that the supply voltage is high enough to fully enhance the gate of external MOSFET Q2. This can be the 5V system supply if a logic level MOSFET is used for Q2. V_{CC} can usually be filtered with an RC from this same high power supply; the low quiescent current (typically 350µA) allows the use of relatively large filter resistors and correspondingly small filter capacitors. 100Ω and 4.7µF usually provide adequate filtering for V_{CC}.

The 8-lead version of the LTC1430A has the PV_{CC2} and V_{CC} pins tied together inside the package (Figure 9). This pin, brought out as V_{CC}/PV_{CC2}, has the same low ripple requirements as the 16-lead part, but must also be able to supply the gate drive current to Q2. This can be obtained

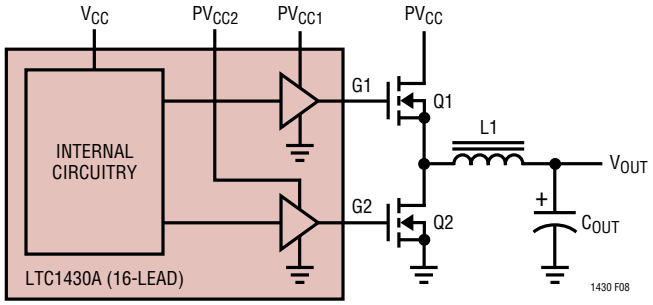


Figure 8. 16-Lead Power Supplies

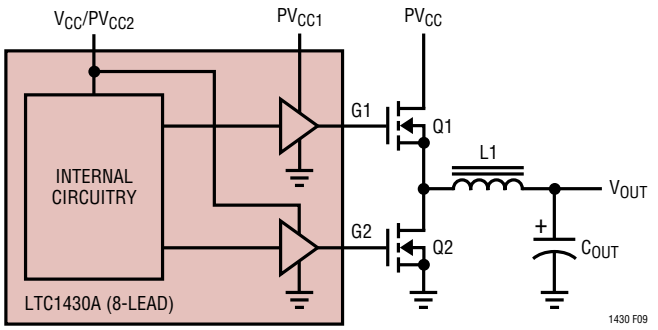


Figure 9. 8-Lead Power Supplies

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by using a larger RC filter from the PV_{CC} pin; 22Ω and 10µF work well here. The 10µF capacitor must be VERY close to the part (preferably right underneath the unit) or output regulation may suffer.

For both versions of the LTC1430A, PV_{CC1} must be higher than PV_{CC} by at least one external MOSFET $V_{GS(ON)}$ to fully enhance the gate of Q1. This higher voltage can be provided with a separate supply (typically 12V) which should power up after PV_{CC}, or it can be generated with a simple charge pump (Figure 5). The charge pump consists of a Schottky diode from PV_{CC} to PV_{CC1} and a 0.1µF capacitor from PV_{CC1} to the switching node at the drain of Q2. This circuit provides $2PV_{CC} – V_F$ to PV_{CC1} while Q1 is ON and $PV_{CC} – V_F$ while Q1 is OFF where V_F is the ON voltage of the Schottky diode. Ringing at the drain of Q2 can cause transients above $2PV_{CC}$ at PV_{CC1}; if PV_{CC} is higher than 7V, a 12V zener diode should be included from PV_{CC1} to PGND to prevent transients from damaging the circuitry at PV_{CC2} or the gate of Q1.

More complex charge pumps can be constructed with the 16-lead versions of the LTC1430A to provide additional voltages for use with standard threshold MOSFETs or very low PV_{CC} voltages. A tripling charge pump (Figure 7) can provide $2PV_{CC}$ and $3PV_{CC}$ voltages. These can be connected to PV_{CC2} and PV_{CC1} respectively, allowing standard threshold MOSFETs to be used with 5V at PV_{CC} or 5V logic level threshold MOSFETs to be used with 3.3V at PV_{CC}. V_{CC} can be driven from the same potential as PV_{CC2}, allowing the entire system to run from a single 3.3V supply. Tripling charge pumps require the use of Schottky diodes to minimize forward drop across the diodes at start-up. The tripling charge pump circuit will tend to rectify any ringing at the drain of Q2 and can provide well more than $3PV_{CC}$ at PV_{CC1}; all tripling (or higher multiplying factor) circuits should include a 12V zener clamp diode D_Z to prevent overvoltage at PV_{CC1}.

3.3V Input Supply Operation

The LTC1430A can be used with input supply voltages lower than 5V as long as a low power 5V supply is available to power the LTC1430A itself and to provide gate drive to the external MOSFETs. A typical 3.3V to 2.5V application is shown in Figure 10. The circuit can supply up to 10A at 2.5V output, and draws this power from the 3.3V supply. The 5V supply typically needs to supply about 20mA to provide gate drive to the external MOSFETs and keep the LTC1430A control circuits powered. For applications where there is no 5V supply available, see the LTC1649 data sheet.

Compensation and Transient Response

The LTC1430A voltage feedback loop is compensated at the COMP pin; this is the output node of the internal g_m error amplifier. The loop can generally be compensated

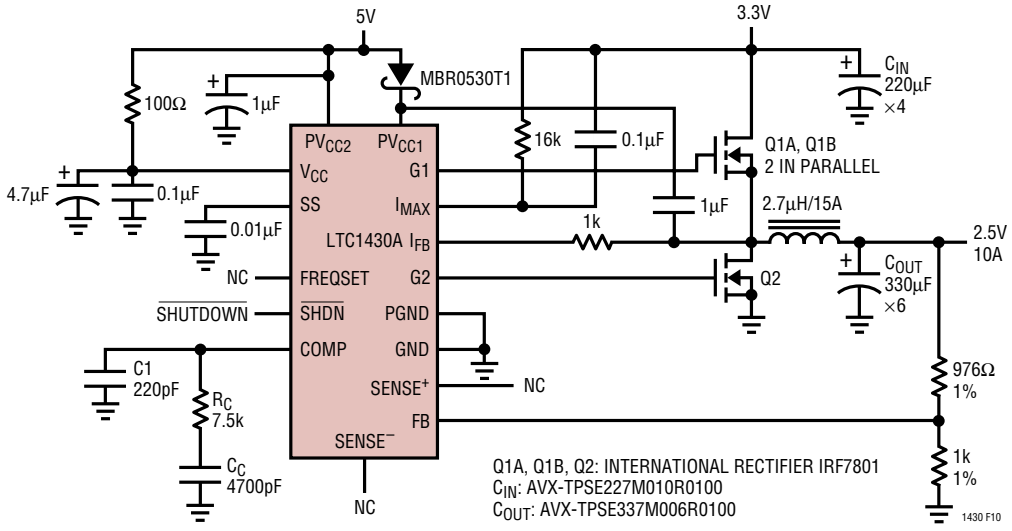


Figure 10. 3.3V to 2.5V, 10A Application

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properly with an RC network from COMP to GND and an additional small C from COMP to GND (Figure 11). Loop stability is affected by inductor and output capacitor values and by other factors. Optimum loop response can be obtained by using a network analyzer to find the loop poles and zeros; nearly as effective and a lot easier is to empirically tweak the R_C values until the transient recovery looks right with an output load step. Table 1 shows recommended compensation components for 5V to 3.3V applications based on the inductor and output capacitor values. The values were calculated using multiple paralleled 330µF AVX TPS series surface mount tantalum capacitors as the output capacitor.

Table 1. Recommended Compensation Network for 5V to 3.3V Application Using Multiple 330µF AVX Output Capacitors

L1 (µH)	C_{OUT} (µF)	R_C (kΩ)	C_C (µF)	C1 (pF)
1	990	1.8	0.022	820
1	1980	3.6	0.01	470
1	4950	9.1	0.0047	150
1	9900	18	0.0022	82
2.7	990	3.6	0.01	470
2.7	1980	7.5	0.0047	220
2.7	4950	18	0.0022	82
2.7	9900	39	0.001	39
5.6	990	9.1	0.0047	150
5.6	1980	18	0.0022	82
5.6	4950	47	820pF	33
5.6	9900	91	470pF	15
10	990	18	0.0022	82
10	1980	39	0.001	39
10	4950	91	470pF	15
10	9900	180	220pF	10

Output transient response is set by three major factors: the time constant of the inductor and the output capacitor, the ESR of the output capacitor, and the loop compensation components. The first two factors usually have much more impact on overall transient recovery time than the third; unless the loop compensation is way off, more improvement can be had by optimizing the inductor and the output capacitor than by fiddling with the loop compensation components. In general, a smaller value inductor will improve transient response at the expense of ripple and inductor core saturation rating. Minimizing output capacitor ESR will also help optimize output transient response. See Input and Output Capacitors for more information.

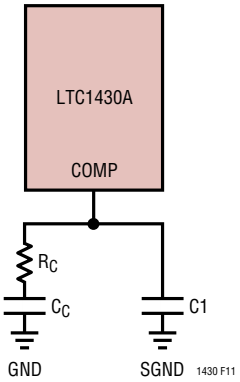


Figure 11. Compensation Pin Hook-Up

Soft Start and Current Limit

The 16-lead versions of the LTC1430A include a soft start circuit at the SS pin; this circuit is used both for initial start-up and during current limit operation. The soft start and current limit circuitry is disabled in the 8-lead version. SS requires an external capacitor to GND with the value determined by the required soft start time. An internal 12µA current source is included to charge the external capacitor. Soft start functions by clamping the maximum voltage that the COMP pin can swing to, thereby controlling the duty cycle (Figure 12). The LTC1430A will begin to operate at low duty cycle as the SS pin rises to about 2V below V_{CC}. As SS continues to rise, the duty cycle will increase until the error amplifier takes over and begins to regulate the output. When SS reaches 1V below V_{CC} the

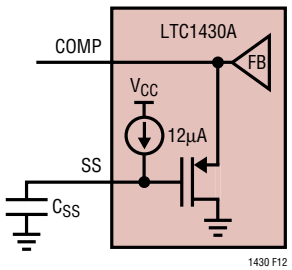


Figure 12. Soft Start Clamps COMP Pin

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LTC1430A will be in full operation. An internal switch shorts the SS pin to GND during shutdown.

The LTC1430A detects the output current by watching the voltage at I_{FB} while Q1 is ON. The I_{LIM} amplifier compares this voltage to the voltage at I_{MAX} (Figure 13). In the ON state, Q1 has a known resistance; by calculating backwards, the voltage generated at I_{FB} by the maximum output current in Q1 can be determined. As I_{FB} falls below I_{MAX}, I_{LIM} will begin to sink current from the soft start pin, causing the voltage at SS to fall. As SS falls, it will limit the output duty cycle, limiting the current at the output. Eventually the system will reach equilibrium, where the pull-up current at the SS pin matches the pull-down current in the I_{LIM} amplifier; the LTC1430A will stay in this state until the overcurrent condition disappears. At this time I_{FB} will rise, I_{LIM} will stop sinking current and the internal pull-up will recharge the soft start capacitor, restoring normal operation. Note that the I_{FB} pin requires an external 1k series resistor to prevent voltage transients at the drain of Q2 from damaging internal structures.

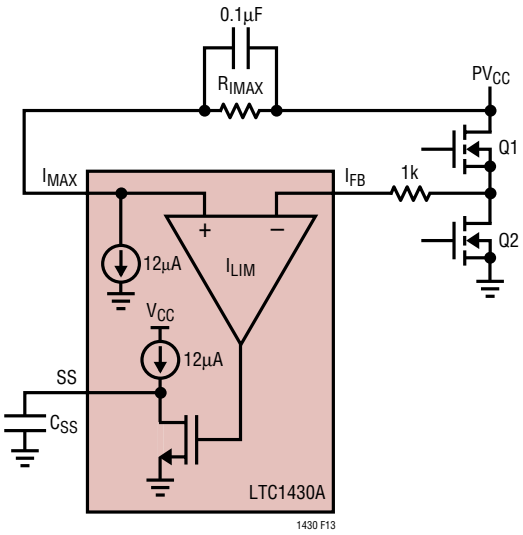


Figure 13. Current Limit Operation

The I_{LIM} amplifier pulls current out of SS in proportion to the difference between I_{FB} and I_{MAX}. Under mild overload conditions, the SS pin will fall gradually, creating a time delay before current limit takes effect. Very short, mild overloads may not trip the current limit circuit at all. Longer overload conditions will allow the SS pin to reach a steady level, and the output will remain at a reduced voltage until the overload is removed. Serious overloads will generate a larger overdrive at I_{LIM}, allowing it to pull SS down more quickly and preventing damage to the output components.

The I_{LIM} amplifier output is disabled when Q1 is OFF to prevent the low I_{FB} voltage in this condition from activating the current limit. It is re-enabled a fixed 170ns after Q1 turns on; this allows for the I_{FB} node to slew back high and the I_{LIM} amplifier to settle to the correct value. As the LTC1430A goes deeper into current limit, it will reach a point where the Q1 on-time needs to be cut to below 170ns to control the output current. This conflicts with the minimum settling time needed for proper operation of the I_{LIM} amplifier. At this point, a secondary current limit circuit begins to reduce the internal oscillator frequency, lengthening the off-time of Q1 while the on-time remains constant at 170ns. This further reduces the duty cycle, allowing the LTC1430A to maintain control over the output current.

Under extreme output overloads or short circuits, the I_{LIM} amplifier will pull the SS pin more than 2V below V_{CC} in a single switching cycle, cutting the duty cycle to zero. At this point all switching stops, the output current decays through Q2 and the LTC1430A runs a partial soft start cycle and restarts. If the short is still present the cycle will repeat. Peak currents can be quite high in this condition, but the average current is controlled and a properly designed circuit can withstand short circuits indefinitely with only moderate heat rise in the output FETs. In addition, the soft start cycle repeat frequency can drop into the low kHz range, causing vibrations in the inductor which provide an audible alarm that something is wrong.

Oscillator Frequency

The LTC1430A includes an onboard current controlled oscillator which will typically free-run at 200kHz. An internal 20µA current is summed with any current in or out of the FREQSET pin (Pin 11), setting the oscillator frequency to approximately 10kHz/µA. FREQSET is internally servoed to the LTC1430A reference voltage (1.265V). With FREQSET floating, the oscillator is biased from the

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internal 20μA source and runs at 200kHz. Connecting a 50k resistor from FREQSET to ground will sink an additional 25μA from FREQSET, causing the internal oscillator to run at approximately 450kHz. Sourcing an external 10μA current into FREQSET will cut the internal frequency to 100kHz. An internal clamp prevents the oscillator from running slower than about 50kHz. Tying FREQSET to V_{CC} will cause it to run at this minimum speed.

Shutdown

The LTC1430A includes a low power shutdown mode, controlled by the logic at the $\overline{SHDN}$ pin. A high at $\overline{SHDN}$ allows the part to operate normally. A low level at $\overline{SHDN}$ stops all internal switching, pulls COMP and SS to ground internally and turns Q1 and Q2 off. In shutdown, the LTC1430A itself will drop below 1μA quiescent current typically, although off-state leakage in the external MOSFETs may cause the total PV_{CC} current to be somewhat higher, especially at elevated temperatures. When $\overline{SHDN}$ rises again, the LTC1430A will rerun a soft start cycle and resume normal operation. Holding the LTC1430A in shutdown during PV_{CC} power up removes any PV_{CC1} sequencing constraints.

External Clock Synchronization

The LTC1430A $\overline{SHDN}$ pin can double as an external clock input for applications that require a synchronized clock or a faster switching speed. The $\overline{SHDN}$ pin terminates the internal sawtooth wave and resets the oscillator immediately when it goes low, but waits 50μs before shutting down the rest of the internal circuitry. A clock signal applied directly to the $\overline{SHDN}$ pin will force the LTC1430A internal oscillator to lock to its frequency as long as the external clock runs faster than the internal oscillator frequency. The LTC1430A can be synchronized to frequencies between 250kHz and 350kHz with no additional components.

The LTC1430A is synchronizable at frequencies from 200kHz to 500kHz. Frequencies above 300kHz can cause a decrease in the maximum obtainable duty cycle as rise/fall time and propagation delay take up a large fraction of the switch cycle. Circuits using these frequencies should be checked carefully in applications where operation near dropout is important—like 3.3V to 2.5V converters. Frequencies above 500kHz can cause erratic current limit operation and are not recommended.

LAYOUT CONSIDERATIONS

Grounding

Proper grounding is critical for the LTC1430A to obtain specified output regulation. Extremely high peak currents (as high as several amps) can flow between the bypass capacitors and the PV_{CC1}, PV_{CC2} and PGND pins. These currents can generate significant voltage differences between two points that are nominally both "ground." As a general rule, GND and PGND should be totally separated on the layout, and should be brought together at only one point, right at the LTC1430A GND and PGND pins. This helps minimize internal ground disturbances in the LTC1430A by keeping PGND and GND at the same potential, while preventing excessive current flow from disrupting the operation of the circuits connected to GND. The PGND node should be as compact and low impedance as possible, with the negative terminals of the input and output capacitors, the source of Q2, the LTC1430A PGND node, the output return and the input supply return all clustered at one point. Figure 14 is a modified schematic showing the common connections in a proper layout. Note that at 10A current levels or above, current density in the PC board itself can become a concern; traces carrying high currents should be as wide as possible.

Output Voltage Sensing

The 16-lead versions of the LTC1430A provide three pins for sensing the output voltage: $SENSE^+$, $SENSE^-$ and FB. $SENSE^+$ and $SENSE^-$ connect to an internal resistor divider which is connected to FB. To set the output of the LTC1430A to 3.3V, connect $SENSE^+$ to the output as near to the load as practical and connect $SENSE^-$ to the common GND/PGND point. Note that $SENSE^-$ is not a true differential input sense input; it is just the bottom of the internal divider string. Connecting $SENSE^-$ to the ground near the load will not improve load regulation. For any other output voltage, the $SENSE^+$ and $SENSE^-$ pins should

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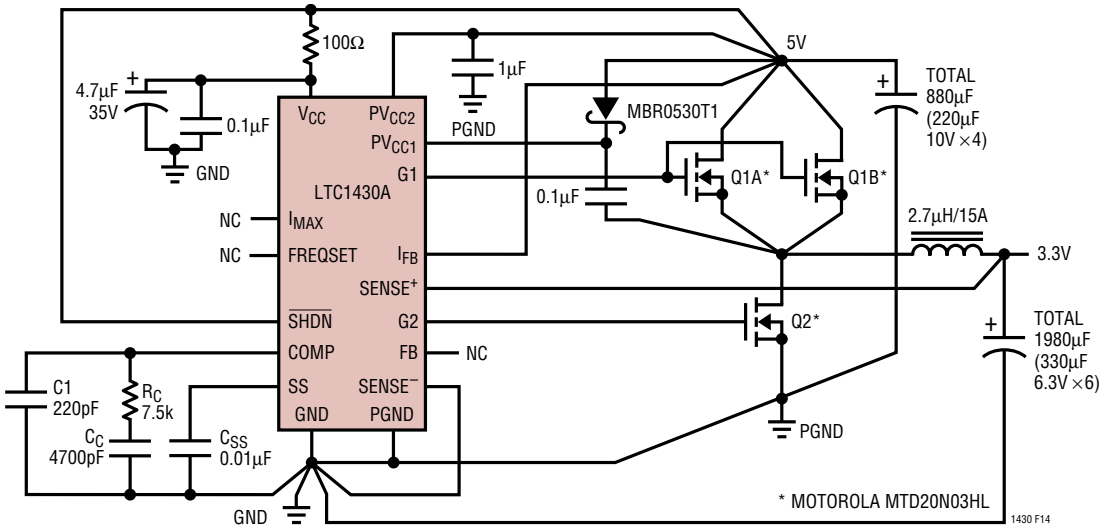


Figure 14. Typical Schematic Showing Layout Considerations

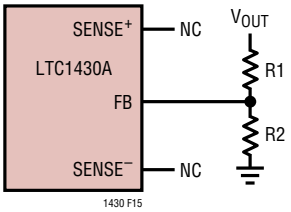


Figure 15. Using External Resistors to Set Output Voltages

be floated and an external resistor string should be connected to FB (Figure 15). As before, connect the top resistor (R1) to the output as close to the load as practical and connect the bottom resistor (R2) to the common GND/PGND point. In both cases, connecting the top of the resistor divider (either SENSE$^+$ or R1) close to the load can significantly improve load regulation by compensating for any drops in PC traces or hookup wires between the LTC1430A and the load.

Power Component Hook-Up/Heat Sinking

As current levels rise much above 1A, the power components supporting the LTC1430A start to become physically large (relative to the LTC1430A, at least) and can require special mounting considerations. Input and output capacitors need to carry high peak currents and must have low ESR; this mandates that the leads be clipped as short as possible and PC traces be kept wide and short. The power inductor will generally be the most massive single component on the board; it can require a mechanical hold-down in addition to the solder on its leads, especially if it is a surface mount type.

The power MOSFETs used require some care to ensure proper operation and reliability. Depending on the current levels and required efficiency, the MOSFETs chosen may be as large as TO-220s or as small as SO-8s. High efficiency circuits may be able to avoid heat sinking the power devices, especially with TO-220 type MOSFETs. As an example, a 90% efficient converter working at a steady 3.3V/10A output will dissipate only (33W/90%)10% = 3.7W. The power MOSFETs generally account for the majority of the power lost in the converter; even assuming that they consume 100% of the power used by the converter, that's only 3.7W spread over two or three devices. A typical SO-8 MOSFET with a R_{ON} suitable to provide 90% efficiency in this design can commonly dissipate 2W when soldered to an appropriately sized piece of copper trace on a PC board. Slightly less efficient or higher output current designs can often get by with standing a TO-220 MOSFET straight up in an area with some airflow; such an arrangement can dissipate as much as 3W without a heat sink. Designs which must work in high ambient temperatures or which will be routinely overloaded will generally fare best with a heat sink.

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Figure 17 is a synchronous buck regulator designed to provide a low voltage, very high current output from a 5V or lower input voltage. The circuit uses two 8-pin LTC1430ACS8s, operated 180° out of phase from each other. Each half of the circuit is good for 15A of output current, giving 30A total. The LT®1006 amplifier forces the two half circuits to share the load current equally. This scheme trades a small amount of additional control circuit complexity for radical reductions in the volume (hence cost) of the capacitors and inductors required. Advantages of this approach include very low input and output ripple voltages, higher ripple frequency and extremely fast transient response.

By incorporating two regulators phased opposite one another, both the input ripple currents and the output ripple currents tend to cancel. This permits running much higher ripple currents in the output inductors than would be tolerable with a single channel. The overall output ripple current in a two phase design is approximately 1/2 of a single channel's ripple current, allowing the inductor value of each channel to be 1/2 that of what a single channel system would require for equal output ripple. Since energy storage varies as the square of inductor current, and directly as the inductance, each inductor stores only 1/8th the energy of a single inductor design. Since there are two inductors, total energy storage, and therefore inductor volume, is 1/4th that of a single phase system.

A similar analysis can be done for the input capacitor requirements. In fact, a two-phase regulator will actually require less input capacitance than a single channel design at 1/2 the load current. Figure 16 shows how the ripple currents tend to cancel one another.

Another significant advantage of the two-phase topology is radically improved transient response. During a load transient, each of the two channels runs to maximum (or minimum) duty cycle. The two ripple current terms now end up reinforcing one another rather than canceling. The result is a very high di/dt, hence, very fast transient recoveries. Once steady state conditions return, the ripple currents begin to cancel again, providing very low output ripple voltage.

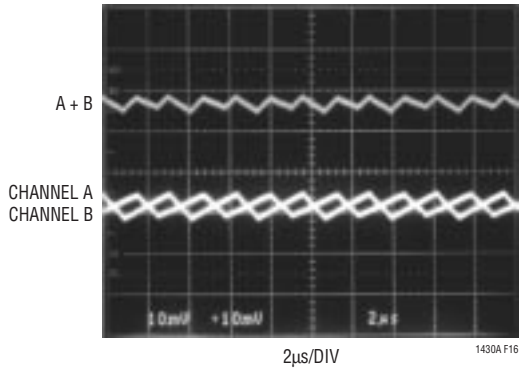


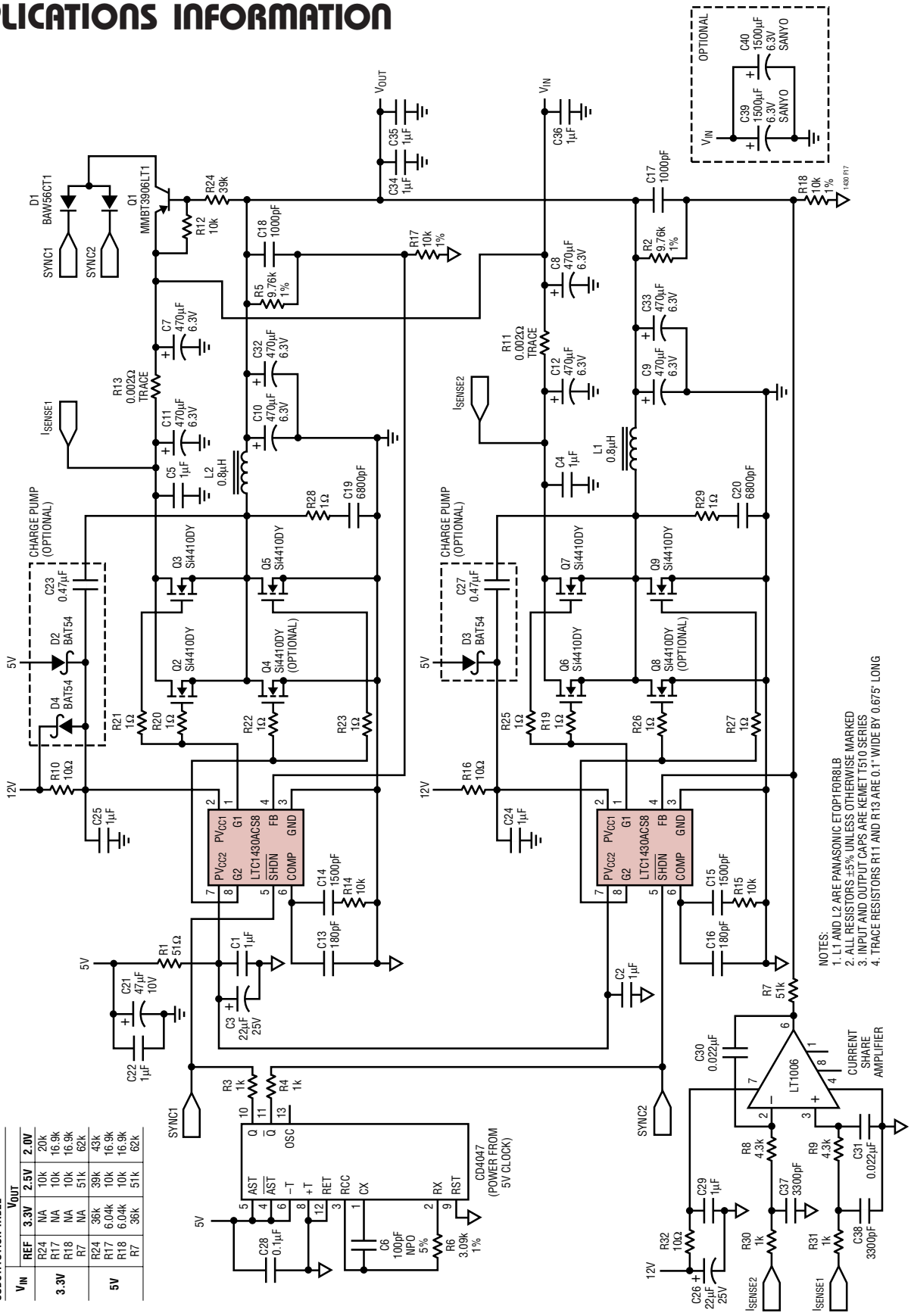
Figure 16. Output Inductor Currents 5A/DIV, 30A Out

The clocking of the two channels is accomplished by the CD4047, a low cost, CMOS mulitvibrator with a built-in divide-by-two flip flop. The CD4047 oscillator is set to run at 600kHz and the Q and $\overline{Q}$ outputs drive the LTC1430A shutdown pins. Since the sync signals are derived from the clock's divide-by-two outputs, they are inherently 180° out of phase and at the desired 300kHz clock frequency. Q1, D1 and the two resistors connected to Q1's base are used to disable the synchronization at turn-on to prevent start-up problems. As long as the input-output differential voltage is large enough to turn on Q1, the sync circuit is disabled and both LTC1430As will free run at 200kHz. Once the output rises above ≈1.5V, the regulators are allowed to lock to the clock.

One challenge with a voltage mode two-phase design is current sharing. Unlike current mode control which offers inherent current sharing, voltage mode control virtually assures that one channel will try to hog a large percentage of the load current. The circuit gets around this problem with a current share amplifier. The LT1006 op amp compares the voltage across both sense resistors and adds or subtracts a small current into the lower LTC1430A's feedback divider, forcing it to match the upper LTC1430A's current. The two PCB trace resistors are intentionally chosen to have a very low value to minimize power losses. The LT1006 features 80µV typical V_{OS}, ensuring reasonably accurate current sharing.

There are three problems associated with this current sharing approach that must be dealt with. The first is that

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NOTES:
1. L1 AND L2 ARE PANASONIC ETQP1F0R8LB
2. ALL RESISTORS ±5% UNLESS OTHERWISE MARKED
3. INPUT AND OUTPUT CAPS ARE KEMET T510 SERIES
4. TRACE RESISTORS R11 AND R13 ARE 0.1" WIDE BY 0.675" LONG

Figure 17. Low Voltage 30A Power Supply

SUBSTITUTION TABLE

V_{IN}	REF	V_{OUT} 3.3V	2.5V	2.0V
3.3V	R24	NA	10k	20k
	R17	NA	10k	16.9k
	R18	NA	10k	16.9k
	R7	NA	51k	62k
5V	R24	36k	39k	43k
	R17	6.04k	10k	16.9k
	R18	6.04k	10k	16.9k
	R7	36k	51k	62k

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the sense resistors should be well matched. This is accomplished by using trace resistors that are laid out symmetrically. Since they are formed of the same material and processed identically, they will inherently match very well. Note that the absolute value of these resistors is not important; only the match between them is of concern.

The second issue is related to the reference point for the two sense voltages. In order to avoid the need to use a true differential amplifier to measure input current, the circuit is configured such that the input side of these resistors must be at the exact same potential. If the layout is not configured this way, the current sharing accuracy will prove disappointing. With only 0.2Ω sense resistors, a seemingly small error will produce a rather large current mismatch between channels.

The last issue is related to having a very noisy sense voltage. The current waveshape at the input to a buck regulator is trapezoidal. Therefore, the sense amplifier must integrate the two current measurements in order that the average input currents be compared. The two-stage RC filter on the sense amplifier provides an adequately clean signal for the share circuit to operate correctly. High speed is not required in the current sense loop. In balanced operation any offsets in the slave regulator are dialed out by the sense amplifier. If a sudden load change should occur, both regulators will respond immediately and in the right direction. If there are any gain differences in the two loops there will need to be a small correction in the current share error voltage. This can occur over a relatively long time period with no adverse effects. As such, the share amplifier's bandwidth is on the order of a few hundred Hz, ensuring good noise immunity.

Figure 18 demonstrates the high efficiency achieved with this two-phase converter. An efficiency > 90% is realized from a few amperes up to 30A. In theory and in practice, this multiphase approach can be extended to even higher current and output power levels. Consult Linear Technology for further details.

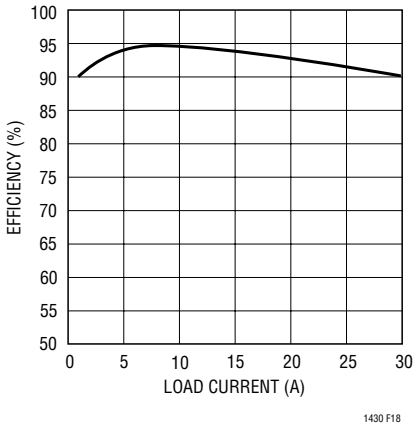
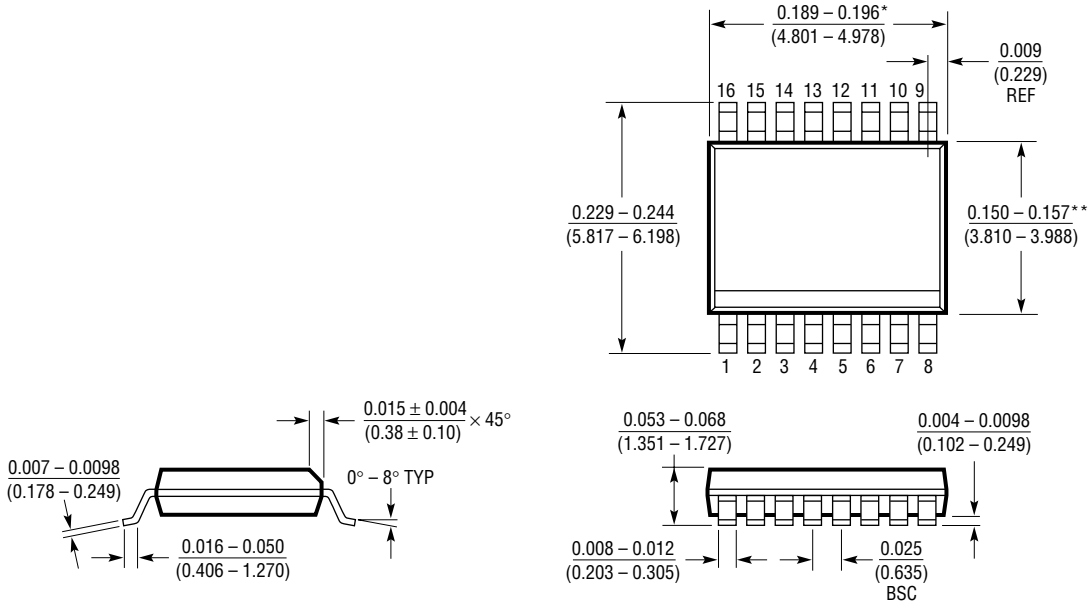


Figure 18. Low Voltage 30A Power Supply Efficiency

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

GN Package
16-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)



* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

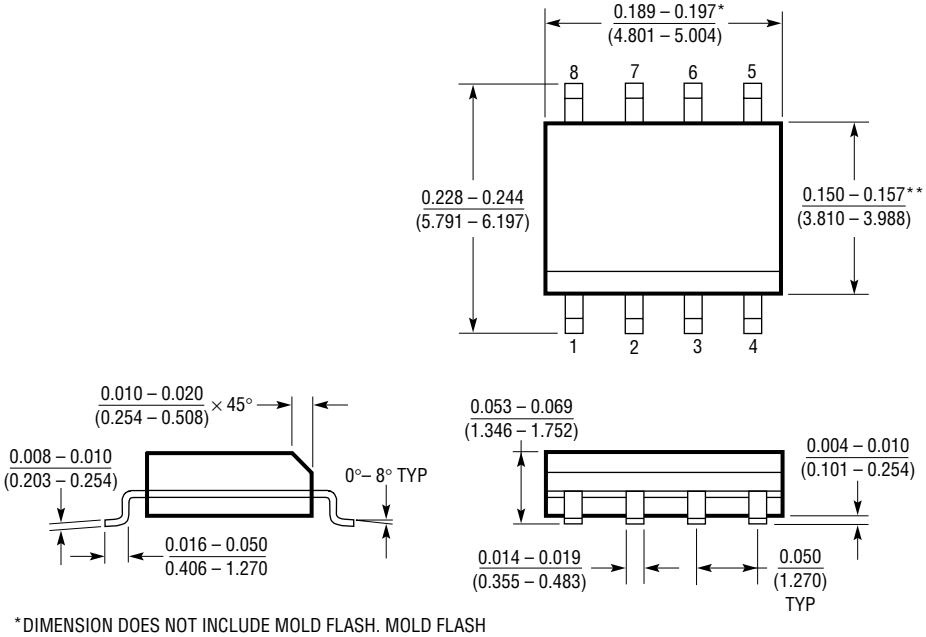
** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 0398

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

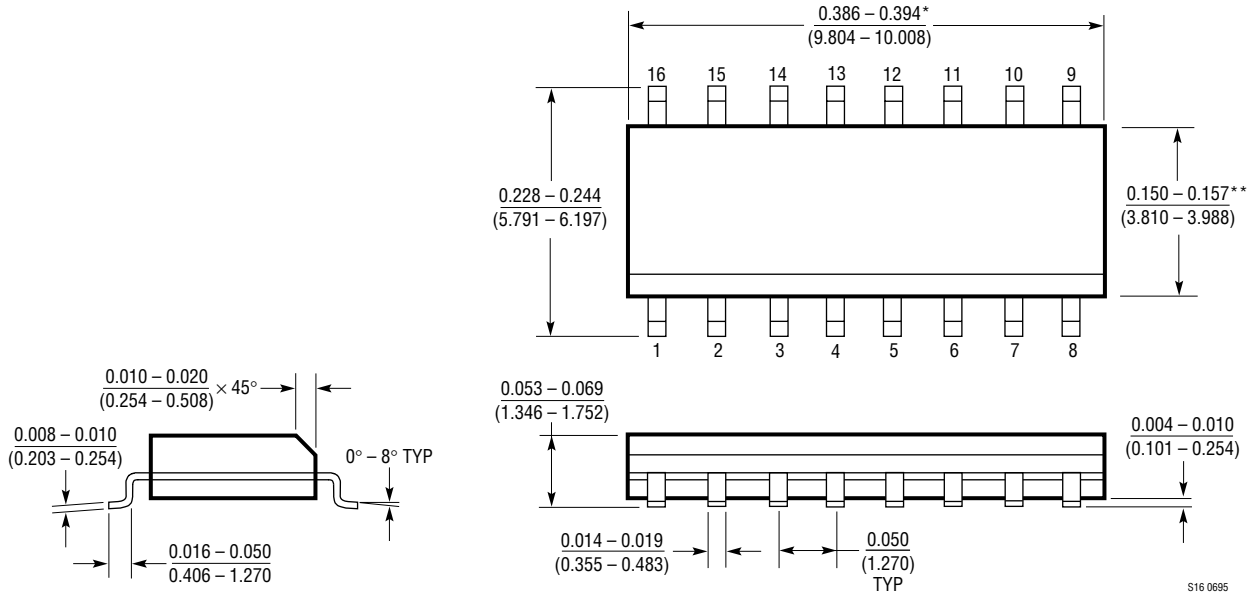
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

SO8 0996

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S Package
16-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



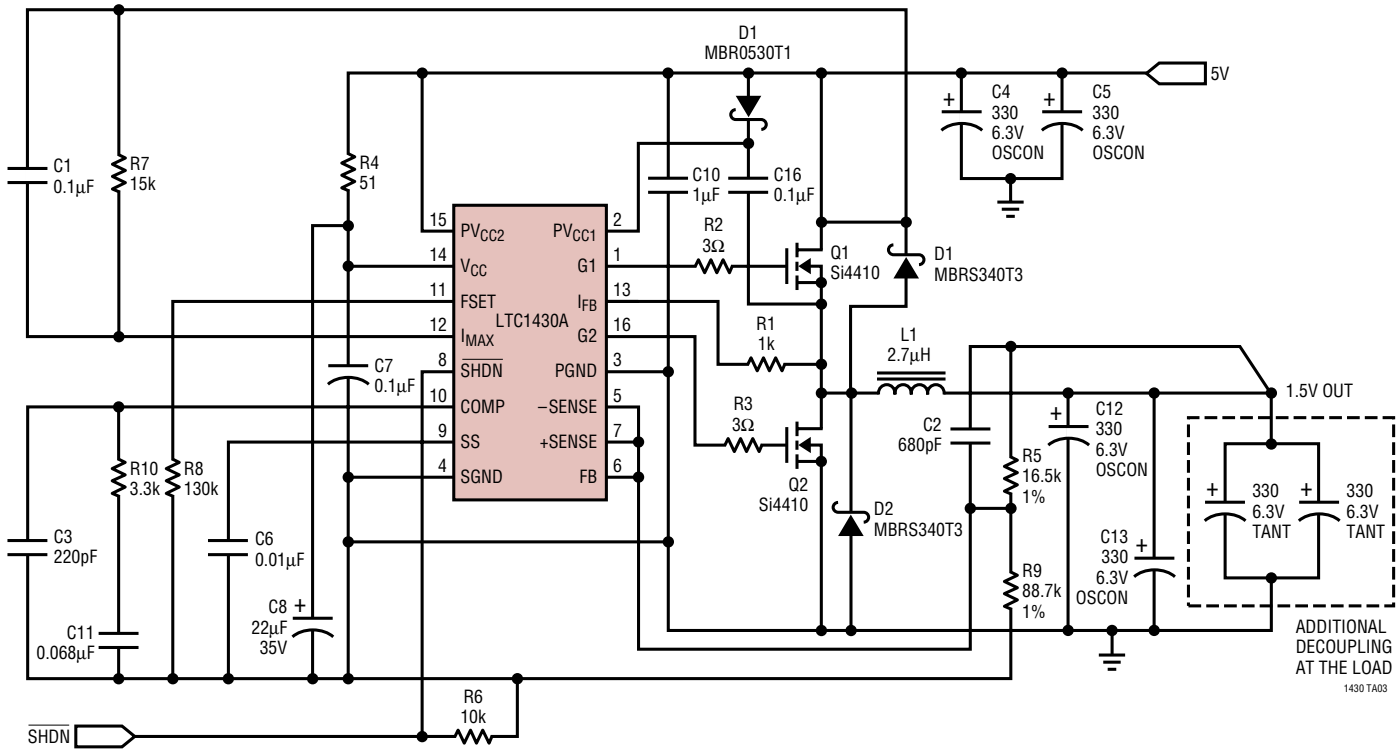
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

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TYPICAL APPLICATION

GTL Terminator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1142	Current Mode Dual Step-Down Switching Regulator Controller	Dual Version of LTC1148
LTC1148	Current Mode Step-Down Switching Regulator Controller	Synchronous, $V_{IN} \leq 20V$
LTC1149	Current Mode Step-Down Switching Regulator Controller	Synchronous, $V_{IN} \leq 48V$, For Standard Threshold FETs
LTC1159	Current Mode Step-Down Switching Regulator Controller	Synchronous, $V_{IN} \leq 40V$, For Logic Threshold FETs
LTC1266	Current Mode Step-Up/Down Switching Regulator Controller	Synchronous N- or P-Channel FETs, Comparator/ Low-Battery Detector
LTC1267	Current Mode Dual Step-Down Switching Regulator Controller	Dual Version of LTC1159
LTC1649	3.3V Input Synchronous Switching Regulator Controller	3.3V Input

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