14-Bit, 65Msps Low Noise ADC

FEATURES

- **Sample Rate: 65Msps**
- **76.5dB SNR and 90dB SFDR (3.2V Range)**
- **72.8dB SNR and 90dB SFDR (2V Range)**
- No Missing Codes
- Single 5V Supply
- Power Dissipation: 1.275W
- Selectable Input Ranges: ±1V or ±1.6V
- 240MHz Full Power Bandwidth S/H
- Pin Compatible Family
  25Msps: LTC1746 (14-Bit), LTC1745 (12-Bit)
  50Msps: LTC1744 (14-Bit), LTC1743 (12-Bit)
  65Msps: LTC1742 (14-Bit), LTC1741 (12-Bit)
  80Msps: LTC1748 (14-Bit), LTC1747 (12-Bit)
- 48-Pin TSSOP Package

APPLICATIONS

- Telecommunications
- Receivers
- Cellular Base Stations
- Spectrum Analysis
- Imaging Systems

LT, LTC and LT are registered trademarks of Linear Technology Corporation.

DESCRIPTION

The LTC®1742 is an 65Msps, sampling 14-bit A/D converter designed for digitizing high frequency, wide dynamic range signals. Pin selectable input ranges of ±1V and ±1.6V along with a resistor programmable mode allow the LTC1742's input range to be optimized for a wide variety of applications.

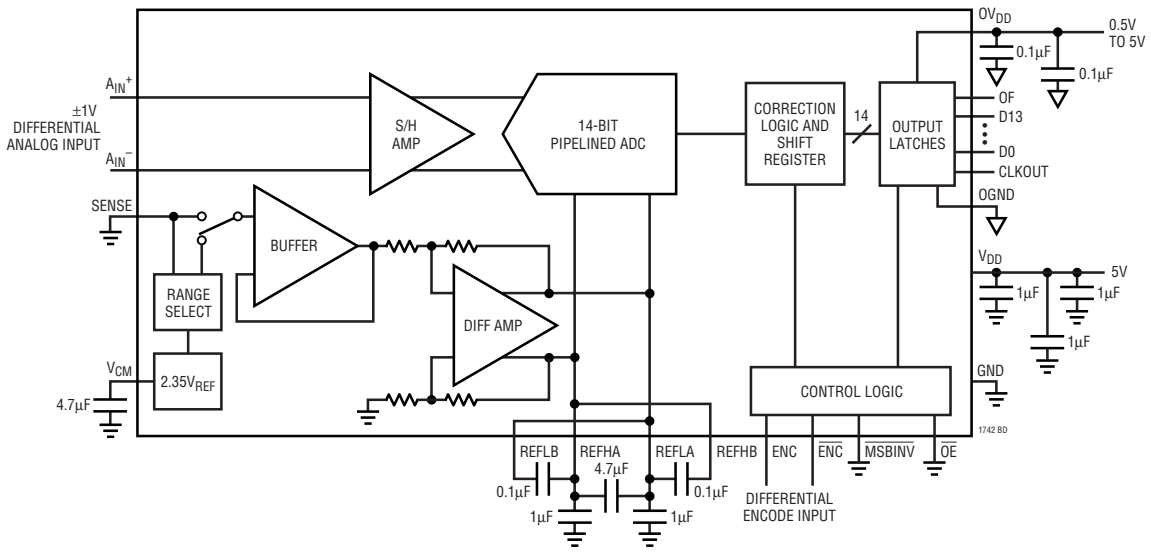
The LTC1742 is perfect for demanding communications applications with AC performance that includes 76.5dB SNR and 90dB spurious free dynamic range. Ultralow jitter of 0.15ps$_{RMS}$ allows undersampling of IF frequencies with excellent noise performance. DC specs include ±3LSB INL and ±1LSB DNL.

The digital interface is compatible with 5V, 3V, 2V and LVDS logic levels. The $\overline{ENC}$ and ENC inputs may be driven differentially from PECL, GTL and other low swing logic families or from single-ended TTL or CMOS. The low noise, high gain $\overline{ENC}$ and ENC inputs may also be driven by a sinusoidal signal without degrading performance. A separate output power supply can be operated from 0.5V to 5V, making it easy to connect directly to low voltage DSPs or FIFOs.

The TSSOP package with a flow-through pinout simplifies the board layout.

BLOCK DIAGRAM

65Msps, 14-Bit ADC with a 2V Differential Input Range

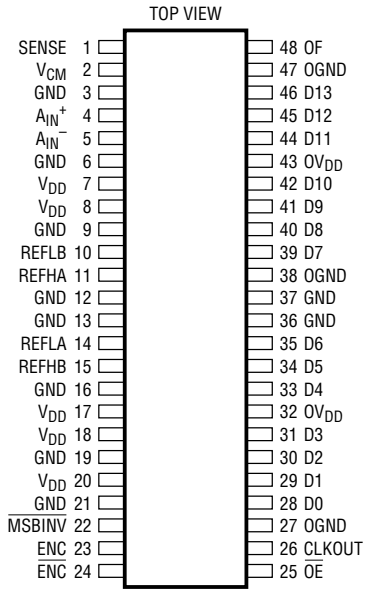


ABSOLUTE MAXIMUM RATINGS

OV_{DD} = V_{DD} (Notes 1, 2)

Supply Voltage (V_{DD}) 5.5V
Analog Input Voltage (Note 3) .... –0.3V to (V_{DD} + 0.3V)
Digital Input Voltage (Except $\overline{OE}$)
(Note 3) ..... –0.3V to (V_{DD} + 0.3V)
$\overline{OE}$ Input Voltage (Note 4) ..... –0.3V to (OV_{DD} + 0.3V)
Digital Output Voltage ..... –0.3V to (V_{DD} + 0.3V)
OGND Voltage ..... –0.3V to 1V
Power Dissipation 2000mW
Operating Temperature Range
LTC1742C ..... 0°C to 70°C
LTC1742I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



FW PACKAGE
48-LEAD PLASTIC TSSOP

T_{JMAX} = 150°C, θ_{JA} = 35°C/W

ORDER PART NUMBER
LTC1742CFW
LTC1742IFW

Consult LTC Marketing for parts specified with wider operating temperature ranges.

CONVERTER CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	14			Bits
Integral Linearity Error	(Note 6)		–3	±0.75	3	LSB
Differential Linearity Error		●	–1	±0.5	1	LSB
Offset Error	(Note 7)		–35	±5	35	mV
Gain Error	External Reference (SENSE = 1.6V)		–3.5	±1	3.5	%FS
Full-Scale Drift	Internal Reference			±40		ppm/°C
Full-Scale Drift	External Reference (SENSE = 1.6V)			±20		ppm/°C
Offset Drift	Internal Reference			±20		µV/°C
Input Referred Noise (Transition Noise)	SENSE = 1.6V			0.82		LSB_{RMS}

ANALOG INPUT

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 8)	4.75V ≤ V_{DD} ≤ 5.25V	●		±1 to ±1.6		V
I_{IN}	Analog Input Leakage Current	0 < A_{IN}^+, A_{IN}^- < V_{DD}	●	–1		1	µA
C_{IN}	Analog Input Capacitance	Sample Mode ENC < $\overline{ENC}$ Hold Mode ENC > $\overline{ENC}$			8 4		pF pF
t_{ACQ}	Sample-and-Hold Acquisition Time		●		5	7.3	ns
t_{AP}	Sample-and-Hold Acquisition Delay Time				0		ns
t_{JITTER}	Sample-and-Hold Acquisition Delay Time Jitter				0.15		ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio	1.5V < (A_{IN}^- = A_{IN}^+) < 3V			80		dB

DYNAMIC ACCURACY $T_A = 25°C$. $A_{IN} = -1dBFS$. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SNR	Signal-to-Noise Ratio	5MHz Input Signal (2V Range) 5MHz Input Signal (3.2V Range)	 75	72.8 76.5		dB dB
		30MHz Input Signal (2V Range) 30MHz Input Signal (3.2V Range)	 74	72.5 76.5		dB dB
		70MHz Input Signal (2V Range) 70MHz Input Signal (3.2V Range)		72.2 75.8		dB dB
SFDR	Spurious Free Dynamic Range	5MHz Input Signal (2V Range)		90		dB
		5MHz Input Signal (3.2V Range) (2nd and 3rd)		90		dB
		5MHz Input Signal (3.2V Range) (Other)		95		dB
		30MHz Input Signal (2V Range)		90		dB
		30MHz Input Signal (3.2V Range) (2nd and 3rd)	80	88		dB
		30MHz Input Signal (3.2V Range) (Other)	85	95		dB
		70MHz Input Signal (2V Range)		83		dB
		70MHz Input Signal (3.2V Range) (2nd and 3rd)		75		dB
		70MHz Input Signal (3.2V Range) (Other)		95		dB
S/(N + D)	Signal-to-(Noise + Distortion) Ratio	5MHz Input Signal (2V Range) 5MHz Input Signal (3.2V Range)	 74.5	72.6 76.2		dB dB
		30MHz Input Signal (2V Range) 30MHz Input Signal (3.2V Range)		72.3 76.0		dB dB
		70MHz Input Signal (2V Range) 70MHz Input Signal (3.2V Range)		71 71		dB dB
THD	Total Harmonic Distortion	5MHz Input Signal, First 5 Harmonics (2V Range) 5MHz Input Signal, First 5 Harmonics (3.2V Range)		–90 –90		dB dB
		30MHz Input Signal, First 5 Harmonics (2V Range) 30MHz Input Signal, First 5 Harmonics (3.2V Range)		–90 –85		dB dB
		70MHz Input Signal, First 5 Harmonics (2V Range) 70MHz Input Signal, First 5 Harmonics (3.2V Range)		–78 –74		dB dB
IMD	Intermodulation Distortion	f_{IN1} = 2.52MHz, f_{IN2} = 5.2MHz (2V Range) f_{IN1} = 2.52MHz, f_{IN2} = 5.2MHz (3.2V Range)		97 93		dBc dBc
	Sample-and-Hold Bandwidth	R_{SOURCE} = 50Ω		240		MHz

INTERNAL REFERENCE CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CM} Output Voltage	I_{OUT} = 0	2.30	2.35	2.40	V
V_{CM} Output Tempco	I_{OUT} = 0		±30		ppm/°C
V_{CM} Line Regulation	4.75V ≤ V_{DD} ≤ 5.25V		3		mV/V
V_{CM} Output Resistance	1mA ≤ $\lvert I_{OUT} \rvert$ ≤ 1mA		4		Ω

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V, $\overline{MSBINV}$ and $\overline{OE}$		●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V, $\overline{MSBINV}$ and $\overline{OE}$		●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}		●			±10	µA
C_{IN}	Digital Input Capacitance	$\overline{MSBINV}$ and $\overline{OE}$ Only				1.5		pF
V_{OH}	High Level Output Voltage	OV_{DD} = 4.75V	I_O = –10µA			4.74		V
			I_O = –200µA	●	4	4.74		V
V_{OL}	Low Level Output Voltage	OV_{DD} = 4.75V	I_O = 160µA			0.05		V
			I_O = 1.6mA	●		0.1	0.4	V
I_{OZ}	Hi-Z Output Leakage D13 to D0	V_{OUT} = 0V to V_{DD}, $\overline{OE}$ = High		●			±10	µA
C_{OZ}	Hi-Z Output Capacitance D13 to D0	$\overline{OE}$ = High (Note 8)		●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V				–50		mA
I_{SINK}	Output Sink Current	V_{OUT} = 5V				50		mA

POWER REQUIREMENTS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage			4.75		5.25	V
I_{DD}	Positive Supply Current		●		255	275	mA
P_{DIS}	Power Dissipation		●		1.275	1.375	W
OV_{DD}	Digital Output Supply Voltage			0.5		V_{DD}	V

TIMING CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_0	ENC Period	(Note 9)	●	15.3		2000	ns
t_1	ENC High	(Note 8)	●	7.3		1000	ns
t_2	ENC Low	(Note 8)	●	7.3		1000	ns
t_3	Aperture Delay	(Note 8)			0		ns
t_4	ENC to CLKOUT Falling	C_L = 10pF (Note 8)	●	1	2.4	4	ns
t_5	ENC to CLKOUT Rising	C_L = 10pF (Note 8)			$t_1 + t_4$		ns
	For 65Msps 50% Duty Cycle	C_L = 10pF (Note 8)	●	8.7	10.1	11.7	ns
t_6	ENC to DATA Delay	C_L = 10pF (Note 8)	●	2	4.9	7.2	ns
t_7	ENC to DATA Delay (Hold Time)	(Note 8)	●	1.4	3.4	4.7	ns
t_8	ENC to DATA Delay (Setup Time)	C_L = 10pF (Note 8)			$t_0 – t_6$		ns
	For 65Msps 50% Duty Cycle	C_L = 10pF (Note 8)	●	8.2	10.5	13.4	ns
t_9	CLKOUT to DATA Delay (Hold Time), 65Msps 50% Duty Cycle	(Note 8)	●	7			ns
t_{10}	CLKOUT to DATA Delay (Setup Time), 65Msps 50% Duty Cycle	C_L = 10pF (Note 8)	●	3			ns
t_{11}	DATA Access Time After $\overline{OE}$	C_L = 10pF (Note 8)			10	25	ns
t_{12}	BUS Relinquish	(Note 8)			10	25	ns
	Data Latency				5		cycles

ELECTRICAL CHARACTERISTICS

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with GND (unless otherwise noted).

Note 3: When these pin voltages are taken below GND or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above V_{DD} without latchup.

Note 4: When this pin voltage is taken below GND or above OV_{DD}, it will be clamped by internal diodes. This product can handle input currents of >100mA below GND or above OV_{DD} without latchup.

Note 5: V_{DD} = 5V, f_{SAMPLE} = 65MHz, differential ENC/$\overline{ENC}$ = $2V_{P-P}$ 65MHz sine wave, input range = ±1.6V differential, unless otherwise specified.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

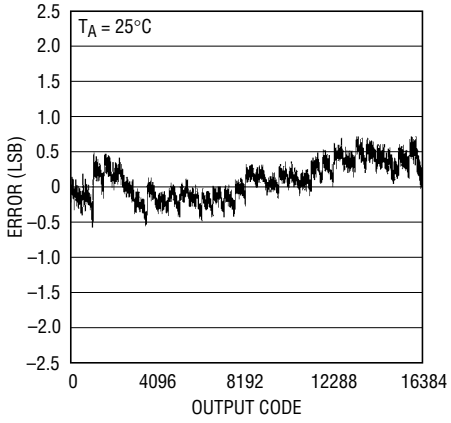
Note 7: Bipolar offset is the offset voltage measured from –0.5 LSB when the output code flickers between 00 0000 0000 0000 and 11 1111 1111 1111.

Note 8: Guaranteed by design, not subject to test.

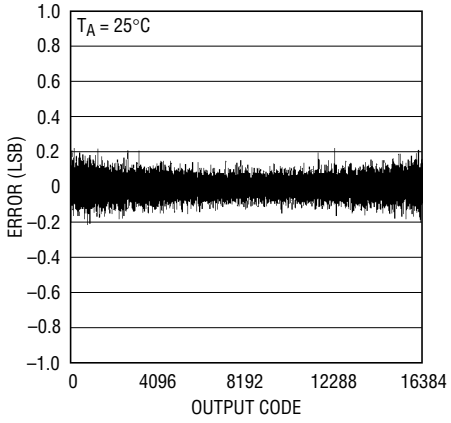
Note 9: Recommended operating conditions.

TYPICAL PERFORMANCE CHARACTERISTICS

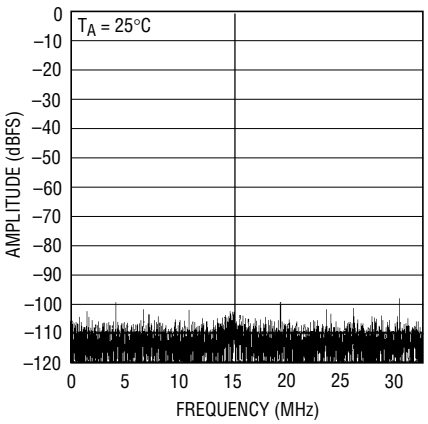
INL, 3.2V Range



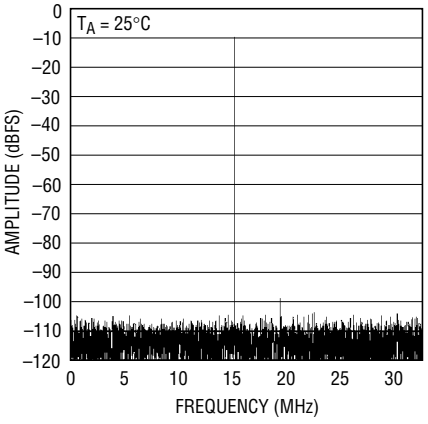
DNL, 3.2V Range



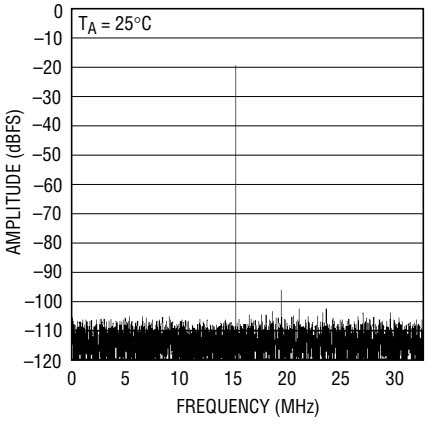
8192 Point FFT, Input Frequency = 15MHz, –1dB, 3.2V Range



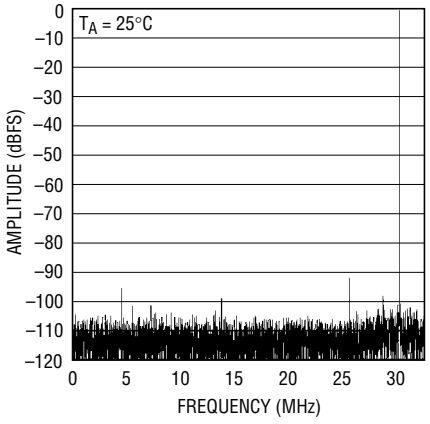
8192 Point FFT, Input Frequency = 15MHz, –10dB, 3.2V Range



8192 Point FFT, Input Frequency = 15MHz, –20dB, 3.2V Range

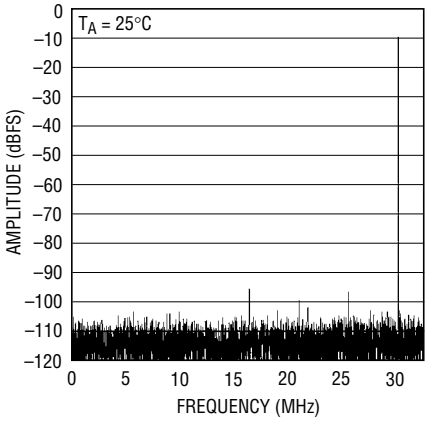


8192 Point FFT, Input Frequency = 30MHz, –1dB, 3.2V Range



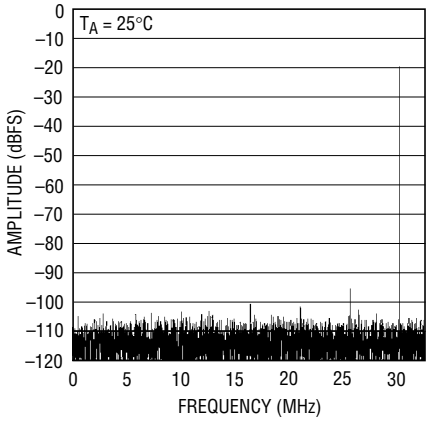
TYPICAL PERFORMANCE CHARACTERISTICS

8192 Point FFT, Input Frequency = 30MHz, –10dB, 3.2V Range



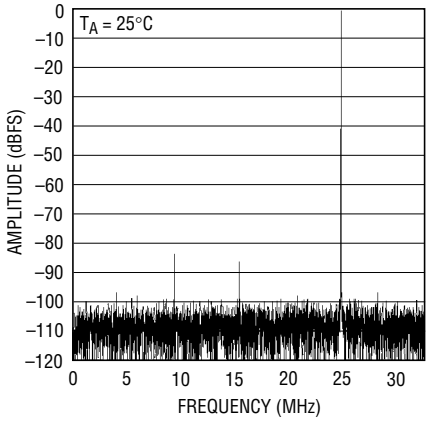
1742 G07

8192 Point FFT, Input Frequency = 30MHz, –20dB, 3.2V Range



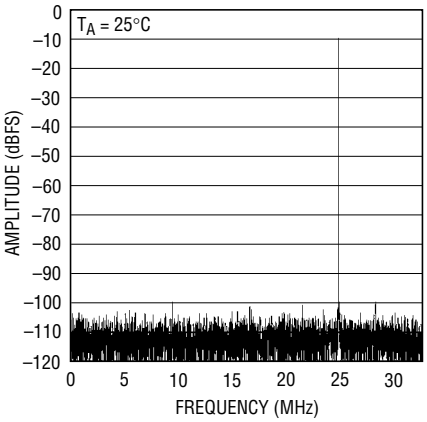
1742 G08

8192 Point FFT, Input Frequency = 40MHz, –1dB, 3.2V Range



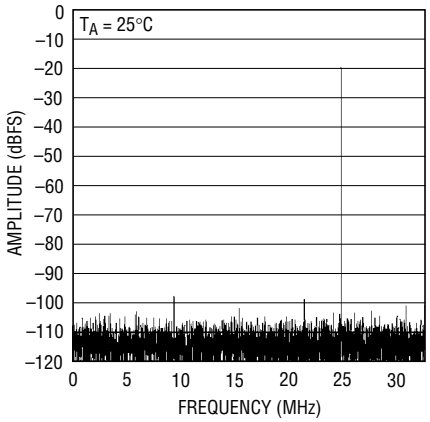
1742 G09

8192 Point FFT, Input Frequency = 40MHz, –10dB, 3.2V Range



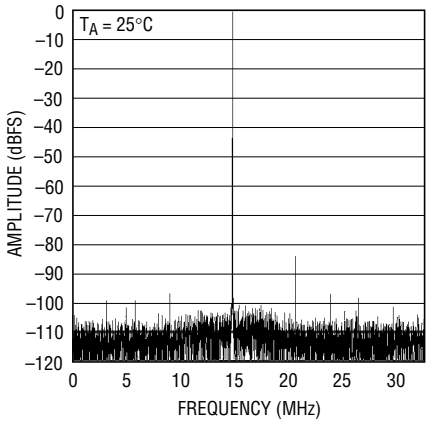
1742 G10

8192 Point FFT, Input Frequency = 40MHz, –20dB, 3.2V Range



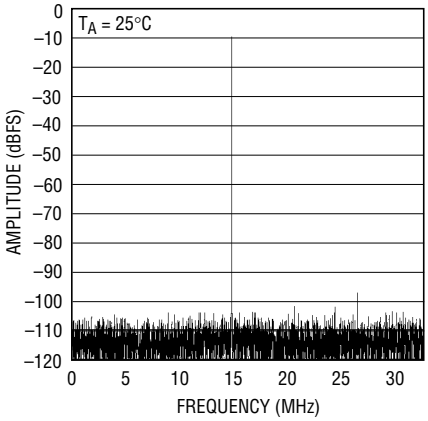
1742 G11

8192 Point FFT, Input Frequency = 50MHz, –1dB, 3.2V Range



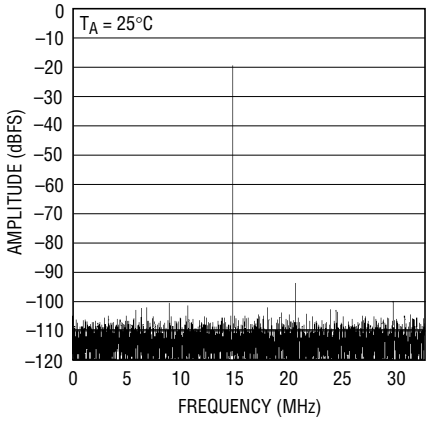
1742 G12

8192 Point FFT, Input Frequency = 50MHz, –10dB, 3.2V Range



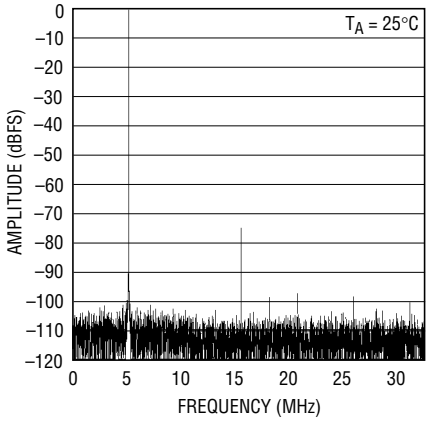
1742 G13

8192 Point FFT, Input Frequency = 50MHz, –20dB, 3.2V Range



1742 G14

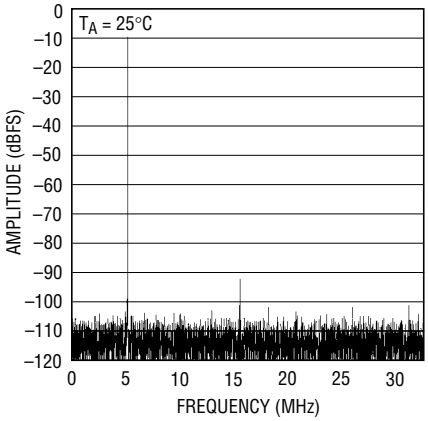
8192 Point FFT, Input Frequency = 70MHz, –1dB, 3.2V Range



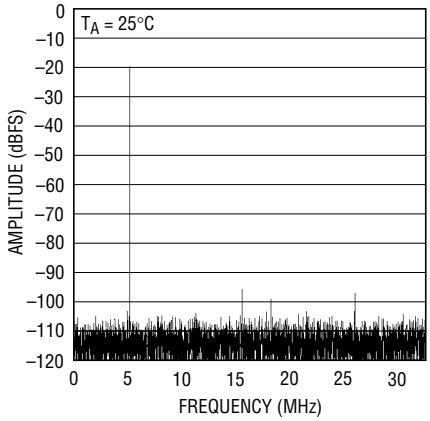
1742 G15

TYPICAL PERFORMANCE CHARACTERISTICS

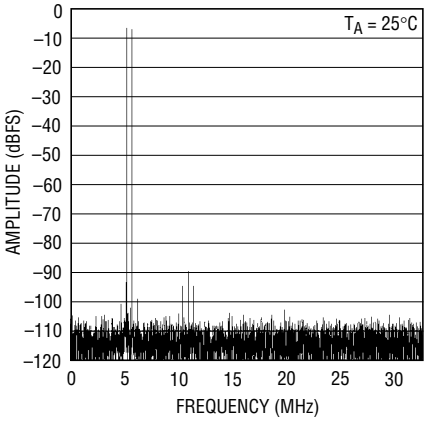
8192 Point FFT, Input Frequency = 70MHz, –10dB, 3.2V Range



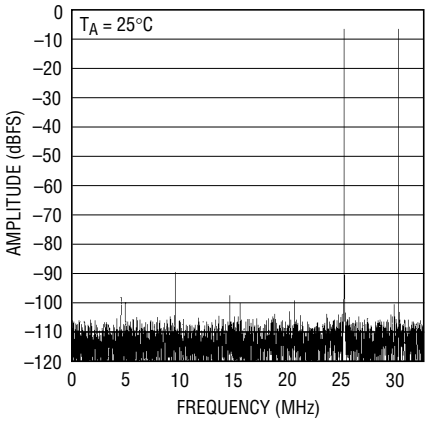
8192 Point FFT, Input Frequency = 70MHz, –20dB, 3.2V Range



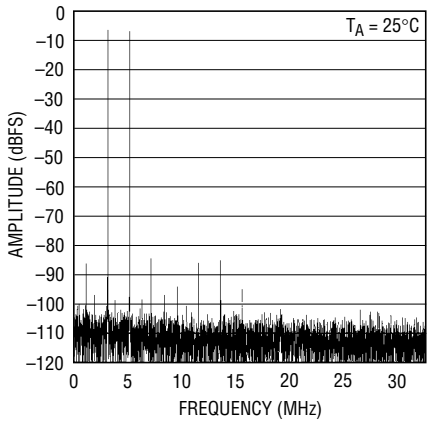
8192 Point 2-Tone FFT, Input Frequency = 5MHz and 7MHz, –7dB, 3.2V Range



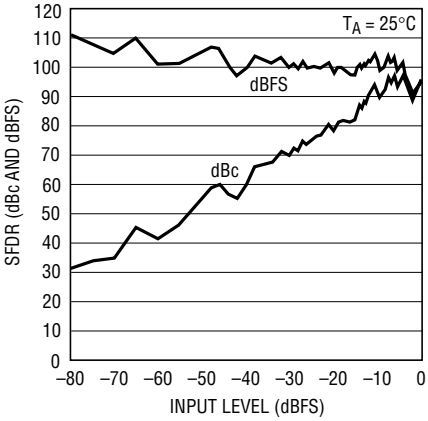
8192 Point 2-Tone FFT, Input Frequency = 25MHz and 30MHz, –7dB, 3.2V Range



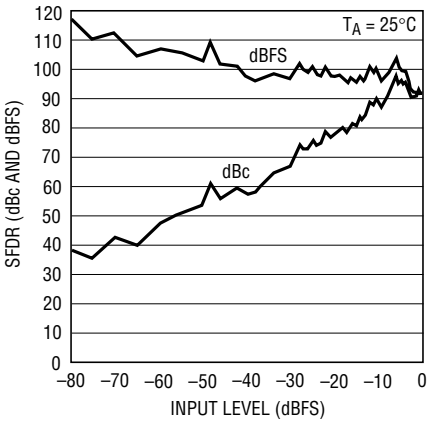
8192 Point 2-Tone FFT, Input Frequency = 68MHz and 70MHz, –7dB, 3.2V Range



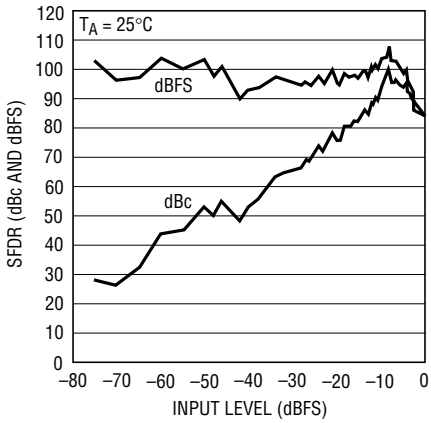
SFDR vs 15MHz Input Level



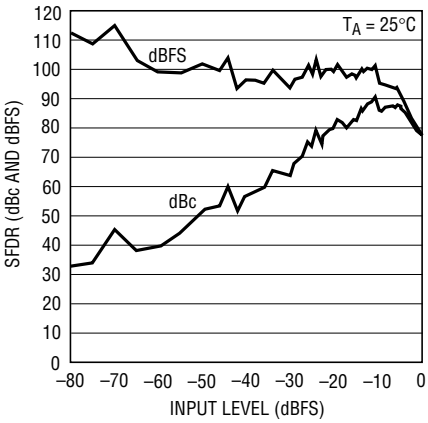
SFDR vs 30MHz Input Level



SFDR vs 50MHz Input Level

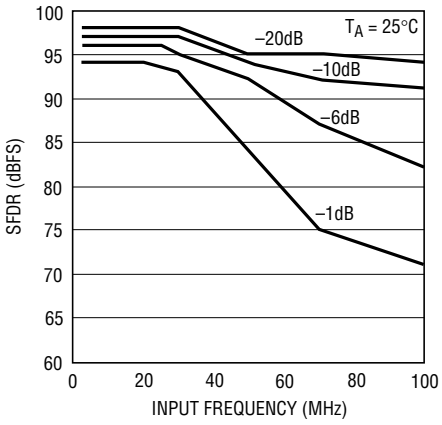


SFDR vs 70MHz Input Level

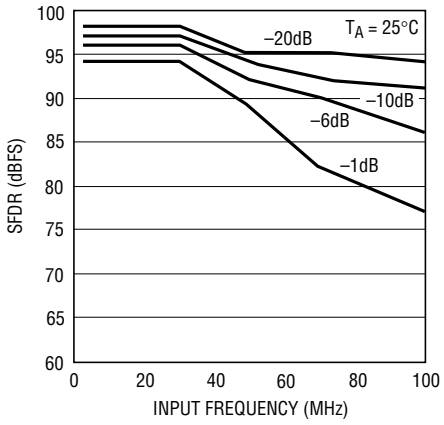


TYPICAL PERFORMANCE CHARACTERISTICS

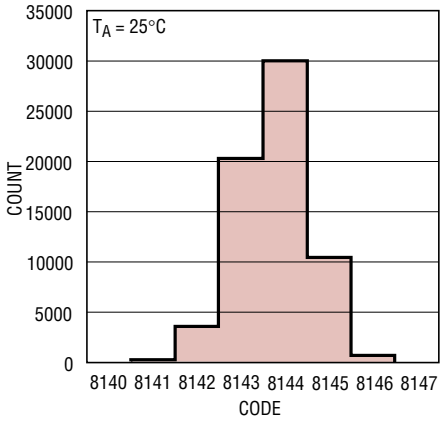
SFDR vs Input Frequency and Amplitude, 3.2V Range, 2nd and 3rd Harmonic



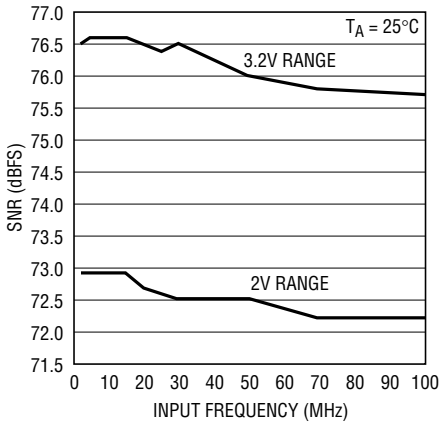
SFDR vs Input Frequency and Amplitude, 2V Range, 2nd and 3rd Harmonic



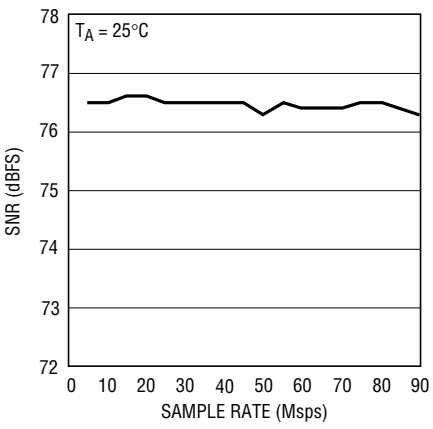
Shorted Input Histogram



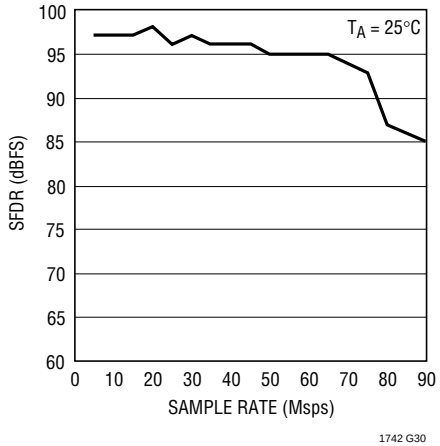
SNR vs Input Frequency 3.2V and 2V Range



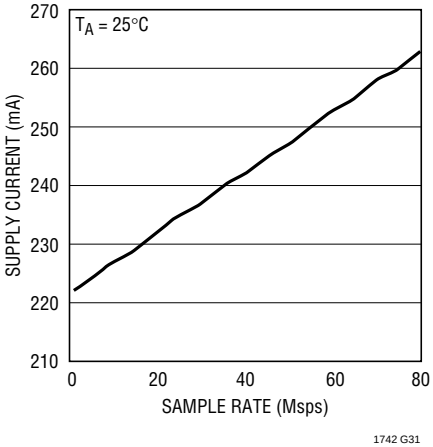
SNR vs Sample Rate, 5MHz Input, –1dB, 3.2V Range



SFDR vs Sample Rate, 5MHz Input, –1dB, 3.2V Range



Supply Current vs Sample Rate



PIN FUNCTIONS

SENSE (Pin 1): Reference Sense Pin. Ground selects ±1V. V_{DD} selects ±1.6V. Greater than 1V and less than 1.6V applied to the SENSE pin selects an input range of $\pm V_{SENSE}$, ±1.6V is the largest valid input range.

V_{CM} (Pin 2): 2.35V Output and Input Common Mode Bias. Bypass to ground with 4.7µF ceramic chip capacitor.

GND (Pins 3, 6, 9, 12, 13, 16, 19, 21, 36, 37): ADC Power Ground.

A_{IN}^+ (Pin 4): Positive Differential Analog Input.

A_{IN}^- (Pin 5): Negative Differential Analog Input.

V_{DD} (Pins 7, 8, 17, 18, 20): 5V Supply. Bypass to AGND with 1µF ceramic chip capacitors at Pin 8 and Pin 18.

REFLB (Pin 10): ADC Low Reference. Bypass to Pin 11 with 0.1µF ceramic chip capacitor. Do not connect to Pin 14.

REFHA (Pin 11): ADC High Reference. Bypass to Pin 10 with 0.1µF ceramic chip capacitor, to Pin 14 with a 4.7µF ceramic capacitor and to ground with 1µF ceramic capacitor.

REFLA (Pin 14): ADC Low Reference. Bypass to Pin 15 with 0.1µF ceramic chip capacitor, to Pin 11 with a 4.7µF ceramic capacitor and to ground with 1µF ceramic capacitor.

REFHB (Pin 15): ADC High Reference. Bypass to Pin 14 with 0.1µF ceramic chip capacitor. Do not connect to Pin 11.

$\overline{\text{MSBINV}}$ (Pin 22): MSB Inversion Control. Low inverts the MSB, 2's complement output format. High does not invert the MSB, offset binary output format.

ENC (Pin 23): Encode Input. The input sample starts on the positive edge.

$\overline{\text{ENC}}$ (Pin 24): Encode Complement Input. Conversion starts on the negative edge. Bypass to ground with 0.1µF ceramic for single-ended ENCODE signal.

$\overline{\text{OE}}$ (Pin 25): Output Enable. Low enables outputs. Logic high makes outputs Hi-Z. $\overline{\text{OE}}$ should not exceed the voltage on OV_{DD}.

CLKOUT (Pin 26): Data Valid Output. Latch data on the rising edge of CLKOUT.

OGND (Pins 27, 38, 47): Output Driver Ground.

D0-D3 (Pins 28 to 31): Digital Outputs.

OV_{DD} (Pins 32, 43): Positive Supply for the Output Drivers. Bypass to ground with 0.1µF ceramic chip capacitor.

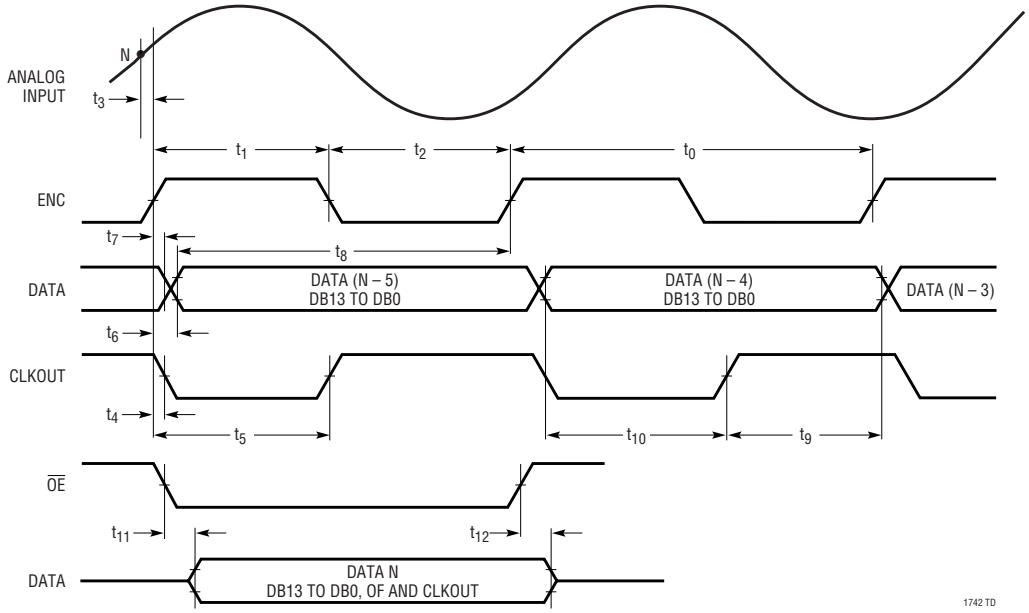
D4-D6 (Pins 33 to 35): Digital Outputs.

D7-D10 (Pins 39 to 42): Digital Outputs.

D11-D13 (Pins 44 to 46): Digital Outputs.

OF (Pin 48): Over/Under Flow Output. High when an over or under flow has occurred.

TIMING DIAGRAM



APPLICATIONS INFORMATION

DYNAMIC PERFORMANCE

Signal-to-Noise Plus Distortion Ratio

The signal-to-noise plus distortion ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the ADC output. The output is band limited to frequencies above DC to below half the sampling frequency.

Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC.

Total Harmonic Distortion

Total harmonic distortion is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20Log\frac{\sqrt{V2^2 + V3^2 + V4^2 + ...Vn^2}}{V1}$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through Vn are the amplitudes of the second through nth harmonics. The THD calculated in this data sheet uses all the harmonics up to the fifth.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. The 3rd order intermodulation products are 2fa + fb, 2fb + fa, 2fa – fb and 2fb – fa. The intermodulation distortion is defined as the ratio of the RMS value of either input tone to the RMS value of the largest 3rd order intermodulation product.

APPLICATIONS INFORMATION

Spurious Free Dynamic Range (SFDR)

Spurious free dynamic range is the peak harmonic or spurious noise that is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full scale input signal.

Input Bandwidth

The input bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full scale input signal.

Aperture Delay Time

The time from when a rising ENC equals the $\overline{ENC}$ voltage to the instant that the input signal is held by the sample and hold circuit.

Aperture Delay Jitter

The variation in the aperture delay time from conversion to conversion. This random variation will result in noise when sampling an AC input. The signal to noise ratio due to the jitter alone will be:

$$SNR_{JITTER} = -20\log(2\pi) \bullet F_{IN} \bullet T_{JITTER}$$

CONVERTER OPERATION

The LTC1742 is a CMOS pipelined multistep converter. The converter has four pipelined ADC stages; a sampled analog input will result in a digitized value five cycles later, see the Timing Diagram section. The analog input is differential for improved common mode noise immunity and to maximize the input range. Additionally, the differential input drive will reduce even order harmonics of the sample-and-hold circuit. The encode input is also differential for improved common mode noise immunity.

The LTC1742 has two phases of operation, determined by the state of the differential ENC/$\overline{ENC}$ input pins. For brevity, the text will refer to ENC greater than $\overline{ENC}$ as ENC high and ENC less than $\overline{ENC}$ as ENC low.

Each pipelined stage shown in Figure 1 contains an ADC, a reconstruction DAC and an interstage residue amplifier.

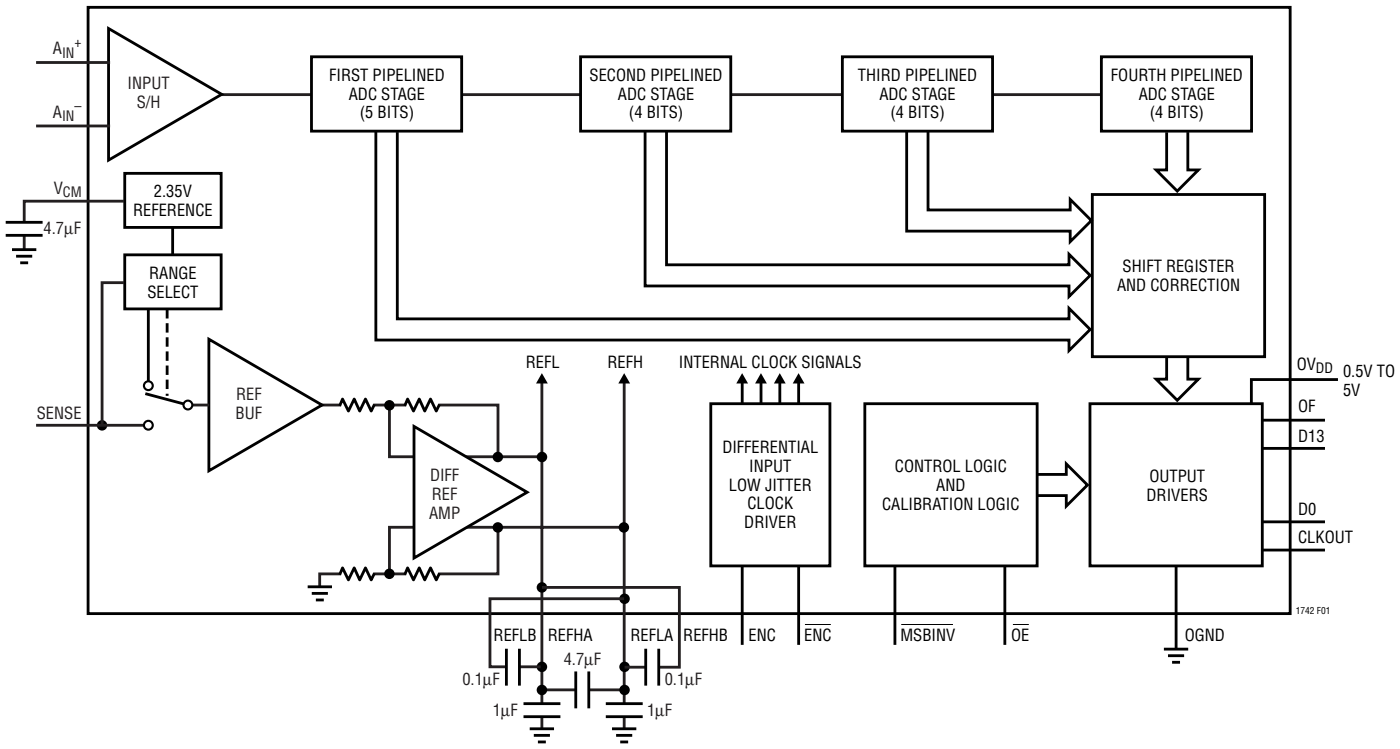


Figure 1. Functional Block Diagram

APPLICATIONS INFORMATION

In operation, the ADC quantizes the input to the stage and the quantized value is subtracted from the input by the DAC to produce a residue. The residue is amplified and output by the residue amplifier. Successive stages operate out of phase so that when the odd stages are outputting their residue, the even stages are acquiring that residue and visa versa.

When ENC is low, the analog input is sampled differentially directly onto the input sample-and-hold capacitors, inside the "Input S/H" shown in the block diagram. At the instant that ENC transitions from low to high, the sampled input is held. While ENC is high, the held input voltage is buffered by the S/H amplifier which drives the first pipelined ADC stage. The first stage acquires the output of the S/H during this high phase of ENC. When ENC goes back low, the first stage produces its residue which is acquired by the second stage. At the same time, the input S/H goes back to acquiring the analog input. When ENC goes back high, the second stage produces its residue which is acquired by the third stage. An identical process is repeated for the third stage, resulting in a third stage residue that is sent to the fourth stage ADC for final evaluation.

Each ADC stage following the first has additional range to accommodate flash and amplifier offset errors. Results from all of the ADC stages are digitally synchronized such that the results can be properly combined in the correction logic before being sent to the output buffer.

SAMPLE/HOLD OPERATION AND INPUT DRIVE

Sample/Hold Operation

Figure 2 shows an equivalent circuit for the LTC1742 CMOS differential sample-and-hold. The differential analog inputs are sampled directly onto sampling capacitors (C_{SAMPLE}) through CMOS transmission gates. This direct capacitor sampling results in lowest possible noise for a given sampling capacitor size. The capacitors shown attached to each input ($C_{PARASITIC}$) are the summation of all other capacitance associated with each input.

During the sample phase when ENC/$\overline{ENC}$ is low, the transmission gate connects the analog inputs to the sampling capacitors and they charge to, and track the differential input voltage. When ENC/$\overline{ENC}$ transitions from low to high the sampled input voltage is held on the sampling capacitors. During the hold phase when ENC/$\overline{ENC}$ is high the sampling capacitors are disconnected from the input and the held voltage is passed to the ADC core for processing. As ENC/$\overline{ENC}$ transitions from high to low the inputs are reconnected to the sampling capacitors to acquire a new sample. Since the sampling capacitors still hold the previous sample, a charging glitch proportional to the change in voltage between samples will be seen at this time. If the change between the last sample and the new sample is small the charging glitch seen at the input will be small. If the input change is large, such as the change seen with input frequencies near Nyquist, then a larger charging glitch will be seen.

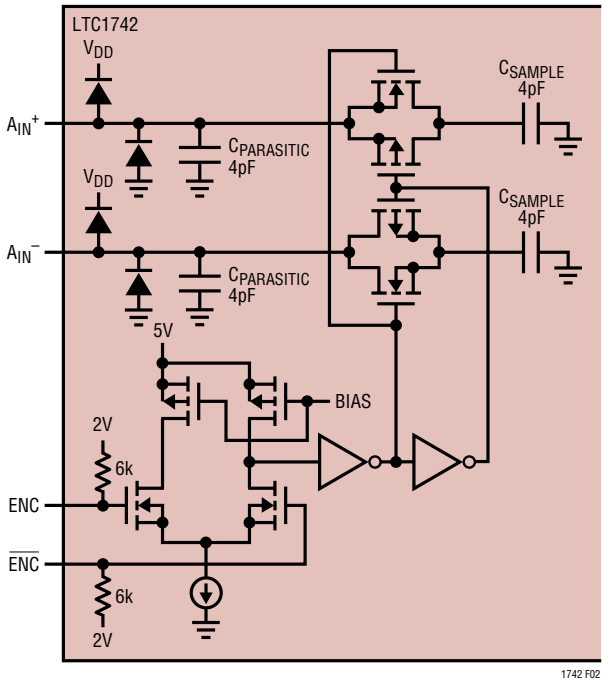


Figure 2. Equivalent Input Circuit

Common Mode Bias

The ADC sample-and-hold circuit requires differential drive to achieve specified performance. Each input should swing ±0.8V for the 3.2V range or ±0.5V for the 2V range, around a common mode voltage of 2.35V. The V_{CM} output pin (Pin 2) may be used to provide the common mode bias level. V_{CM} can be tied directly to the center tap of a transformer to set the DC input level or as a reference level to an op amp differential driver circuit. The V_{CM} pin must be bypassed to ground close to the ADC with a 4.7µF or greater capacitor.

APPLICATIONS INFORMATION

Input Drive Impedance

As with all high performance, high speed ADCs the dynamic performance of the LTC1742 can be influenced by the input drive circuitry, particularly the second and third harmonics. Source impedance and input reactance can influence SFDR. At the falling edge of encode the sample-and-hold circuit will connect the 4pF sampling capacitor to the input pin and start the sampling period. The sampling period ends when encode rises, holding the sampled input on the sampling capacitor. Ideally the input circuitry should be fast enough to fully charge the sampling capacitor during the sampling period $1/(2F_{ENCODE})$; however, this is not always possible and the incomplete settling may degrade the SFDR. The sampling glitch has been designed to be as linear as possible to minimize the effects of incomplete settling.

For the best performance, it is recomended to have a source impedence of 100Ω or less for each input. The S/H circuit is optimized for a 50Ω source impedance. If the source impedance is less than 50Ω, a series resistor should be added to increase this impedance to 50Ω. The source impedence should be matched for the differential inputs. Poor matching will result in higher even order harmonics, especially the second.

Input Drive Circuits

Figure 3 shows the LTC1742 being driven by an RF transformer with a center tapped secondary. The secondary center tap is DC biased with V_{CM}, setting the ADC input signal at its optimum DC level. Figure 3 shows a 1:1 turns ratio transformer. Other turns ratios can be used if the source impedence seen by the ADC does not exceed 100Ω for each ADC input. A disadvantage of using a transformer is the loss of low frequency response. Most small RF transformers have poor performance at frequencies below 1MHz.

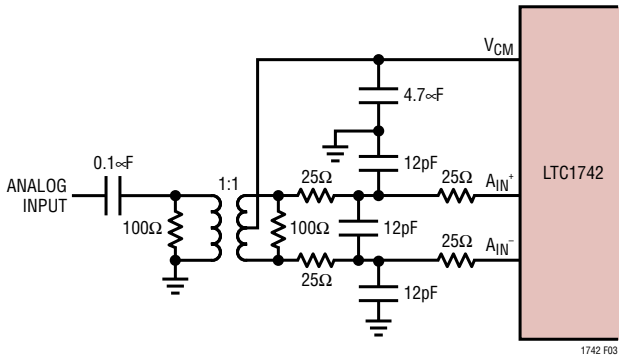


Figure 3. Single-Ended to Differential Conversion Using a Transformer

Figure 4 demonstrates the use of operational amplifiers to convert a single ended input signal into a differential input signal. The advantage of this method is that it provides low frequency input response; however, the limited gain bandwidth of most op amps will limit the SFDR at high input frequencies.

The 25Ω resistors and 12pF capacitors on the analog inputs serve two purposes: isolating the drive circuitry from the sample-and-hold charging glitches and limiting the wideband noise at the converter input. For input frequencies higher than 100MHz, the capacitors may need to be decreased to prevent excessive signal loss.

Reference Operation

Figure 5 shows the LTC1742 reference circuitry consisting of a 2.35V bandgap reference, a difference amplifier and switching and control circuit. The internal voltage reference can be configured for two pin selectable input ranges of 2V(±1V differential) or 3.2V(±1.6V differential). Tying the SENSE pin to ground selects the 2V range; tying the SENSE pin to V_{DD} selects the 3.2V range.

The 2.35V bandgap reference serves two functions: its output provides a DC bias point for setting the common

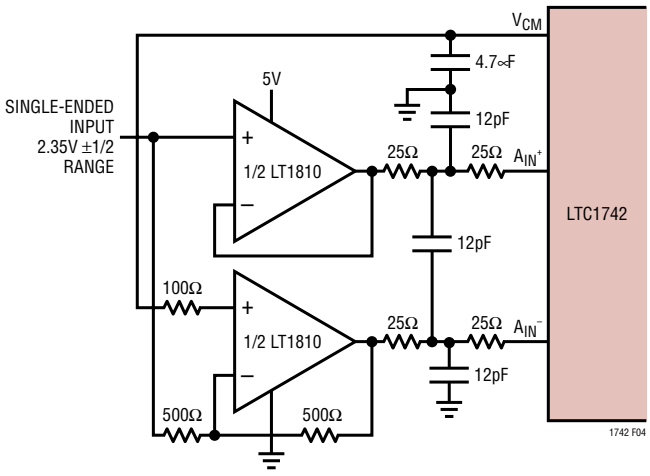


Figure 4. Differential Drive with Op Amps

APPLICATIONS INFORMATION

mode voltage of any external input circuitry; additionally, the reference is used with a difference amplifier to generate the differential reference levels needed by the internal ADC circuitry.

An external bypass capacitor is required for the 2.35V reference output, V_{CM}. This provides a high frequency low impedance path to ground for internal and external circuitry. This is also the compensation capacitor for the reference. It will not be stable without this capacitor.

The difference amplifier generates the high and low reference for the ADC. High speed switching circuits are connected to these outputs and they must be externally bypassed. Each output has two pins: REFHA and REFHB for the high reference and REFLA and REFLB for the low reference. The doubled output pins are needed to reduce package inductance. Bypass capacitors must be connected as shown in Figure 5.

Other voltage ranges in between the pin selectable ranges can be programmed with two external resistors as shown in Figure 6a. An external reference can be used by applying its output directly or through a resistor divider to SENSE. It is not recommended to drive the SENSE pin with a logic device since the logic threshold is close to ground and V_{DD}. The SENSE pin should be tied high or low as close to the converter as possible. If the SENSE pin is driven externally, it should be bypassed to ground as close to the device as possible with a 1µF ceramic capacitor.

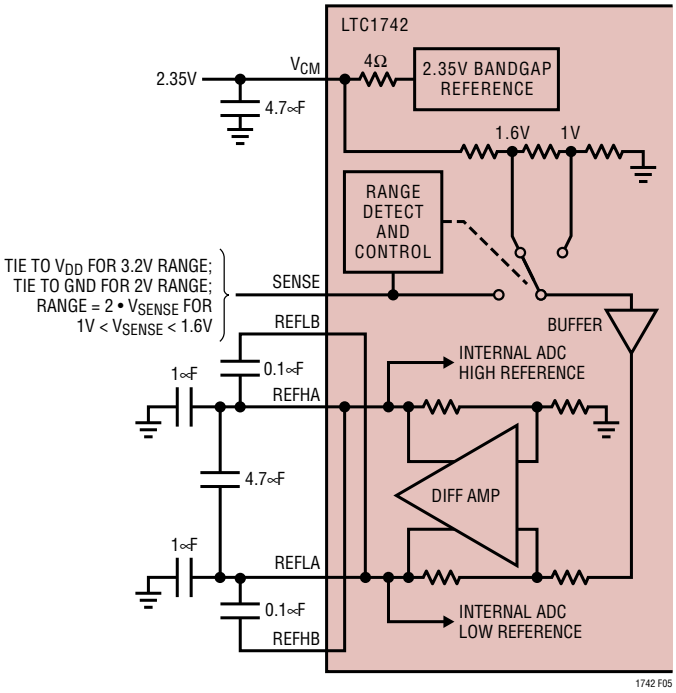


Figure 5. Equivalent Reference Circuit

Input Range

The input range can be set based on the application. For oversampled signal processing in which the input frequency is low (<10MHz), the largest input range will provide the best signal-to-noise performance while maintaining excellent SFDR. For high input frequencies (>40MHz), the 2V range will have the best SFDR performance for the 2nd and 3rd harmonics, but the SNR will degrade by 3.5dB. See the Typical Performance Characteristics section.

Driving the Encode Inputs

The noise performance of the LTC1742 can depend on the encode signal quality as much as on the analog input. The ENC/$\overline{\text{ENC}}$ inputs are intended to be driven differentially, primarily for noise immunity from common mode noise sources. Each input is biased through a 6k resistor to a 2V bias. The bias resistors set the DC operating point for transformer coupled drive circuits and can set the logic threshold for single-ended drive circuits.

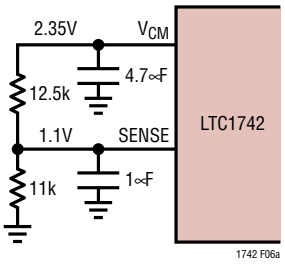


Figure 6a. 2.2V Range ADC

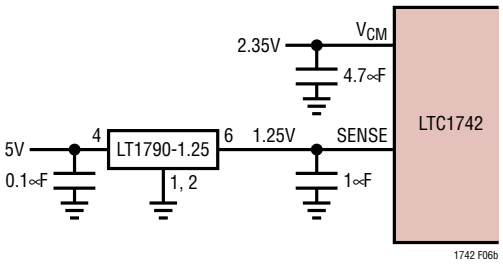


Figure 6b. 2.5V Range ADC with External Reference

APPLICATIONS INFORMATION

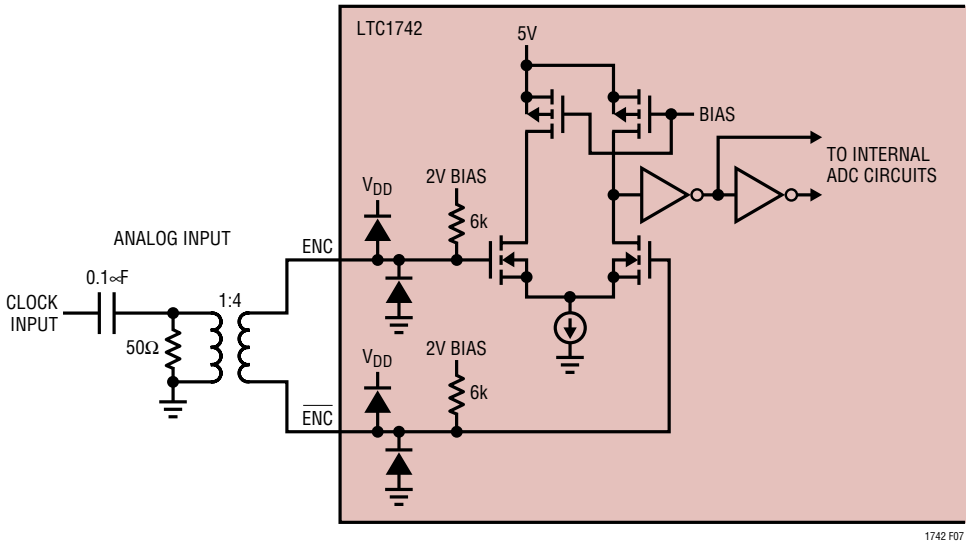


Figure 7. Transformer Driven ENC/$\overline{ENC}$

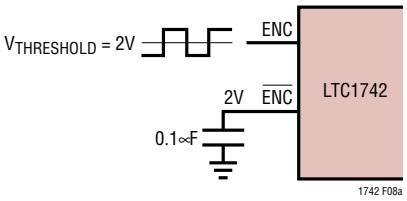


Figure 8a. Single-Ended ENC Drive, Not Recommended for Low Jitter

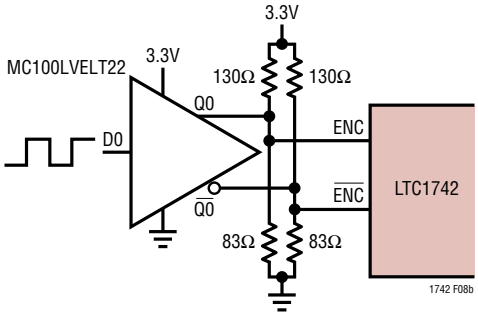


Figure 8b. ENC Drive Using a CMOS-to-PECL Translator

Any noise present on the encode signal will result in additional aperture jitter that will be RMS summed with the inherent ADC aperture jitter.

In applications where jitter is critical (high input frequencies) take the following into consideration:

1. Differential drive should be used.
2. Use as large an amplitude as possible; if transformer coupled use a higher turns ratio to increase the amplitude.
3. If the ADC is clocked with a sinusoidal signal, filter the encode signal to reduce wideband noise.
4. Balance the capacitance and series resistance at both encode inputs so that any coupled noise will appear at both inputs as common mode noise.

The encode inputs have a common mode range of 1.8V to V_{DD}. Each input may be driven from ground to V_{DD} for single-ended drive.

Maximum and Minimum Encode Rates

The maximum encode rate for the LTC1742 is 65Msps. For the ADC to operate properly the encode signal should have a 50% (±5%) duty cycle. Each half cycle must have at least 7.3ns for the ADC internal circuitry to have enough settling time for proper operation. Achieving a precise 50% duty cycle is easy with differential sinusoidal drive using a transformer or using symmetric differential logic such as PECL or LVDS. When using a single-ended encode signal asymmetric rise and fall times can result in duty cycles that are far from 50%.

APPLICATIONS INFORMATION

At sample rates slower than 65Msps the duty cycle can vary from 50% as long as each half cycle is at least 7.3ns.

The lower limit of the LTC1742 sample rate is determined by droop of the sample-and-hold circuits. The pipelined architecture of this ADC relies on storing analog signals on small valued capacitors. Junction leakage will discharge the capacitors. The specified minimum operating frequency for the LTC1742 is 1Msps.

DIGITAL OUTPUTS

Digital Output Buffers

Figure 9 shows an equivalent circuit for a single output buffer. Each buffer is powered by OV_{DD} and OGND, isolated from the ADC power and ground. The additional N-channel transistor in the output driver allows operation down to low voltages. The internal resistor in series with the output makes the output appear as 50Ω to external circuitry and may eliminate the need for external damping resistors.

Output Loading

As with all high speed/high resolution converters the digital output loading can affect the performance. The digital outputs of the LTC1742 should drive a minimal capacitive load to avoid possible interaction between the digital outputs and sensitive input circuitry. The output should be buffered with a device such as an ALVCH16373 CMOS latch. For full speed operation the capacitive load should be kept under 10pF. A resistor in series with the output may be used but is not required since the ADC has a series resistor of 43Ω on chip.

Lower OV_{DD} voltages will also help reduce interference from the digital outputs.

Format

The LTC1742 parallel digital output can be selected for offset binary or 2's complement format. The format is selected with the $\overline{\text{MSBINV}}$ pin; high selects offset binary.

Overflow Bit

An overflow output bit indicates when the converter is overranged or underranged. When OF outputs a logic high the converter is either overranged or underranged.

Output Clock

The ADC has a delayed version of the $\overline{\text{ENC}}$ input available as a digital output, CLKOUT. The CLKOUT pin can be used to synchronize the converter data to the digital system. This is necessary when using a sinusoidal encode. Data will be updated just after CLKOUT falls and can be latched on the rising edge of CLKOUT.

Output Driver Power

Separate output power and ground pins allow the output drivers to be isolated from the analog circuitry. The power supply for the digital output buffers, OV_{DD}, should be tied to the same power supply as for the logic being driven. For example if the converter is driving a DSP powered by a 3V supply then OV_{DD} should be tied to that same 3V supply.

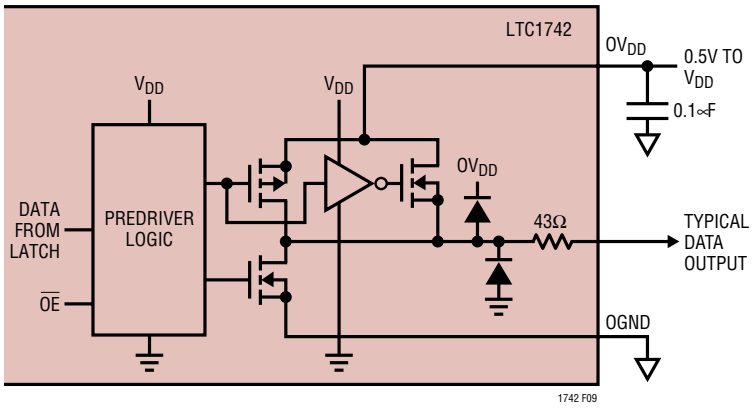


Figure 9. Equivalent Circuit for a Digital Output Buffer

APPLICATIONS INFORMATION

OV_{DD} can be powered with any voltage up to 5V. The logic outputs will swing between OGND and OV_{DD}.

Output Enable

The outputs may be disabled with the output enable pin, $\overline{OE}$. $\overline{OE}$ low disables all data outputs including OF and CLKOUT. The data access and bus relinquish times are too slow to allow the outputs to be enabled and disabled during full speed operation. The output Hi-Z state is intended for use during long periods of inactivity. The voltage on $\overline{OE}$ can swing between GND and OV_{DD}. $\overline{OE}$ should not be driven above OV_{DD}.

GROUNDING AND BYPASSING

The LTC1742 requires a printed circuit board with a clean unbroken ground plane. A multilayer board with an internal ground plane is recommended. The pinout of the LTC1742 has been optimized for a flowthrough layout so that the interaction between inputs and digital outputs is minimized. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC.

High quality ceramic bypass capacitors should be used at the V_{DD}, V_{CM}, REFHA, REFHB, REFLA and REFLB pins as shown in the block diagram on the front page of this data sheet. Bypass capacitors must be located as close to the pins as possible. Of particular importance are the capacitors between REFHA and REFLB and between REFHB and REFLA. These capacitors should be as close to the device as possible (1.5mm or less). Size 0402 ceramic capacitors are recomended. The large 4.7µF capacitor between REFHA and REFLA can be somewhat further away. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The LTC1742 differential inputs should run parallel and close to each other. The input traces should be as short as possible to minimize capacitance and to minimize noise pickup.

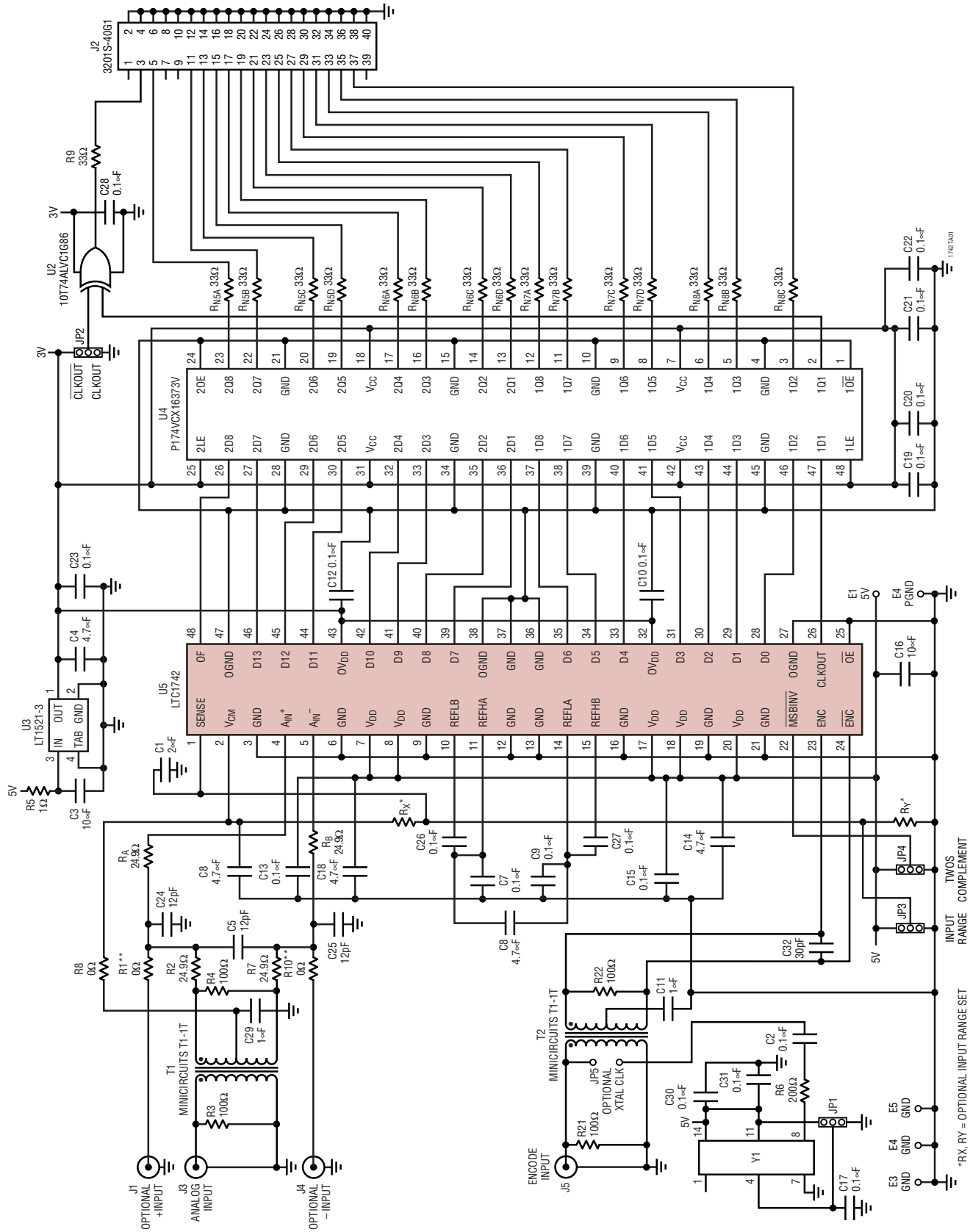
An analog ground plane separate from the digital processing system ground should be used. All ADC ground pins labeled GND should connect to this plane. All ADC V_{DD} bypass capacitors, reference bypass capacitors and input filter capacitors should connect to this analog plane. The LTC1742 has three output driver ground pins, labeled OGND (Pins 27, 38 and 47). These grounds should connect to the digital processing system ground. The output driver supply, OV_{DD} should be connected to the digital processing system supply. OV_{DD} bypass capacitors should bypass to the digital system ground. The digital processing system ground should be connected to the analog plane at ADC OGND (Pin 38).

HEAT TRANSFER

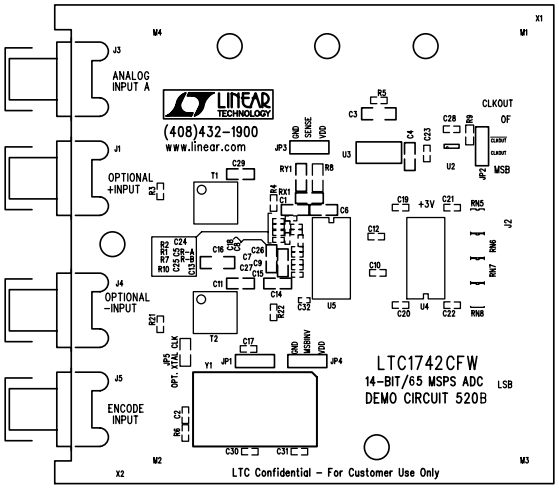
Most of the heat generated by the LTC1742 is transferred from the die through the package leads onto the printed circuit board. In particular, ground pins 12, 13, 36 and 37 are fused to the die attach pad. These pins have the lowest thermal resistance between the die and the outside environment. It is critical that all ground pins are connected to a ground plane of sufficient area. The layout of the evaluation circuit shown on the following pages has a low thermal resistance path to the internal ground plane by using multiple vias near the ground pins. A ground plane of this size results in a thermal resistance from the die to ambient of 35°C/W. Smaller area ground planes or poorly connected ground pins will result in higher thermal resistance.

APPLICATIONS INFORMATION

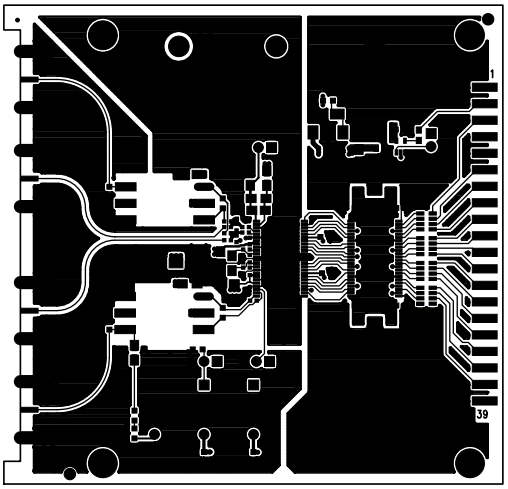
Evaluation Circuit Schematic of the LTC1742



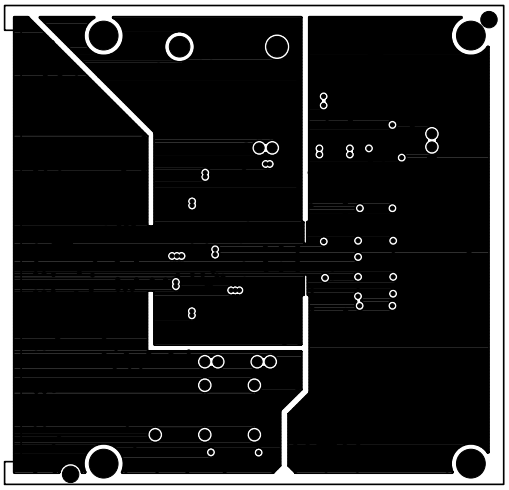
APPLICATIONS INFORMATION



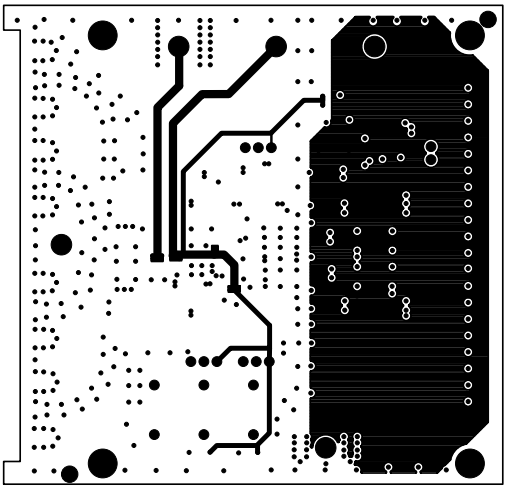
Silkscreen Top



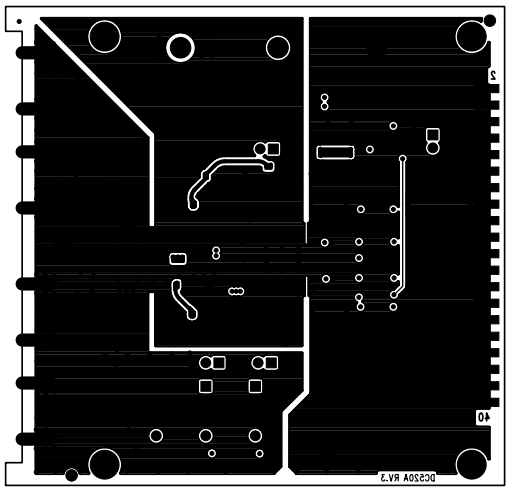
Layer 1 Component Side



Layer 2 GND Plane



Layer 3 Power Plane

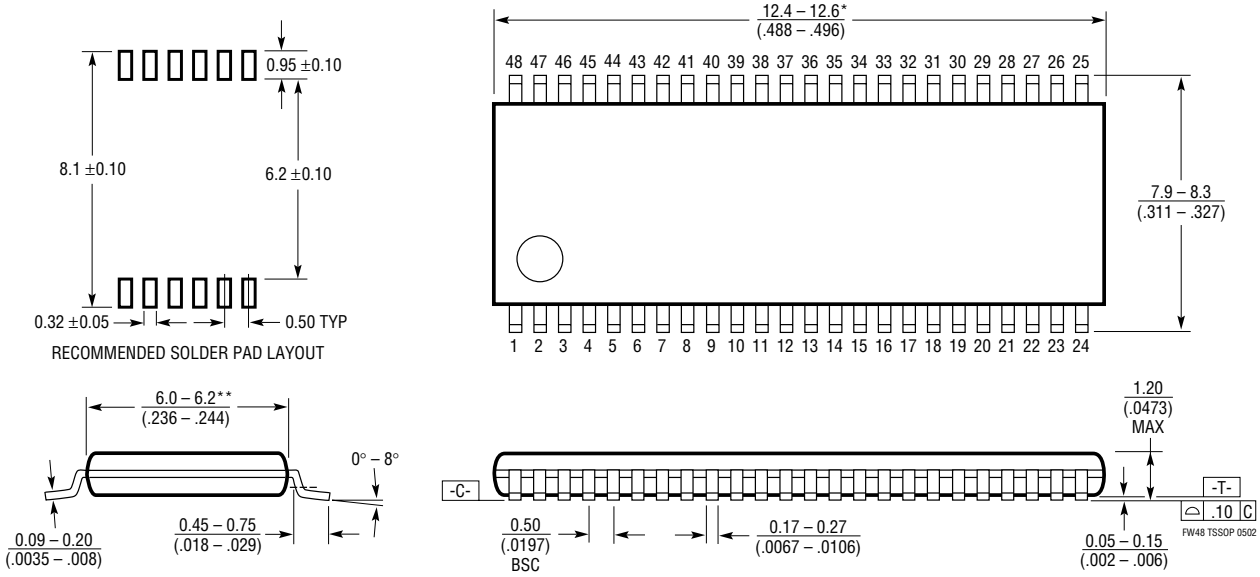


Layer 4 Solder Side

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

PACKAGE DESCRIPTION

FW Package
48-Lead Plastic TSSOP (6.1mm)
(Reference LTC DWG # 05-08-1651)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1405	12-Bit, 5Msps Sampling ADC with Parallel Output	Pin Compatible with the LTC1420
LTC1406	8-Bit, 20Msps ADC	Undersampling Capability up to 70MHz
LTC1411	14-Bit, 2.5Msps ADC	5V, No Pipeline Delay, 80dB SINAD
LTC1412	12-Bit, 3Msps, Sampling ADC	±5V, No Pipeline Delay, 72dB SINAD
LTC1414	14-Bit, 2.2Msps ADC	±5V, 81dB SINAD and 95dB SFDR
LTC1420	12-Bit, 10Msps ADC	71dB SINAD and 83dB SFDR at Nyquist
LT®1461	Micropower Precision Series Reference	0.04% Max Initial Accuracy, 3ppm/°C Drift
LTC1666	12-Bit, 50Msps DAC	Pin Compatible with the LTC1668, LTC1667
LTC1667	14-Bit, 50Msps DAC	Pin Compatible with the LTC1668, LTC1666
LTC1668	16-Bit, 50Msps DAC	16-Bit, No Missing Codes, 90dB SINAD, –100dB THD
LTC1741	12-Bit, 65Msps ADC	Pin Compatible with the LTC1742
LTC1743	12-Bit, 50Msps ADC	Pin Compatible with the LTC1742
LTC1744	14-Bit, 50Msps ADC	Pin Compatible with the LTC1742
LTC1745	12-Bit, 25Msps ADC	Pin Compatible with the LTC1742
LTC1746	14-Bit, 25Msps ADC	Pin Compatible with the LTC1742
LTC1747	12-Bit, 80Msps ADC	Pin Compatible with the LTC1742
LTC1748	14-Bit, 80Msps ADC	Pin Compatible with the LTC1742
LT1807	325MHz, Low Distortion Dual Op Amp	Rail-to-Rail Input and Output

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

LT/TP 0603 1K • PRINTED IN THE USA

© LINEAR TECHNOLOGY CORPORATION 2003