8-Channel, ±10V Input 12-/14-/16-Bit, 100ksps ADC Converters with Shutdown

FEATURES

- **Single 5V Supply**
- **Sample Rate: 100ksps**
- **8-Channel Multiplexer with ±30V Protection**
- **±10V Bipolar Input Range**
  Single Ended or Differential
- **±3LSB INL for the LTC1856, ±1.5LSB INL for the LTC1855, ±1LSB INL for the LTC1854**
- **Power Dissipation: 40mW (Typ)**
- **SPI/MICROWIRE™ Compatible Serial I/O**
- Power Shutdown: Nap and Sleep
- SINAD: 87dB (LTC1856)
- Operates with Internal or External Reference
- Internal Synchronized Clock
- 28-Pin SSOP Package

APPLICATIONS

- Industrial Process Control
- Multiplexed Data Acquisition Systems
- High Speed Data Acquisition for PCs
- Digital Signal Processing

DESCRIPTION

The LTC®1854/LTC1855/LTC1856 are 8-channel, low power, 12-/14-/16-bit, 100ksps, analog-to-digital converters (ADCs). These ADCs operate from a single 5V supply and the 8-channel multiplexer can be programmed for single-ended inputs, pairs of differential inputs, or combinations of both. In addition, all channels are fault protected to ±30V. A fault condition on any channel will not affect the conversion result of the selected channel.

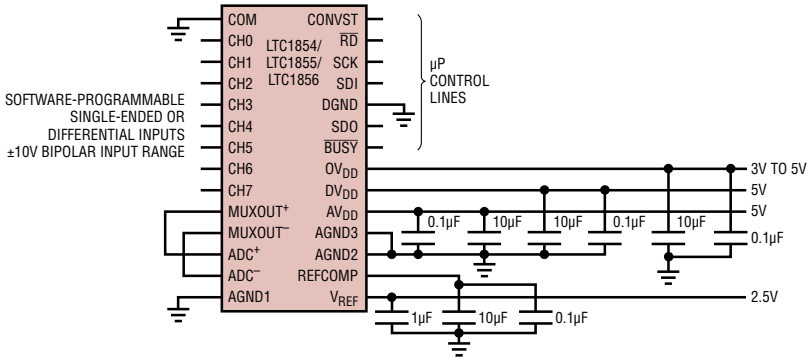
An onboard precision reference minimizes external components. Power dissipation is 40mW at 100ksps and lower in two power shutdown modes (27.5mW in Nap mode and 40µW in Sleep mode.) DC specifications include ±3LSB INL for the LTC1856, ±1.5LSB INL for the LTC1855 and ±1LSB for the LTC1854.

The internal clock is trimmed for 5µs maximum conversion time and the sampling rate is guaranteed at 100ksps. A separate convert start input and data ready signal ($\overline{BUSY}$) ease connections to FIFOs, DSPs and microprocessors.

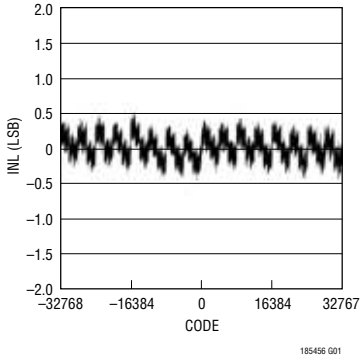
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All other trademarks are the property of their respective owners.

TYPICAL APPLICATION

100kHz, 12-Bit/14-/16-Bit Sampling ADC



LTC1856 Typical INL Curve

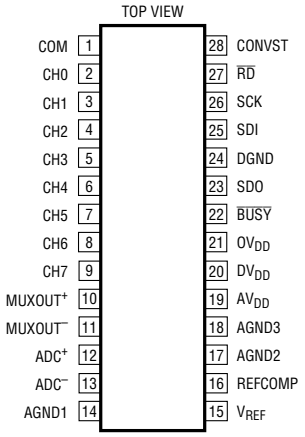


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (OV_{DD} = DV_{DD} = AV_{DD} = V_{DD}) 6V
Ground Voltage Difference
DGND, AGND1, AGND2, AGND3 ..... ±0.3V
Analog Input Voltage
ADC^+, ADC^-
(Note 3) .....(AGND1 – 0.3V) to (AV_{DD} + 0.3V)
CH0-CH7, COM ..... ±30V
Digital Input Voltage (Note 4) .....(DGND – 0.3V) to 10V
Digital Output Voltage ....(DGND – 0.3V) to (DV_{DD} + 0.3V)
Power Dissipation..... 500mW
Operating Temperature Range
LTC1854C/LTC1855C/LTC1856C..... 0°C to 70°C
LTC1854I/LTC1855I/LTC1856I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 160°C/W
EXPOSED PAD (PIN #) IS GND, MUST BE SOLDERED TO PCB

ORDER PART NUMBER

LTC1854CG	LTC1855CG	LTC1856CG
LTC1854IG	LTC1855IG	LTC1856IG

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

CONVERTER AND MULTIPLEXER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. MUXOUT connected to ADC inputs. (Notes 5, 6)

PARAMETER	CONDITIONS		LTC1854 MIN	LTC1854 TYP	LTC1854 MAX	LTC1855 MIN	LTC1855 TYP	LTC1855 MAX	LTC1856 MIN	LTC1856 TYP	LTC1856 MAX	UNITS
Resolution		●	12			14			15			Bits
No Missing Codes		●	12			14			15			Bits
Transition Noise				0.06			0.25			1		LSB_{RMS}
Integral Linearity Error	(Note 7)	●			±1			±1.5			±3	LSB
Differential Linearity Error		●	–1		1	–1		1.5	–2		4	LSB
Bipolar Zero Error	(Note 8)	●			±5			±8			±23	LSB
Bipolar Zero Error Drift				±0.1			±0.1			±0.1		ppm/°C
Bipolar Zero Error Match					3			4			10	LSB
Bipolar Full-Scale Error	External Reference (Note 11) Internal Reference (Note 11)	●			±0.34 ±0.45			±0.14 ±0.40			±0.1 ±0.4	% %
Bipolar Full-Scale Error Drift	External Reference Internal Reference			±2.5 ±7			±2.5 ±7			±2.5 ±7		ppm/°C ppm/°C
Bipolar Full-Scale Error Match					5			10			15	LSB
Input Common Mode Range		●		±10			±+10			±10		V
Input Common Mode Rejection Ratio				96			96			96		dB

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Input Range	CH0 to CH7, COM			±10		V
	ADC^+, ADC^- (Note 3)			ADC^- ±2.048		V
Impedance	CH0 to CH7, COM			31		kΩ
	$MUXOUT^+$, $MUXOUT^-$			5		kΩ
Capacitance	CH0 to CH7, COM			5		pF
	Sample Mode ADC^+, ADC^-			12		pF
	Hold Mode ADC^+, ADC^-			4		pF
Input Leakage Current	ADC^+, ADC^-, CONVST = Low	●			±1	µA

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. MUXOUT connected to ADC inputs. (Note 5)

				LTC1854			LTC1855			LTC1856			
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-(Noise + Distortion) Ratio	1kHz Input Signal			74			83			87		dB
THD	Total Harmonic Distortion	1kHz Input Signal First Five Harmonics			–102			–95			–101		dB
	Peak Harmonic or Spurious Noise	1kHz Input Signal			–99			–99			–103		dB
	Channel-to-Channel Isolation	1kHz Input Signal			–120			–120			–120		dB
	–3dB Input Bandwidth				1			1			1		MHz
	Aperture Delay				–70			–70			–70		ns
	Aperture Jitter				60			60			60		ps
	Transient Response	Full-Scale Step (Note 9)				4			4			4	µs
	Overvoltage Recovery	(Note 12)			150			150			150		ns

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0	●	2.475	2.50	2.525	V
V_{REF} Output Temperature Coefficient	I_{OUT} = 0			±10		ppm/°C
V_{REF} Output Impedance	–0.1mA ≤ I_{OUT} ≤ 0.1mA			8		kΩ
$V_{REFCOMP}$ Output Voltage	I_{OUT} = 0			4.096		V

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{DD} = 4.75V, I_O = –10µA, OV_{DD} = V_{DD} V_{DD} = 4.75V, I_O = –200µA, OV_{DD} = V_{DD}	 ●	 4	4.74		V V
V_{OL}	Low Level Output Voltage	V_{DD} = 4.75V, I_O = 160µA, OV_{DD} = V_{DD} V_{DD} = 4.75V, I_O = 1.6mA, OV_{DD} = V_{DD}	 ●		0.05 0.10	 0.4	V V
I_{OZ}	Hi-Z Output Leakage	V_{OUT} = 0V to V_{DD}, $\overline{RD}$ = High	●			±10	µA
C_{OZ}	Hi-Z Output Capacitance	$\overline{RD}$ = High			15		pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			10		mA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Positive Supply Voltage	(Notes 9 and 10)		4.75	5.00	5.25	V
Positive Supply Current Nap Mode Sleep Mode	 CONVST = 0V or 5V	●		8.0 5.5 8.0	12 7 13	mA mA µA
Power Dissipation Nap Mode Sleep Mode	 CONVST = 0V or 5V			40.0 27.5 40.0		mW mW µW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency	Through CH0 to CH7 Inputs Through ADC+, ADC– Only	●	100	 166		kHz kHz
t_{CONV}	Conversion Time		●		4	5	µs
t_{ACQ}	Acquisition Time	Through CH0 to CH7 Inputs Through ADC+, ADC– Only	●		 1	4	µs µs
f_{SCK}	SCK Frequency	(Note 13)	●	0		20	MHz
t_r	SDO Rise Time	See Test Circuits			6		ns
t_f	SDO Fall Time	See Test Circuits			6		ns
t_1	CONVST High Time		●	40			ns
t_2	CONVST to $\overline{BUSY}$ Delay	C_L = 25pF, See Test Circuits	●		15	30	ns
t_3	SCK Period		●	50			ns
t_4	SCK High		●	10			ns
t_5	SCK Low		●	10			ns
t_6	Delay Time, SCK↓ to SDO Valid	C_L = 25pF, See Test Circuits	●		25	45	ns
t_7	Time from Previous SDO Data Remains Valid After SCK↓	C_L = 25pF, See Test Circuits	●	5	20		ns
t_8	SDO Valid After $\overline{RD}$↓	C_L = 25pF, See Test Circuits	●		11	30	ns
t_9	$\overline{RD}$↓ to SCK Setup Time		●	20			ns
t_{10}	SDI Setup Time Before SCK↑		●	0			ns
t_{11}	SDI Hold Time After SCK↑		●	7			ns
t_{12}	SDO Valid Before $\overline{BUSY}$↑	$\overline{RD}$ = Low, C_L = 25pF, See Test Circuits	●	5	20		ns
t_{13}	Bus Relinquish Time	See Test Circuits	●		10	30	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground with DGND, AGND1, AGND2 and AGND3 wired together unless otherwise noted.

Note 3: When these pin voltages are taken below ground or above AV_{DD} = DV_{DD} = OV_{DD} = V_{DD}, they will be clamped by internal diodes. This product can handle currents of greater than 100mA below ground or above V_{DD} without latchup.

Note 4: When these pin voltages are taken below ground they will be clamped by internal diodes. This product can handle currents of greater than 100mA below ground without latchup. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 5V, f_{SAMPLE} = 100kHz, t_r = t_f = 5ns unless otherwise specified.

Note 6: Linearity, offset and full-scale specifications apply for a single-ended analog MUX input with respect to ground or ADC+ with respect to ADC– tied to ground.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual end points of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Bipolar zero error is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111 for the LTC1856, between 00 0000 0000 0000 and 11 1111 1111 1111 for the LTC1855 and between 0000 0000 0000 and 1111 1111 1111 for the LTC1854.

Note 9: Guaranteed by design, not subject to test.

Note 10: Recommended operating conditions.

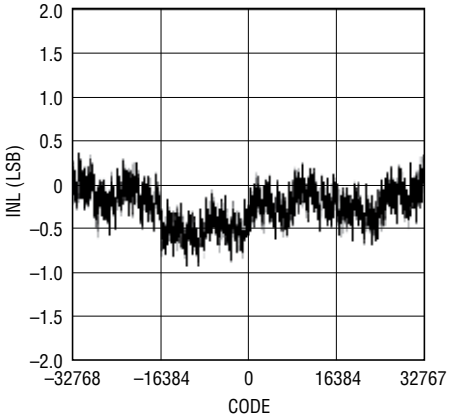
Note 11: Full-scale bipolar error is the worst case of –FS or +FS untrimmed deviation from ideal first and last code transitions, divided by the full-scale range, and includes the effect of offset error.

Note 12: Recovers to specified performance after (2 • FS) input overvoltage.

Note 13: t_6 of 45ns maximum allows f_{SCK} up to 10MHz for rising capture with 50% duty cycle and f_{SCK} up to 20MHz for falling capture (with 5ns setup time for the receiving logic).

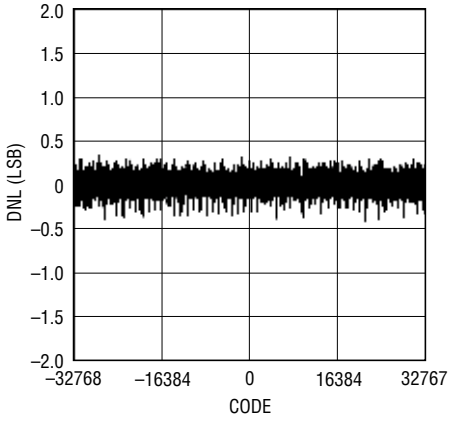
TYPICAL PERFORMANCE CHARACTERISTICS

LTC1856 Typical INL Curve



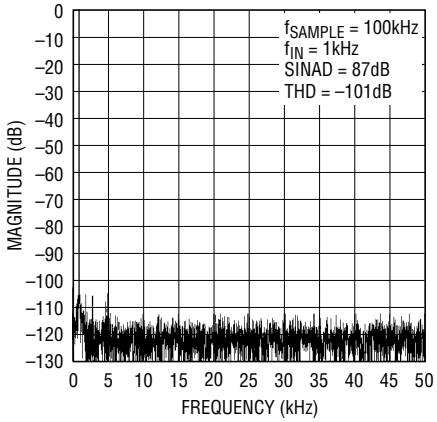
185456 G01

LTC1856 Typical DNL Curve



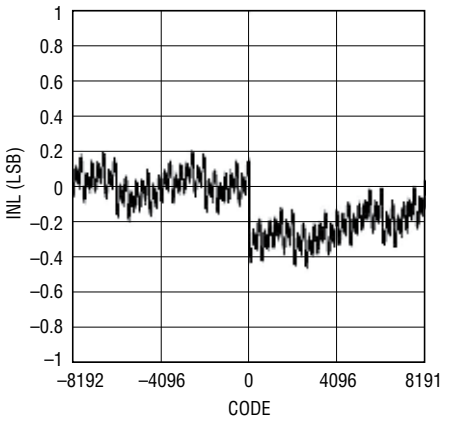
185456 G02

LTC1856 Nonaveraged 4096-Point FFT Plot



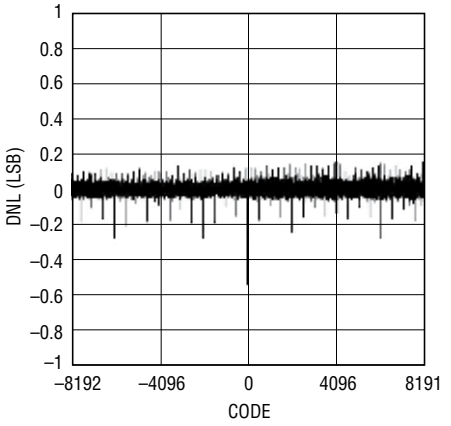
185456 G03

LTC1855 Typical INL Curve



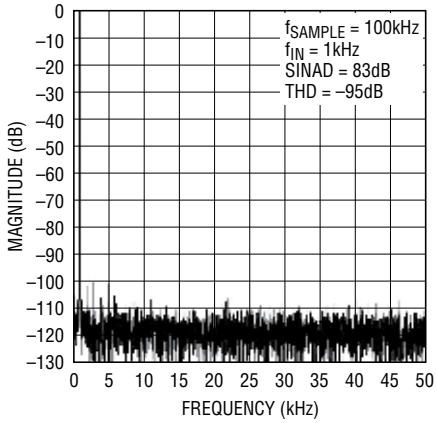
185455 G04

LTC1855 Typical DNL Curve



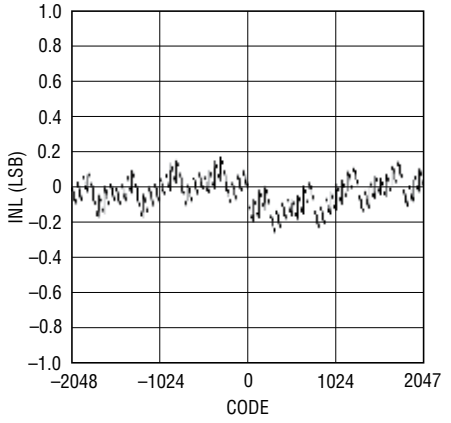
185456 G05

LTC1855 Nonaveraged 4096-Point FFT Plot



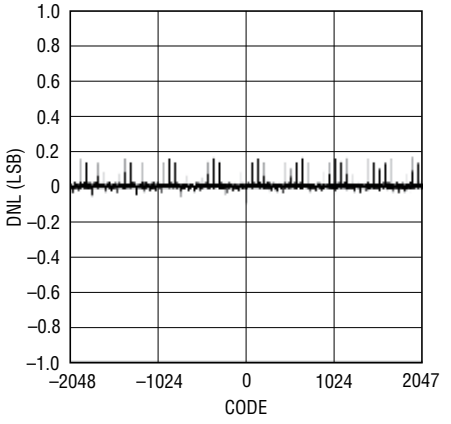
185456 G06

LTC1854 Typical INL Curve



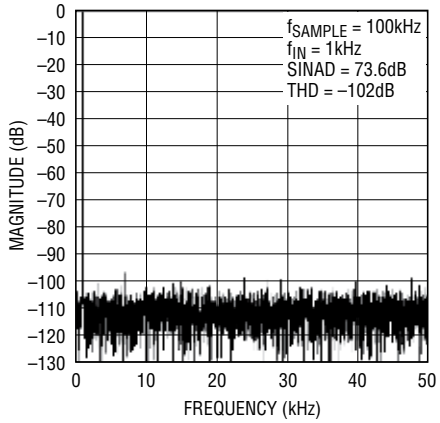
185456 G07

LTC1854 Typical DNL Curve



185456 G08

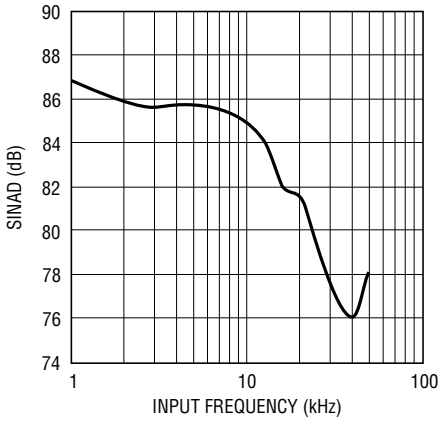
LTC1854 Nonaveraged 4096-Point FFT Plot



185456 G09

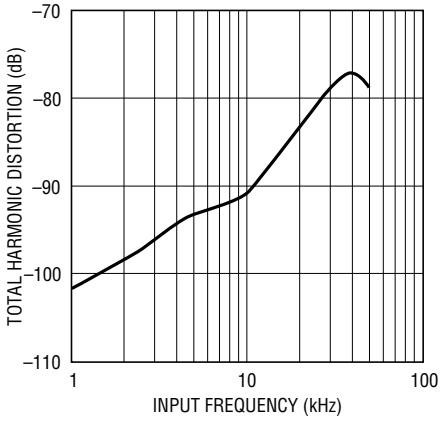
TYPICAL PERFORMANCE CHARACTERISTICS

LTC1856 SINAD vs Input Frequency



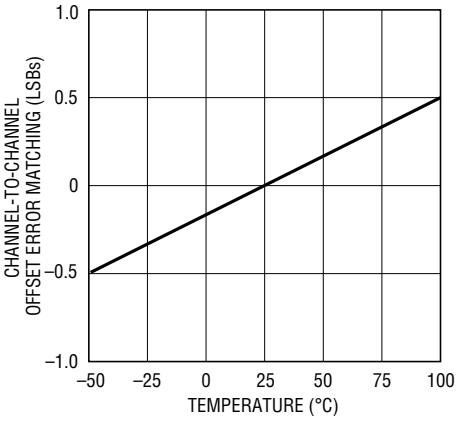
185456 G10

LTC1856 Total Harmonic Distortion vs Input Frequency



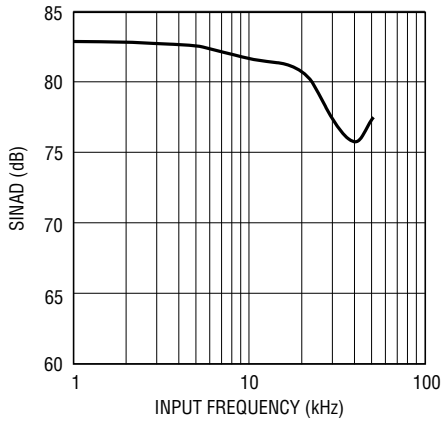
185456 G11

LTC1856 Channel-to-Channel Offset Error Matching vs Temperature



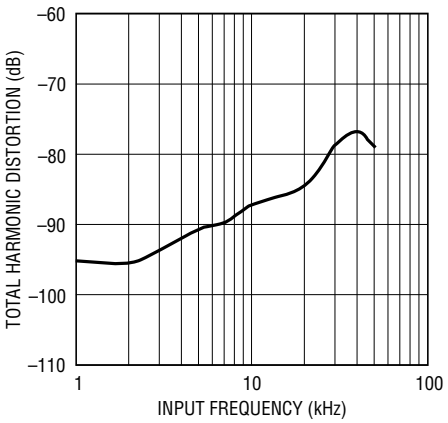
185456 G12

LTC1855 SINAD vs Input Frequency



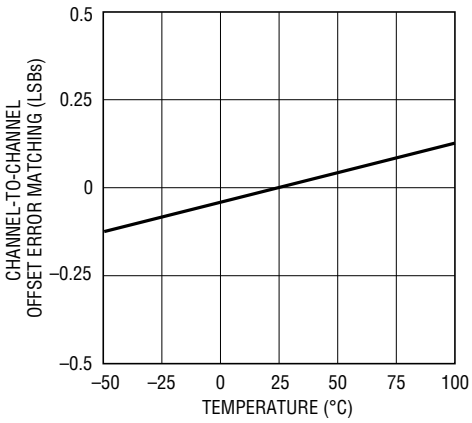
185456 G13

LTC1855 Total Harmonic Distortion vs Input Frequency



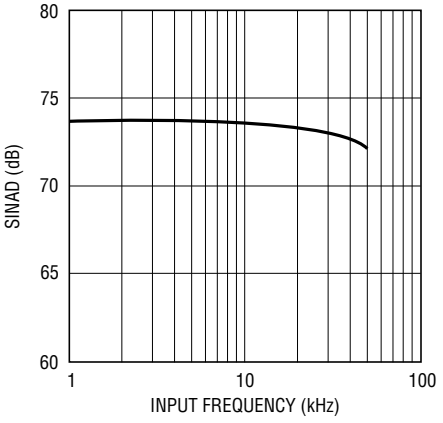
185456 G14

LTC1855 Channel-to-Channel Offset Error Matching vs Temperature



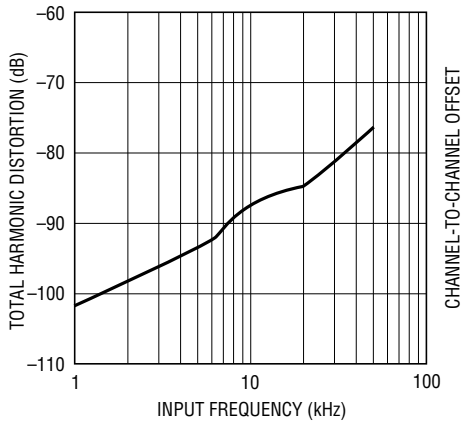
185456 G15

LTC1854 SINAD vs Input Frequency



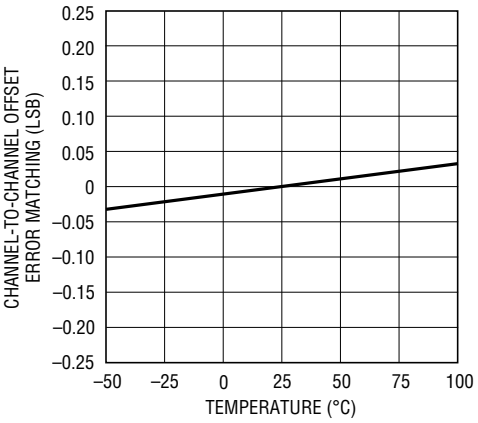
185456 G16

LTC1854 Total Harmonic Distortion vs Input Frequency



185456 G17

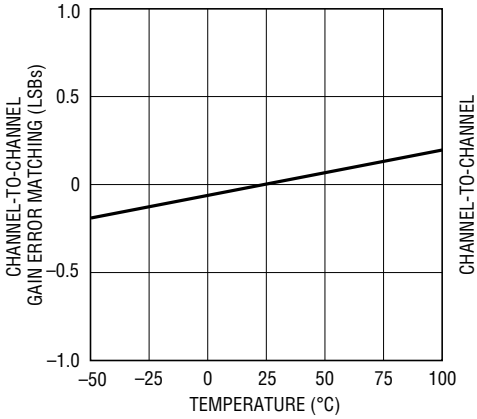
LTC1854 Channel-to-Channel Offset Error Matching vs Temperature



185456 G18

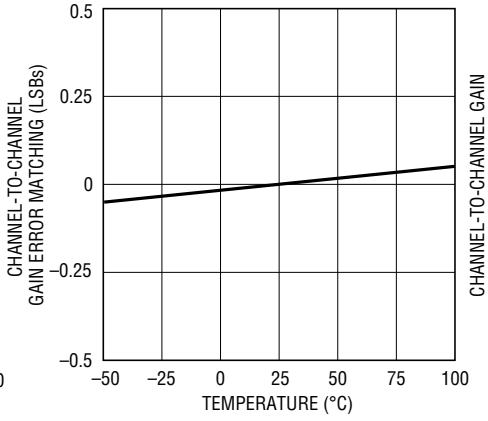
TYPICAL PERFORMANCE CHARACTERISTICS

LTC1856 Channel-to-Channel Gain Error Matching vs Temperature



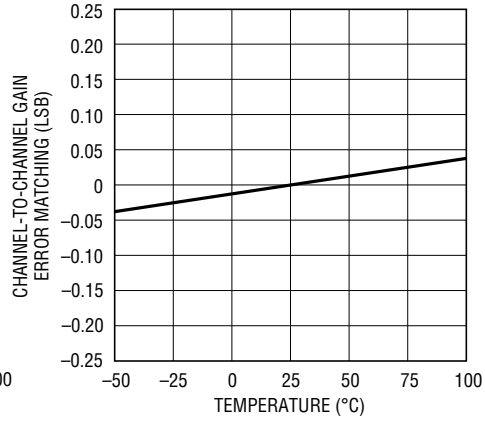
185456 G19

LTC1855 Channel-to-Channel Gain Error Matching vs Temperature



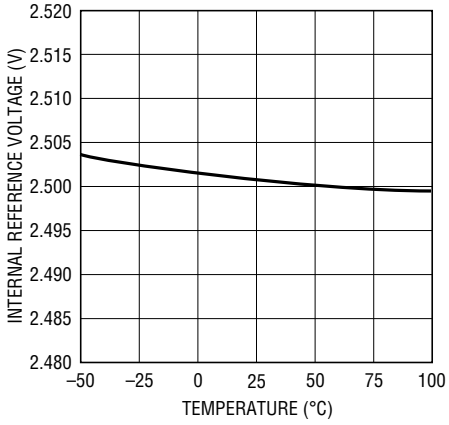
185456 G20

LTC1854 Channel-to-Channel Gain Error Matching vs Temperature



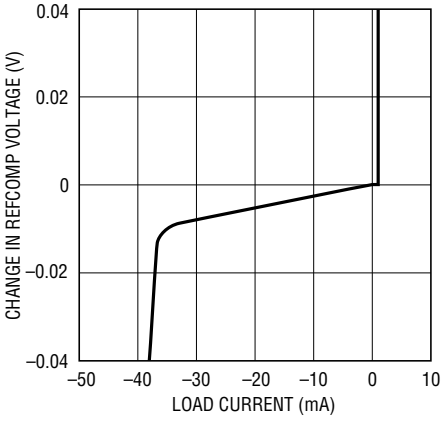
185456 G21

Internal Reference Voltage vs Temperature



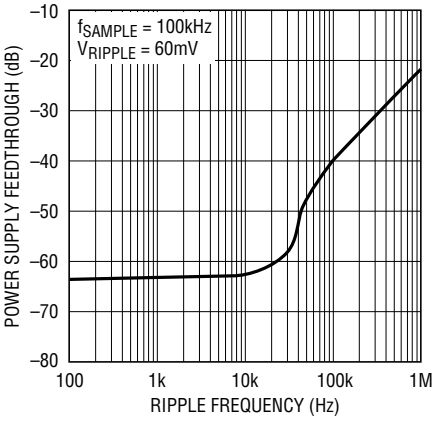
185456 G22

Change in REFCOMP Voltage vs Load Current



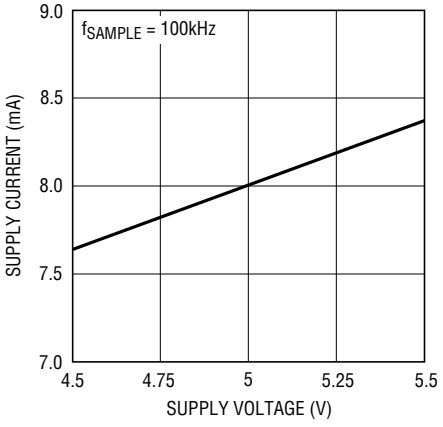
185456 G23

LTC1856 Power Supply Feedthrough vs Ripple Frequency



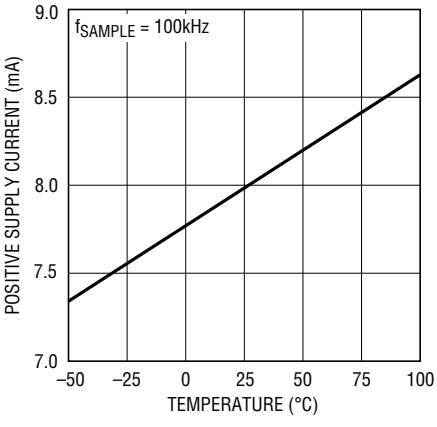
185456 G24

Supply Current vs Supply Voltage



185454 G25

Supply Current vs Temperature



185456 G26

PIN FUNCTIONS

COM (Pin 1): Common Input. This is the negative reference point for all single-ended inputs. It must be free of noise and is usually connected to the analog ground plane.

CH0 (Pin 2): Analog MUX Input.

CH1 (Pin 3): Analog MUX Input.

CH2 (Pin 4): Analog MUX Input.

CH3 (Pin 5): Analog MUX Input.

CH4 (Pin 6): Analog MUX Input.

CH5 (Pin 7): Analog MUX Input.

CH6 (Pin 8): Analog MUX Input.

CH7 (Pin 9): Analog MUX Input.

MUXOUT$^+$ (Pin 10): Positive MUX Output. Output of the analog multiplexer. Connect to ADC$^+$ for normal operation.

MUXOUT$^-$ (Pin 11): Negative MUX Output. Output of the analog multiplexer. Connect to ADC$^-$ for normal operation.

ADC$^+$ (Pin 12): Positive Analog Input to the Analog-to-Digital Converter.

ADC$^-$ (Pin 13): Negative Analog Input to the Analog-to-Digital Converter.

AGND1 (Pin 14): Analog Ground.

V_{REF} (Pin 15): 2.5V Reference Output. Bypass to analog ground with a 1µF tantalum capacitor.

REFCOMP (Pin 16): Reference Buffer Output. Bypass to analog ground with a 10µF tantalum and a 0.1µF ceramic capacitor. Nominal output voltage is 4.096V.

AGND2 (Pin 17): Analog Ground.

AGND3 (Pin 18): Analog Ground. This is the substrate connection.

AV_{DD} (Pin 19): 5V Analog Supply. Bypass to analog ground with a 0.1µF ceramic and a 10µF tantalum capacitor.

DV_{DD} (Pin 20): 5V Digital Supply. Bypass to digital ground with a 0.1µF ceramic and a 10µF tantalum capacitor.

OV_{DD} (Pin 21): Positive Supply for the Digital Output Buffers (3V to 5V). Bypass to digital ground with a 0.1µF ceramic and a 10µF tantalum capacitor.

$\overline{BUSY}$ (Pin 22): Output shows converter status. It is low when a conversion is in progress.

SDO (Pin 23): Serial Data Output.

PIN FUNCTIONS

DGND (Pin 24): Digital Ground.

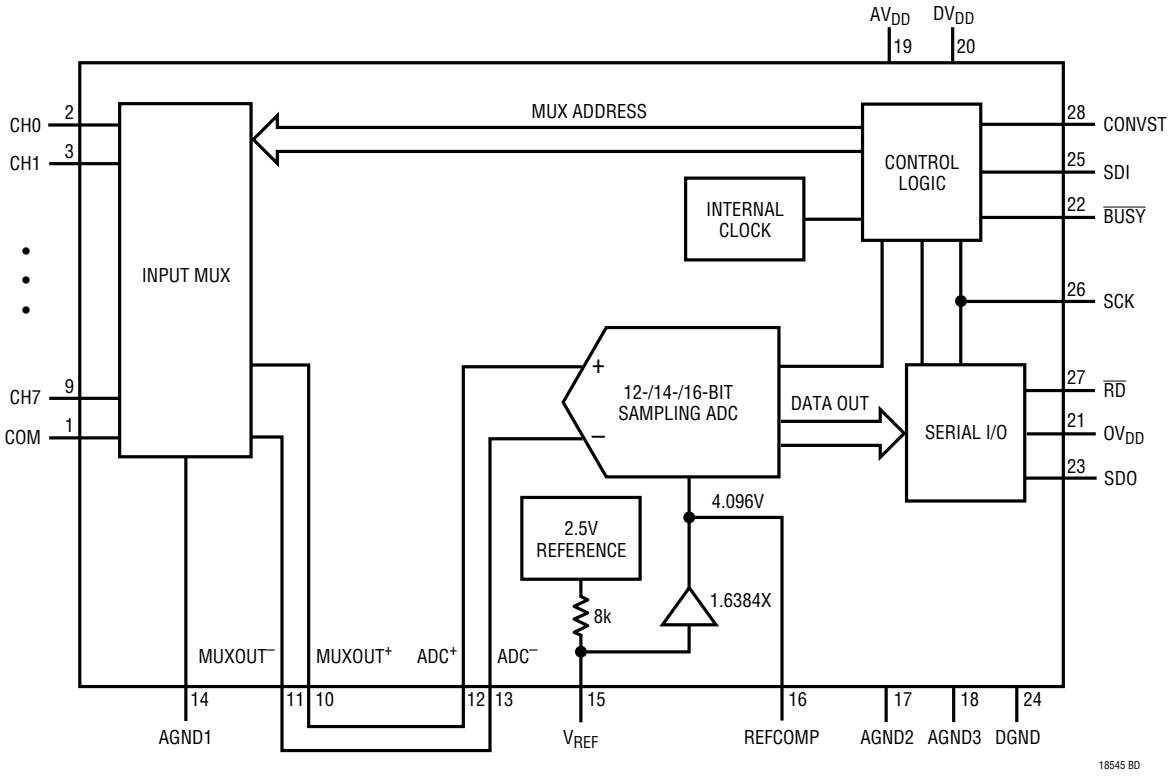
SDI (Pin 25): Serial Data Input.

SCK (Pin 26): Serial Data Clock.

$\overline{RD}$ (Pin 27): Read Input. This active low signal enables the digital output pin SDO and enables the serial interface, SDI and SCK are ignored when $\overline{RD}$ is high.

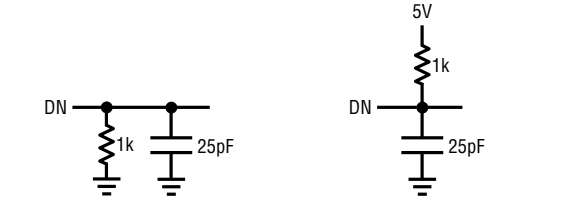
CONVST (Pin 28): Conversion Start. The ADC starts a conversion on CONVST's rising edge.

FUNCTIONAL BLOCK DIAGRAM



TEST CIRCUITS

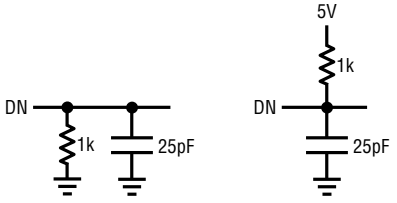
Load Circuits for Access Timing



(A) Hi-Z TO V_{OH} AND V_{OL} TO V_{OH} (B) Hi-Z TO V_{OL} AND V_{OH} TO V_{OL}

18545 TC01

Load Circuits for Output Float Delay

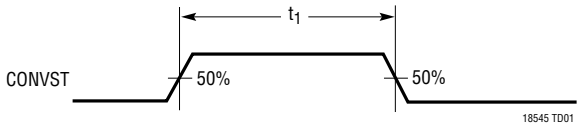


(A) V_{OH} TO Hi-Z (B) V_{OL} TO Hi-Z

18545 TC02

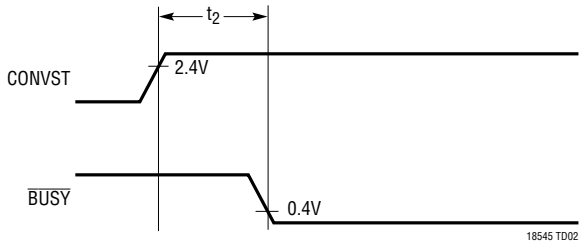
TIMING DIAGRAMS

t_1 (For Short Pulse Mode)



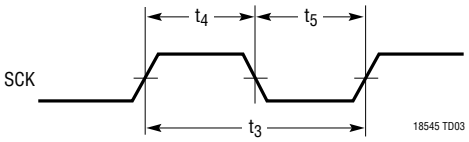
18545 TD01

t_2 (CONVST to $\overline{BUSY}$ Delay)



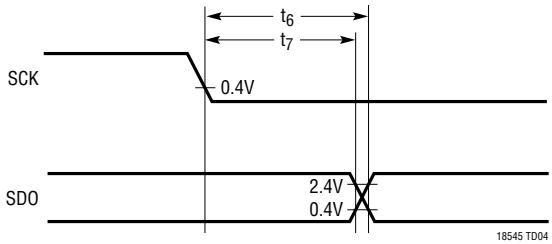
18545 TD02

t_3, t_4, t_5 (SCK Timing)



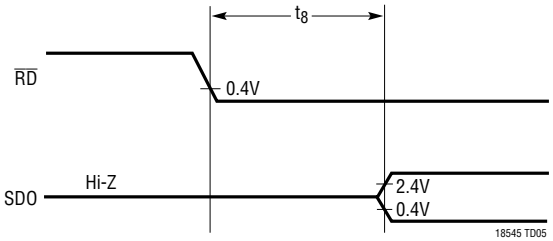
18545 TD03

t_6 (Delay Time, SCK↓ to SDO Valid)
t_7 (Time from Previous Data Remains Valid After SCK↓)



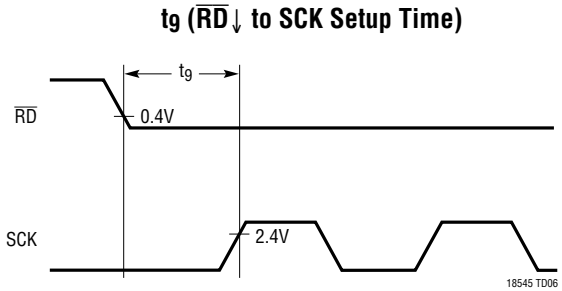
18545 TD04

t_8 (SDO Valid After $\overline{RD}$↓)



18545 TD05

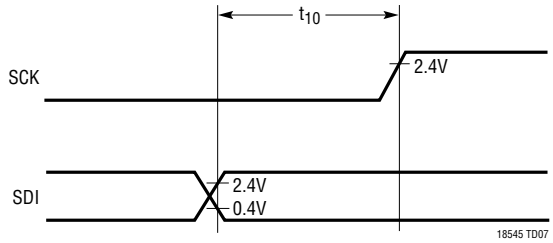
t_9 ($\overline{RD}$↓ to SCK Setup Time)



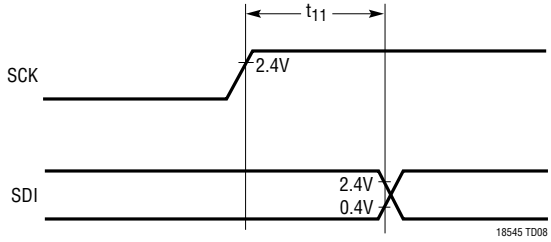
18545 TD06

TIMING DIAGRAMS

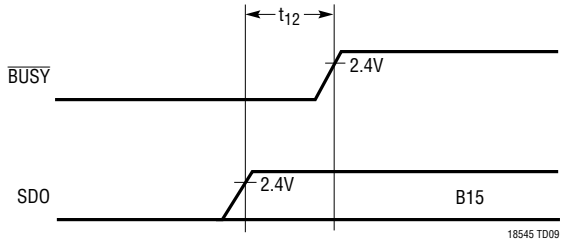
t_{10} (SDI Setup Time Before SCK↑)



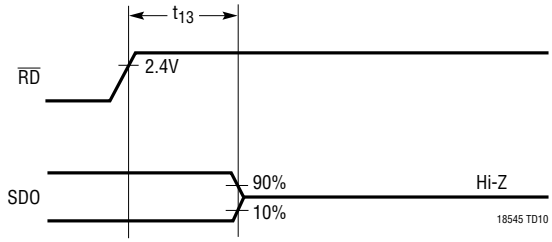
t_{11} (SDI Hold Time After SCK↑)



t_{12} (SDO Valid Before $\overline{BUSY}$↑, $\overline{RD}$ = 0)



t_{13} (BUS Relinquish Time)



APPLICATIONS INFORMATION

OVERVIEW

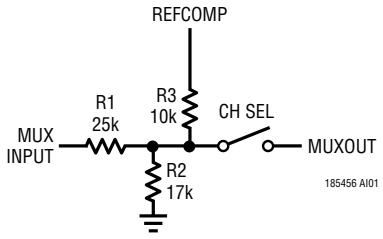
The LTC1854/LTC1855/LTC1856 are innovative, multichannel ADCs. The on-chip resistors provide attenuation and offset for each channel. The precisely trimmed attenuators ensure an accurate input range. Because they precede the multiplexer, errors due to multiplexer on-resistance are eliminated.

The input word selects the single ended or differential inputs for each channel or pair of channels. Overrange protection is provided for unselected channels. An overrange condition on an unused channel will not affect the conversion result on the selected channel.

CONVERSION DETAILS

The LTC1854/LTC1855/LTC1856 use a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 12-/14-/16-bit serial output respectively. The ADCs are complete with a precision reference and an internal clock. The control logic provides easy interface to microprocessors and DSPs. (Please refer to the Digital Interface section for the data format.)

The analog signals applied at the MUX input channels are rescaled by the resistor divider network formed by R1, R2 and R3 as shown below. The rescaled signals appear on the MUXOUT (Pins 10, 11) which are also connected to the ADC inputs (Pins 12, 13) under normal operation.



Before starting a conversion, an 8-bit data word is clocked into the SDI input on the first eight rising SCK edges to select the MUX address and power down mode. The ADC enters acquisition mode on the falling edge of the sixth clock in the 8-bit data word and ends on the rising edge of the CONVST signal which also starts a conversion (see Figure 7). A minimum time of 4µs will provide enough time for the sample-and-hold capacitors to acquire the analog signal. Once a conversion cycle has begun, it cannot be restarted.

During the conversion, the internal differential 12-/14-/16-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). The input is successively compared with the binary weighted charges supplied by the differential capacitive DAC. Bit decisions are made by a high speed comparator. At the end of a conversion, the DAC output balances the analog input ($ADC^+ - ADC^-$). The SAR contents (a 12-/14-/16-bit data word) which represents the difference of ADC^+ and ADC^- are loaded into the 12-/14-/16-bit shift register.

DRIVING THE ANALOG INPUTS

The input range for the LTC1854/LTC1855/LTC1856 is ±10V and the MUX inputs are overvoltage protected to ±30V. The input impedance is typically 31kΩ; therefore, it should be driven with a low impedance source. Wideband noise coupling into the input can be minimized by placing a 3000pF capacitor at the input as shown in Figure 2. An NPO-type capacitor gives the lowest distortion. Place the capacitor as close to the device input pin as possible. If an amplifier is to be used to drive the input, care should be taken to select an amplifier with adequate accuracy, linearity and noise for the application. The following list is a summary of the op amps that are suitable for driving the LTC1854/LTC1855/LTC1856. More detailed information is available in the Linear Technology data books and online at www.linear.com.

LT®1007: Low noise precision amplifier. 2.7mA supply current ±5V to ±15V supplies. Gain bandwidth product 8MHz. DC applications.

APPLICATIONS INFORMATION

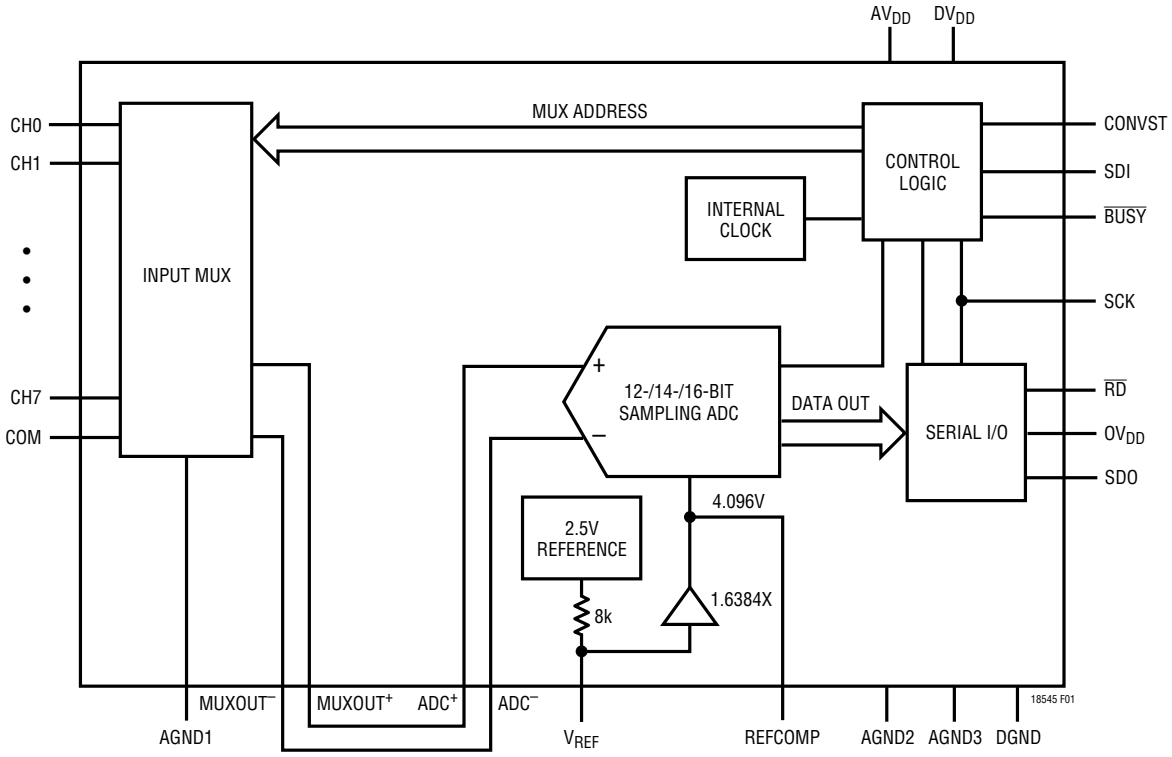


Figure 1. LTC1854/LTC1855/LTC1856 Simplified Equivalent Circuit

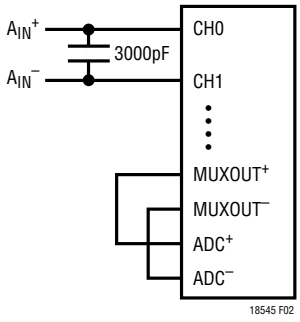


Figure 2. Analog Input Filtering

LT1227: 140MHz video current feedback amplifier. 10mA supply current. ±5V to ±15V supplies. Low noise and low distortion.

LT1468/LT1469: Single and dual 90MHz, 16-bit accurate op amp. Good AC/DC specs. ±5V to ±15V supplies.

LT1677: Single, low noise op amp. Rail-to-rail input and output. Up to ±15V supplies.

LT1792: Single, low noise JFET input op amp, ±5V supplies.

LT1793: Single, low noise JFET input op amp, 10pA bias current, ±5V supplies.

LT1881/LT1882: Dual and quad, 200pA bias current, rail-to-rail output op amps. Up to ±15V supplies.

LT1844/LT1885: Dual and quad, 400pA bias current, rail-to-rail output op amps. Up to ±15V supplies. Faster response and settling time.

INTERNAL VOLTAGE REFERENCE

The LTC1854/LTC1855/LTC1856 have an on-chip, temperature compensated, curvature corrected, bandgap reference, which is factory trimmed to 2.50V. The full-scale range of the LTC1854/LTC1855/LTC1856 is equal to ±10V. The output of the reference is connected to the input of a gain of 1.6384x buffer through an 8k resistor (see Figure 3). The input to the buffer or the output of the reference

APPLICATIONS INFORMATION

is available at V_{REF} (Pin 15). The internal reference can be overdriven with an external reference if more accuracy is needed. The buffer output drives the internal DAC and is available at REFCOMP (Pin 16). The REFCOMP pin can be used to drive a steady DC load of less than 2mA. Driving an AC load is not recommended because it can cause the performance of the converter to degrade.

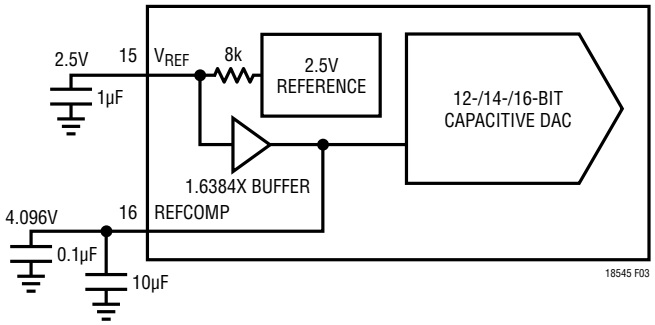


Figure 3. Internal or External Reference Source

For minimum code transition noise the V_{REF} pin and the REFCOMP pin should each be decoupled with a capacitor to filter wideband noise from the reference and the buffer.

FULL SCALE AND OFFSET

Figure 4 shows the ideal input/output characteristics for the LTC1856. The code transitions occur midway between successive integer LSB values (i.e., –FS+0.5LSB, –FS+1.5LSB, –FS+2.5LSB, … FS–1.5LSB, FS–0.5LSB). The output is two's complement binary with:

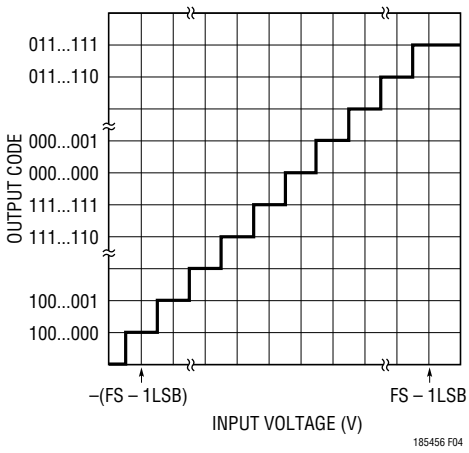


Figure 4. Bipolar Transfer Characteristics

$$1\,LSB = \frac{FS-(-FS)}{65566} = \frac{20V}{65536} = 305.2\mu V$$

In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero during a calibration sequence. Offset error must be adjusted before full-scale error. Zero offset is achieved by adjusting the offset applied to the "–" input. For single-ended inputs, this offset should be applied to the COM pin. For differential inputs, the "–" input is dictated by the MUX address.

For zero offset error, apply –0.5LSB to the "+" input and adjust the offset at the "–" input until the output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111 for the LTC1856, between 00 0000 0000 0000 and 11 1111 1111 1111 for the LTC1855 and between 0000 0000 0000 and 1111 1111 1111 for the LTC1854.

For full-scale adjustment, an input voltage of FS – 1.5LSBs should be applied to the "+" input and the appropriate reference adjusted until the output code flickers between 0111 1111 1111 1110 and 0111 1111 1111 1111 for the LTC1856, between 01 1111 1111 1110 and 01 1111 1111 1111 for the LTC1855 and between 0111 1111 1110 and 0111 1111 1111 for the LTC1854.

These adjustments as well as the factory trims affect all channels. The channel-to-channel offset and gain error matching are guaranteed by design to meet the specifications in the Converter Characteristics table.

APPLICATIONS INFORMATION

DC PERFORMANCE

One way of measuring the transition noise associated with a high resolution ADC is to use a technique where a DC signal is applied to the input of the MUX and the resulting output codes are collected over a large number of conversions. For example in Figure 5 the distribution of output code is shown for a DC input that has been digitized 4096 times. The distribution is Gaussian and the RMS code transition is about 1LSB for the LTC1856.

DIGITAL INTERFACE

Internal Clock

The ADC has an internal clock that is trimmed to achieve a typical conversion time of 4µs. No external adjustments are required and, with the maximum acquisition time of 4µs, throughput performance of 100ksps is assured.

3V Input/Output Compatible

The LTC1854/LTC1855/LTC1856 operate on a 5V supply, which makes the devices easy to interface to 5V digital systems. These devices can also interface to 3V digital systems: the digital input pins (SCK, SDI, CONVST and $\overline{RD}$) of the LTC1854/LTC1855/LTC1856 recognize 3V or 5V inputs. The LTC1854/LTC1855/LTC1856 have a dedicated output supply pin (OV_{DD}) that controls the output swings of the digital output pins (SDO, $\overline{BUSY}$) and allows the part to interface to either 3V or 5V digital systems. The SDO output is two's complement.

Timing and Control

Conversion start and data read are controlled by two digital inputs: CONVST and $\overline{RD}$. To start a conversion and put the sample-and-hold into the hold mode bring CONVST high for at least 40ns. Once initiated it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output, which goes low while the conversion is in progress.

Figures 6a and 6b show two different modes of operation for the LTC1856. For the 12-bit LTC1854 and 14-bit LTC1855, the last four and two bits of the SDO will output zeros, respectively. In mode 1 (Figure 6a), $\overline{RD}$ is tied low. The rising edge of CONVST starts the conversion. The data outputs are always enabled. The MSB of the data output is available after the conversion. In mode 2 (Figure 6b), CONVST and $\overline{RD}$ are tied together. The rising edge of the CONVST signal starts the conversion. Data outputs are in three-state at this time. When the conversion is complete ($\overline{BUSY}$ goes high), CONVST and $\overline{RD}$ go low to enable the data output for the previous conversion.

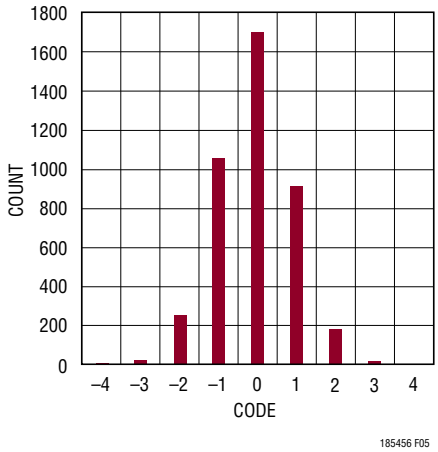


Figure 5. LTC1856 Histogram for 4096 Conversions

APPLICATIONS INFORMATION

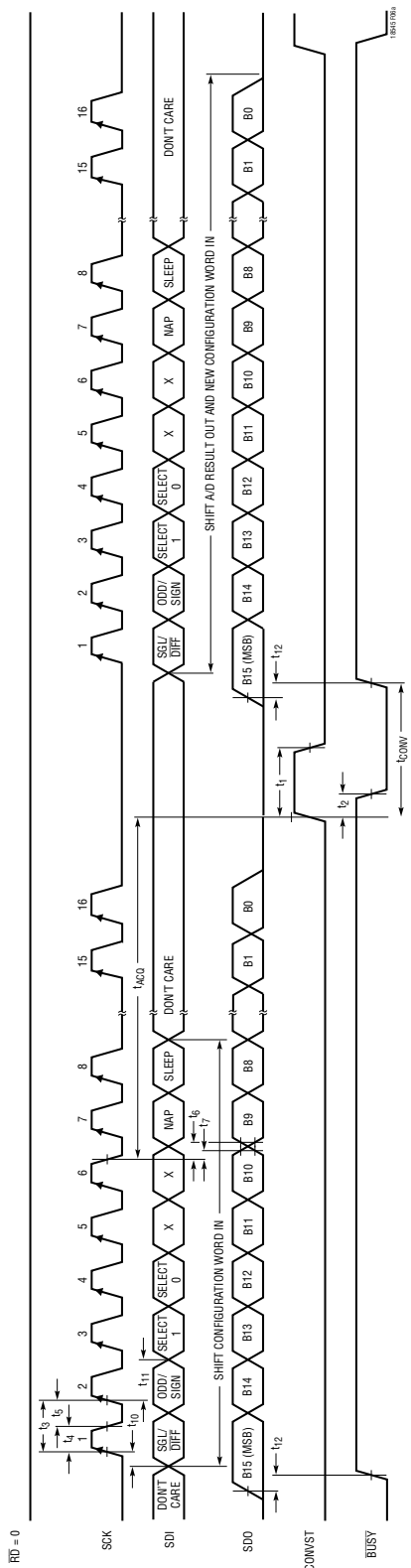


Figure 6a. Mode 1 for the LTC1856*. CONVST Starts a Conversion, Data Output is Always Enabled ($\overline{RD}$ = 0)

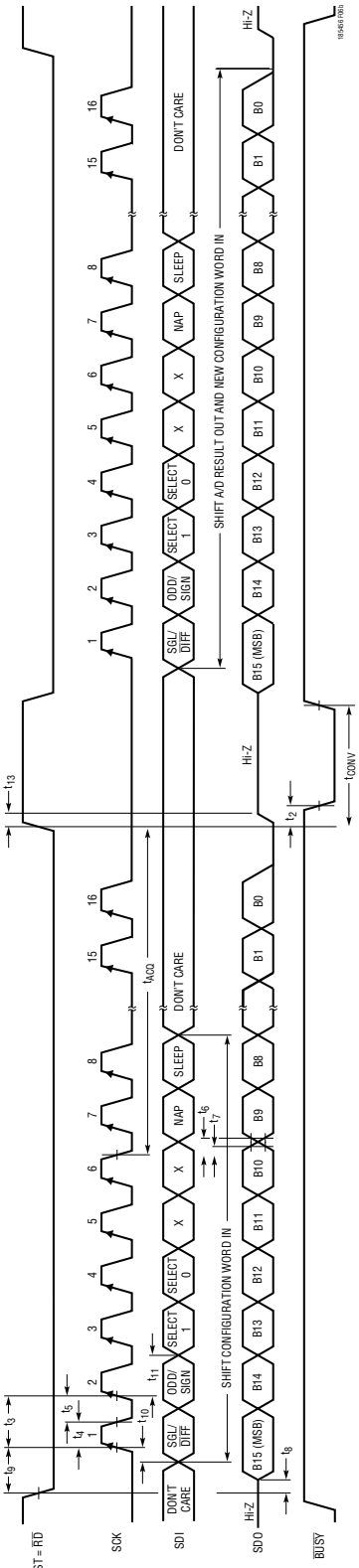


Figure 6b. Mode 2 for the LTC1856*. CONVST and $\overline{RD}$ Tied Together. CONVST Starts a Conversion, Data is Read by $\overline{RD}$

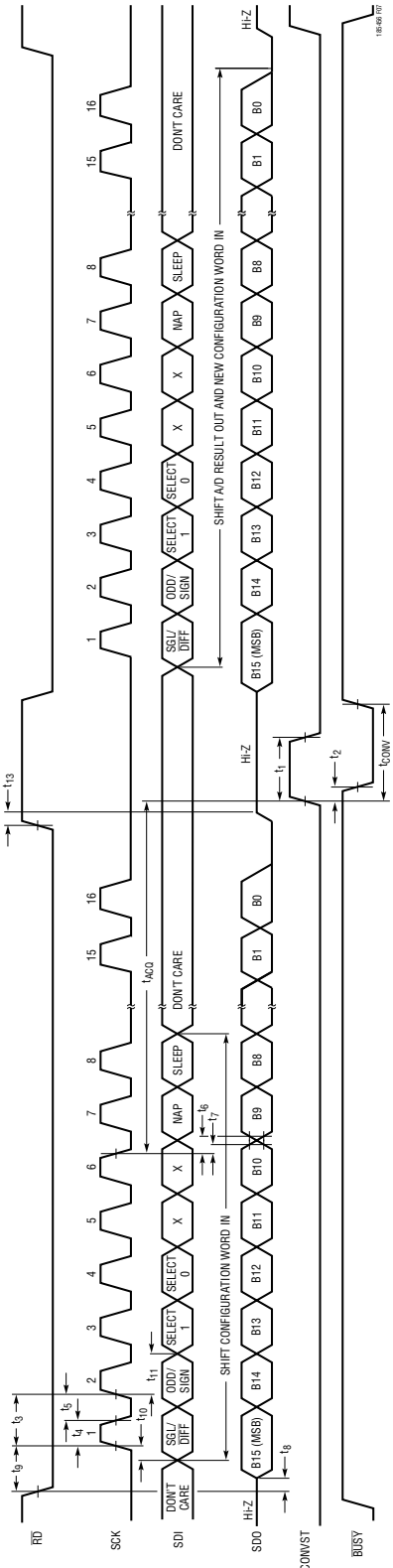


Figure 7. Operating Sequence for the LTC1856*

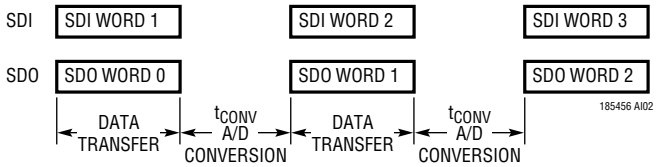
*For the 12-bit LTC1854 and the LTC1855 the last four and two bits of the SDO will output zeros, respectively.

APPLICATIONS INFORMATION

SERIAL DATA INPUT (SDI) INTERFACE

The LTC1854/LTC1855/LTC1856 communicate with microprocessors and other external circuitry via a synchronous, full duplex, 3-wire serial interface (see Figure 7). The shift clock (SCK) synchronizes the data transfer with each bit being transmitted on the falling SCK edge and captured on the rising SCK edge in both transmitting and receiving systems. The data is transmitted and received simultaneously (full duplex).

An 8-bit input word is shifted into the SDI input which configures the LTC1854/LTC1855/LTC1856 for the next conversion. Simultaneously, the result of the previous conversion is output on the SDO line. At the end of the data exchange the requested conversion begins by applying a rising edge on CONVST. After t_{CONV}, the conversion is complete and the results will be available on the next data transfer cycle. As shown below, the result of a conversion is delayed by one conversion from the input word requesting it.



INPUT DATA WORD

The LTC1854/LTC1855/LTC1856 8-bit data word is clocked into the SDI input on the first eight rising SCK edges. Further inputs on the SDI pin are then ignored until the next conversion. The eight bits of the input word are defined as follows:

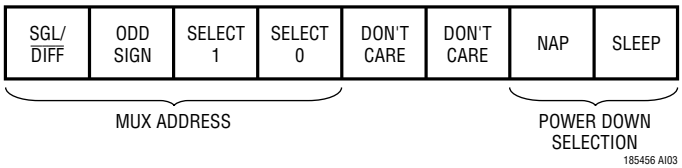


Table 1. Multiplexer Channel Selection

MUX ADDRESS			DIFFERENTIAL CHANNEL SELECTION								MUX ADDRESS			SINGLE-ENDED CHANNEL SELECTION							
SGL/DIFF	ODD SIGN	SELECT 1 0	0	1	2	3	4	5	6	7	SGL/DIFF	ODD SIGN	SELECT 1 0	0	1	2	3	4	5	6	7	COM
0	0	0 0	+	–							1	0	0 0	+								–
0	0	0 1			+	–					1	0	0 1			+						–
0	0	1 0					+	–			1	0	1 0					+				–
0	0	1 1							+	–	1	0	1 1							+		–
0	1	0 0	–	+							1	1	0 0		+							–
0	1	0 1			–	+					1	1	0 1				+					–
0	1	1 0					–	+			1	1	1 0						+			–
0	1	1 1							–	+	1	1	1 1								+	–

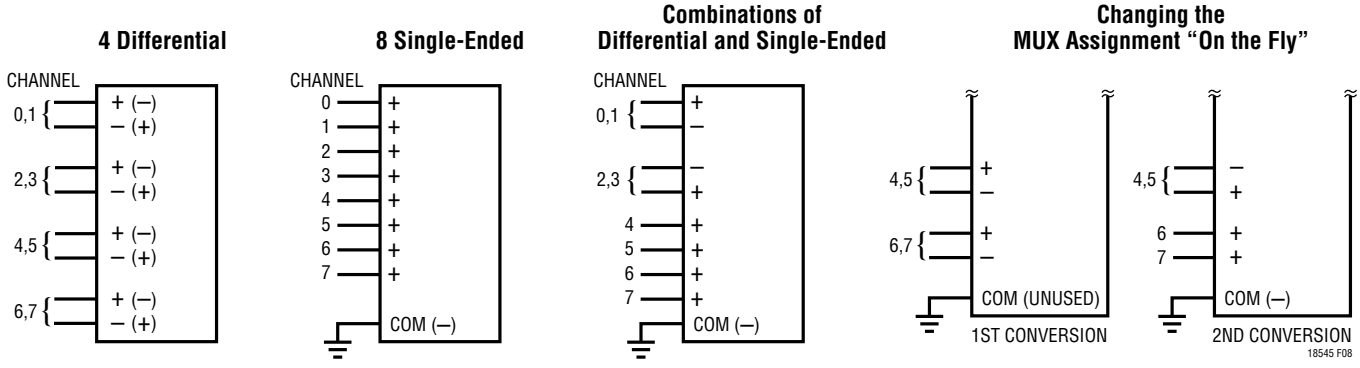


Figure 8. Examples of Multiplexer Options on the LTC1854/LTC1855/LTC1856

APPLICATIONS INFORMATION

MUX ADDRESS

The first four bits of the input word assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the + and – signs in the selected row of Table 1. Note that in differential mode (SGL/$\overline{DIFF}$ = 0) measurements are limited to four adjacent input pairs with either polarity. In single-ended mode, all input channels are measured with respect to COM. Both the "+" and "–" inputs are sampled simultaneously so common mode noise is rejected. Bits 5 and 6 of the input words are Don't Care bits.

POWER DOWN SELECTION (NAP, SLEEP)

The last two bits of the input word (Nap and Sleep) determine the power shutdown mode of the LTC1854/LTC1855/LTC1856. See Table 2. Nap mode is selected when Nap = 1 and Sleep = 0. The previous conversion result will be clocked out and a conversion will occur before entering the Nap mode. The Nap mode starts at the end of the conversion which is indicated by the rising edge of the $\overline{BUSY}$ signal. Nap mode lasts until the falling edge of the 2nd SCK (see Figure 9). Automatic nap will be achieved if Nap = 1 is selected each time an input word is written to the ADC.

Table 2. Power Down Selection

NAP	SLEEP	POWER DOWN MODE
0	0	Power On
1	0	Nap
X	1	Sleep

Sleep mode will occur when Sleep = 1 is selected, regardless of the selection of the Nap input. The previous conversion result can be clocked out and the Sleep mode will start on the falling edge of the last (16th) SCK. Notice that the CONVST should stay either high or low in sleep mode (see Figure 10). To wake up from the sleep mode, apply a rising edge on the CONVST signal and then apply Sleep = 0 on the next SDI word and the part will wake up on the falling edge of the last (16th) SCK (see Figure 11).

In Sleep mode, all bias currents are shut down and only the power on reset circuit and leakage currents (about 10µA) remain. Sleep mode wake-up time is dependent on the value of the capacitor connected to the REFCOMP (Pin 16). The wake-up time is typically 40ms with the recommended 10µF capacitor connected on the REFCOMP pin.

DYNAMIC PERFORMANCE

FFT (Fast Fourier Transform) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 12 shows a typical LTC1856 FFT plot which yields a SINAD of 87dB and THD of –101dB.

APPLICATIONS INFORMATION

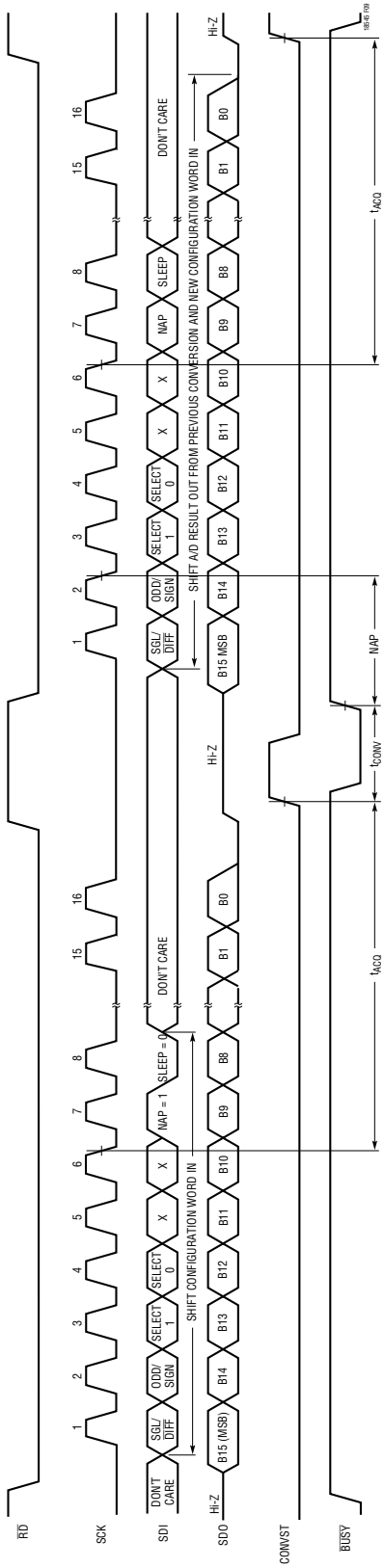


Figure 9. Nap Mode Operation for the LTC1856*

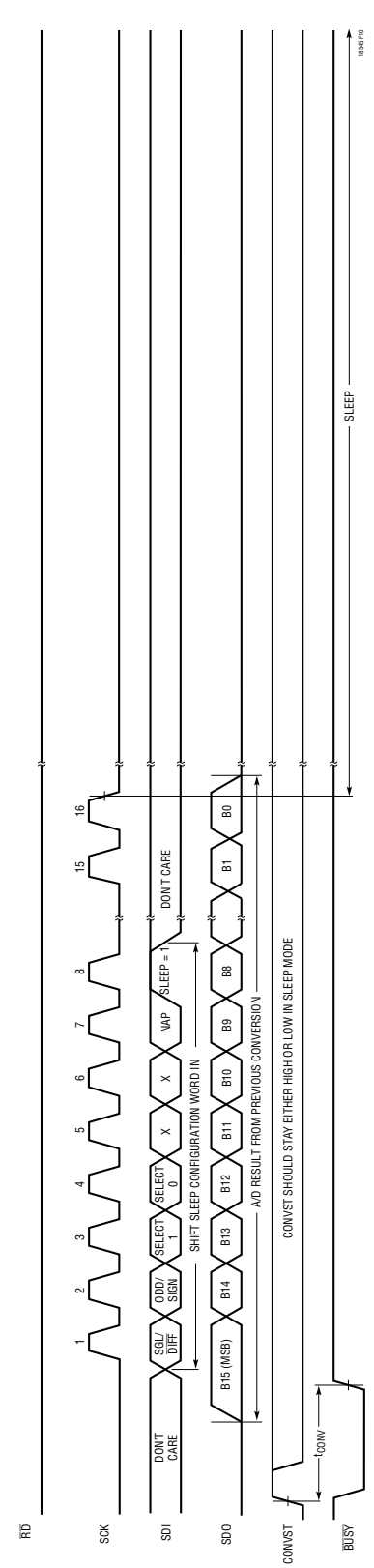


Figure 10. Sleep Mode Operation for the LTC1856*

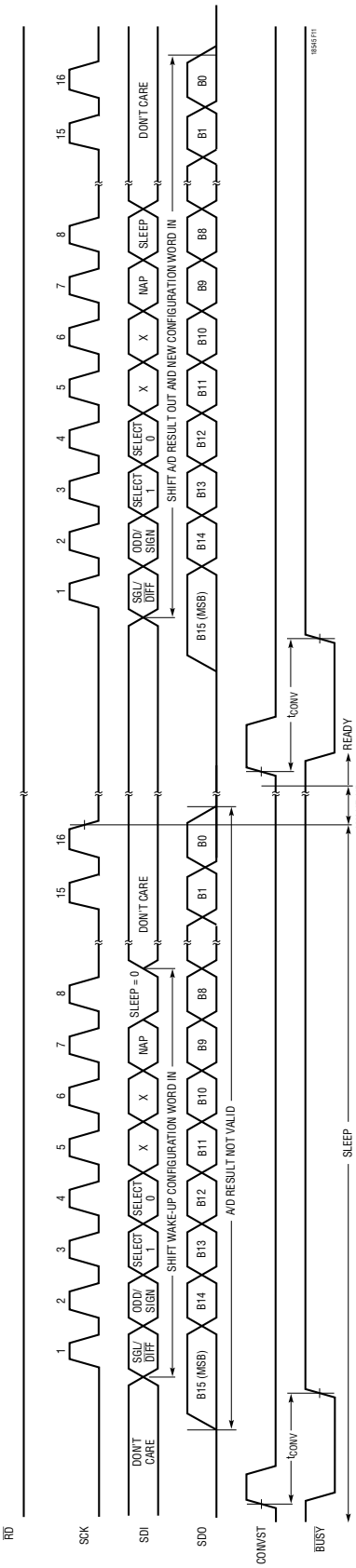


Figure 11. Wake Up from Sleep Mode for the LTC1856*

*For the 12-bit LTC1854 and the LTC1855 the last four and two bits of the SDO will output zeros, respectively.

APPLICATIONS INFORMATION

SIGNAL-TO-NOISE AND DISTORTION RATIO

The Signal-to-Noise and Distortion Ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from above DC and below half the sampling frequency. Figure 12 shows a typical SINAD of 87dB with a 100kHz sampling rate and a 1kHz input.

TOTAL HARMONIC DISTORTION

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 ... + V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through Nth harmonics.

BOARD LAYOUT, POWER SUPPLIES AND DECOUPLING

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1854/LTC1855/LTC1856, a printed circuit board is required. Layout for the printed circuit board should ensure the digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC. The analog input should be screened by AGND.

In applications where the MUX is connected to the ADC, it is possible to get noise coupling into the ADC from the trace connecting the MUXOUT to the ADC. Therefore, reducing the length of the traces connecting the MUXOUT pins (Pins 10, 11) to the ADC pins (Pins 12, 13) can minimize the problem. The unused MUX inputs should be grounded to prevent noise coupling into the inputs.

Figure 13 shows the power supply grounding that will help obtain the best performance from the 12-bit/14-bit/16-bit ADCs. Pay particular attention to the design of the analog and digital ground planes. The DGND pin of the LTC1854/

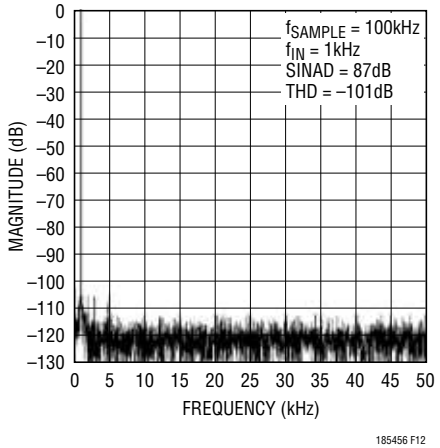


Figure 12. LTC1856 Nonaveraged 4096 Point FFT Plot

APPLICATIONS INFORMATION

LTC1855/LTC1856 can be tied to the analog ground plane. Placing the bypass capacitor as close as possible to the power supply pins, the reference and reference buffer output is very important. Low impedance common returns for these bypass capacitors are essential to low noise operation of the ADC, and the foil width for these tracks should be as wide as possible. Also, since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedance as much as possible. The digital output latches and the onboard sampling clock have been placed on the digital ground plane. The two ground planes are tied together at the ADC through a wide, low inductance path.

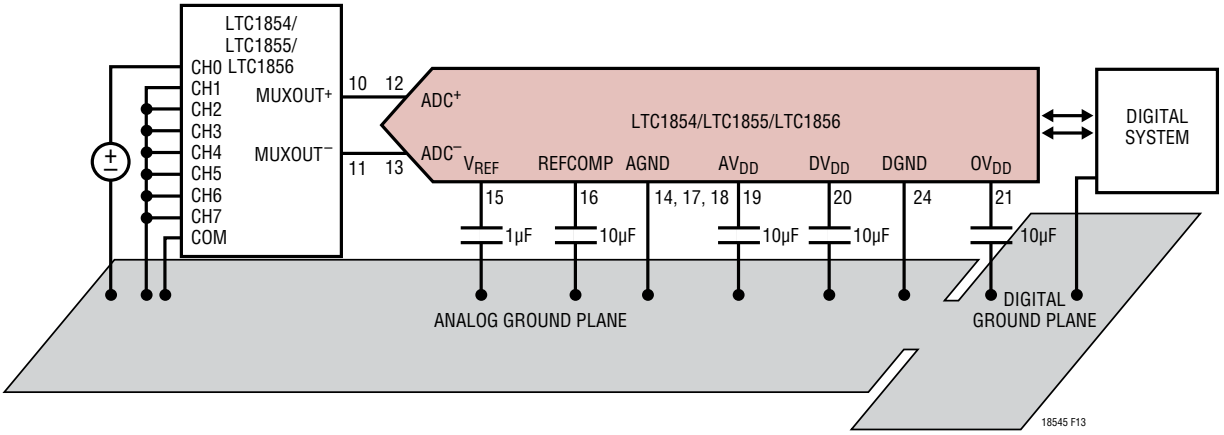
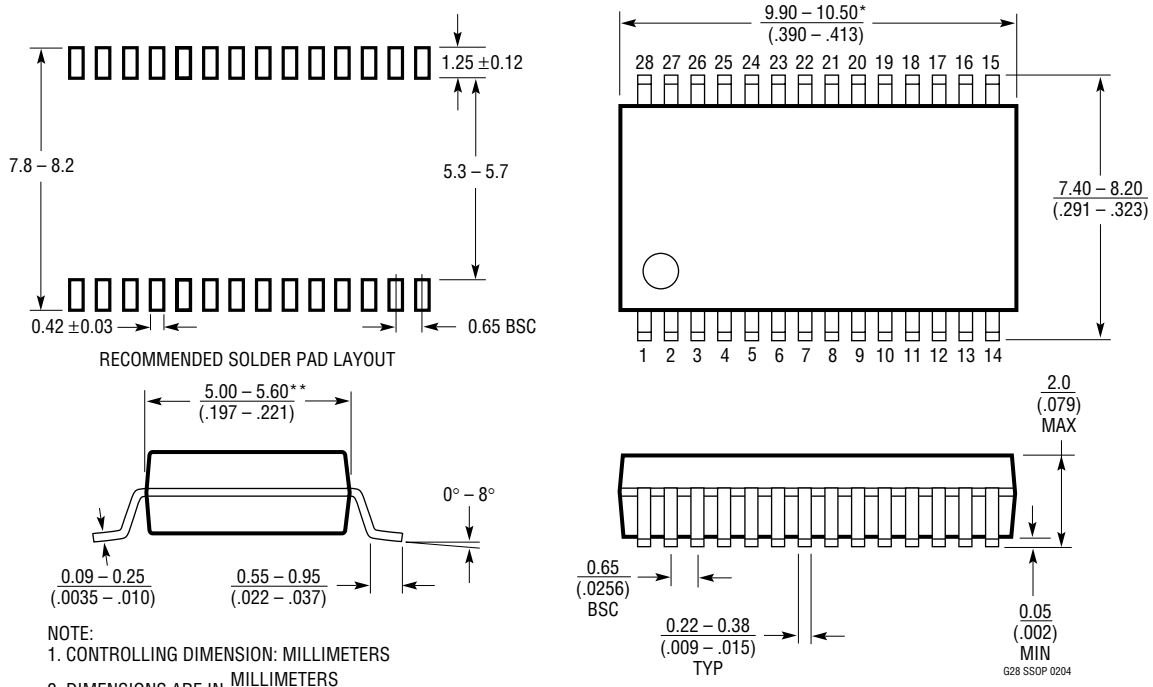


Figure 13. Power Supply Grounding Practice

PACKAGE DESCRIPTION

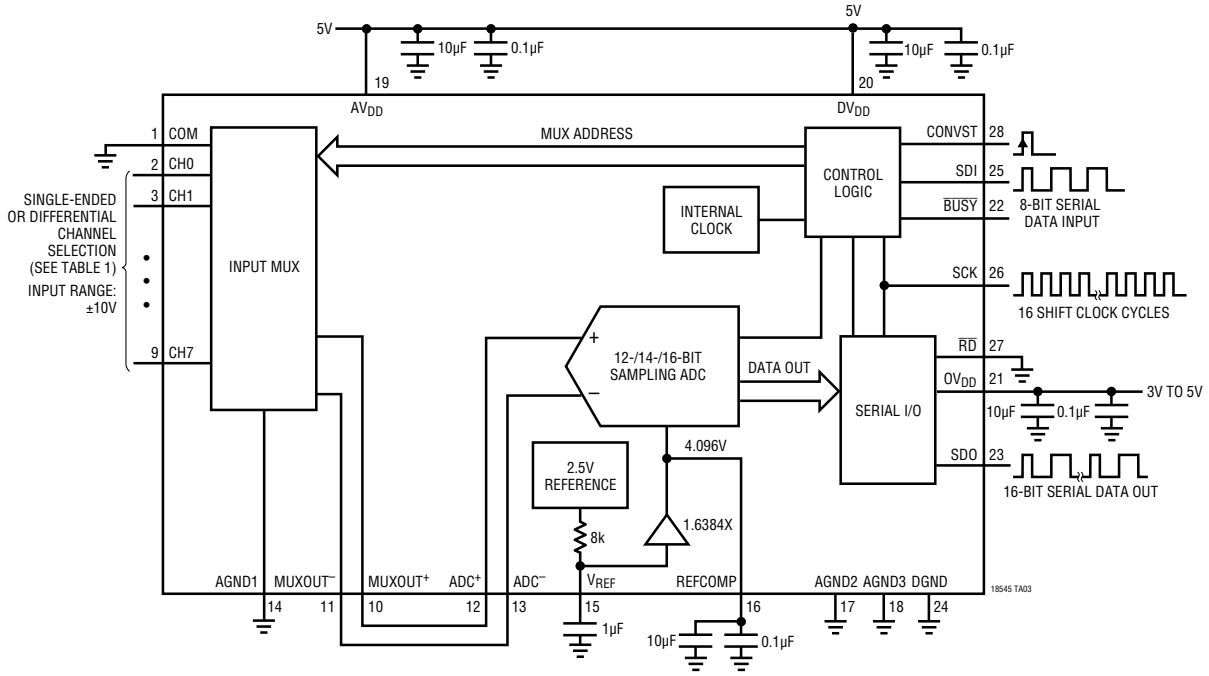
G Package
28-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

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TYPICAL APPLICATION



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Sampling ADCs		
LTC1418	14-Bit, 200ksps, Single 5V or ±5V ADC	15mW, Serial/Parallel I/O
LTC1604	16-Bit, 333ksps, ±5V ADC	90dB SINAD, 220mW Power Dissipation, Pin Compatible with LTC1608
LTC1605	16-Bit, 100ksps, Single 5V ADC	±10V Inputs, 55mW, Byte or Parallel I/O, Pin Compatible with LTC1606
LTC1606	16-Bit, 250ksps, Single 5V ADC	±10V Inputs, 75mW, Byte or Parallel I/O, Pin Compatible with LTC1605
LTC1608	16-Bit, 500ksps, ±5V ADC	90dB SINAD, 270mW Power Dissipation, Pin Compatible with LTC1604
LTC1609	16-Bit, 200ksps Serial ADC	Configurable Unipolar/Bipolar Input, Up to 10V Single 5V Supply
LTC1850/LTC1851	10-Bit/12-Bit, 8-Channel, 1.25Msps ADC	Programmable MUX and Sequencer, Parallel I/O
LTC1859/LTC1858/ LTC1857	16-Bit, 14-Bit, 12-Bit, 100ksps, SoftSpan ADCs	Software-Selectable Spans, Pin Compatible with
LTC1864/LTC1865	16-Bit, 1-/2-Channel, 250ksps ADC in MSOP	Single 5V Supply, 850µA with Autoshutdown
LTC1864L/LTC1865L	3V, 16-Bit, 1-/2-Channel, 150ksps ADC in MSOP	Single 3V Supply, 450µA with Autoshutdown LTC1856/LTC1855/LTC1854
DACs		
LTC1588/LTC1589 LTC1592	12-/14-/16-Bit, Serial, SoftSpan I_{OUT} DACs	Software-Selectable Spans, ±1LSB INL/DNL
LTC1595	16-Bit Serial Multiplying I_{OUT} DAC in SO-8	±1LSB Max INL/DNL, Low Glitch, DAC8043 16-Bit Upgrade
LTC1596	16-Bit Serial Multiplying I_{OUT} DAC	±1LSB Max INL/DNL, Low Glitch, AD7543/DAC8143 16-Bit Upgrade
LTC1597	16-Bit Parallel, Multiplying DAC	±1LSB Max INL/DNL, Low Glitch, 4 Quadrant Resistors
LTC1650	16-Bit Serial V_{OUT} ±5V DAC	Low Power, Low Glitch, 4-Quadrant Multiplication
LTC2704-16/ LTC2704-14/ LTC2704-12	16-Bit, 14-Bit, 12-Bit, Serial, Quad SoftSpan V_{OUT} DACs	Software-Selectable Spans, ±2LSB INL, ±1LSB INL, Force/Sense Output

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