MIC68400

4A Sequencing LDO with Tracking and Ramp Control

Features

- Stable with 10 µF Ceramic Capacitor
- Input Voltage Range: 1.65V to 5.5V
- 0.5V Reference
- ±2.0% Output Tolerance over Temperature
- 4A Maximum Output Current – Peak Start-Up
- 3A Continuous Operating Current
- Tracking on Turn-On and Turn-Off with Pin Strapping
- Timing Controlled Sequencing On/Off
- Programmable Ramp Control for In-Rush Current Limiting and Slew Rate Control of the Output Voltage During Turn-On and Turn-Off
- Power-On Reset (POR) Supervisor with Programmable Delay Time
- Single Master can Control Multiple Slave Regulators with Tracking Output Voltages
- Tiny 4 mm x 4 mm QFN Package
- Maximum Dropout ($V_{IN} – V_{OUT}$) of 500 mV over Temperature at 3A Output Current
- Fixed and Adjustable Output Voltages
- Excellent Line and Load Regulation Specifications
- Logic Controlled Shutdown
- Thermal Shutdown and Current-Limit Protection

Applications

- FPGA/PLD Power Supply
- Networking/Telecom Equipment
- Microprocessor Core Voltage
- High Efficiency Linear Post Regulator
- Sequenced or Tracked Power Supply

General Description

The MIC68400 is a high peak current LDO regulator designed specifically for powering applications such as FPGA core voltages that require high start up current with lower nominal operating current. Capable of sourcing 4A of current for start-up, the MIC68400 provides high power from a small QFN leadless package. The MIC68400 can also implement a variety of power-up and power-down protocols such as sequencing, tracking, and ratiometric tracking.

The MIC68400 operates from a wide input range of 1.65V to 5.5V, which includes all of the main supply voltages commonly available today. It is designed to drive digital circuits requiring low voltage at high currents (i.e. PLDs, DSP, microcontroller, etc.). The MIC68400 incorporates a delay pin (Delay) for control of power on reset output (POR) at turn-on and power-down delay at turn-off. In addition there is a ramp control pin (RC) for either tracking applications or output voltage slew rate adjustment at turn-on and turn-off. This is important in applications where the load is highly capacitive and in-rush currents can cause supply voltages to fail and microprocessors or other complex logic chips to hang up.

Multiple MIC68400s can be daisy chained in two modes. In tracking mode the output voltage of the Master drives the RC pin of a Slave so that the Slave tracks the main regulator during turn-on and turn-off. In sequencing mode the POR of the Master drives the enable (EN) of the Slave so that it turns on after the Master and turns off before (or after) the Master. This behavior is critical for power-up and power-down control in multi-output power supplies. The MIC68400 is fully protected offering both thermal, current limit protection, and reverse current protection.

The MIC68400 has a junction temperature range of –40°C to +125°C and is available in fixed as well as an adjustable option. The MIC68400 is offered in the tiny 16-pin 4 mm x 4 mm QFN package.

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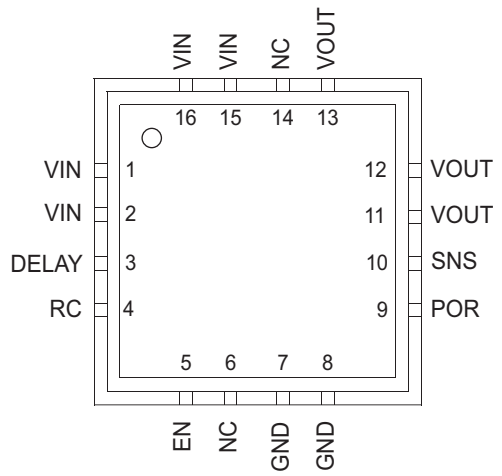
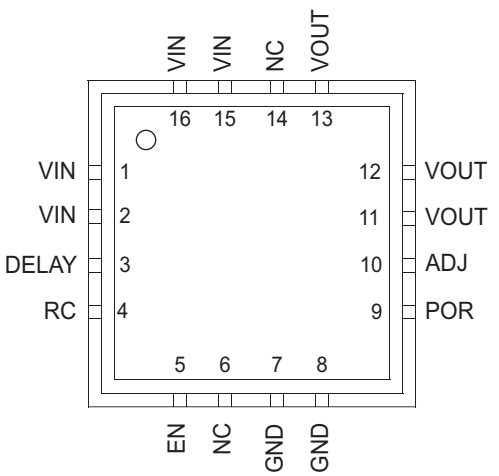
Package Types

MIC68400, FIXED VOLTAGES
16-Lead QFN (ML)

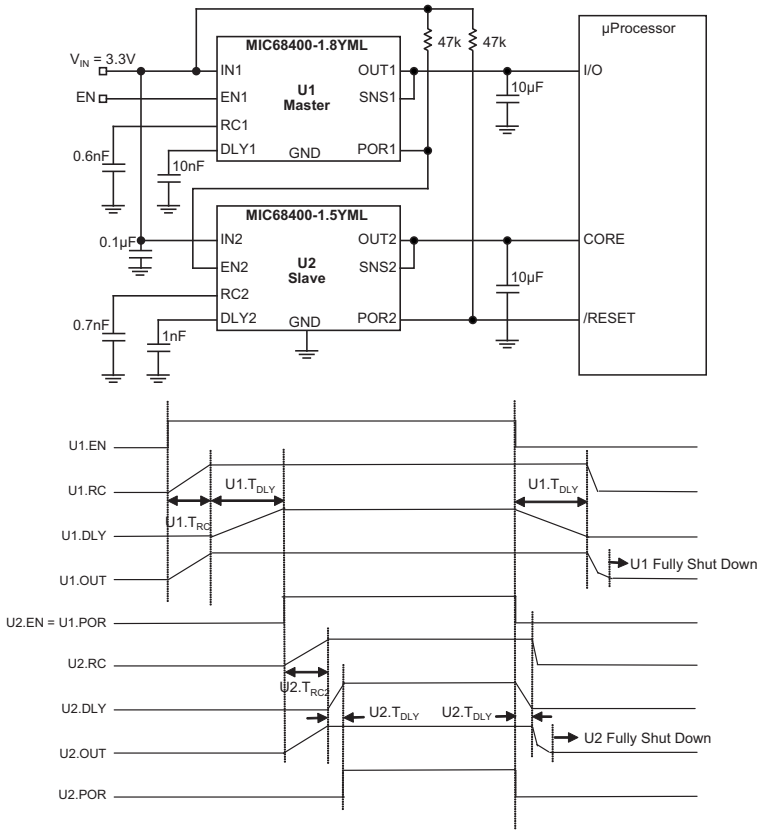


MIC68400, ADJ. VOLTAGES
16-Lead QFN (ML)



Typical Application Circuits

MIC68400
Sequenced Dual Power Supply for I/O and Core Voltage of µProcessor



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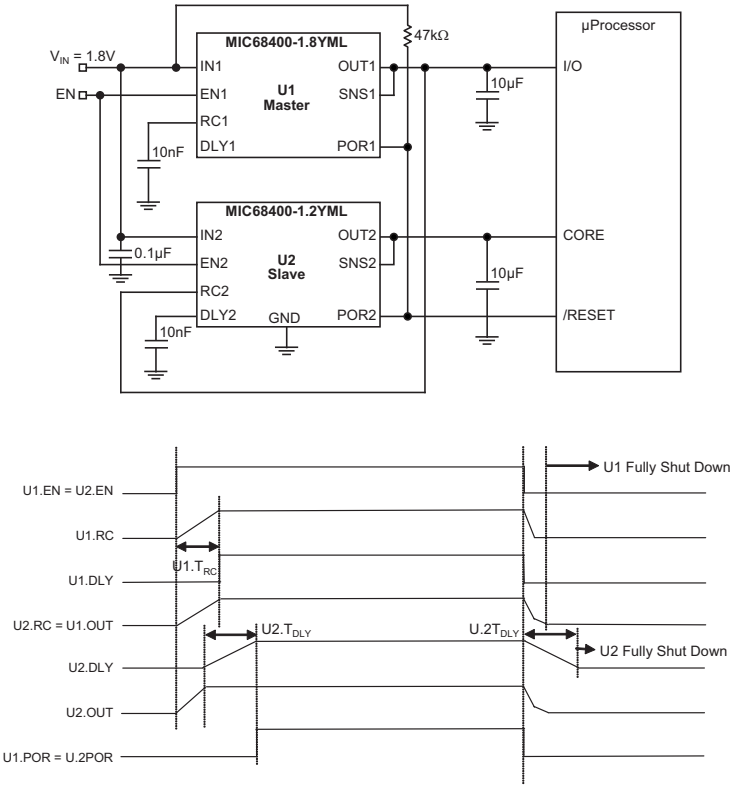
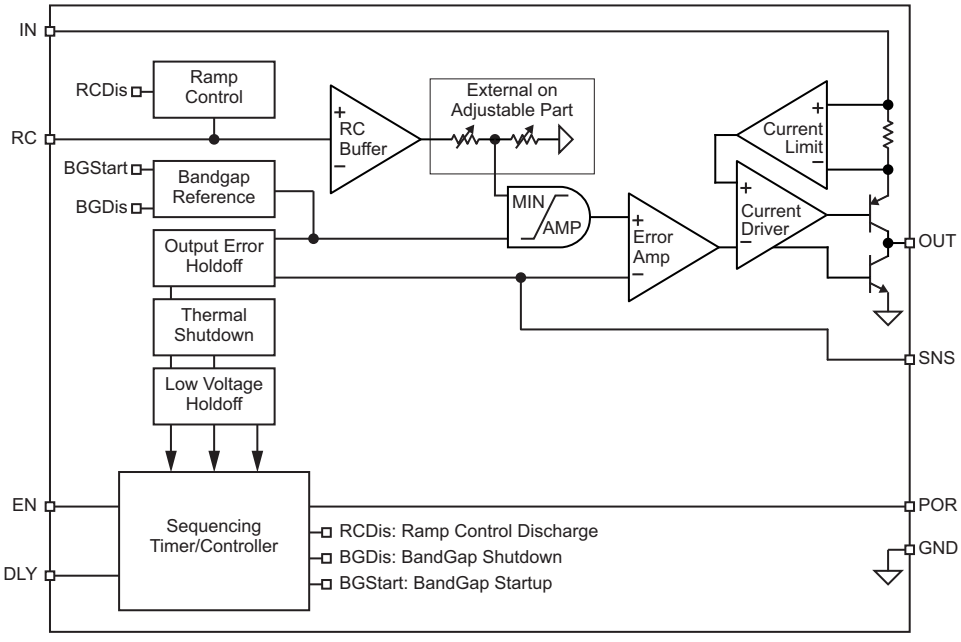
Typical Application Circuits (Continued)

MIC68400

Tracking Dual Power Supply for I/O and Core Voltage of µProcessor



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{IN}) ..... +6V
Enable Input Voltage (V_{EN}) ..... +6V
POR (V_{POR}) ..... V_{IN} + 0.3V
RC ..... V_{IN} + 0.3V
Power Dissipation (P_D), (Note 1) ..... Internally Limited

Operating Ratings ‡

Supply Voltage (V_{IN}) ..... +1.65V to +5.5V
Enable Input Voltage (V_{EN}) ..... 0V to V_{IN}
Ramp Control (V_{RC}) ..... 0V to +5.5V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: The maximum allowable power dissipation of any T_A (ambient temperature) is $P_{D(MAX)} = T_{J(MAX)} – T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Characteristics: T_A = +25°C with $V_{IN} = V_{OUT}$ + 1V; $V_{EN} = V_{IN}$; I_{OUT} = 10 mA; **bold** values indicate –40°C ≤ T_J ≤ +125°C, unless noted. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Voltage Accuracy		**–2**	—	**2**	%	10 mA < I_{OUT} < $I_{L(MAX)}$, V_{OUT} + 1 ≤ V_{IN} ≤ 5.5V
Feedback Voltage	V_{FB}	**0.49**	0.50	**0.51**	V	Adjustable version only
Feedback Current	I_{FB}	—	20	—	nA	Adjustable version only
Output Voltage Line Regulation		—	0.06	**0.5**	%	$V_{IN} = V_{OUT}$ + 1V to 5.0V
Output Voltage Load Regulation		—	0.5	**1**	%	I_L = 10 mA to 3A
$V_{IN} – V_O$; Dropout Voltage		—	—	**400**	mV	I_L = 1.5A
		—	300	**500**		I_L = 3.0A
		—	360	**800**		I_L = 4.0A
Ground Pin Current	I_{GND}	—	1.2	—	mA	I_L = 10 mA
		—	20	—		I_L = 1.5A
		—	55	—		I_L = 3.0A
		—	90	**130**		I_L = 4.0A
Shutdown Current	I_{SHDN}	—	0.01	**10**	µA	V_{EN} = 0V; V_{OUT} = 0V
Current Limit	I_{LIMIT}	**4.0**	6.0	—	A	V_{OUT} = 0V; V_{IN} = 3.0V
Start-Up Time	t_{SU}	—	35	**150**	µs	$V_{EN} = V_{IN}$; CRC = Open
Enable Input						
Enable Input Threshold		**1**	—	—	V	Regulator enable
		—	—	**0.2**		Regulator shutdown
Enable Hysteresis		**20**	120	**200**	mV	—

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TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: T_A = +25°C with V_{IN} = V_{OUT} + 1V; V_{EN} = V_{IN}; I_{OUT} = 10 mA; **bold** values indicate –40°C ≤ T_J ≤ +125°C, unless noted. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Enable Input Current		—	0.02	—	µA	V_{IL} ≤ 0.2V (Regulator shutdown)
		—	3	—		V_{IH} ≥ 1V (Regulator enable)
POR Output						
POR Leakage Current	$I_{POR(LEAK)}$	—	—	1	µA	V_{POR} = 5.5V; POR = High
		—	—	**2**		
	$V_{POR(LO)}$	—	60	**90**	mV	Output Logic-Low Voltage (undervoltage condition), I_{POR} = 1 mA
	V_{POR}	7.5	10	12.5	%	V_{OUT} Ramping Up, Threshold, Percent of V_{OUT} below nominal
		10	12.5	15		V_{OUT} Ramping Down, Threshold, Percent of V_{OUT} below nominal
		—	3	—		Hysteresis
Delay Current	I_{DELAY}	**0.7**	1	**1.3**	µA	V_{DELAY} = 0.75V
Delay Voltage (Note 2)	V_{DELAY}	**1.185**	1.235	**1.285**	V	V_{POR} = High
Ramp Control						
Ramp Control Current	I_{RC}	**0.7**	1	**1.3**	µA	V_{RC} = 0.75V
Output Discharge Current (Note 3)	$I_{DC(OUT)}$	25	45	70	mA	V_{OUT} = 0.5V_{NOM}, V_{RAMP} =0V
Fixed Tracking Accuracy (Note 4)		–50	25	100	mV	200 mV < V_{RC} < V_{TARGET}; Measure (V_{OUT} – V_{RC})
Adjustable Tracking Accuracy (Note 4)		–10	15	50	mV	Measure (V_{OUT} – V_{RC} x (V_{TARGET}/500 mV))

Note 1: Specification for packaged product only.

2: Timer High Voltage along with Delay pin current (1 µA nom.) determines the delay per µF of capacitance. Typical delay is 1.1 sec/µF.

3: Discharge current is the current drawn from the output to ground to actively discharge the output capacitor during the shutdown process.

4: V_{TARGET} is the output voltage of an adjustable with customer resistor divider installed between V_{OUT} and ADJ/SNS pin, or the rated output voltage of a fixed device.

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TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature Range	T_J	–40	—	+125	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Package Thermal Resistances						
Thermal Resistance 16-LD 4x4 QFN	θ_{JA}	—	30	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

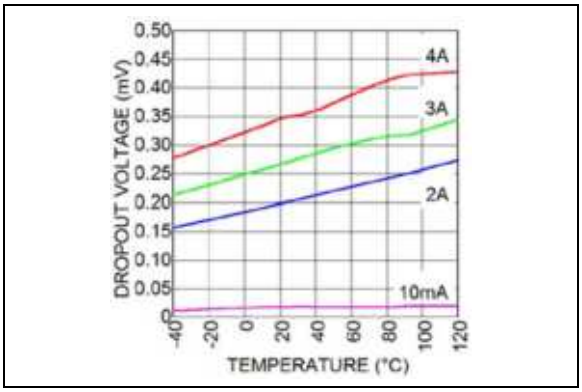

FIGURE 2-1: *Dropout Voltage vs. Temperature.*

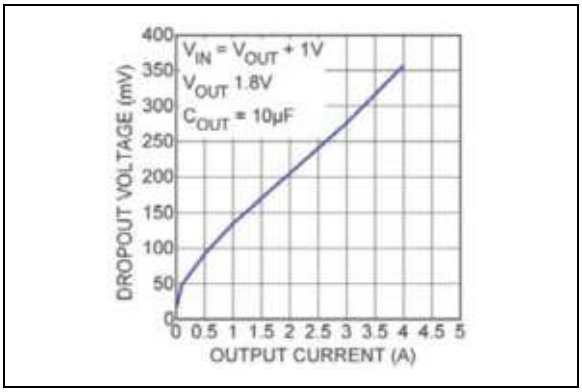

FIGURE 2-4: *Dropout Voltage vs. Output Current.*

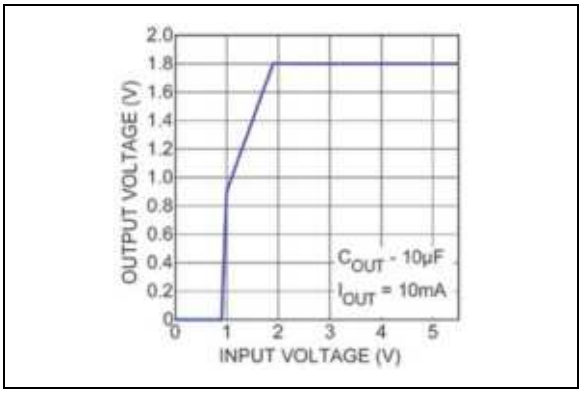

FIGURE 2-2: *Output Voltage vs. Input Voltage.*

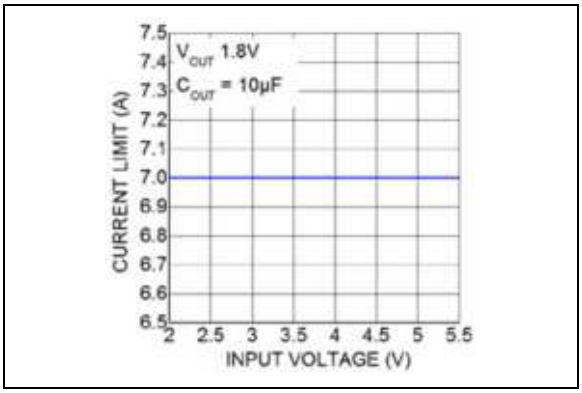

FIGURE 2-5: *Current Limit vs. Input Voltage.*

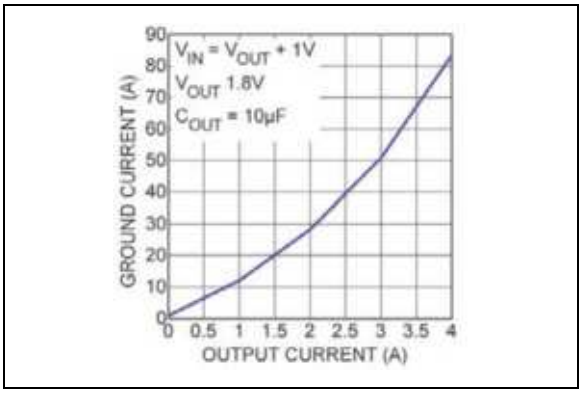

FIGURE 2-3: *Ground Current vs. Output Current.*

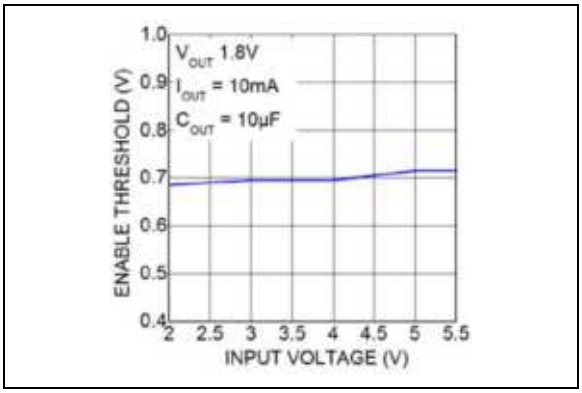

FIGURE 2-6: *Enable Threshold vs. Input Voltage.*

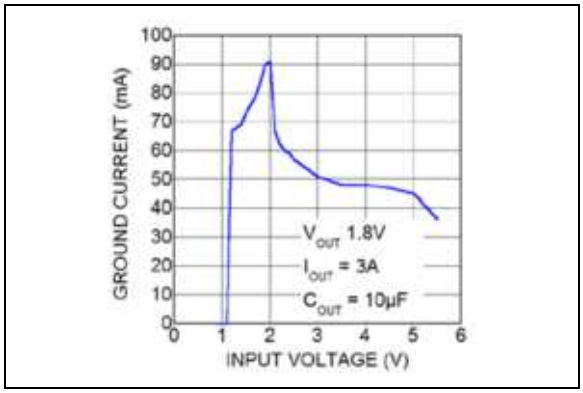

FIGURE 2-7: *Ground Current vs. Input Voltage.*

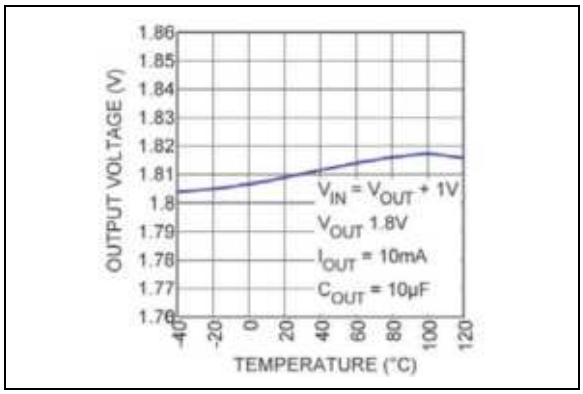

FIGURE 2-8: *Output Voltage vs. Temperature.*

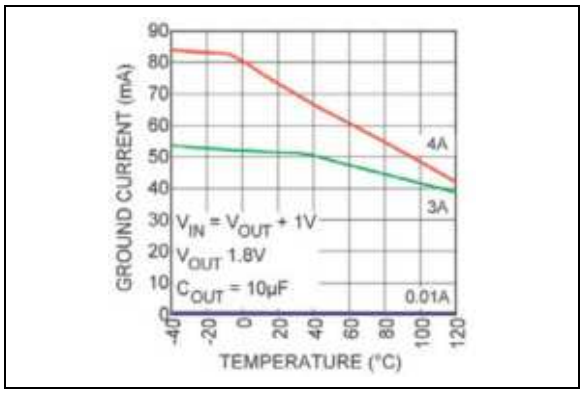

FIGURE 2-9: *Ground Current vs. Temperature.*

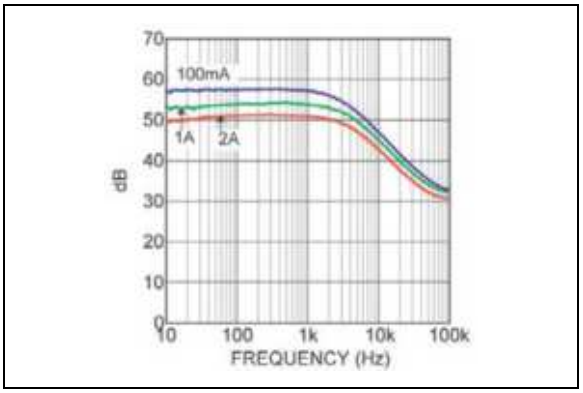

FIGURE 2-10: *Power Supply Rejection Ratio.*

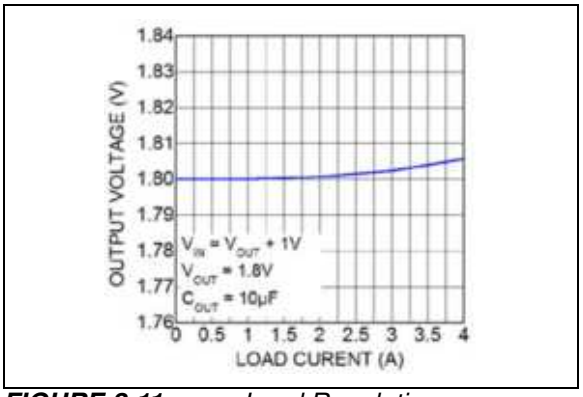

FIGURE 2-11: *Load Regulation.*

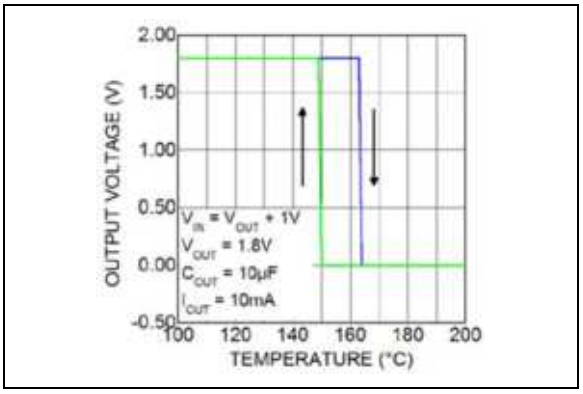

FIGURE 2-12: *Thermal Shutdown.*

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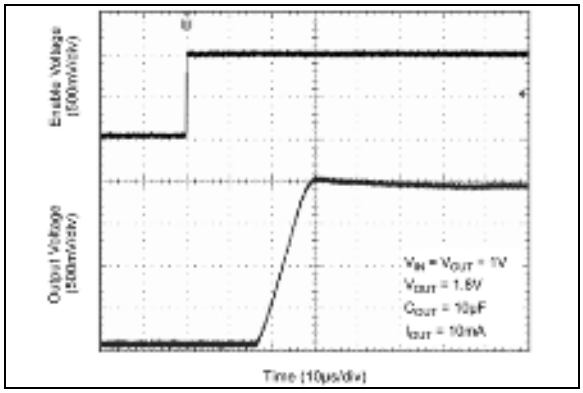

FIGURE 2-13: *Enable Turn-On.*

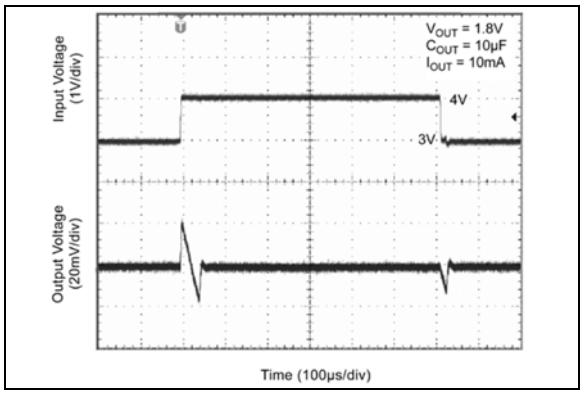

FIGURE 2-14: *Line Transient.*

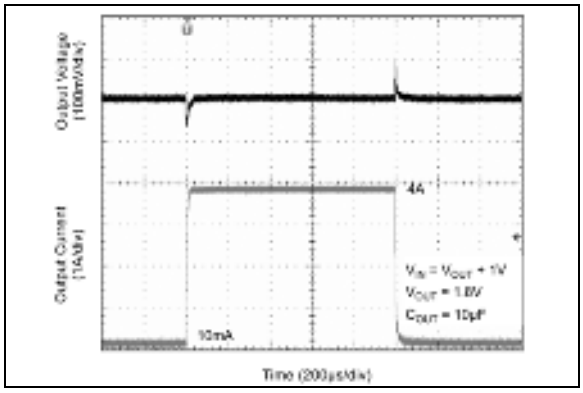

FIGURE 2-15: *Load Transient.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1, 2, 15, 16	V_{IN}	Input: Input voltage supply pin. Place a capacitor to ground to bypass the input supply.
3	DELAY	Delay: Capacitor to ground sets internal delay timer. Timer delays power-on reset (POR) output at turn-on, and ramp down at turn-off.
4	RC	Ramp Control: May be voltage driven for tracking applications or a capacitor to ground will set the slew rate of output voltage during start-up.
5	EN	Enable (Input): CMOS compatible input. Logic-high = enable, logic-low = shutdown.
6, 14	NC	Not internally connected.
7, 8, Tab	GND	Ground.
9	POR	Power-on Reset: Open-drain output device indicates when the output is in regulation. High (open) means device is regulating within 10%. POR onset can be delayed using a single capacitor from Delay to ground.
10 (Fixed)	SNS	Output Voltage Sense Pin: Connect directly to output pin.
10 (Adj.)	ADJ	Adjustable regulators: Feedback input. Connect to resistor voltage divider.
11, 12, 13	V_{OUT}	Output Voltage: Output of voltage regulator. Place capacitor to ground to bypass the output voltage. Minimum load current is 100 µA. Nominal bypass capacitor is 10 µF.

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4.0 APPLICATION INFORMATION

4.1 Enable Input

The MIC68400 features a TTL/CMOS-compatible positive logic enable input for on/off control of the device. High (>1V) enables the regulator while low (<0.2V) disables the regulator. In shutdown, the regulator consumes very little current (only a few microamps of leakage). For simple applications, the enable (EN) can be connected to V_{IN} (IN). While MIC68400 only requires a few microamps of enable current to turn on, the actual enable pin current will depend on the overdrive (enable voltage exceeding 1V) in each particular application.

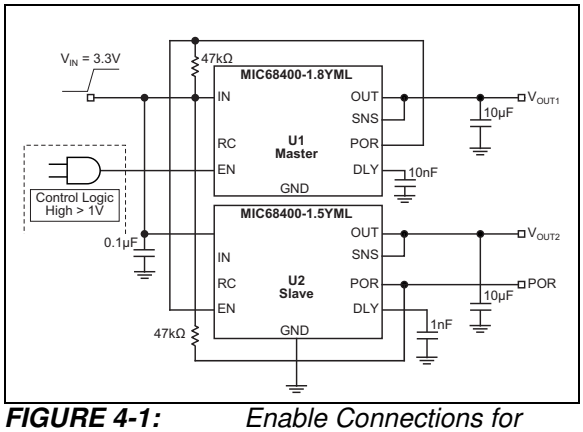

FIGURE 4-1: *Enable Connections for Logic-Driven Input.*

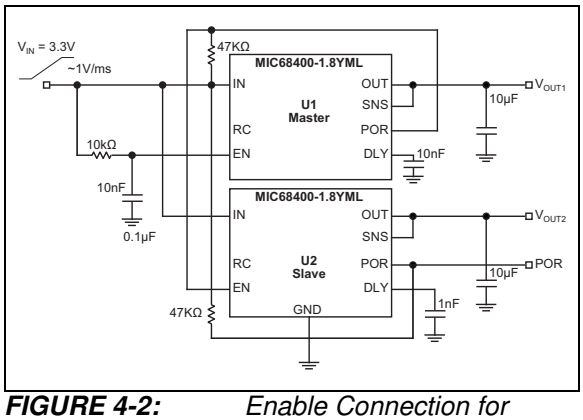

FIGURE 4-2: *Enable Connection for V_{IN}-Driven and/or Slow Rise Time Inputs.*

If MIC68400 is used in standalone mode, it is not recommended to connect the enable (EN) pin to the input voltage supply (IN). In this case, the enable (EN) input should be externally controlled, as indicated in the Electrical Characteristics section (regulator enable for V_{EN} > 1.0V and regulator disable for V_{EN} < 0.2V).

4.2 Input Capacitor

An input capacitor of 0.1 µF or greater is recommended when the device is more than four inches away from the bulk supply capacitance, or when the supply is a battery. Small, surface-mount chip capacitors can be used for bypassing. The capacitor should be placed within one inch of the device for optimal performance. Larger values will help to improve ripple rejection by bypassing the regulator input, further improving the integrity of the output voltage.

4.3 Output Capacitor

The MIC68400 requires an output capacitor for stable operation. As a µCap LDO, the MIC68220 can operate with ceramic output capacitors of 10 µF or greater with ESR's ranging from 3 mΩ to over 300 mΩ. Values greater than 10 µF improve transient response and noise reduction at high frequencies. X7R/X5R dielectric-type ceramic capacitors are recommended because of their superior temperature performance. X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Larger output capacitances can be achieved by placing tantalum or aluminum electrolytics in parallel with the ceramic capacitor. For example, a 100 µF electrolytic in parallel with a 10 µF ceramic can provide the transient and high frequency noise performance of a 100 µF ceramic at a significantly lower cost. Specific undershoot/overshoot performance will depend on both the values and ESR/ESL of the capacitors.

4.4 Adjustable Regulator Design

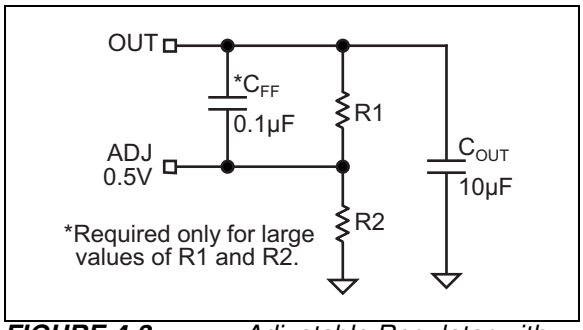

FIGURE 4-3: *Adjustable Regulator with Resistors.*

The adjustable MIC68400 output voltage can be programmed from 0.5V to 5.5V using a resistor divider from output to the SNS pin. Resistors can be quite large, up to 1 MΩ because of the very high input impedance and low bias current of the sense amplifier. Typical sense input currents are less than 30 nA which causes less than 0.3% error with R1 and R2 less than or equal to 100 kΩ. For large value resistors (>50 kΩ)

R1 should be bypassed by a small capacitor (C_{FF} = 0.1 µF bypass capacitor) to avoid instability due to phase lag at the ADJ/SNS input.

The output resistor divider values are calculated by:

EQUATION 4-1:

$$V_{OUT} = 0.5V\left(\frac{R1}{R2} + 1\right)$$

4.5 Power on Reset (POR) and Delay (DLY)

The power-on reset output (POR) is an open-drain N-Channel device requiring a pull-up resistor to either the input voltage or output voltage for proper voltage levels. POR is driven by the internal timer so that the release of POR at turn-on can be delayed for as much as one second. POR is always pulled low when enable (EN) is pulled low or the output goes out of regulation by more than 10% due to loading conditions.

The internal timer is controlled by the DLY pin which has a bidirectional current source and two limiting comparators. A capacitor connected from DLY to GND sets the delay time for two functions. On start up, DLY sets the time from the nominal output voltage is reached to the release of the POR. At shut down, the delay sets the time from disable (EN pin driven low) to actual ramp down of the output voltage. The current source is ±1 µA, which charges the capacitor from ~150 mV (nominal disabled DLY voltage) to ~1.25V. At turn on, the DLY cap begins to charge when the output voltage reaches 90% of the target value. When the capacitor reaches 1.25V, the output of the POR is released to go high. At turn off, the DLY cap begins to discharge when the EN is driven low. When the cap reaches ~150 mV the output is ramped down. Both delays are nominally the same, and are calculated by the same formula:

EQUATION 4-2:

$$t_{DLY} = (1.1)\left(\frac{C_{DLY}}{1\mu A}\right)$$

The scale factor is 1.1 seconds/µF, 1.1 ms/nF, or 1.1 µs/pF. t_{DLYOFF} is the time from lowering of EN to the start of ramp down on the off cycle. T_{POR} is the time from the rising of EN to the release (low to high edge) of the POR. This behavior means that a µProcessor or other complex logic system is guaranteed that the nominal output voltage is stable for a known time before the POR is released, and they are further guaranteed that once POR is pulled low, they have a known time to 'tidy up' memory or other registers for a well-controlled shutdown. In Master/Slave configurations, the timers can be used to ensure that the Master is always accurately regulating when the Slave is on.

4.6 Ramp Control

The ramp control (RC) has a bidirectional current source and a sense amplifier, which together are used to control the voltage at the output. When RC is below the target voltage (nominal output voltage for fixed voltage parts, 0.5V for adjustable parts) the RC pin controls the output voltage. When RC is at or above the target voltage, the output is controlled by the internal regulator.

4.6.1 TRACKING APPLICATIONS: DRIVING RC FROM A VOLTAGE SOURCE

Fixed Parts: If RC is driven from another (Master) regulator the two outputs will track each other until the Master exceeds the target voltage of the Slave regulator. Typically the output of the MIC68400 will track above the RC input by 30 mV to 70 mV. This offset is designed to allow Master/Slave tracking of same-voltage regulators. Without the offset, same-voltage Master/Slave configurations could suffer poor regulation.

Adjustable Parts: The RC pin on adjustable versions operates from 0V to 0.5V. To implement tracking on an adjustable version, an external resistor divider must be used. This divider is the nearly same ratio as the voltage setting divider used to drive the SNS/ADJ pin. It is recommended that the ratio be adjusted to track ~50 mV (2% to 3%) above the target voltage if the Master and Slave are operating at the same target voltage.

4.6.2 RAMP UP: CAP-CONTROLLED SLEW RATE

If a capacitor is connected to RC, the bidirectional current source will charge the cap during startup and discharge the cap during shutdown. The size of the capacitor and the RC current (1 µA nom.) control the slew rate of the output voltage during startup. For example, to ramp up a 1.8V regulator from zero to full output in 10 ms requires a 5.6 nF capacitor.

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For Fixed Versions:

EQUATION 4-3:

$$t_{RC} = V_{OUT}\left(\frac{C_{RC}}{1\mu A}\right) \qquad SR_{ON} = \left(\frac{1\mu A}{C_{RC}}\right)$$

Similarly, to slew an adjustable (any output voltage) from zero to full output in 10 ms requires a 20 nF cap.

For Adjustable Versions:

EQUATION 4-4:

$$t_{RC} = 0.5V\left(\frac{C_{RC}}{1\mu A}\right) \qquad SR_{ON} = 2V_{OUT}\left(\frac{1\mu A}{C_{RC}}\right)$$

4.6.3 RAMP DOWN: TURN OFF SLEW RATE

When EN is lowered and the DLY pin has discharged, the RC pin and the OUT pin slew toward zero. For fixed voltage devices, the RC pin slew rate is 2 to 3 times the SR_{ON} defined above. For adjustable voltage devices, the RC pin slew is much higher. In both cases, turn off slew rate may be determined by the RC pin for low values of output capacitor, or by the maximum discharge current available at the output for large values of output capacitor. Turn off slew rate is not a specified characteristic of the MIC68400.

4.7 Sequencing Configurations

Sequencing refers to timing-based Master/Slave control between regulators. It allows a Master device to control the start and stop timing of a single or multiple Slave devices. In typical sequencing the Master POR drives the Slave EN. The sequence begins with the Master EN driven high. The Master output ramps up and triggers the Master DLY when the Master output reaches 90%. The Master DLY then determines when the POR is released to enable the Slave device. When the Master EN is driven low, the Master POR is immediately pulled low causing the Slave to ramp down. However, the Master output will not ramp down until the Master DLY has fully discharged. In this way, the Master power can remain good after the Slave has been ramped down.

In sequencing configurations the Master DLY controls the turn-on time of the Slave and the Slave DLY controls the turn-off time of the Slave.

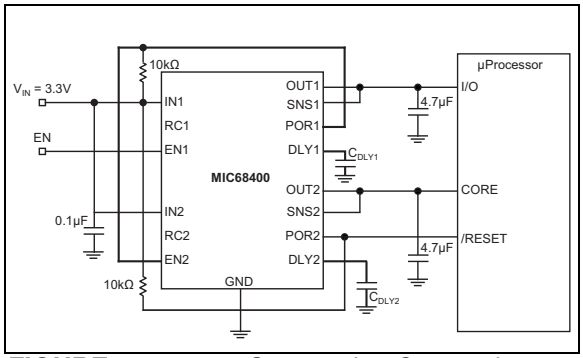

FIGURE 4-4: *Sequencing Connections.*

In the figure below, $C_{DLYS} > C_{DLYM}$. C_{DLYS} = 2 nF, C_{DLYM} = 1 nF.

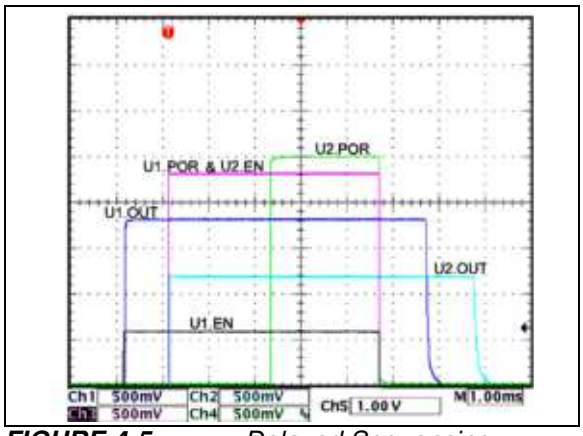

FIGURE 4-5: *Delayed Sequencing.*

In the figure below, $C_{DLYS} < C_{DLYM}$. C_{DLYS} = 1 nF, C_{DLYM} = 2 nF.

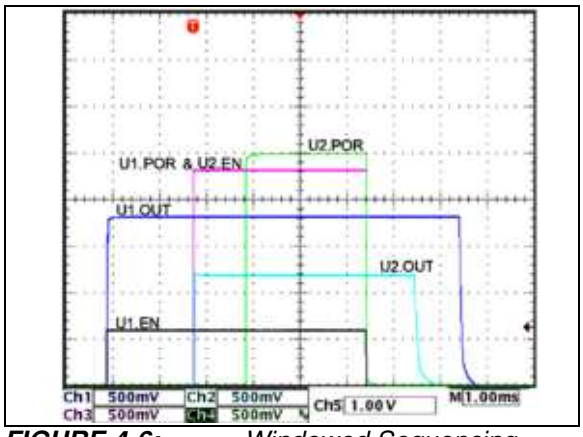

FIGURE 4-6: *Windowed Sequencing.*

4.8 Tracking Configurations

4.8.1 NORMAL TRACKING

In normal tracking, the Slave RC pin is driven from the Master output. The internal control buffering ensures that the output of the Slave is always slightly above the Master to guarantee that the Slave properly regulates

(based on its own internal reference) if Master and Slave are both fixed voltage devices of the same output voltage. The schematic and plot below show a 1.2V device tracking a 1.8V device through the entire turn-on/turn-off sequence. Note that because the RC pin will overdrive the target voltage (to ensure proper regulation), the ramp down delay is longer than the POR delay during turn-on.

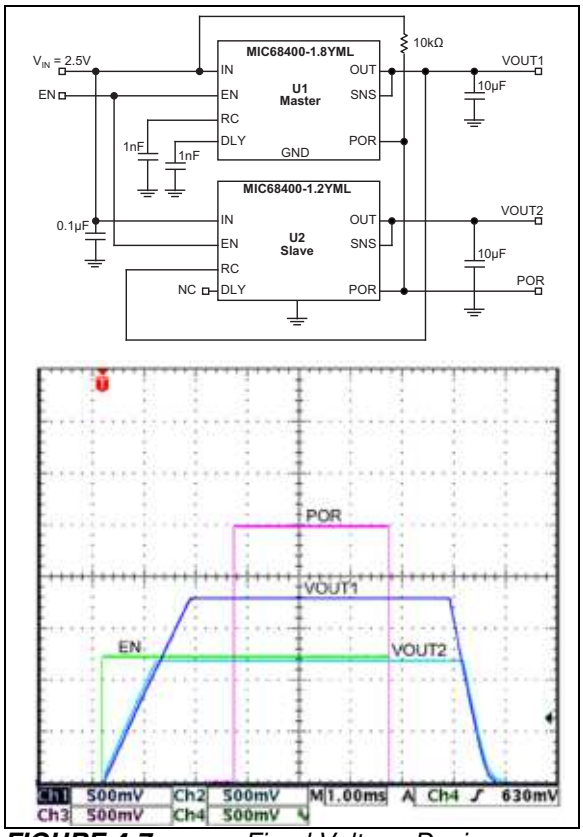

FIGURE 4-7: *Fixed Voltage Devices.*

Fixed voltage versions of MIC68400 have two internal voltage dividers: one for setting the output voltage and the other for driving the tracking circuitry. Adjustable parts have up to two external dividers: one from output to SNS (to set the output voltage) and one from the output to the Slave RC pin (in tracking configurations). Also, the RC pin in fixed parts operates at the same voltage as the output, whereas the RC pin in adjustable parts operates at the 0.5V reference. To set up a normal tracking configuration, the divider driving the Slave RC pin is the same ratio (or nearly the same – if both Master and Slave are set to the same output voltage, the Slave RC divider should be adjusted 2% to 4% higher) as the divider driving the Slave SNS pin. This is shown in Figure 4-8.

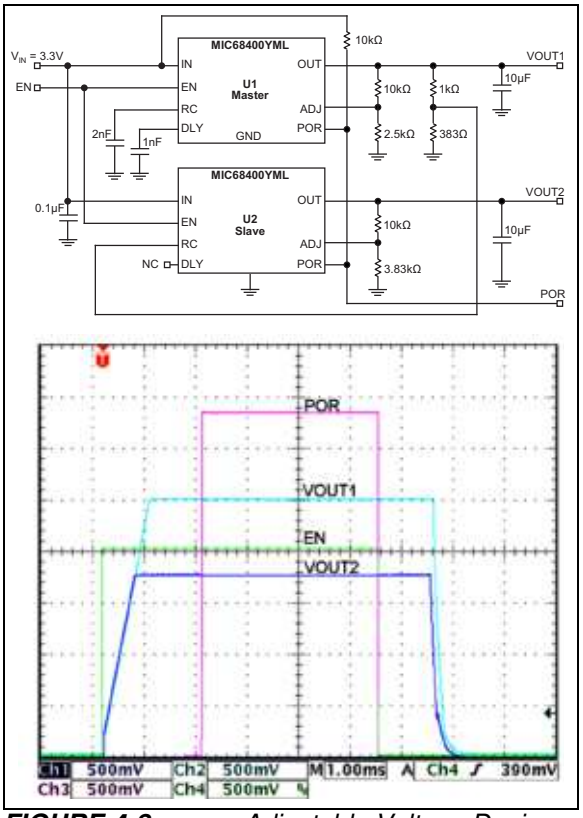

FIGURE 4-8: *Adjustable Voltage Devices.*

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4.8.2 RATIOMETRIC TRACKING

Ratiometric tracking allows independent ramping speeds for both regulators so that the regulation voltage is reached at the same time. This is accomplished by adding a resistor divider between the Master output pin and the Slave RC pin. The divider should be scaled such that the Slave RC pin reaches or exceeds the target output voltage of the Slave as the Master reaches its target voltage.

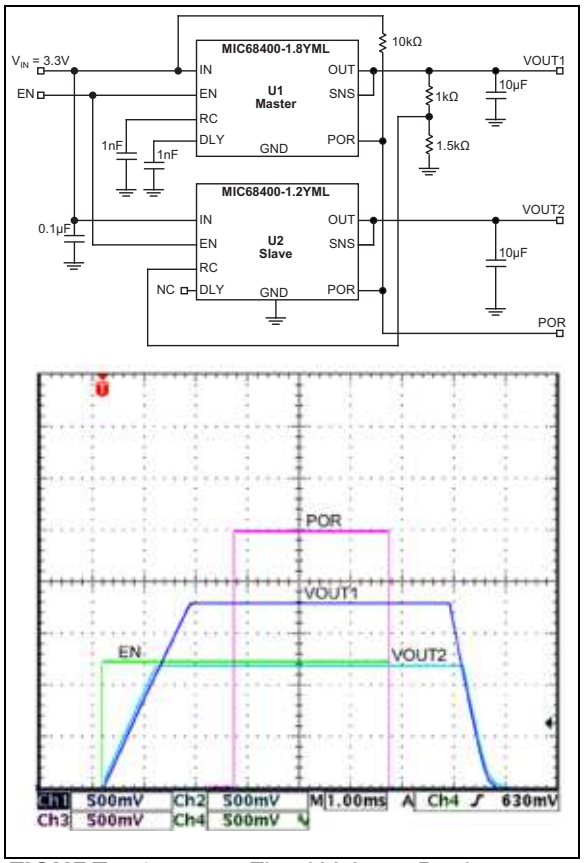


FIGURE 4-9: *Fixed Voltage Devices.*

Ratiometric tracking may be used with adjustable parts by simply connecting the RC pins of the Master and Slave. Use a single RC capacitor of twice the normal value (because twice the current is injected into the single RC cap). Alternatively, fixed parts may use ratiometric tracking in a manner similar to adjustable normal tracking, with the tracking divider changed to the same resistor ratio driving the Master ADJ/SNS pin.

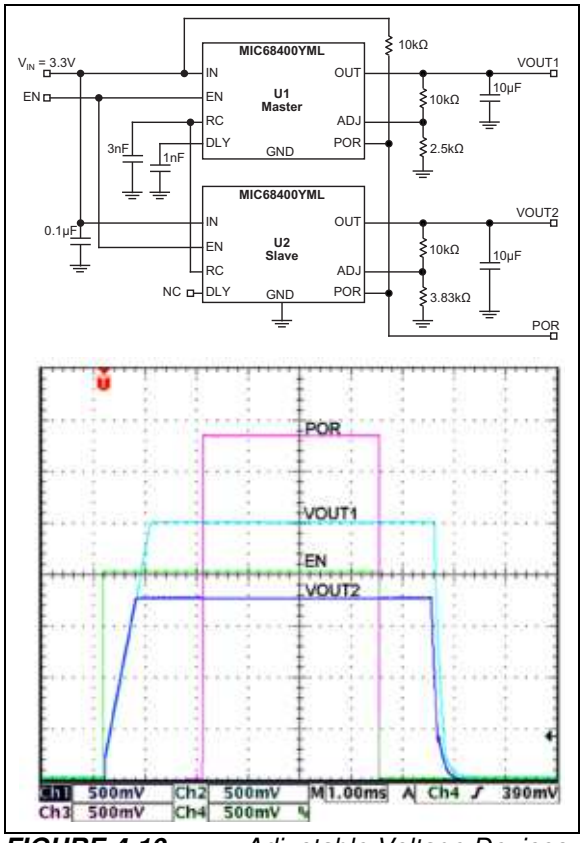


FIGURE 4-10: *Adjustable Voltage Devices.*

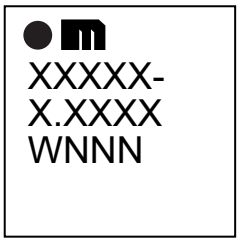
4.9 Final Note on Tracking

The MIC68400 does not fully shut down until the output load is discharged to near zero. If RC is driven from an external source in a tracking configuration, and the external source does not go to zero on shutdown, it may prevent complete shutdown of the MIC68400. This will cause no damage, but some Q current will remain and may cause concern in battery operated portable equipment. Also, when RC is driven in tracking mode, pulling EN low will not cause the output to drop. Maintaining low EN in tracking mode simply means that the MIC68400 will shutdown when the tracking voltage gets near zero. In no case can the MIC68400 enter the tracking mode unless EN is pulled high.

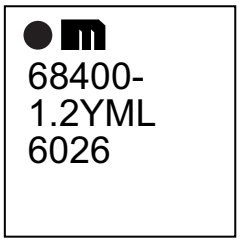
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

16-Lead QFN*
(Fixed)

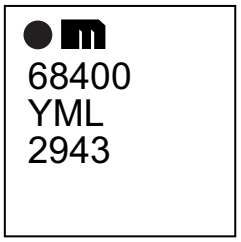


Example



16-Lead QFN*
(Adjustable)

Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

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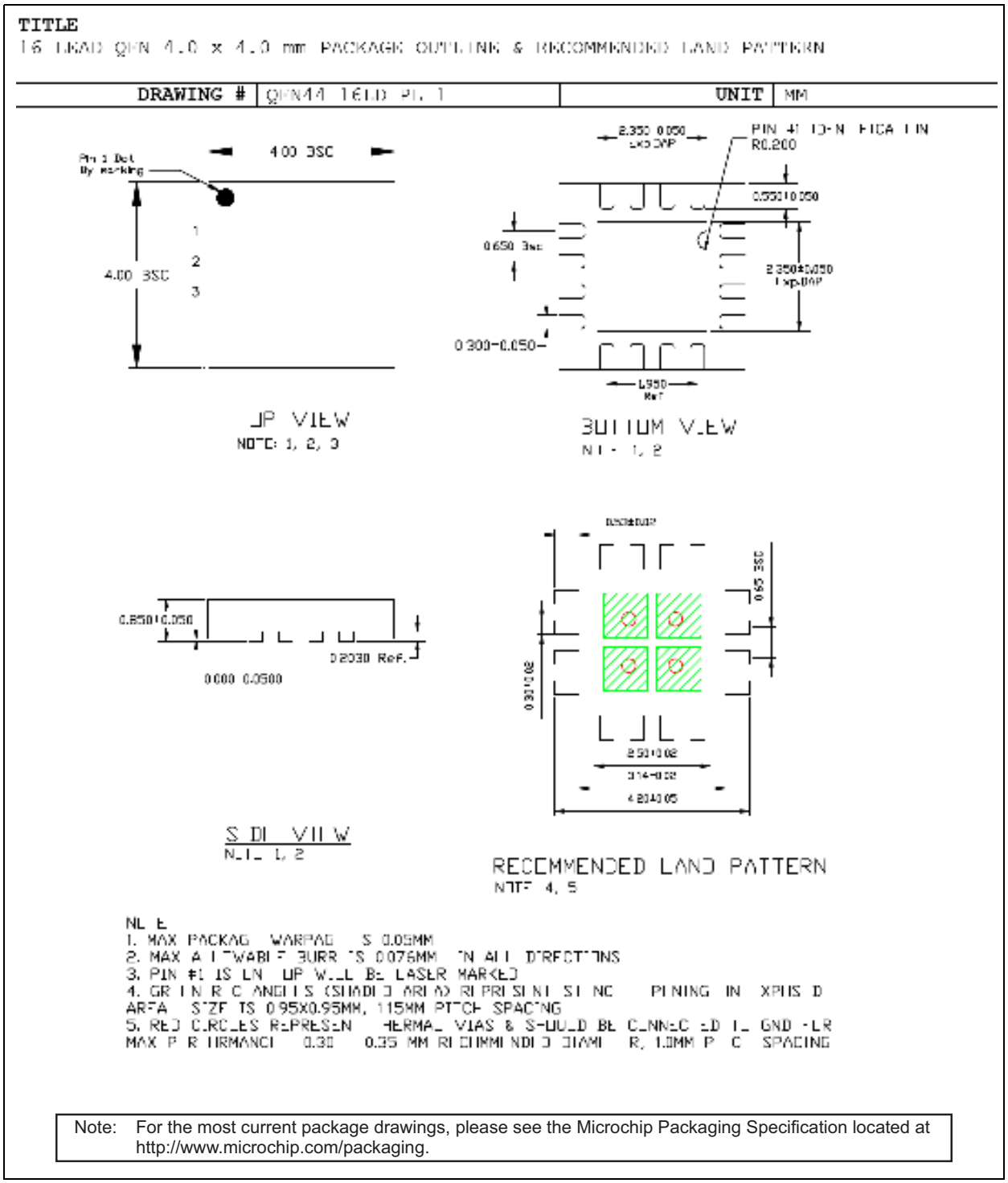
16-Lead 4 mm x 4 mm QFN Package Outline and Recommended Land Pattern



Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (August 2017)

- Converted Micrel document MIC68400 to Microchip data sheet DS20005824A.
- Minor text changes throughout.
- Paragraph added after Figure 4-2 in **Section 4.2 "Input Capacitor"**.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	–X.X	X	XX	–XX
Device	Voltage	Temperature	Package	Media Type

Device:	MIC68400:		4A Sequencing LDO with Tracking and Ramp Control
Voltage:	1.2	=	1.2V
	1.8	=	1.8V
	blank	=	Adjustable
Temperature:	Y	=	–40°C to +125°C
Package:	ML	=	16-Lead 4 mm x 4 mm QFN
Media Type:	TR	=	5,000/Reel

Examples:

a) MIC68400-1.2YML-TR: 4A Sequencing LDO with Tracking and Ramp Control, 1.2V, –40°C to +125°C, 16-Lead QFN, 5,000/Reel

b) MIC68400-1.8YML-TR: 4A Sequencing LDO with, Tracking and Ramp Control 1.8V, –40°C to +125°C, 16-Lead QFN, 5,000/Reel

c) MIC68400YML-TR: 4A Sequencing LDO with, Tracking and Ramp Control Adjustable Voltage, –40°C to +125°C, 16-Lead QFN, 5,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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