General Description



BDE-BDM209A is a Bluetooth 5.1 BR/EDR & BLE Dual Mode module.

The module offers a unique combination of Bluetooth classic and Bluetooth Low Energy radio TI's CC2564C and an ARM 32-bit Cortex-M4F CPU MSP432, with integration of all external components including antenna at a very affordable cost.

The module provides the best-in-class RF performance with transmit power and receive sensitivity that provides twice the range and higher throughput than other Bluetooth-low-energy-only solutions. The power-management hardware and software algorithms provide significant power savings in all commonly used Bluetooth BR/EDR and low energy modes of operation.

The certified and royalty free Dual-mode Bluetooth 4.2 protocol stack software provides a complete Bluetooth BR/EDR, and Bluetooth Low Energy sample applications that reduce design effort and ensure a faster time to market.

Key Features

- Processing and memories
  - Arm® 32-bit Cortex®-M4F CPU with floating point unit and memory protection unit
  - Frequency up to 48 MHz
  - 256KB flash main memory (organized into two banks enabling simultaneous read or execute during erase)
  - 16KB of flash information memory
  - 64KB of SRAM (including 6KB of backup memory)
  - 32KB of ROM with MSP432™ peripheral driver libraries
- Bluetooth 5.1 Declaration ID D049226
- BR and EDR Features Include:
  - Up to Seven Active Devices
  - Scatternet: Up to Three Piconets Simultaneously, One as Master and Two as Slaves
  - Up to Two Synchronous Connection Oriented (SCO) Links on the Same Piconet
  - Support for All Voice Air-Coding—Continuously Variable Slope Delta (CVSD), A-Law, μ-Law, and Transparent (Uncoded)
  - Assisted Mode for HFP 1.6 Wideband Speech (WBS) Profile or A2DP Profile to Reduce Host Processing and Power
  - Support of Multiple Bluetooth Profiles with Enhanced QoS
- Bluetooth Low Energy Features Include:
  - Support of up to 10 Simultaneous Connections
  - Multiple Sniff Instances Tightly Coupled to Achieve Minimum Power Consumption
  - Independent Buffering for Low Energy Allows Large Numbers of Multiple Connections Without Affecting BR or EDR Performance
  - Built-In Coexistence and Prioritization Handling for BR, EDR, and Low Energy
- Best-in-Class Bluetooth (RF) Performance (TX Power, RX Sensitivity, Blocking)
  - Class 1.5 TX Power up to +10 dBm
  - –93 dBm Typical RX Sensitivity
  - Internal Temperature Detection and Compensation to Ensure Minimal Variation in RF Performance Over Temperature, No External Calibration Required
  - Improved Adaptive Frequency Hopping (AFH) Algorithm with Minimum Adaptation Time
  - Provides Longer Range, Including Twice the Range of Other Low-Energy-Only Solutions
- Advanced Power Management for Extended Battery Life and Ease of Design
  - Low Power Consumption for Active,

Standby, and Scan Bluetooth Modes
- Shutdown and Sleep Modes to Minimize Power Consumption

- MCU Ultra-low-power operating modes when Bluetooth is Shutdown
  - Active: 80 µA/MHz
  - Low-frequency active: 83 µA at 128 kHz
  - LPM3 (with RTC): 660 nA
  - LPM3.5 (with RTC): 630 nA
  - LPM4: 500 nA
  - LPM4.5: 25 nA
- Operating characteristics
  - Wide supply voltage range: 2.05V to 3.7V
  - Temperature range: –40°C to 85°C
- Flexible clocking features
  - Tunable internal DCO (up to 48 MHz)
  - 32.768-kHz low-frequency crystal support (LFXT)
  - High-frequency crystal support (HFXT) up to 48 MHz
  - Low-frequency internal reference oscillator (REFO)
  - Very low-power low-frequency internal oscillator (VLO)
  - Module oscillator (MODOSC)
  - System oscillator (SYSOSC)
- Code security features
  - JTAG and SWD lock
  - IP protection (up to four secure flash zones, each with configurable start address and size)
- Enhanced system features
  - Programmable supervision and monitoring of supply voltage
  - Multiple-class resets for better control of application and debug
  - RTC with calendar and alarm functions
- Timing and control
  - Up to four 16-bit timers, each with up to five capture, compare, PWM capability
  - Two 32-bit timers, each with interrupt generation capability
- Physical Interfaces:
  - UART with automatic baud-rate detection
  - I2C (with multiple-slave addressing)
  - SPI (up to 16 Mbps)
  - Up to 17 GPIOs for users
  - All GPIOs with capacitive-touch capability
  - Ultra-low-leakage I/Os (±20 nA maximum)
  - Up to 15 I/Os with interrupt and wake-up capability
  - Two I/Os with glitch filtering capability
  - Fully Programmable Digital Pulse-Code Modulation (PCM)–I2S Codec Interface
- Antenna: Chip antenna or U.FL connector
- Encryption and data integrity accelerators
  - 128-, 192-, or 256-bit AES encryption and decryption accelerator
  - 32-bit hardware CRC engine
- Bluetooth 4.2 Dual-mode stack
  - dual-mode Bluetooth 4.2 certified and royalty free
  - Fully qualified Bluetooth stack (QDID 85355 and QDID 69886)
- Classic Bluetooth Profiles Available
  - A2DP1.2, AVDTP1.2, AVRCP1.3, HSP1.2, GAP, HID1.0, MAP1.0, PBAP1.0, RFCOMM, SDP, SPP.
- Bluetooth low energy Profiles Available
  - ANS1.0, BAS1.0, CSCS1.0, DIS1.0, FMP1.0, GAPS1.0, GATT1.0, HTS1.0, HRS1.0, HIDS1.0, IAS1.0, LLS1.0, PASS1.0, PXP1.0, TPS1.0.
- MFi Support
  - iAP Protocol (iAP 1/iAP 2) provided as an add-on upon request
- Packaging
  - 12 mm x 22 mm x 2.1 mm package
- Large variety of Sample Applications
  - Classic Bluetooth Sample Applications include: A3DP Sink/Source, HFP, HID, HSP, MAP, PBAP, SPP application demos.
  - BLE Sample Applications include: ANP, iBeacon, HRP, HTP, PASP, HOGP, PXP, FMP, CSCP application demos.
  - Classic Bluetooth + Bluetooth low energy Sample Applications include: SPP+SPPLE, SPP DMMulti application demos.
- Development Environment supports:
  - CCS, Keil®, and IAR Embedded Workbench® IDEs.
- Standards Conformance
  - Bluetooth- DID: D054396, QDID: 165249
  - FCC ID: 2ABRUBDM209A
  - IC: 25657-BDM209A
  - CE-RED
  - Japan

- Korea
- Taiwan
- Australia
- New Zealand
- China

Applications

- Mobile Accessories
- Sports and Fitness Applications
- Wireless Audio Solutions
- Set-Top Boxes and Remote Controls
- Toys
- Test and Measurement
- Industrial: Cable Replacement
- Wireless Sensors
- Automotive Aftermarket
- Wellness and Health

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1. References

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2. Block Diagram

BDM209A is highly integrated System on Module Bluetooth Dual-mode device that comprises of TI's CC2564C Bluetooth Dual-mode controller, MSP432 ARM 32-bit Cortex-M4F MCU, a high-performance chip antenna and peripherals.

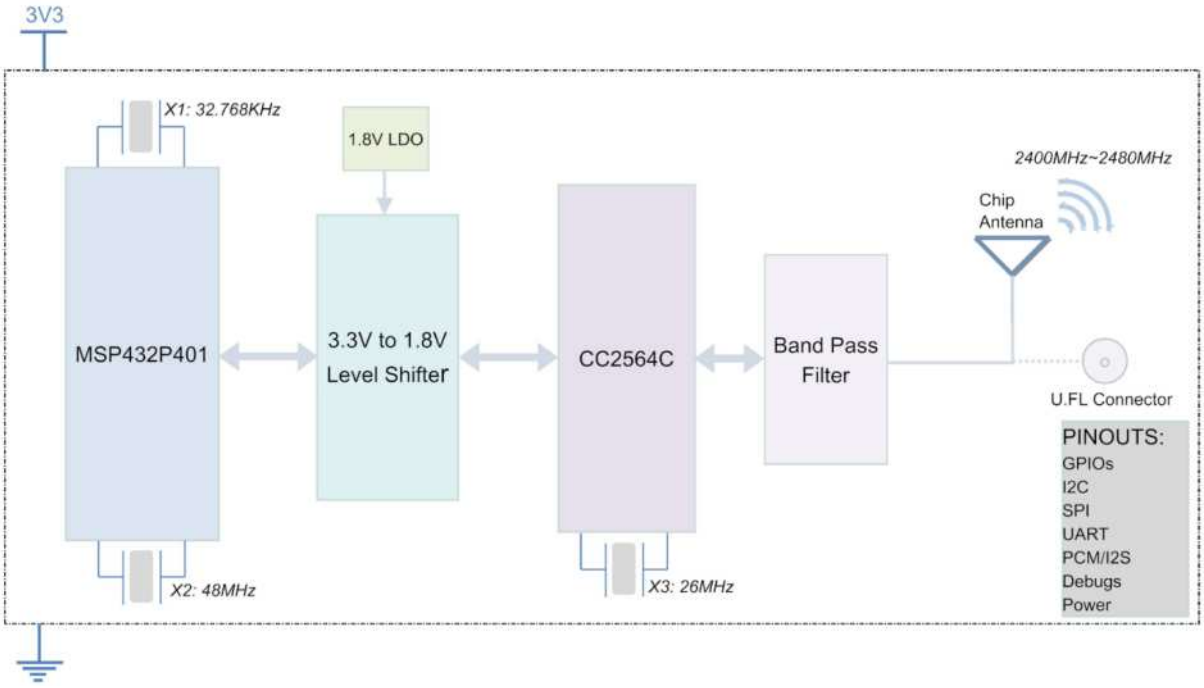


Figure 1: BDM209A Module Block Diagram

3. Pinout

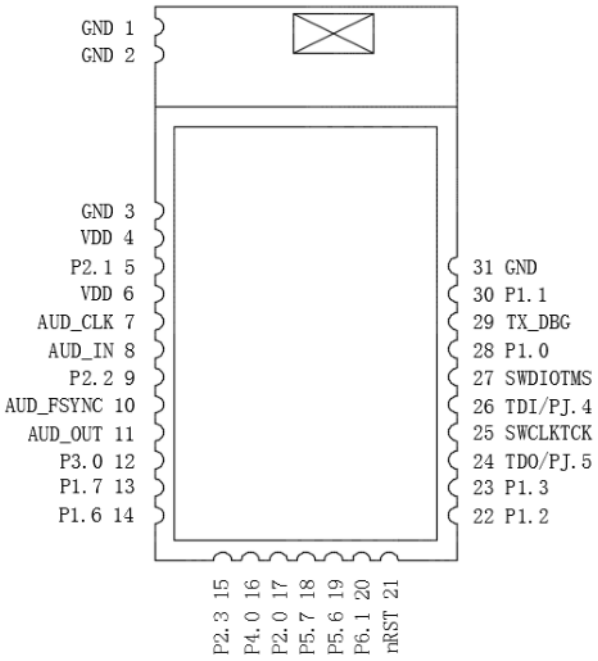


Figure 2: Pinout Diagram Top View

Table 1: Pin Description

Pin #	Pin Name		Type	Reset State	Description
1	GND		GND	N/A	Ground
2	GND		GND	N/A	Ground
3	GND		GND	N/A	Ground
4	VDD		GND	N/A	3.3V DC voltage supply
5	P2.1	P2.1	DIO	OFF	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function. This I/O can be configured for high drive operation with up to 20-mA drive capability.
		PM_UCA1CLK		N/A	eUSCI_A1 clock input/output (direction controlled by eUSCI)
6	VDD		PWR	N/A	3.3V DC voltage supply
7	AUD_CLK		DIO, HY, 4 mA	PD	PCM clock, Fail-safe
8	AUD_IN		DI, 4 mA	PD	PCM data input, Fail-safe

Pin #	Pin Name		Type	Reset State	Description
9	P2.2	P2.2	DIO	OFF	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function. This I/O can be configured for high drive operation with up to 20-mA drive capability.
		PM_UCA1RXD	DI	N/A	eUSCI_A1 UART RXD (direction controlled by eUSCI – input)
		PM_UCA1SOMI	DIO	N/A	eUSCI_A1 SPI slave out master in (direction controlled by eUSCI)
10	AUD_FSYNC		DIO, 4 mA	PD	PCM frame sync, Fail-safe
11	AUD_OUT		DO, 4 mA	PD	PCM data output, Fail-safe
12	P3.0		DIO	OFF	General-purpose digital I/O with port interrupt, wakeup, and glitch filtering capability.
13	P1.7	P1.7	DIO	OFF	General-purpose digital I/O with port interrupt and wake-up capability
		UCB0SCL		N/A	I2C clock – eUSCI_B0 I2C mode
14	P1.6	P1.6	DIO	OFF	General-purpose digital I/O with port interrupt and wake-up capability
		UCB0SDA		N/A	I2C data – eUSCI_B0 I2C mode
15	P2.3	P2.3	DIO	OFF	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function. This I/O can be configured for high drive operation with up to 20-mA drive capability.
		PM_UCA1TXD	DO	N/A	eUSCI_A1 UART TXD (direction controlled by eUSCI – output)
		PM_UCA1SIMO	DIO	N/A	eUSCI_A1 SPI slave in master out (direction controlled by eUSCI)
16	P4.0	P4.0	DIO	OFF	General-purpose digital I/O with port interrupt and wake-up capability
		A13	AI	N/A	ADC analog input A13
17	P2.0	P2.0	DIO	OFF	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function. This I/O can be configured for high drive operation with up to 20-mA drive capability.
		PM_UCA1STE		N/A	eUSCI_A1 SPI slave transmit enable (direction controlled by eUSCI)
18	P5.7	P5.7	DIO	OFF	General-purpose digital I/O with port interrupt and wake-up capability
		TA2.2	DIO	N/A	TA2 CCR2 capture: CCI2A input, compare: Out2
		VREF-	AO	N/A	Internal shared reference voltage

Pin #	Pin Name		Type	Reset State	Description
					negative terminal
		VeREF-	AI	N/A	Negative terminal of external reference voltage to ADC (recommended to connect to onboard ground)
		C1.6	AI	N/A	Comparator_E1 input 6
19	P5.6	P5.6	DIO	OFF	General-purpose digital I/O with port interrupt and wake-up capability
		TA2.1	DIO	N/A	TA2 CCR1 capture: CCI1A input, compare: Out1
		VREF+	AO	N/A	Internal shared reference voltage positive terminal
		VeREF+	AI	N/A	Positive terminal of external reference voltage to ADC
		C1.7	AI	N/A	Comparator_E1 input 7
20	P6.1	P6.1	DIO	OFF	General-purpose digital I/O with port interrupt and wake-up capability
		A14	DI	N/A	ADC analog input A14
21	nRST	nRST	DI	PU	External reset (active low)
		NMI		N/A	External nonmaskable interrupt
22	P1.2	P1.2	DIO	OFF	General-purpose digital I/O with port interrupt and wake-up capability
		UCA0RXD	DI	N/A	Receive data – eUSCI_A0 UART mode
		UCA0SOMI	DIO	N/A	Slave out, master in – eUSCI_A0 SPI mode
23	P1.3	P1.3	DIO	OFF	General-purpose digital I/O with port interrupt and wake-up capability
		UCA0TXD	DO	N/A	Transmit data – eUSCI_A0 UART mode
		UCA0SIMO	DIO	N/A	Slave in, master out – eUSCI_A0 SPI mode
24	TDO	TDO	DO	N/A	JTAG test data output
		SWO	DO		Serial wire trace output
		PJ.5	DIO		General-purpose digital I/O
25	SWCLKTCK	TCK	DI	PD	JTAG clock input (TCK)
		SWCLK			Serial wire clock input (SWCLK)
26	TDI	TDI	DI	PU	JTAG test data input
		PJ.4	DIO	N/A	General-purpose digital I/O
27	SWDIOTMS	TMS	DIO	PU	JTAG test mode select (TMS)
		SWDIO			Serial wire data input/output (SWDIO)
28	P1.0	P1.0	DIO	OFF	General-purpose digital I/O with port interrupt, wakeup, and glitch filtering capability
		UCA0STE		N/A	Slave transmit enable – eUSCI_A0 SPI mode
29	TX_DBG		DO		CC2564C Internal debug messages
30	P1.1	P1.1	DIO	OFF	General-purpose digital I/O with port interrupt, wakeup, and glitch filtering capability

Pin #	Pin Name		Type	Reset State	Description
		UCA0CLK		N/A	Clock signal input – eUSCI_A0 SPI slave mode Clock signal output – eUSCI_A0 SPI master mode
31	GND		GND		Ground

1. Type:
   DIO = Digital Input-Output, DI = Digital Input, DO = Digital Output, AI = Analog Input, AO = Analog Output, PWR = Power, GND = Ground, HY = Input Hysteresis, x mA = Typical output current.
2. Reset States:
   - OFF = High-impedance with Schmitt trigger and pullup or pulldown (if available) disabled
   - PD = High-impedance input with pulldown enabled
   - PU = High-impedance input with pullup enabled
   - N/A = Not applicable
3. For detail information, please refer to References.

Table 2. Connection for Unused Pins

PIN	POTENTIAL	COMMENT
Px.0 to Px.7	Open	Set to port function in output direction, and leave unconnected.
RSTn/NMI	DVCC or VCC	47-kΩ pullup with 1.1-nF pulldown.
PJ.4/TDI	Open	The JTAG TDI pin is shared with general-purpose I/O function (PJ.4). If not being used, this pin should be set to port function in the output direction. When used as JTAG TDI pin, it should remain open.
PJ.5/TDO/SWO	DVCC or VCC	The JTAG TDO/SWO pin is shared with general-purpose I/O function (PJ.5). If not being used, this pin should be set to port function in the output direction. When used as JTAG TDO/SWO pin, it should be pulled down externally.
SWDIOTMS	DVCC or VCC	This pin should be pulled up externally.
SWCLKTCK	DVSS or VSS	This pin should be pulled down externally.
TX_DUG	Open	Remain open.

1. For any unused pin with a secondary function that is shared with general-purpose I/O, follow the guidelines for the Px.0 to Px.7 pins. Refer to References.

4. Characteristics

All MIN/MAX specification limits are guaranteed by design, production testing and/or statistical characterization. Typical values are based on characterization results at default measurement conditions and are informative only.
Default measurement conditions (unless otherwise specified): VDD= 3.0 V, TA = 25 ℃. All radio measurements are performed with standard RF measurement equipment.

4.1. Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Parameter	Description	Conditions	Min	Max	Unit
VDD	Power Supply voltage at VDD pins		-0.3	4.17	V
T_{STG}	Storage temperature		-40	125	°C

4.2. Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
VDD	Power supply voltage		2.05	3.0	3.7	V
T			-40		85	°C
I_{INRUSH}	Inrush current into the VDD pins				100	mA

4.3. Device Characteristics

Table 5: Digital IO - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IT+}	Positive-going input threshold voltage	VDD = 3V	1.35		2.25	V
V_{IT-}	Negative-going input threshold voltage	VDD = 3V	0.75		1.65	V
V_{OH}	High-level output voltage	VDD = 3V, I_{OHmax} = -6mA	VDD-0.6		VDD	V
V_{OL}	Low-level output voltage	VDD = 3V, I_{OLmax} = 6mA	VSS		VSS+0.6	

Table 6: Radio for Bluetooth BR EDR - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_{OPER}	Operating frequency		2402		2480	MHz
N_{CH}	Number of channels			79		1
F_{CH}	Channel frequency	K = 0 to 78		2402+K		MHz

Table 7: Radio for Bluetooth Low Energy - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_{OPER}	Operating frequency		2402		2480	MHz
N_{CH}	Number of channels			40		1
F_{CH}	Channel frequency	K = 0 to 39		2402+K*2		MHz

Table 8: RF - AC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
TX_{GFSK}	Maximum RF output Power - GFSK	GFSK		12		dBm
TX_{EDR}	Maximum RF output Power - EDR	EDR		10		dBm
RX_{SEN_1}	RX sensitivity - GFSK	GFSK, BER = 0.1%		-95		dBm
RX_{SEN_2}	RX sensitivity - π /4-DQPSK	π /4-DQPSK, BER = 0.01%		-94.5		dBm
RX_{SEN_3}	RX sensitivity - DPSK	8DPSK, BER = 0.01%		-87.5		dBm

5. Mechanical Specifications

5.1. Dimensions

The module dimensions are presented in the following figure:

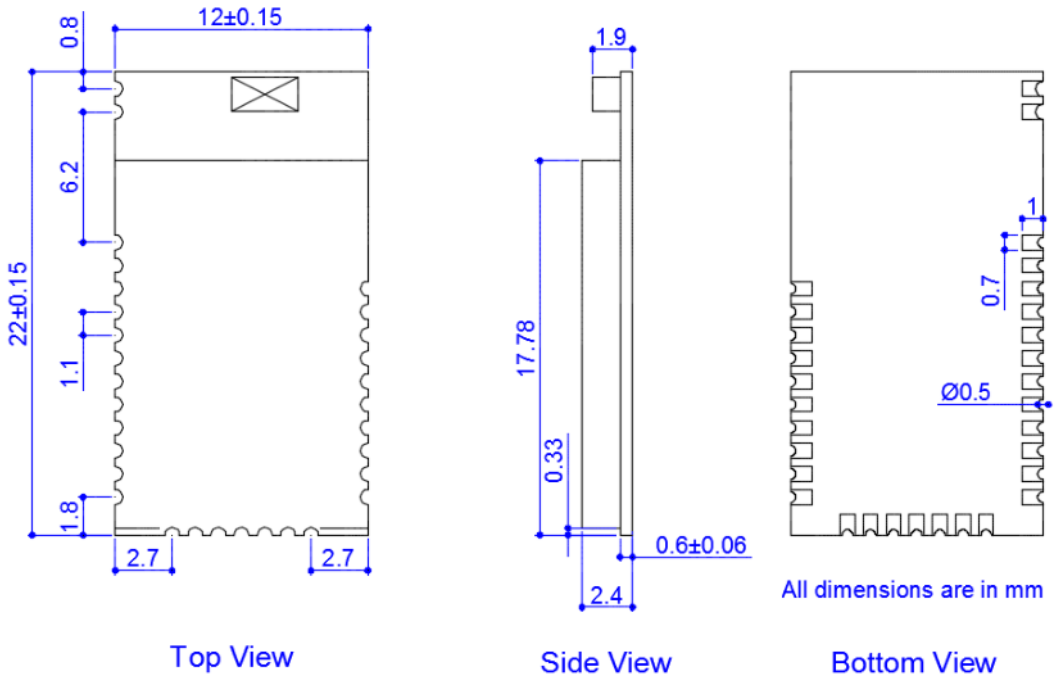


Figure 3: Mechanical Drawing

5.2. PCB Footprint

The footprint for the PCB is presented in the following figure:

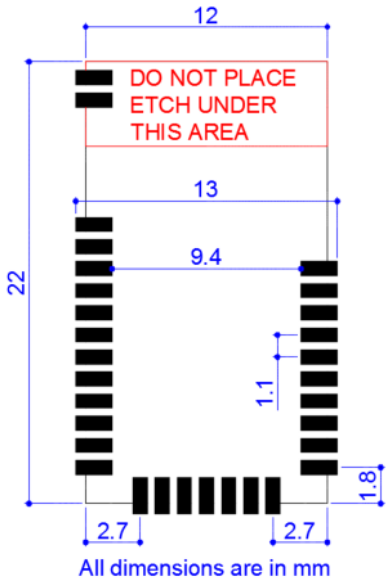


Figure 4: Module Footprint Top View

5.3. Marking



Figure 5: Indicative Module Shield Marking

6. Ordering Information

Table 11: Ordering Information

Part Number	Size (mm)	Shipping Form	MOQ
BDE-BDM209A	12 x 22 x 2.4	Tape & Reel	1000

Revision History

Revision	Date	Description
V0.9	20-October-2020	Preliminary version
V1.0	30-October-2020	Formal Release version.
V1.1	28-December-2020	Add Bluetooth 5.1 DID D049226 and device photo

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