EMC2101

SMBus Fan Control with 1°C Accurate Temperature Monitoring

PRODUCT FEATURES

Datasheet

General Description

The EMC2101 is an SMBus 2.0 compliant, integrated fan control solution complete with two temperature monitors, one external and one internal. Each temperature channel has programmable high limits that can assert an interrupt.

The fan drive is selectable as a Pulse Width Modulator (PWM) or Linear (DAC) output. The fan control output, whether the PWM or DAC drive circuit, uses an eight position look-up table to allow the user to program the fan speed profile based on temperature. The DAC output ranges from 0V to V_{DD} with up to 6 bit resolution while the PWM output has a range of 0% to 100% with up to 64 steps.

The EMC2101 has an option to automatically upload the contents of an attached SMBus compatible EEPROM for auto-programming upon power up.

Advanced thermal sensing enables reduced validation and characterization time as well as accurately operating with smaller-geometry processors. Resistance Error Correction (REC) automatically corrects the offset errors of board trace and device resistance, up to 100Ω. Automatic Beta Compensation allows the user the flexibility to design applications that include processor substrate transistors.

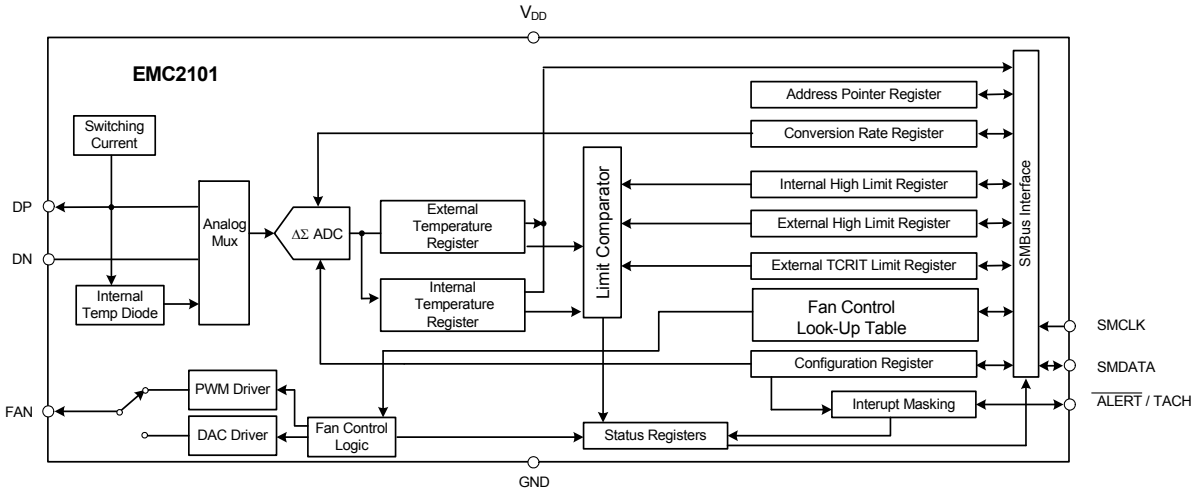
Features

- Automatic Beta Compensation
- Resistance Error Correction
- Self-programming with available SMBus compatible EEPROM
- Selectable PWM or DAC fan driver output
- Temperature Monitors
  - — External channel ±1°C accuracy
  - — Internal channel ±2°C accuracy
- 3.3 Volt Operation (5 Volt Tolerant Input Buffers)
- SMBus 2.0 Compliant Interface, supports TIMEOUT
- 8-Pin MSOP Lead-free RoHS Compliant Packages
- 8-Pin SOIC Lead-free RoHS Compliant Package

Applications

- Graphics Processors
- Embedded Application Fan Drive
- PWM Controller + Temp Sensor

Block Diagram



ORDER NUMBERS:

EMC2101-ACZL-TR FOR 8-PIN, MSOP LEAD-FREE ROHS COMPLIANT PACKAGE

EMC2101-R-ACZL-TR FOR 8-PIN, MSOP LEAD-FREE ROHS COMPLIANT PACKAGE

EMC2101-ACZT-TR FOR 8-PIN, SOIC LEAD-FREE ROHS COMPLIANT PACKAGE

REEL SIZE IS 4,000 PIECES

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

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Chapter 1 Device Selection

The EMC2101 is available with the following options and configurations as shown in Table 1.1.

Table 1.1 Device Selection

PART NUMBER	FAN OPERATION	COMMUNICATIONS	PACKAGE	PRODUCT ID
EMC2101	PWM Drive, 0% drive	SMBus	8 pin SOIC and 8 pin MSOP	16h
EMC2101-R	Selected via pull-up	Selected via pull-up	8 pin MSOP	28h

Chapter 2 Pin Layout

2.1 Pin Diagram for EMC2101

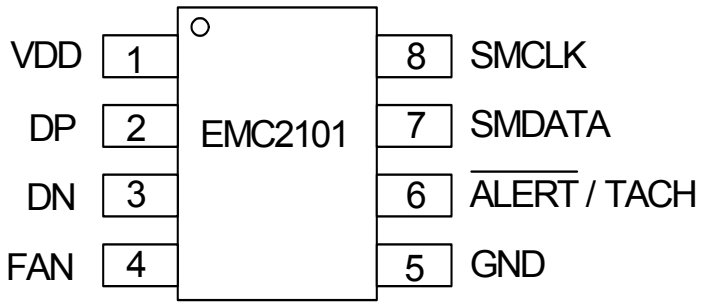


Figure 2.1 EMC2101 Pinout

2.2 Pin Description for EMC2101

Table 2.1 Pin Description

PIN	NAME	FUNCTION	TYPE
1	VDD	3.3V Power supply	Power
2	DP	External diode positive (anode) connection	AI
3	DN	External diode negative (cathode) connection	AI
4	FAN	PWM Output (default - software programmed)	OD (5V)
		DAC Output software programmed	AO
5	GND	Ground	Power
6	$\overline{\text{ALERT}}$ / TACH	$\overline{\text{ALERT}}$ - Open drain I/O operates as active low interrupt or TACH input - requires pull-up resistor, which defines auto-configuration mode (see Table 5.1)	OD (5V)
		TACH - TACH input	DI (5V)
7	SMDATA	SMBus Data input/output	DIOD Output (5V)
8	SMCLK	SMBus Clock input	DIOD Output (5V)

The pin types are described below. All pins labelled with (5V) are 5V tolerant.

APPLICATION NOTE: For the 5V tolerant pins that have a pull-up resistor, the voltage difference between VDD and the pull-up voltage must never exceed 3.6V.

Table 2.2 Pin Types

PIN TYPE	DESCRIPTION
Power	This pin is used to supply power or ground to the device.
DI	Digital Input - this pin is used as a digital input. This pin is 5V tolerant.
AI	Analog Input - this pin is used as an input for analog signals.
AO	Analog Output - this pin is used as an output for analog signals.
DIOD	Digital Input / Open Drain Output - this pin is used as a digital I/O. When it is used as an output, it is open drain and requires a pull-up resistor. This pin is 5V tolerant.
OD	Open Drain Digital Output - this pin is used as a digital output. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.

Chapter 3 Electrical Specifications

3.1 Absolute Maximum Ratings

Table 3.1 Absolute Maximum Ratings

DESCRIPTION	RATING	UNIT
Supply Voltage (V_{DD})	-0.3 to 5.0	V
Voltage on 5V tolerant pins (V_{5VT_pin})	-0.3 to 5.5	V
Voltage on 5V tolerant pins ($\|V_{5VT_pin} - V_{DD}\|$) (see Note 3.1)	-0.3 to 3.6	V
Voltage on any other pin to Ground	-0.3 to V_{DD} +0.3	V
Operating Temperature Range	-40 to 125	°C
Storage Temperature Range	-55 to 150	°C
Lead Temperature Range	Refer to JEDEC Spec. J-STD-020	
Package Thermal Characteristics for MSOP-8		
Thermal Resistance	140.8	°C/W
Package Thermal Characteristics for SOIC-8		
Thermal Resistance	135.9	°C/W
ESD Rating, All pins HBM	2000	V

Note: Stresses above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

Note 3.1 For the 5V tolerant pins that have a pull-up resistor, the pull-up voltage must not exceed 3.6V when the EMC2101 is unpowered.

3.2 Electrical Specifications

Table 3.2 Electrical Specifications

V_{DD} = 3.0V to 3.6V, T_A = 0°C - 85°C, Typical values are at T_A = 27°C unless otherwise noted						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
DC Power						
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	

Table 3.2 Electrical Specifications (continued)

V_{DD} = 3.0V to 3.6V, T_A = 0°C - 85°C, Typical values are at T_A = 27°C unless otherwise noted						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Supply Current	I_{DD}		0.6	1	mA	16 conversion / second - PWM or DAC driver operational
Supply Current	I_{DD}		200		uA	1 conversion / 16 seconds - PWM driver operational
Supply Current	I_{DD}		300		uA	1 conversion / 16 seconds - DAC Driver, no load
Supply Current	I_{DD}		300	400	uA	Temp monitoring Disabled, DAC Driver enabled, no load
Standby Current	$I_{STANDBY}$			270	µA	PWM disabled, Monitoring disabled
Internal Temperature Monitor						
Temperature Accuracy			±1	±2	°C	
Temperature Resolution			±1		°C	8 bit resolution
Conversion Time Internal Channel	t_{CONV}		3		ms	
External Temperature Monitor						
Temperature Accuracy			±0.5	±1	°C	60°C < T_{DIODE} < 100°C, 10°C < T_A < 70°C
			±1	±3	°C	0°C < T_{DIODE} < 125°C
Temperature Resolution			0.125		°C	11 bit resolution
Conversion Time External Channel	t_{CONV}		21		ms	
Diode Decoupling Capacitor	C_{FILTER}			2.2	nF	Connected across External Diode (2N3904)
Diode Decoupling Capacitor	C_{FILTER}			470	pF	Connected across Substrate Transistor (CPU diode)
Resistance Error Correction	R_{SERIES}		100		Ω	Series resistance in DP and DN lines
TACH Measurement						
TACH Accuracy				10	%	TACH valid
Fan Counter Clock Frequency			90		kHz	
Pulse Width Modulator Fan Driver						
PWM Resolution			64		steps	
PWM Frequency	f_{PWM}	22		5k	Hz	For 64 steps, higher frequencies are possible with reduced resolution (see Appendix A "Advanced PWM Options").

Table 3.2 Electrical Specifications (continued)

V_{DD} = 3.0V to 3.6V, T_A = 0°C - 85°C, Typical values are at T_A = 27°C unless otherwise noted						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
PWM Duty cycle	D_{PWM}	0		100	%	
DAC Fan Driver						
Output Voltage Drive	V_{DAC}	0.2		V_{DD} - 0.2	V	Current Load = ±1mA
Total Unadjusted Error	TUE		5		%	Measured at 3/4 full scale
DAC Resolution			6		bits	
Settling Time to within 1%	t_{SETTLE}		40		us	Capacitive Load = 100pF
Digital I/O pins (PWM, SMDATA, SMCLK, $\overline{\text{ALERT}}$ / TACH)						
Output High Voltage	V_{OH}	V_{DD} - 0.3			V	8mA Current Source
Output Low Voltage	V_{OL}			0.3	V	8mA Current Sink
Output Leakage Current	I_{LEAK}			10	uA	Device powered or unpowered T_A < 85°C pull-up voltage ≤ 3.6V

3.3 SMBus Client Electrical Specifications

Table 3.3 SMBus Electrical Specifications

V_{DD} = 3.0V to 3.6V, T_A = 0°C - 85°C, Typical values are at T_A = 27°C unless otherwise noted						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
SMBus Interface						
Input High Voltage	V_{IH}	2.1			V	
Input Low Voltage	V_{IL}			0.8	V	
Input High/Low Current	I_{IH} / I_{IL}	-1		1	uA	
Hysteresis			500		mV	
Input Capacitance	C_{IN}		5		pF	
Output Low Sink Current			8		mA	V_{OL} = 0.4V
SMBus Timing						
Clock Frequency	f_{SMB}	10		400	kHz	
Spike Suppression	t_{SP}			50	ns	
Bus free time Start to Stop	t_{BUF}	1.3			us	
Hold Time: Start	$t_{HD:STA}$	0.6			us	
Setup Time: Start	$t_{SU:STA}$	0.6			us	

Table 3.3 SMBus Electrical Specifications (continued)

V_{DD} = 3.0V to 3.6V, T_A = 0°C - 85°C, Typical values are at T_A = 27°C unless otherwise noted						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Setup Time: Stop	$t_{SU:STO}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0.3			us	
Data Setup Time	$t_{SU:DAT}$	100			ns	
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock/Data Fall time	t_{FALL}			300	ns	Min = 20+0.1C_{LOAD} ns
Clock/Data Rise time	t_{RISE}			300	ns	Min = 20+0.1C_{LOAD} ns (Note 3.2)
Capacitive Load	C_{LOAD}			400	pF	per bus line

Note 3.2 300ns rise time max is required for 400kHz bus operation. For lower clock frequencies the maximum rise time is (0.1 / f_{SMB})+ 50ns.

3.4 EEPROM Loader Electrical Specifications (EMC2101-R only)

Table 3.4 EEPROM Loader Electrical Specifications

V_{DD} = 3.0V to 3.6V, T_A = 0°C - 85°C, Typical values are at T_A = 27°C unless otherwise noted						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Interface						
Input High Voltage	V_{IH}	2.1			V	
Input Low Voltage	V_{IL}			0.8	V	
Input High/Low Current	I_{IH} / I_{IL}	-1		1	uA	
Hysteresis			500		mV	
Input Capacitance	C_{IN}		5		pF	
Output Low Sink Current			8		mA	V_{OL} = 0.4V
Timing						
Loading Delay	t_{DLY}		10		ms	Delay after power-up until EEPROM loading begins. (See Section 4.9.)
Loading Time	t_{LOAD}		50		ms	
Clock Frequency	f_{SMB}		50		kHz	
Spike Suppression	t_{SP}			50	ns	
Bus free time Start to Stop	t_{BUF}	1.3			us	
Hold Time: Start	$t_{HD:STA}$	0.6			us	
Setup Time: Start	$t_{SU:STA}$	0.6			us	

Table 3.4 EEPROM Loader Electrical Specifications (continued)

V_{DD} = 3.0V to 3.6V, T_A = 0°C - 85°C, Typical values are at T_A = 27°C unless otherwise noted						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Setup Time: Stop	$t_{SU:STO}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0.3			us	
Data Setup Time	$t_{SU:DAT}$	100			ns	
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock/Data Fall time	t_{FALL}			300	ns	Min = 20+0.1C_{LOAD} ns
Clock/Data Rise time	t_{RISE}			300	ns	Min = 20+0.1C_{LOAD} ns
Capacitive Load	C_{LOAD}			400	pF	per bus line

Chapter 4 System Management Bus Interface Protocol

4.1 System Management Bus Interface Protocol

The EMC2101 communicates with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 4.1. Stretching of the SMCLK signal is supported, however the EMC2101 will not stretch the clock signal.

The EMC2101 powers up as an SMBus client (after loading from EEPROM as applicable).

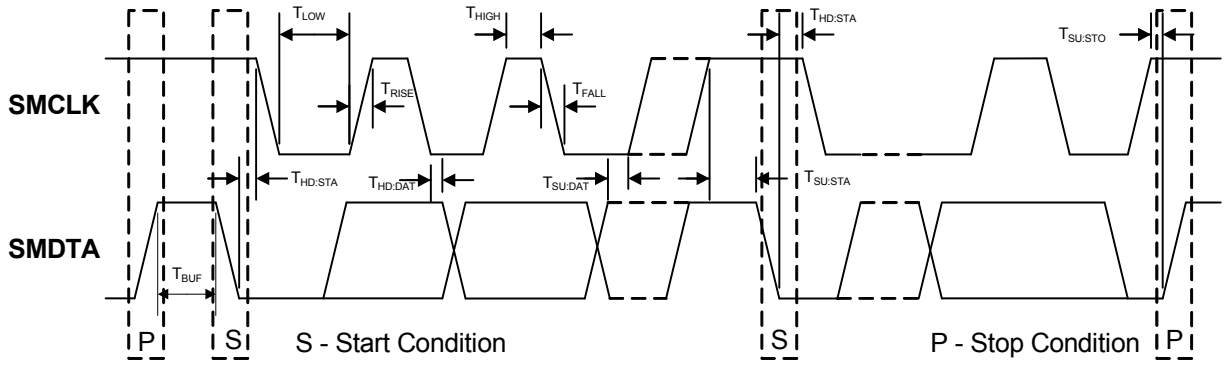


Figure 4.1 SMBus Timing Diagram

The EMC2101 is SMBus 2.0 compatible and supports Send Byte, Read Byte, Receive Byte and the Alert Response Address as valid protocols as shown below.

All of the below protocols use the convention in Table 4.1.

Table 4.1 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST
# of bits sent	# of bits sent

4.2 Write Byte

The Write Byte is used to write one byte of data to the registers as shown below Table 4.2.

Table 4.2 Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
1	7	1	1	8	1	8	1	1

4.3 Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 4.3.

Table 4.3 Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	Register Address	ACK	START	Slave Address	RD	ACK	Register Data	NACK	STOP
1	7	1	1	8	1	1	7	1	1	8	1	1

4.4 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 4.4.

Table 4.4 Send Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	STOP
1	7	1	1	8	1	1

4.5 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 4.5.

Table 4.5 Receive Byte Protocol

START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1	7	1	1	8	1	1

4.6 Alert Response Address

The $\overline{\text{ALERT}}$ / TACH output can be used as a processor interrupt or as an SMBus Alert when configured to operate as an interrupt.

When it detects that the $\overline{\text{ALERT}}$ / TACH pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 000_1100b. All devices with active interrupts will respond with their client address as shown in Table 4.6.

Table 4.6 Alert Response Address Protocol

START	ALERT RESPONSE ADDRESS	RD	ACK	DEVICE ADDRESS	NACK	STOP
1	7	1	1	8	1	1

The EMC2101 will respond to the ARA in the following way when the $\overline{\text{ALERT}}$ / TACH pin is configured as an Interrupt:

1. Send Slave Address and verify that full slave address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
2. Set the MASK bit to clear the $\overline{\text{ALERT}}$ / TACH pin only if there are no bits set in the Status Register. If there are error condition bits set in the Status Register, it must be read before the MASK bit will be set.

When the $\overline{\text{ALERT}}$ / TACH pin is configured to operate in Comparator Mode, or as a TACH input, (see Section 5.4.1), it will not respond to the ARA command. Additionally, the EMC2101 will not respond to the ARA command if the $\overline{\text{ALERT}}$ / TACH pin is not asserted.

4.7 SMBus Address

The EMC2101 is addressed on the SMBus as 100_1100b.

Attempting to communicate with the EMC2101 SMBus interface with an invalid slave address or invalid protocol will result in no response from the device and will not affect its register contents.

4.8 SMBus Time-out

The EMC2101 includes an SMBus time-out feature. Following a 25ms period of inactivity on the SMBus, the device will time-out and reset the SMBus interface.

4.9 Programming from EEPROM

The EMC2101-R acts as a simple SMBus Master to read data from a connected EEPROM using the following procedure:

1. After power-up the EMC2101-R waits for 10ms with the SMDATA and SMCLK pins tri-stated.
2. Once the wait period has elapsed, the EMC2101-R sends a START signal followed by the 7 bit client address 101_0000b followed by a ‘1b’ and waits for an ACK signal from the EEPROM.
3. When the EEPROM sends the ACK signal, the EMC2101-R will send a second start signal and continue sending the Block Read Command (see Table 4.7) to the same slave address. It reads 256 data bytes from the EEPROM sending an ACK between each data byte. When 256 data bytes have been received, it sends a NACK signal followed by a STOP bit.
4. Resets the device as an SMBus Client.

If the EMC2101-R does not receive an acknowledge bit from the EEPROM then the following will occur:

1. The $\overline{\text{ALERT}}$ / TACH pin will be asserted and will remain asserted until a Host device initiates communication with the EMC2101 and reads the Status Register at offset 0x02. The $\overline{\text{ALERT}}$ / TACH pin will be de-asserted after a single Status Register read, i.e. it is not sticky.
2. The EMC2101-R will reset its SMBus protocol as a slave interface and start operating from the default conditions.

Table 4.7 Block Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	Register Address	ACK	START	SLAVE ADDRESS	RD	ACK	Register Data	. . .
1	7	1	1	8	1	1	7	1	1	8	. . .
ACK	Register Data (00h)	ACK	Register Data (01h)	ACK	Register Data (02h)	. . .	ACK	Register Data (FFh)		NACK	STOP
1	8	1	8	1	8	. . .	1	8		1	1

Note: The shaded columns represent data sent from the EMC2101 to the EEPROM device.

APPLICATION NOTE: It is recommended that the EEPROM that is used be an AT24C02B or equivalent device. The EEPROM slave address must be 101_0000b. The device must support a block-read command, 8-bit addressing, and 8-bit data formatting using a 2-wire bus. The device must support 3.3V digital switching logic and may not pull the SMCLK and SMDATA pins above 5V. Data must be transmitted MSB first.

APPLICATION NOTE: No other SMBus Master should exist on the SMDATA and SMCLK lines. The presence of another SMBus Master will cause errors in reading from the EEPROM.

The EEPROM should be loaded to mirror the register set of the EMC2101 with the desired configuration set. All undefined registers in the EMC2101 register set should be loaded with 00h in the EEPROM. Likewise, all registers that are read-only in the EMC2101 register set should be loaded with 00h in the EEPROM.

Because of the interaction between the Fan Control Look-up Table and the Fan Configuration Register, the EEPROM Loader stores the contents of the Fan Configuration Register and updates this register at the end of the EEPROM loading cycle. (See Section 6.16 and Section 6.22).

Chapter 5 General Description

The EMC2101 is an environmental monitoring device with a selectable PWM or DAC fan driver output, one external temperature monitoring channel and one internal temperature monitor. It contains advanced circuitry to remove errors induced by series resistance and CPU thermal diode process differences to provide accurate temperature measurements and accurate fan control.

Thermal management is performed automatically. The EMC2101 reads the temperature from both the external and internal temperature diodes and uses the external temperature data to control the fan speed.

The FAN output can be configured as a PWM (default) or DAC output. The PWM fan driver uses an eight entry look up table to create a programmable temperature response. The DAC output provides a linear drive for the system fan circuit using this same look up table.

Each temperature measurement channel is continuously compared against programmed high limits. The external diode channel is compared against a programmed low limit. $\overline{\text{ALERT}}$ / TACH interrupt pin is asserted if the measured value exceeds the high limit or drops below the low limit. In addition, the external diode contains a programmable critical temperature, TCRIT. If the measured temperature exceeds this T_{CRIT} an interrupt is asserted on the $\overline{\text{ALERT}}$ / TACH pin and the fan is set to full on.

Finally, the EMC2101-R (only) has two configuration modes and two default fan settings based on the value of the pull-up-resistor on the $\overline{\text{ALERT}}$ / TACH pin. In the Manual Configuration Mode, the device acts as an SMBus client and waits to be configured by the system SMBus host. In the Automatic Configuration mode, the device automatically queries the SMBus for an EEPROM device and uploads configuration information from the EEPROM into its internal registers.

Figure 5.1 shows a system level block diagram of the EMC2101. Figure 5.2 shows a system level block diagram of the EMC2101-R.

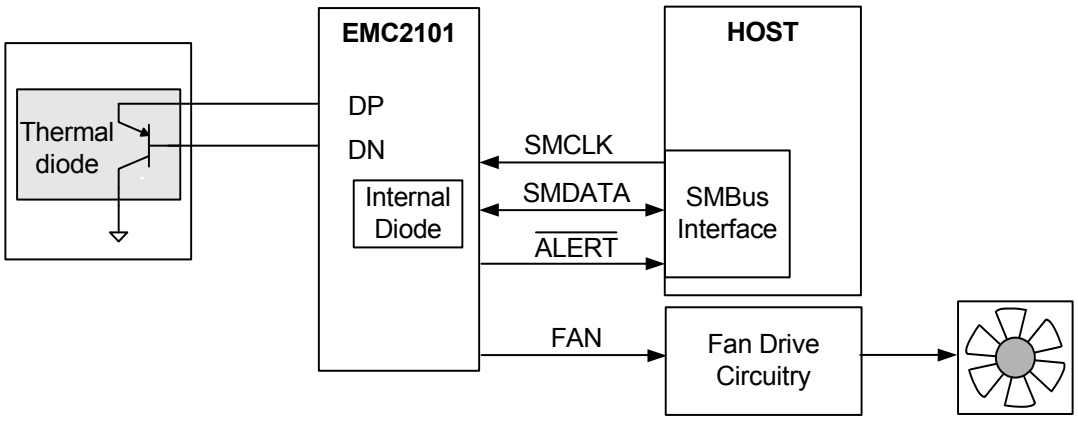


Figure 5.1 System Diagram for EMC2101

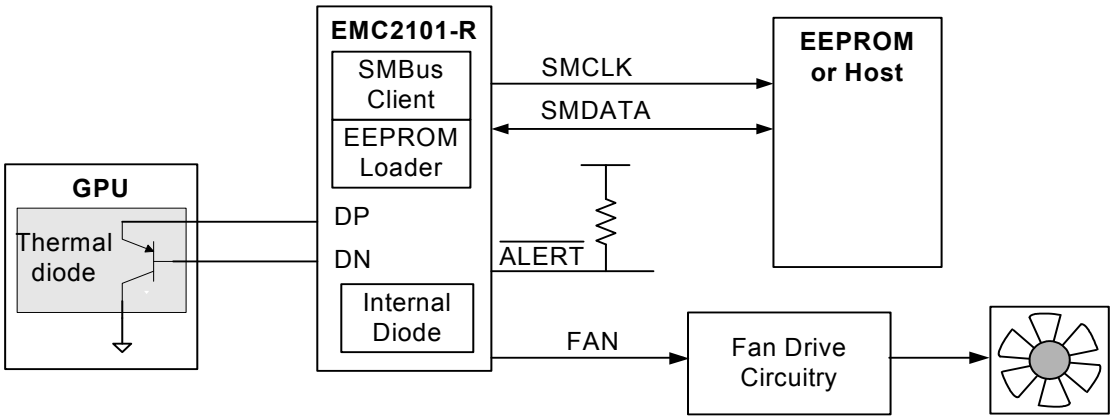


Figure 5.2 System Diagram for EMC2101-R

5.1 Modes of Operation (EMC2101-R Only)

The EMC2101-R has two modes of operation based on the pull-up resistor on the $\overline{\text{ALERT}}$ pin (see Table 5.1). The modes of operation are:

1. Host Configuration Mode - An SMBus Host configures the EMC2101-R upon startup to allow for polling for temperature or fan information or the user can use the $\overline{\text{ALERT}}$ pin interrupt to determine which action is required.
2. Automatic Configuration Mode - The EMC2101-R queries an SMBus compatible EEPROM located at a known address (see Section 4.9) and automatically loads its registers with the contents of the EEPROM. This mode does not require host intervention but a host can poll the device for temperature and fan information.

5.2 Power Up (EMC2101-R Only)

The EMC2101-R (only) will power up with the fan driver set to either 100% duty cycle or 0% duty cycle, depending on the value of the pull-up resistor on the $\overline{\text{ALERT}}$ / TACH pin. (See Table 5.1.) It will remain in this state until either the Fan Setting Register is written or until the following activities have occurred:

1. The Fan Control Look-Up Table is loaded and the PROG bit is set to ‘0’
2. The temperature monitoring block performs its first comparison against the Look-Up Table.

If the Fan Control Look-Up Table is used, the EMC2101-R Fan Driver will be immediately set to the appropriate setting in the table based on the measured temperature.

5.3 Power Modes

The EMC2101 supports multiple power modes that are user configurable. The temperature monitoring and fan control functions of the device are independent. The power modes are:

1. Normal - the temperature monitoring and fan driver circuits are both active. The device updates all temperature channels at the user programmed conversion rate (see Table 6.6). Every time the temperature is updated, the limits are checked and the fan driver is updated based on the values in the Fan Control Look-Up Table (if the Fan Control Look-Up Table is enabled).
2. Standby - the temperature monitoring and fan driver circuits are both disabled. The device will not update temperature data automatically and the fan output will be set to default drive. A one-shot

command can be issued that will refresh the temperature data. The limits are only checked when the temperature data is updated.

3. Mixed - the temperature monitoring block is disabled, but the fan driver block is active. The device will not update temperature data automatically and the fan driver output will not be updated automatically based on temperature. A one-shot command can be issued that will refresh the temperature data and update the fan driver based on the values in the Fan Control Look-Up Table (if the Fan Control Look-Up Table is enabled).

5.4 $\overline{\text{ALERT}}$ / TACH Output

The $\overline{\text{ALERT}}$ / TACH pin (Pin 6) is an open drain output and requires a pull-up resistor to V_{DD} when configured as an ALERT output.

APPLICATION NOTE: When configured as a TACH input, the $\overline{\text{ALERT}}$ / TACH pin will not function as an ALERT output. Error conditions will not trigger an interrupt (though will be updated in the Status Registers as normal) and the MASK bits will do nothing. Likewise, the device will not respond to the ARA command.

For the EMC2101-R, the value of this pull-up resistor determines the initial FAN output mode of operation as well as whether the device auto loads from an EEPROM or via an SMBus host per Table 5.1.

After power-up, the EMC2101-R requires 10ms to initialize and determine the operating mode.

When configured as an interrupt, the $\overline{\text{ALERT}}$ / TACH pin is maskable for each alert condition. If the $\overline{\text{ALERT}}$ / TACH pin is masked, then it will not respond to the corresponding condition (though the Alert Status Register will update normally). This pin has multiple functions described below and is controlled by ALERT_COMP bit (bit 0) in the Averaging Filter Register (BFh) (see Section 6.23).

Table 5.1 $\overline{\text{ALERT}}$/ TACH Pull-up Resistors - SMBus / FAN MODE for EMC2101-R

$\overline{\text{ALERT}}$ / TACH PULL-UP RESISTOR	SMBUS MODE	FAN MODE	POLARITY BIT SETTING (SEE Section 6.16)
5.6k Ohm ±5%	Host Load via SMBus	FAN output initialize to 100% Duty Cycle	1
10k Ohm ±5%	Host Load via SMBus	FAN output initialize to 0% Duty Cycle	0
18k Ohm ±5%	Auto Load via EEPROM	FAN output initialize to 100% Duty Cycle	1
33k Ohm ±5%	Auto Load via EEPROM	FAN output initialize to 0% Duty Cycle	0

5.4.1 $\overline{\text{ALERT}}$ / TACH as a Temperature Comparator

When the $\overline{\text{ALERT}}$ / TACH pin is used as a temperature comparator, the $\overline{\text{ALERT}}$ / TACH output is asserted when an out of limit measurement (> high limit, < low limit, or > TCRIT limit) is detected on any diode (low limits only apply to the external diode channel) or when the external diode connections are open. When the condition is no longer true, the $\overline{\text{ALERT}}$ / TACH output will de-assert. Reading from the Status Register will cause the $\overline{\text{ALERT}}$ / TACH pin to be released however it will not prevent it from being re-asserted based on the temperature comparisons.

Setting the MASK bit will not affect the $\overline{\text{ALERT}}$ / TACH pin when it is configured as a temperature comparator, however the individual channel mask bits will block the $\overline{\text{ALERT}}$ / TACH pin from being asserted.

5.4.2 $\overline{\text{ALERT}}$ / TACH as an Interrupt

When the $\overline{\text{ALERT}}$ / TACH pin is used as an interrupt signal the pin is asserted whenever an out-of-limit condition is detected. The $\overline{\text{ALERT}}$ / TACH pin will remain asserted until it is cleared even if the error condition is removed.

5.4.3 Mask Bit

The MASK bit behaves differently depending on which mode the $\overline{\text{ALERT}}$ / TACH pin is configured to operate in.

If the EMC2101 is configured with the $\overline{\text{ALERT}}$ / TACH pin operating in Interrupt Mode, the MASK bit will be set in the following cases:

1. Automatically after the Status Register has been read if any bits in the Status Register have been set (except BUSY and FAULT) (See Table 6.3).
2. Automatically when the EMC2101 responds to an Alert Response Address (ARA) command on an SMBus and the $\overline{\text{ALERT}}$ / TACH pin is asserted. The ARA command does not clear the Status Register. If the MASK bit is cleared prior to reading and clearing the Status Register, then the $\overline{\text{ALERT}}$ / TACH pin will be asserted.
3. Directly via the SMBus.

In Interrupt Mode, the MASK bit will block the $\overline{\text{ALERT}}$ / TACH pin from being asserted in response to an error condition.

If the EMC2101 is configured with the $\overline{\text{ALERT}}$ / TACH pin operating in Comparator Mode, the MASK bit can only be set via the SMBus. In this mode, setting the MASK bit willl not affect the $\overline{\text{ALERT}}$ / TACH pin.

In either mode, setting the individual channel mask bits will block the appropriate channel from asserting the $\overline{\text{ALERT}}$ / TACH pin.

5.5 Temperature Monitors

In general, thermal diode temperature measurements are based on the change in forward bias voltage of a diode when operated at two different currents. The change in forward bias voltage is proportional to absolute temperature (T).

$$\Delta V_{BE} = V_{BE_HIGH} - V_{BE_LOW} = \frac{\eta k T}{q} \ln\left(\frac{I_{HIGH}}{I_{LOW}}\right) \quad \textbf{Eq: [1]}$$

Where:

k = Boltzmann's constant

T = Absolute Temperature in Kelvin

q = electron charge

η = Diode Ideality Factor

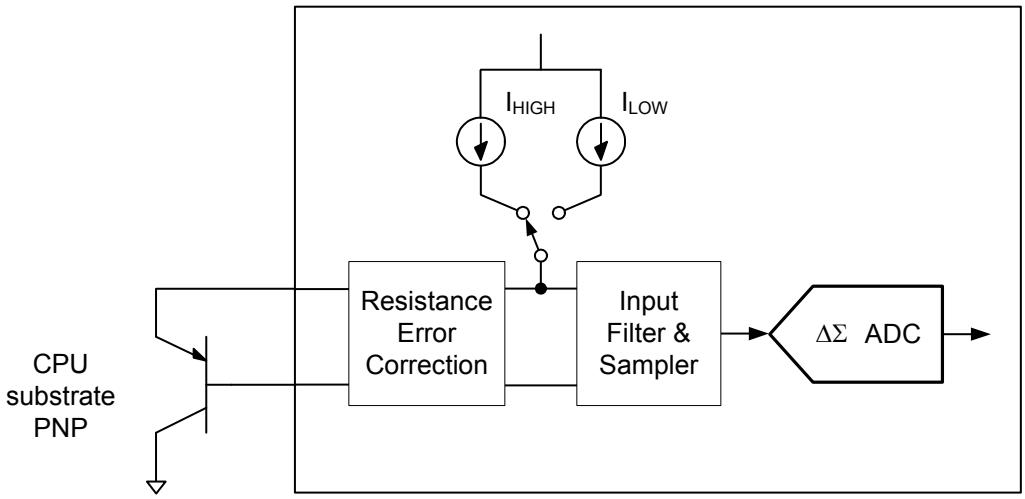


Figure 5.3 Block Diagram of Temperature Monitoring Circuit

Figure 5.3 shows a block diagram of the temperature measurement circuit. As shown, the EMC2101 incorporates a delta-sigma analog to digital converter that integrates the temperature diode voltage from multiple bias currents.

The external temperature diodes can be connected as shown in Figure 5.4.

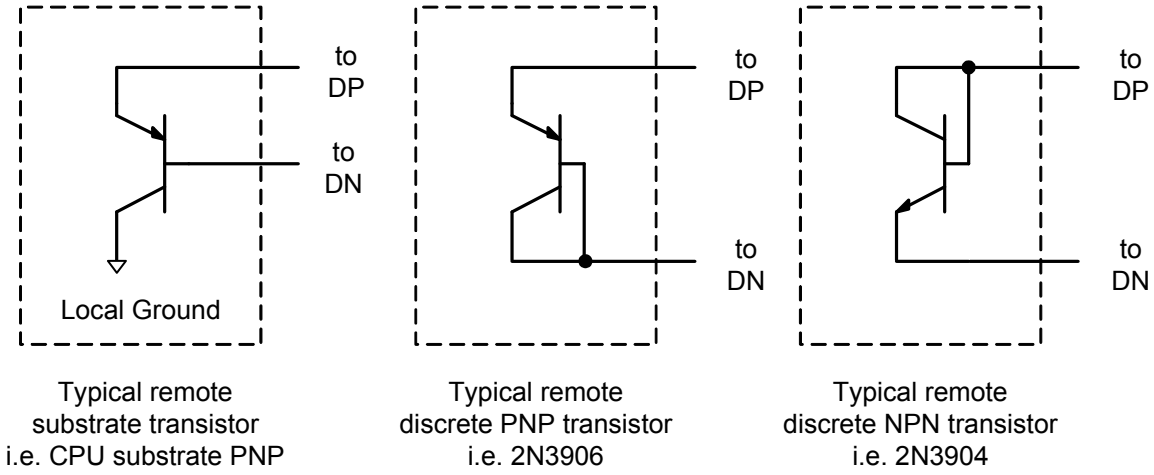


Figure 5.4 External Diode configurations

5.5.1 Temperature Measurement Results and Data

The results of the internal and external temperature measurements are stored in the internal and external temperature registers respectively. These are then compared with the values stored in the High Limit Registers. The internal temperature measurements are stored in 8-bit format while the external temperature measurements are stored in 11-bit format.

The EMC2101 measures temperatures from -64°C to 127°C represented as a binary two's complement number. Internal temperatures are in 1°C steps, external temperatures are in 0.125°C steps.

Table 5.2 shows the temperature format for the external diode and Table 5.3 shows the temperature format for the internal diode.

Table 5.2 EMC2101 External Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)
<= -64	1 1 0 0 0 0 0 0 0 0 0
-55	1 1 0 0 1 0 0 1 0 0 0
-1	1 1 1 1 1 1 1 1 0 0 0
-0.125	1 1 1 1 1 1 1 1 1 1 1
0	0 0 0 0 0 0 0 0 0 0 0
0.125	0 0 0 0 0 0 0 0 0 0 1
1	0 0 0 0 0 0 0 1 0 0 0
25	0 0 0 1 1 0 0 1 0 0 0
125	0 1 1 1 1 1 0 1 0 0 0
>= 127.875	0 1 1 1 1 1 1 1 1 1 0
Diode Fault (Open condition)	0 1 1 1 1 1 1 1 0 0 0
Diode Fault (Short condition)	0 1 1 1 1 1 1 1 1 1 1

Table 5.3 EMC2101 Internal Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)
<= -64	1 1 0 0 0 0 0 0
-55	1 1 0 0 1 0 0 1
-1	1 1 1 1 1 1 1 1
0	0 0 0 0 0 0 0 0
1	0 0 0 0 0 0 0 1
25	0 0 0 1 1 0 0 1
125	0 1 1 1 1 1 0 1
126	0 1 1 1 1 1 1 0
>= 127	0 1 1 1 1 1 1 1

5.5.2 Temperature Filter

The EMC2101 contains variable filtering options to suppress thermally or electrically noisy signals on the External Diode lines. This filter can be configured as Level 1, Level 2, or Disabled (see Section 6.23). The typical filter performance is shown in Figure 5.5 and Figure 5.6.

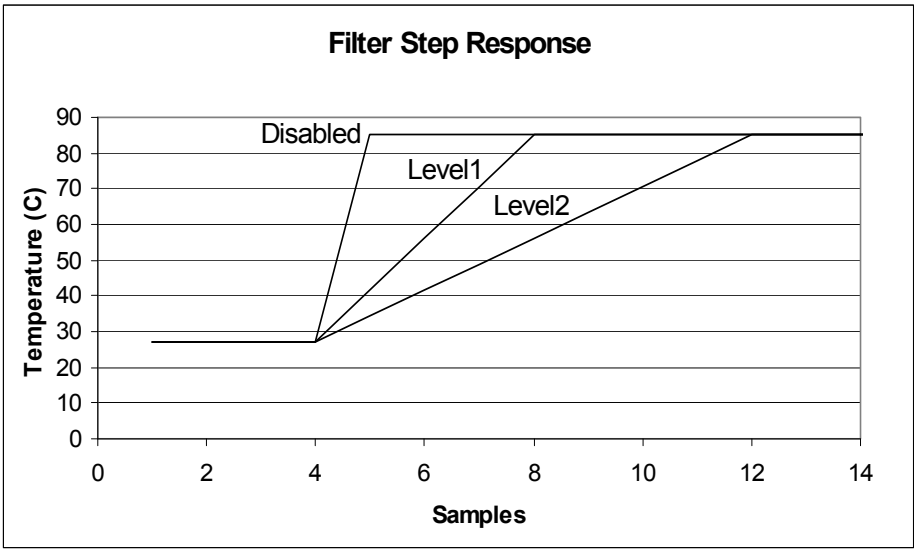


Figure 5.5 Temperature Filter Step Response

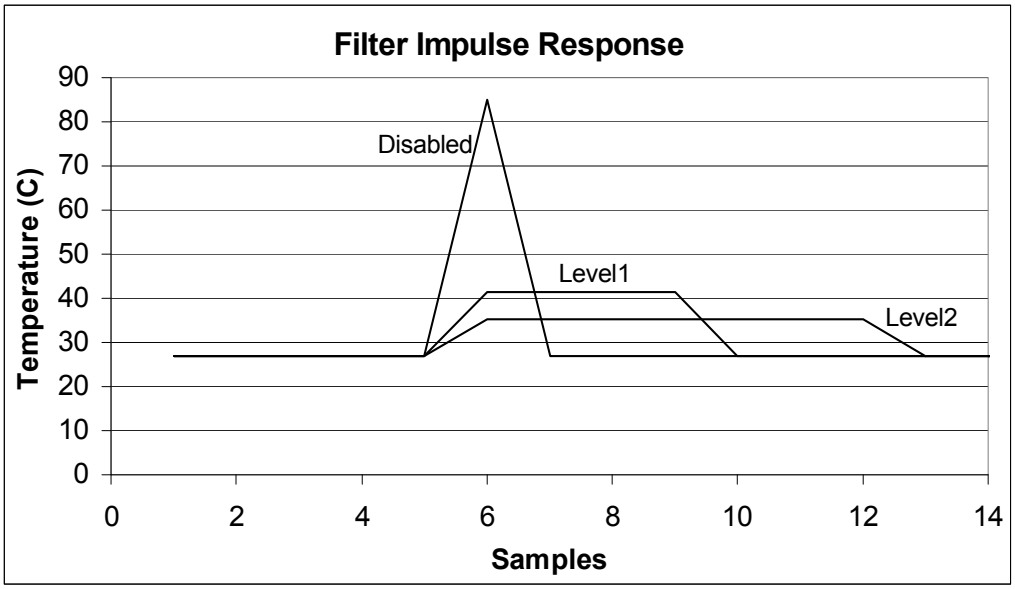


Figure 5.6 Temperature Filter Impulse Response

5.5.3 Beta Compensation

The EMC2101 is software configurable to monitor the temperature of basic diodes (e.g. 2N3904), or CPU thermal diodes. It automatically detects the type of external diode (CPU diode, diode connected transistor, or PN diode) and determines the optimal setting to reduce temperature errors introduced by beta variation.

5.5.4 Resistance Error Correction (REC)

Parasitic resistance in series with the external diode limits the accuracy obtainable from temperature measurement devices. The voltage developed across this resistance by the switching diode currents cause the temperature measurement to read higher than the true temperature. Contributors to series resistance are PCB trace resistance, on die (i.e. on the processor) metal resistance, bulk resistance in the base and emitter of the temperature transistor. Typically, the error caused by series resistance is +0.7°C per ohm. Temperature errors caused by up to 100Ω of series resistance are automatically corrected.

5.5.5 Programmable Ideality Factor

The EMC2101 is designed for an external diode with an ideality factor of 1.008. When an external diode, processor or discrete, has a different ideality factor, an error is introduced in the temperature measurement which must be corrected. This is typically done using programmable offset registers but this correction is only accurate at one temperature since an ideality factor mismatch introduces an error that is a linear function of temperature. To provide maximum flexibility to the user, the EMC2101 provides a 6-bit register to set the ideality factor for the external diode which eliminates errors across all temperatures. (See Table 6.13.)

APPLICATION NOTE: This feature is only required in rare circumstances. The majority of errors introduced are corrected with the Beta Compensation and Resistance Error Correction circuitry.

5.5.6 Diode Faults

The EMC2101 detects the major types of diode faults; an open input DP-DN, a short across DP-DN, short to GND, and short to V_{DD}. For each temperature measurement made, the device checks for a diode fault on the external diode.

If an open fault or a short of the DP pin to VDD is detected, then the temperature data is changed to +127C and the Fault bit in the Status Register will bet set. If the high and / or TCRIT limits are set below this value, and they are not masked, then the $\overline{\text{ALERT}}$ / TACH pin will be asserted. In addition, the HIGH and TCRIT status bits will be set accordingly.

If a short between the diode pins or a short to GND is detected, then the temperature data is changed to +127.875°C. If the high and / or TCRIT limits are set below this value, and they are not masked, then the $\overline{\text{ALERT}}$ / TACH pin will be asserted. In addition, the HIGH and TCRIT status bits will be set accordingly. The FAULT bit will not be set.

APPLICATION NOTE: If the Temperature Filter is enabled and a diode fault occurs, the diode fault status bit will be set and the temperature data is updated immediately. The Filter will stop accumulating data so long as the diode fault remains in effect.

APPLICATION NOTE: When a Diode Fault is detected, the $\overline{\text{ALERT}}$ / TACH pin behavior is still subject to the Fault Queue.

5.6 Fan Control

The EMC2101 includes either a PWM or a linear DAC based fan driver on the shared FAN pin. Both PWM and DAC use the Fan Control Look-Up Table and/or Fan Setting Register interchangeably as well as the Spin-Up Routine.

In addition, the EMC2101 can monitor the fan speed using the $\overline{\text{ALERT}}$ / TACH pin.

5.6.1 DAC Driver

The Linear DAC driver included in the EMC2101 has 6-bits of resolution based on the supply voltage and is used for linear drive fan circuits. Its advantages over PWM drive circuits include reduced circuit complexity at the expense of reduced effective signal range.

APPLICATION NOTE: When using the DAC Driver, the pull-up resistor on the FAN pin should be removed.

APPLICATION NOTE: The DAC driver output voltage is controlled by either the Fan Setting Register (see Section 6.18) or the Fan Control Look-Up Table Registers (see Section 6.22). It is also controlled by the POLARITY bit (see Section 6.16). The PWM Frequency Register (see Section 6.19) and PWM Divider Register (see Section 6.20) have no effect on the DAC's output voltage range, resolution, or response.

5.6.2 PWM Driver

The PWM driver included in the EMC2101 has, at most, 64 steps equalling 1.5% resolution. The effective resolution, duty cycle, and frequency are all adjustable based on programmed values. It's advantages over linear drive circuits include a large signal range (0% to 100% duty cycle) at the expense of added complexity on the drive circuit.

The PWM output is open drain and requires a pull-up resistor to VDD.

5.6.3 TACH Monitor

The TACH monitor counts the number of clock pulses that occur between five edges of the TACH signal. The monitor assumes that the tachometer signal is always valid (such as generated from a 4-wire fan or a direct drive fan) and that the tachometer signal generates 2 TACH pulses per fan revolution.

5.6.4 Fan Control Look-Up Table

The EMC2101 uses an 8 entry look-up table to apply a user-programmable fan control profile based on measured temperature. The user programs the Fan Control Look-Up Table using incrementally higher temperatures and the desired fan output that should be set when that temperature is reached.

If the measured temperature on the External Diode channel exceeds any of these temperature thresholds, the fan output will be automatically programmed to the desired setting corresponding to the exceeded temperature. When the measured temperature drops to a point below any lower threshold minus the hysteresis value, the fan output will be set to the corresponding lower set point.

Figure 5.7 shows an example of this operation.

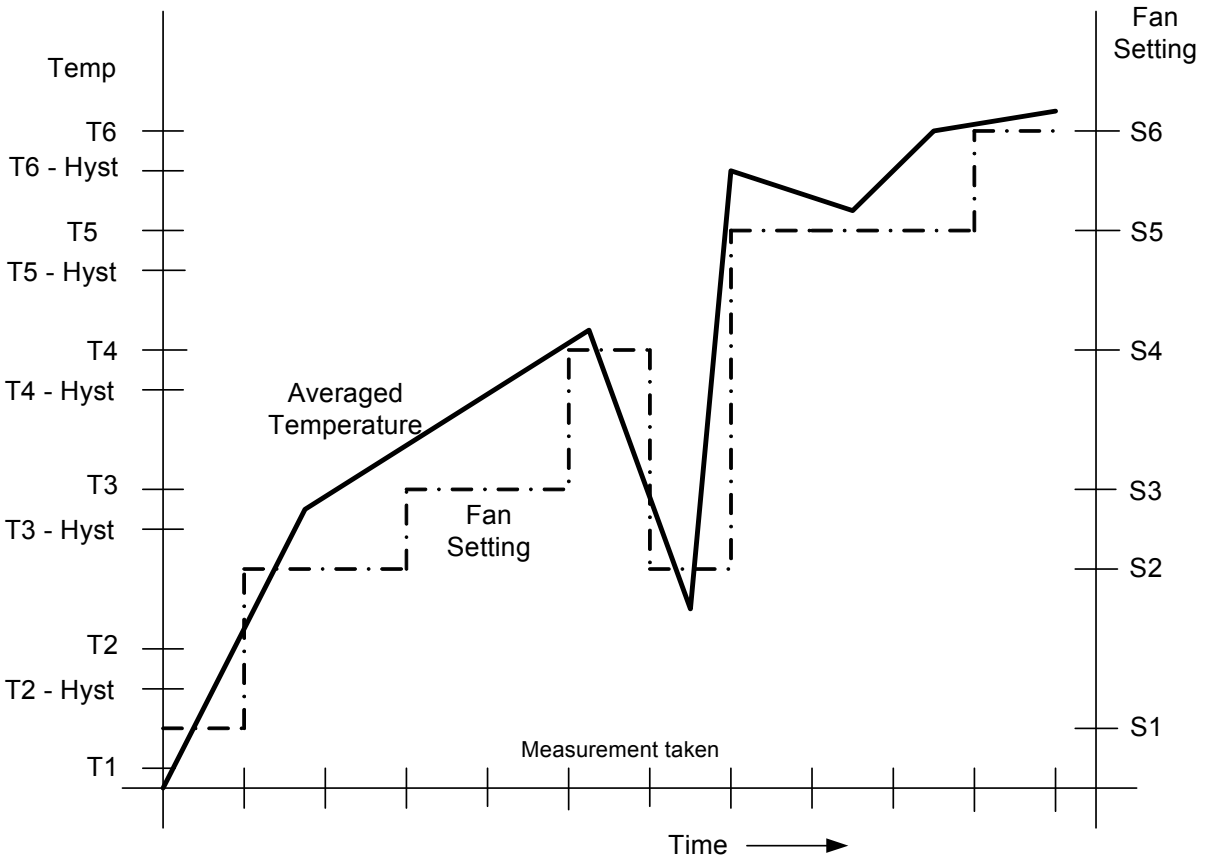


Figure 5.7 Fan Control Look-Up Table Example

If the Fan Control Look-Up Table is not used, the user may program the fan output directly by writing to the Fan Setting Register (4Ch - see Section 6.18).

5.7 Fault Queue

The EMC2101 supports a Fault Queue feature to reduce interrupts caused by spurious temperature readings. This feature, (see Section 6.5), will not trigger an interrupt until the device has measured three consecutive out-of-limit HIGH, LOW, or T_CRIT temperature readings. Figure 5.8 shows an example of this behavior. The Fault Queue only applies to the External Diode channels.

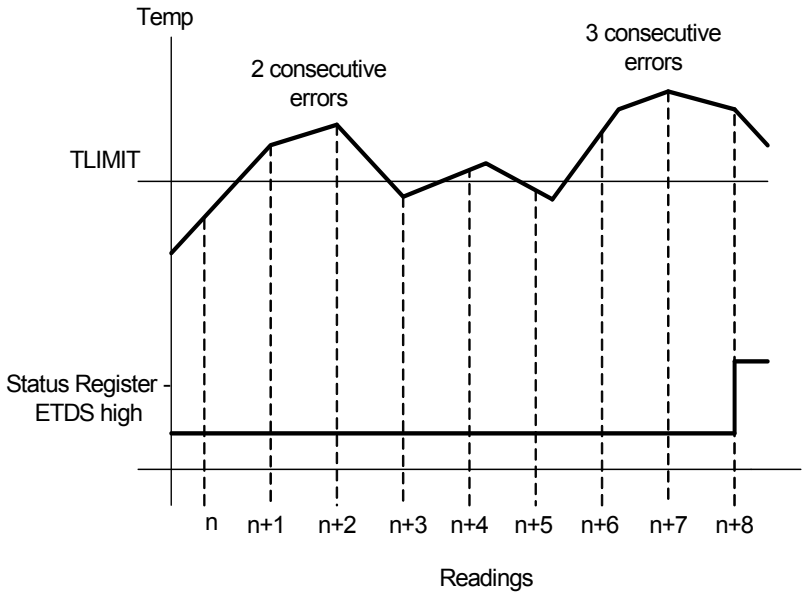


Figure 5.8 Example Fault Queue Response

Chapter 6 Register Set

The following registers are accessible through the SMBus Interface. The registers are described in functional order. Registers with multiple addresses are included for software compatibility. Writing or reading from either address will point to the same internal register.

Table 6.1 Register Set in Hexadecimal Order

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
00h	R	Internal Temperature	Stores the Internal Temperature	00h	Page 33
01h	R	External Diode Temperature High Byte	Stores the External Temperature High Byte	00h	Page 33
02h	R	Status	Reports internal, external, and TCRIT alarms	00h	Page 33
03h and 09h	R/W	Configuration	Alert Mask, STANDBY, TCRIT override, Alert Fault Queue	00h	Page 34
04h and 0Ah	R/W	Conversion Rate	Sets conversion rate	08h (16 / sec)	Page 35
05h and 0Bh	R/W	Internal Temp Limit	$\overline{\text{ALERT}}$ / TACH asserted if measured temp above this value	46h (70°C)	Page 36
07h and 0Dh	R/W	External Temp High Limit High Byte	$\overline{\text{ALERT}}$ / TACH asserted if measured temp above this value	46h (70°C)	Page 36
08h and 0Eh	R/W	External Temp Low Limit High Byte	$\overline{\text{ALERT}}$ / TACH asserted if measured temp below this value	00h (0°C)	Page 36
0Ch	R/W	External Temperature Force	Force the temperature for determining the next fan speed used in the Fan Control Look-Up Table	00h	Page 36
0Fh	R/W	One Shot	When written, performs a one-shot conversion.	00h	Page 37
10h	R	External Diode Temperature Low Byte	Stores the External Temperature Low Byte	00h	Page 33
11h	R/W	Scratchpad	Scratchpad - This register is read/write but does nothing	00h	Page 37
12h	R/W	Scratchpad	Scratchpad - This register is read/write but does nothing	00h	Page 37
13h	R/W	External Diode High Limit Low Byte	Fractional data of High Limit	00h	Page 36
14h	R/W	External Diode Low Limit Low Byte	Fractional data of Low Limit	00h	Page 36
16h	R/W	Alert Mask	Disables alarms	A4h	Page 37

Table 6.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
17h	R/W	External Diode Ideality Factor	Sets ideality factor based on diode type	12h (1.008)	Page 38
18h	R/W	Beta Compensation Factor	Compensates for transistors with various beta factors	08h	Page 39
19h	R/W	TCRIT Temp Limit	Fan will be set to full speed if external temp above this value	55h (85°C)	Page 36
21h	R/W	TCRIT Hysteresis	Amount of hysteresis applied to TCRIT Temp (1LSB = 1°C)	0Ah (10°C)	Page 36
46h	R	TACH Reading Low Byte	Stores the lower 6 bits of the TACH count. and the TACH configuration bits	FFh	Page 40
47h	R	TACH Reading High Byte	Stores the upper 8 bits of the TACH count.	FFh	Page 40
48h	R/W	TACH Limit Low Byte	Stores the lower 6 bits of the TACH Limit	FFh	Page 40
49h	R/W	TACH Limit High Byte	Stores the upper 8 bits of the TACH Limit	FFh	Page 40
4Ah	R/W	FAN Configuration	defines polarity of PWM or DAC	20h	Page 41
4Bh	R/W	Fan Spin-up	Sets Spin Up options	3Fh	Page 42
4Ch	R/W	Fan Setting	Sets PWM or DAC value	00h	Page 43
4Dh	R/W	PWM Frequency	Sets the final PWM Frequency	17h	Page 44
4Eh	R/W	PWM Frequency Divide	Sets the base PWM frequency	01h	Page 44
4Fh	R/W	Lookup Table Hysteresis	Amount of hysteresis applied to Lookup Table Temp (1LSB = 1°C)	04h (4°C)	Page 45
50h	R/W (See Note 6.1)	Lookup Table Temp Setting 1	Look Up Table Temperature Setting 1	7Fh	Page 46
51h	R/W (See Note 6.1)	Lookup Table Fan Setting 1	Associated Fan Setting for Temp Setting 1	3Fh	Page 46
52h	R/W (See Note 6.1)	Lookup Table Temp Setting 2	Look Up Table Temperature Setting 2	7Fh	Page 46
53h	R/W (See Note 6.1)	Lookup Table Fan Setting 2	Associated Fan Setting for Temp Setting 2	3Fh	Page 46
54h	R/W (See Note 6.1)	Lookup Table Temp Setting 3	Look Up Table Temperature Setting 3	7Fh	Page 46
55h	R/W (See Note 6.1)	Lookup Table Fan Setting 3	Associated Fan Setting for Temp Setting 3	3Fh	Page 46
56h	R/W (See Note 6.1)	Lookup Table Temp Setting 4	Look Up Table Temperature Setting 4	7Fh	Page 46

Table 6.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
57h	R/W (See Note 6.1)	Lookup Table Fan Setting 4	Associated Fan Setting for Temp Setting 4	3Fh	Page 46
58h	R/W (See Note 6.1)	Lookup Table Temp Setting 5	Look Up Table Temperature Setting 5	7Fh	Page 46
59h	R/W (See Note 6.1)	Lookup Table Fan Setting 5	Associated Fan Setting for Temp Setting 5	3Fh	Page 46
5Ah	R/W (See Note 6.1)	Lookup Table Temp Setting 6	Look Up Table Temperature Setting 6	7Fh	Page 46
5Bh	R/W (See Note 6.1)	Lookup Table Fan Setting 6	Associated Fan Setting for Temp Setting 6	3Fh	Page 46
5Ch	R/W (See Note 6.1)	Lookup Table Temp Setting 7	Look Up Table Temperature Setting 7	7Fh	Page 46
5Dh	R/W (See Note 6.1)	Lookup Table Fan Setting 7	Associated Fan Setting for Temp Setting 7	3Fh	Page 46
5Eh	R/W (See Note 6.1)	Lookup Table Temp Setting 8	Look Up Table Temperature Setting 8	7Fh	Page 46
5Fh	R/W (See Note 6.1)	Lookup Table Fan Setting 8	Associated Fan Setting for Temp Setting 8	3Fh	Page 46
BFh	R/W	Averaging Filter	Selects averaging function for external diode	00h	Page 47
FDh	R	Product ID	ID	16h or 28h	Page 48
FEh	R	Manufacturer ID	SMSC	5Dh	Page 48
FFh	R	Revision Register	REV	01h	Page 48

Note 6.1 The Look Up Table Registers are made Read Only if the PWM Program bit (bit 5) in PWM Configuration Register (4Ah) is set.

6.1 Data Read Interlock

When the External Diode High Byte Register is read, the External Diode Low byte is copied into an internal ‘shadow’ register. The user is free to read the low byte at any time and be guaranteed that it will correspond to the previously read high byte. Regardless if the low byte is read or not, reading from an External Diode High Byte Register will automatically refresh this stored low byte data.

When the TACH Reading Low Byte Register is read, the TACH Reading high byte is copied into an internal ‘shadow’ register. The user is free to read the high byte at any time and be guaranteed that it will correspond to the previously read low byte. Regardless if the high byte is read or not, reading from the TACH Reading Low Byte Register will automatically refresh this stored high byte data.

6.2 Register Descriptions

The registers are described in detail below. A bit entry of a ‘-’ indicates that the bit is not used and will always read 0.

6.3 Temperature Data Registers

Table 6.2 Temperature Data Registers

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
00h	R	Internal Temperature	Sign	64	32	16	8	4	2	1	00h
01h	R	External Diode Temperature High Byte	Sign	64	32	16	8	4	2	1	00h
10h	R	External Diode Temperature Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h

As shown in Table 6.2, the internal temperature monitor is stored as an 8-bit value while the external temperature is stored as an 11-bit value.

Please note that the internal temperature monitor is limited to the operating temperature limits of the part resulting in a guaranteed range of 0ºC to 85ºC.

6.4 Status Register

Table 6.3 Status Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
02h	R	Status	BUSY	INT_HIGH	EEPROM	EXT_HIGH	EXT_LOW	FAULT	TCRIT	TACH	00h

The Status Register is a read only register and returns the operational status of the part.

If the $\overline{\text{ALERT}}$ / TACH pin is configured as an $\overline{\text{ALERT}}$ output and any of these bits are set to '1' (except the BUSY bit and the FAULT bit), then the $\overline{\text{ALERT}}$ / TACH pin is asserted low (if interrupts are not masked (see Section 6.5).

Reading from the Status Register will cause the MASK bit to be set if any bit (other than BUSY and FAULT) have been set. Each bit is automatically cleared when the error condition has been removed, however the internal error condition flags may still be set. The ARA command must be used to clear the $\overline{\text{ALERT}}$ / TACH pin if there are no bits set in the Status Register. In addition, reading from the Status Register will clear all bits. If the error condition persists, then the bits will be reset at the end of the next conversion.

When the device is configured in Comparison Mode (see Section 6.23), reading the Status Register will not clear any active status bits (except EEPROM and FAULT). These bits are automatically cleared when the error condition is removed.

Bit 7 - Busy - indicates that the ADC is converting - does not trigger an interrupt.

Bit 6 - INT_HIGH - Internal temperature has met or exceeded the high limit.

Bit 5 - EEPROM - Indicates that the EEPROM could not be found when the device powers up in the Auto-Program Mode (see Section 5.1). This bit only applies to the EMC2102-R. It will always read ‘0’ for the EMC2101 device.

Bit 4 - EXT_HIGH - External Diode temperature has exceeded the high limit.

Bit 3 - EXT_LOW - External Diode temperature has fallen below the low limit.

Bit 2 - FAULT - A diode fault has occurred on the External Diode.

Bit 1 - TCRIT - External Diode Temperature has met or exceeded the TCRIT limit.

Bit 0 - TACH - The TACH count has exceeded the TACH Limit.

6.5 Configuration Register

Table 6.4 Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
03h and 09h	R/W	Configuration	MASK	STANDBY	FAN_ STANDBY	DAC	DIS_ TO	ALT_ TCH	TCRIT OVRD	QUEUE	00h

The configuration register controls the basic functionality of the EMC2101. The bits are described below:

Bit 7 - MASK - Masks the $\overline{\text{ALERT}}$ / TACH pin functionality when the device is configured as an ALERT output in Interrupt Mode. This bit is ignored if the $\overline{\text{ALERT}}$ / TACH pin is configured as an ALERT output in Comparator Mode or if it is configured as a TACH input.

The internal error condition flags are not affected by setting the MASK bit. Therefore, if the MASK bit is set manually (instead of by reading the Status Register or sending the ARA command), and it is cleared, the $\overline{\text{ALERT}}$ / TACH pin may be reasserted without any apparent error conditions present. It is not recommended that the MASK bit be manually set to clear the $\overline{\text{ALERT}}$ / TACH pin.

- '0' (default) - The $\overline{\text{ALERT}}$ / TACH pin will be asserted if any bit is set in the Status Register. Once the pin is asserted, it will remain asserted.
- '1' - the $\overline{\text{ALERT}}$ / TACH pin will be masked and will not generate an interrupt. The Status Register will still be updated normally.

Bit 6- STANDBY - Determines operational mode of the device.

- '0' (default) - Operational mode, monitoring temperatures, updating FAN output
- '1' - Low power standby mode. In this mode, the Temperature monitor is disabled and the Fan drivers may be disabled depending on the status of the FAN_STANDBY bit.

Bit 5 - FAN_STANDBY - Determines the operation of the FAN driver when the device is put into low power standby mode.

- '0' (default) - FAN output will remain active when the STANDBY bit is set.
- '1' - FAN output will be inactive when the STANBDY bit is set. The driver will be set at the default drive based on the pull-up resistors on the $\overline{\text{ALERT}}$ / TACH pin (see Table 5.1).

Bit 4 - DAC - Determines FAN output mode

- '0' (default) - PWM output enabled at FAN pin.
- '1' - DAC output enabled at FAN pin.

Bit 3 - DIS_TO - disables the SMBus Time-out functionality.

- '0' (default) - the SMBus Time-out functionality is enabled and will reset the client block if the clock is held in a single state for more than 25ms and less than 35ms.
- '1' - the SMBus Time-out functionality is disabled. The client block will only reset if it receives a STOP bit.

Bit 2 - ALT_TCH - Determines the functionality of the $\overline{\text{ALERT}}$ / TACH pin.

- '0' (default) - The $\overline{\text{ALERT}}$ / TACH pin will function as an open drain, active low interrupt.
- '1' - The $\overline{\text{ALERT}}$ / TACH pin will function as a high impedance TACH input. This may require an external pull-up resistor to set the proper signaling levels.

Bit 1 - TCRITOVRD - Allows the TCRIT limit to be overridden.

- '0' (default) - TCRIT limit is set to default value and locked.
- '1' - The TCRIT limit is unlocked for modification. The TCRIT limit can only be changed once. To adjust TCRIT again, a power cycle is required.

Bit 0 - QUEUE - Sets the number of external diode over-temp measurements required to assert $\overline{\text{ALERT}}$ / TACH pin.

- '0' (default) - $\overline{\text{ALERT}}$ / TACH pin is asserted (and status bit set) after one external temperature measurement exceeds the high limit or the TCRIT limit or drops below the low limit.
- '1' - $\overline{\text{ALERT}}$ / TACH pin is asserted (and status bit set) after three consecutive external temperature measurements exceed the high limit or the TCRIT limit or drop below the low limit.

6.6 Conversion Rate Register

Table 6.5 Conversion Rate Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
04h and 0Ah	R/W	Conversion Rate	-	-	-	-	CONV3	CONV2	CONV1	CONV0	08h

Bits 3- 0 - CONV[3:0] - The Conversion Rate Register controls the conversion rate per Table 6.6.

Table 6.6 Conversion Rates

CONV[3:0]				CONVERSIONS PER SECOND
3	2	1	0	
0	0	0	0	1/16
0	0	0	1	1/8
0	0	1	0	1/4
0	0	1	1	1/2
0	1	0	0	1
0	1	0	1	2
0	1	1	0	4
0	1	1	1	8
1	0	0	0	16 (default)
1	0	0	1	32
all others				32

6.7 Temperature Limit Registers

Table 6.7 Temperature Data Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
05h and 0Bh	R/W	Internal Temp Limit	-	64	32	16	8	4	2	1	46h (70°C)
07h and 0Dh	R/W	External Diode High Limit MSB	-	64	32	16	8	4	2	1	46h (70°C)
08h and 0Eh	R/W	External Diode Low Limit MSB	-	64	32	16	8	4	2	1	00h (0°C)
13h	R/W	External Diode High Limit LSB	0.5	0.25	0.125	-	-	-	-	-	00h
14h	R/W	External Diode Low Limit LSB	0.5	0.25	0.125	-	-	-	-	-	00h
19h	R/W	TCRIT Temp Limit	-	64	32	16	8	4	2	1	55h (85°C)
21h	R/W	TCRIT Hysteresis	-	64	32	16	8	4	2	1	0Ah (10°C)

The EMC2101 has two 8-bit limit registers, two 11-bit limit registers, and one hysteresis register. The limits are checked after every temperature conversion.

If the measured temperature for the internal diode exceeds the Internal Temperature limit, then the INT_HIGH bit is set in the Status Register. It will remain set until the internal temperature drops below the high limit.

If the measured temperature for the External Diode exceeds the 11-bit External Diode High Limit, or drops below the 11-bit External Diode Low Limit, then the appropriate status bit will be set. The status bit will remain set until the temperature is no longer violating the respective limits.

If the External Diode exceeds the TCRIT Temp Limit (even if it does not exceed the External Diode Temperature Limit), the TCRIT bit will be set in the Status Register.

The TCRIT bit will remain set in the Status Register until the External Diode Temperature drops below a lower threshold given by equation [2].

$$TEMP = (T_{CRIT} - T_{CRITHYS}) \quad \textbf{[2]}$$

See Section 6.3 and Section 6.5 for $\overline{\text{ALERT}}$ / TACH pin functionality.

6.8 External Temperature Force Register

Table 6.8 External Diode Force Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
0Ch	R/W	External Temperature Force	Sign	64	32	16	8	4	2	1	00h

The External Diode Force Register is used to force the Fan Control Look-Up Table to a specific fan-speed setting. When this function is enabled (see Section 6.16), the contents of this register are compared against the temperature thresholds in the Fan Control Look-Up Table to determine the fan setting to use.

The contents of this register represent temperature data in the same format as the data registers and can be updated at any time.

The External Diode Temperature Registers are updated normally with the measured temperature and compared against the THIGH and TCRIT limits normally but not used to determine the fan speed.

APPLICATION NOTE: This mode is used if the host or system requires temperature data from a source other than the EMC2101 External Diode to be used for fan control.

6.9 One Shot Register

Table 6.9 One Shot Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
0Fh	W	One Shot	Writing to this register initiates a one shot update of the temperature data. Data is not relevant and is not stored.								00h

The One Shot Register initiates an update of the temperature measurements. This register can be written at any time, however will only perform a one-shot conversion when the temperature monitoring is in standby mode. When the one shot temperature conversion is complete the temperature data registers are updated and the fan setting is updated if necessary. This register is self-clearing.

6.10 Scratchpad Registers

Table 6.10 Scratchpad Registers

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
11h	R/W	Scratchpad	B7	B6	B5	B4	B3	B2	B1	B0	00h
12h	R/W	Scratchpad	B7	B6	B5	B4	B3	B2	B1	B0	00h

The Scratchpad Registers are R/W registers that perform no function. They are included for software compatibility.

6.11 Alert Mask Register

Table 6.11 Alert Mask Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
16h	R/W	Alert Mask	1	INT_ MSK	1	HIGH MSK	LOW_ MSK	1	TCRIT_ MSK	TACH_ MSK	A4h

The Alert Mask Register enables interrupts from the temperature monitors and limits. Regardless of the condition of the individual mask bits, the Status Register will be updated normally.

Bit 6 - INT_MSK - Disables interrupts for the Internal Diode.

- '0' (default) - The Internal Diode will generate an interrupt if its measured temperature exceeds the Internal Diode high limit.
- '1' - the Internal Diode will not generate interrupts.

Bit 4 - HIGH_MSK - Disables interrupts for the External Diode high limit.

- '0' (default) - The External Diode will generate an interrupt if its measured temperature exceeds the External Diode high limit.
- '1' - the External Diode will not generate an interrupt when the high limit is exceeded.

Bit 3 - LOW_MSK - Disables interrupts for the External Diode low limit.

- '0' (default) - The External Diode will generate an interrupt if its measured temperature drops below the External Diode low limit.
- '1' - the External Diode will not generate an interrupt when the temperature drops below the low limit.

Bit 1 - TCRIT_MSK - Disables interrupts for the TCRIT Limit.

- '0' (default) - An interrupt will be generated if the External Diode Temperature exceeds TCRIT.
- '1' - An interrupt will not be generated if TCRIT is exceeded.

Bit 0 - TACH_MSK - Disables interrupts for the TACH Limit.

- '0' (default) - An interrupted will be generated if the measured TACH value exceeds the TACH Limit (indicating that the fan speed is too slow).
- '1' - An interrupt will not be generated if the TACH limit is exceeded.

6.12 External Ideality Factor Register

Table 6.12 External Ideality Factor Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
17h	R/W	External Ideality Factor	-	-	IDCF[5:0]						12h

This register stores the ideality factor that is automatically applied to the external diode. The Ideality factor is a 6 bit value that allows for a bi-directional trim centered on an ideality factor of 1.008. Table 6.13 defines each setting and the corresponding Ideality factor.

Table 6.13 Ideality Factor Look-Up Table

SETTING	FACTOR		SETTING	FACTOR		SETTING	FACTOR
08h	0.9949		18h	1.0159		28h	1.0371
09h	0.9962		19h	1.0172		29h	1.0384
0Ah	0.9975		1Ah	1.0185		2Ah	1.0397
0Bh	0.9988		1Bh	1.0200		2Bh	1.0410
0Ch	1.0001		1Ch	1.0212		2Ch	1.0423
0Dh	1.0014		1Dh	1.0226		2Dh	1.0436

Table 6.13 Ideality Factor Look-Up Table (continued)

SETTING	FACTOR		SETTING	FACTOR		SETTING	FACTOR
0Eh	1.0027		1Eh	1.0239		2Eh	1.0449
0Fh	1.0040		1Fh	1.0253		2Fh	1.0462
10h	1.0053		20h	1.0267		30h	1.0475
11h	1.0066		21h	1.0280		31h	1.0488
12h	1.0080		22h	1.0293		32h	1.0501
13h	1.0093		23h	1.0306		33h	1.0514
14h	1.0106		24h	1.0319		34h	1.0527
15h	1.0119		25h	1.0332		35h	1.0540
16h	1.0133		26h	1.0345		36h	1.0553
17h	1.0146		27h	1.0358		37h	1.0566

6.13 Beta Compensation Register

Table 6.14 Beta Compensation Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
18h	R/W	Beta Compensation	-	-	-	-	ENABLE	BETA[2:0]			08h

This register is used to set the Beta Compensation factor that is used for the External Diode channel.

When using a diode-connected transistor (such as the 2N3904) or CPUs that implement the thermal diode as a two-terminal diode, the CPU compensation circuit must be disabled by writing a value of 07h to this register.

Bit 3 - ENABLE - enables the Beta Compensation Factor Autodetection Algorithm

- '0' - the Beta Compensation Factor Autodetection circuitry is disabled. The External Diode will always use the Beta Compensation factor set by the BETA[2:0] bits.
- '1' (default) - the Beta Compensation Factor Autodetection circuitry is enabled. At the beginning of every conversion, the circuitry will determine the optimal Beta Compensation factor setting and use the detected setting. The value of the BETA[2:0] bits will be ignored.

Bit 2-0 - BETA[2:0] - selects the Beta Compensation factor that the External Diode will use if the autodetection circuitry is disabled. Table 6.15 shows the setting that should be used based on the expected beta value of the substrate transistor connected to the External Diode channel.

Care should be taken when setting the BETA[2:0] bits. If the Beta Compensation factor is set at a beta value that is higher than the transistor beta, then the circuit may introduce measurement errors.

Table 6.15 CPU Beta Values

ENABLE	B2	B1	B0	MINIMUM BETA
0	0	0	0	0.11
0	0	0	1	0.18
0	0	1	0	0.25
0	0	1	1	0.33
0	1	0	0	0.43
0	1	0	1	1.00
0	1	1	0	2.33
0	1	1	1	Disabled
1	X	X	X	Automatic detection

6.14 TACH Reading Registers

Table 6.16 TACH Reading Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
46h	R	TACH Reading Low Byte	TACH7 (128)	TACH6 (64)	TACH5 (32)	TACH4 (16)	TACH3 (8)	TACH2 (4)	TACH1 (2)	TACH0 (1)	FFh
47h	R	TACH Reading High Byte	TACH15 (32768)	TACH14 (16384)	TACH13 (8192)	TACH12 (4096)	TACH11 (2048)	TACH10 (1024)	TACH9 (512)	TACH8 (256)	FFh

The TACH Registers hold the 16-bit TACH Reading. This reading represents the number of TACH counts detected. The RPM of the fan can be determined by Equation [3] (see also Appendix B "TACH Reference Table"). The bit weighting of each TACH[15:0] bit is shown in parenthesis after the value. When determining the final fan speed, the TACH[15:0] bits need to be decoded into an equivalent decimal number.

$$RPM = \frac{5,400,000}{TACH_COUNT} \quad \text{[3]}$$

Where: TACH_COUNT is the decimal representation of the TACH[13:0] bits.

6.15 TACH Limit Registers

Table 6.17 TACH Reading Low Byte Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
48h	R/W	TACH Limit Low Byte	TACH_ L7	TACH_ L6	TACH_ L5	TACH_ L4	TACH_ L3	TACH_ L2	TACH_ L1	TACH_ L0	FFh
49h	R/W	TACH Limit High Byte	TACH_ L15	TACH_ L14	TACH_ L13	TACH_ L12	TACH_ L11	TACH_ L10	TACH_ L9	TACH_ L8	FFh

The TACH Limit Registers store the maximum TACH count that the fan is expected to operate at. TACH count is inversely proportional to the actual fan speed. This limit is used to guarantee that the fan has spun up properly. If the measured TACH is higher than this limit (indicating that the fan speed is lower than the minimum RPM value), then the TACH bit is set in the Status Register.

Additionally if the measured TACH count exceeds this limit, depending on the status of the TACH_M[1:0] bits (see Section 6.16), the TACH reading registers may be forced to FFFFh.

6.16 Fan Configuration Register

Table 6.18 Fan Configuration Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
4Ah	R/W	Fan Config	-	FORCE	PROG	POLARITY	CLK_SEL	CLK_OVR	TACH_M[1:0]		20h

The Fan Configuration Register enables the Fan Control Look-Up Table and polarity of the PWM signal driving the output.

Bit 6 - FORCE - enables the External Temperature Force Register. This bit is not used if the Fan Control Look-Up Table is not used.

- '0' (default) - the External Diode Force Register is not used. The measured External Diode temperature is used to determine the position in the Fan Control Look-Up Table.
- '1' - the External Temperature Force Register is used. When determining the position in the Fan Control Look-Up Table, the contents of the External Temperature Force Register will be used instead of the measured External Diode temperature. All limits will be checked against the measured External Diode temperature as normal.

Bit 5 - PROG - enables the Fan Control Look-Up Table for update and sets fan driver output based on Fan Control Look-Up Table values.

- '0' - the Fan Setting Register and Fan Control Look-Up Table Registers are read-only and the Fan Control Look-Up Table Registers will be used.
- '1' (default) - the Fan Setting Register and Fan Control Look-Up Table Registers can be written. The value written into the Fan Setting Register will be instantly applied to the fan driver and the Fan Control Look-Up Table will not be used.

Bit 4 - POLARITY- sets the polarity of the Fan output driver. For the EMC2101-R, the value of this bit is determined by the value of the pull-up resistor on the $\overline{\text{ALERT}}$ / TACH pin (see Table 5.1). When the PWM default value is set at 100% duty cycle, the default value is set to '1' and when the PWM default value is set to 0% duty cycle, the default value is set to '0'. This occurs within 10ms after power-up.

- '0' (default - EMC2101) - The polarity of the Fan output driver is non-inverted. A '00h' setting will correspond to a 0% duty cycle or minimum DAC output voltage.
- '1' - The polarity of the Fan output driver is inverted. A '00h' setting will correspond to a 100% duty cycle or maximum DAC output voltage.

Bit 3 - CLK_SEL - Determines the base clock that is used to determine the final PWM frequency.

- '0' (default) - The base clock that is used to determine the PWM frequency is 360kHz.
- '1' - The base clock that is used to determine the PWM frequency is 1.4kHz.

Bit 2 - CLK_OVR - Overrides the CLK_SEL bit and uses the Frequency Divide Register to determine the base PWM frequency. It is recommended that this bit be set for maximum PWM resolution.

- '0' (default) - The base clock frequency for the PWM is determined by the CLK_SEL bit.
- '1' (recommended) - The base clock that is used to determine the PWM frequency is set by the Frequency Divide Register

Bit 1-0 - TACH_M[1:0] - Determines the basic operation of the tachometer input as shown in Table 6.19.

Table 6.19 TACH Modes

TACH_M[1]	TACH_M[0]	TACH MODE
0	0	False readings when under minimum detectable RPM (TACH Limit). (Default condition - See Note 6.2)
0	1	FFFFh reading when under minimum detectable RPM.
1	0	
1	1	

Note 6.2 When the PWM base clock is set at 360kHz mode 00b is used regardless of the setting of the TACH_M[1:0] bits.

6.17 Fan Spin Up Configuration Register

Table 6.20 Fan Spin Up Configuration Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
4Bh	R/W	Fan Spin Up Config	-	-	FAST_ TACH	SPIN_DRIVE[1:0]		SPIN_TIME[2:0]			3Fh

The Fan Spin Up Configuration register controls the spin-up behavior of the device. The Fan driver enters its spin-up routine any time it transitions from a minimum fan setting (00h) to a higher fan setting (but does not invoke the spin-up routine upon power up). Once the spin-up time has been met, the fan driver is reduced to the programmed setting.

Bit 5 - FAST_TACH - Determines whether the Spin-Up routine aborts when the measured TACH is less than the TACH Limit.

- '0' - The Spin-Up routine uses the duty cycle and spin-up time independently of the TACH reading.
- '1' (default) - The Spin-Up routine will abort when the TACH measurement is less than the TACH Limit or the programmed Spin-Up time is met, whichever is less. In this case, the SPIN_DRIVE[1:0] bits are ignored and the drive will always be at 100%.

APPLICATION NOTE: This bit will be ignored if the ALT_TCH bit in the Configuration Register (see Section 6.5) is set to '0'.

APPLICATION NOTE: If the SPIN_TIME[2:0] bits are set at 000b, then the Spin-Up Routine is bypassed regardless of the status of this bit.

Bit 4 - 3 SPIN_DRIVE[1:0] - Determines the setting of the drive circuit during the Spin-Up routine according to Table 6.21.

Table 6.21 Spin-Up Drive

SPIN_DRIVE[1:0]		SPIN UP DRIVE
1	**0**	
0	0	0 - Spin-Up Cycle bypassed
0	1	50% (half drive)
1	0	75% (3/4 drive)
1	1	100% (full drive) (default)

Bit 2-0 - SPIN_TIME[2:0] - determines the length of time that the fan drive will remain at the SPIN_DRIVE[1:0] setting as shown in Table 6.22.

Table 6.22 Spin-Up Time

SPIN_TIME[2:0]			SPIN UP TIME
2	**1**	**0**	
0	0	0	0 - Spin-Up Cycle bypassed
0	0	1	0.05 sec.
0	1	0	0.1 sec.
0	1	1	0.2 sec.
1	0	0	0.4 sec.
1	0	1	0.8 sec.
1	1	0	1.6 sec.
1	1	1	3.2 sec. (default)

6.18 Fan Setting Register

Table 6.23 Fan Setting Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
4Ch	R/W (see text)	Fan Setting	-	-	32	16	8	4	2	1	00h

The Fan Setting Register drives the fan driver when the Fan Control Look-Up Table is not used (see Section 6.16). Any data written to the Fan Setting registers is applied immediately to the fan driver (PWM or DAC). When the Fan Control Look-Up Table is being used, any writes to this register will be ignored. If the Fan Control Look-Up Table is disabled, then the fan drive will be set at the last value that was used by the Fan Control Look-Up Table.

When the Fan Control Look-Up Table Registers are being used, the register is read-only.

The register applies to the fan driver in both PWM and DAC operating modes. The DAC output is determined by equation [4] below.

$$FAN = \left(\frac{FAN_SETTING}{64}\right) \times V_{DD} \quad \textbf{[4]}$$

These values are independent of the POLARITY bit (see Section 6.16). Therefore, a value of 00h in the Fan Setting Register will always refer to minimum output drive while a setting of 3Fh in the Fan Setting Register will always refer to maximum output drive.

APPLICATION NOTE: The output of the DAC driver is dependent upon the current load. With a low current load, the output will be from 0V to an LSB (approximately 52mV at V_{DD} = 3.3V) below V_{DD} with a maximum of 64 linear steps.

6.19 PWM Frequency Register

Table 6.24 PWM Frequency Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
4Dh	R/W	PWM Frequency	-	-	-	PWM_F[4:0]					17h

The PWM Frequency Register determines the final PWM frequency and “effective resolution” of the PWM driver. It has no affect on the DAC output resolution.

It is recommended that this register be set at 1Fh for maximum resolution. See Appendix A "Advanced PWM Options" for full operation of the PWM_F register and its interactions with the PWM Resolution and Duty Cycle.

6.20 PWM Frequency Divide Register

Table 6.25 PWM Frequency Divide Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
4Eh	R/W	PWM Frequency Divide	PWM_D[7:0]								01h

This register holds an alternate PWM Frequency divide value that can be used instead of the CLK_SEL bit function. This register can be written at any time, however unless the CLK_OVR bit is set to a logic ‘1’, it is not used.

When the CLK_OVR bit is set to a logic ‘1’, the PWM Frequency Divide Register is used in conjunction with the PWM Frequency Register to determine the final PWM frequency that the load will see. When the CLK_OVR bit is set to a logic ‘0’, the setting of this register is not changed and is not used to determine the effective PWM frequency.

The PWM frequency when the PWM Frequency Divide Register is used is shown in Equation [5].

$$PWM_D = \left(\frac{360k}{2 \times PWM_F}\right) \times \frac{1}{FREQ} = \frac{5806}{FREQ} \quad [5]$$

Where:

PWM_F is the setting of the PWM Frequency register (4Dh)

PWM_D is the setting of the PWM Frequency Divide Register (4Eh)

FREQ is the desired PWM Frequency

Maximum resolution is achieved by setting the PWM Frequency Register to 1Fh. With maximum resolution, the desired PWM frequency can be achieved by adjusting the PWM Frequency Divide Register setting (PWM_D[7:0]) as shown in Table 6.26.

For example, if the user desires a 30Hz PWM frequency with maximum PWM resolution, then the PWM_F[4:0] bits should be set at 1Fh (31d) and the PWM_D bits should be set at C1h (193d).

Table 6.26 Examples of Fan PWM Frequency with Maximum Resolution

PWM_F[4:0] = 1Fh					
PWM_D[7:0] SETTING	**EFFECTIVE RESOLUTION (%)**	**EFFECTIVE DUTY CYCLE (AT 50% FAN_SETTING)**	**EFFECTIVE DUTY CYCLE (AT 75% FAN_SETTING)**	**FAN_SETTING TO GET 75% DUTY CYCLE**	**EFFECTIVE PWM FREQUENCY (HZ)**
01h	1.61	51.6%	77.4%	2Eh (74.2%)	5806.5
11h	1.61	51.6%	77.4%	2Eh (74.2%)	341.6
20h	1.61	51.6%	77.4%	2Eh (74.2%)	181.5
47h	1.61	51.6%	77.4%	2Eh (74.2%)	81.8
C0	1.61	51.6%	77.4%	2Eh (74.2%)	30.2
C1	1.61	51.6%	77.4%	2Eh (74.2%)	30.0
FFh	1.61	51.6%	77.4%	2Eh (74.2%)	22.7

6.21 Fan Control Look-Up Table Hysteresis Register

Table 6.27 Look Up Table Hysteresis Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
4Fh	R/W	Fan Control Look-Up Table Hysteresis	-	-	-	16	8	4	2	1	04h (4°C)

The Fan Control Look-Up Table Hysteresis Register determines the amount of hysteresis applied to the temperature inputs of the fan control Fan Control Look-Up Table. See Section 5.6.4.

6.22 Fan Control Look-Up Table Registers

Table 6.28 Fan Control Look Up Table Registers

ADDR.	R/W Note 6.3	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
50h	R/W	Fan Control Look-Up Table T1	0	64	32	16	8	4	2	1	7Fh
51h	R/W	Fan Control Look-Up Table S1	-	-	32	16	8	4	2	1	3Fh
52h	R/W	Fan Control Look-Up Table T2	0	64	32	16	8	4	2	1	7Fh
53h	R/W	Fan Control Look-Up Table S2	-	-	32	16	8	4	2	1	3Fh
54h	R/W	Fan Control Look-Up Table T3	0	64	32	16	8	4	2	1	7Fh
55h	R/W	Fan Control Look-Up Table S3	-	-	32	16	8	4	2	1	3Fh
56h	R/W	Fan Control Look-Up Table T4	0	64	32	16	8	4	2	1	7Fh
57h	R/W	Fan Control Look-Up Table S4	-	-	32	16	8	4	2	1	3Fh
58h	R/W	Fan Control Look-Up Table T5	0	64	32	16	8	4	2	1	7Fh
59h	R/W	Fan Control Look-Up Table S5	-	-	32	16	8	4	2	1	3Fh
5Ah	R/W	Fan Control Look-Up Table T6	0	64	32	16	8	4	2	1	7Fh
5Bh	R/W	Fan Control Look-Up Table S6	-	-	32	16	8	4	2	1	3Fh
5Ch	R/W	Fan Control Look-Up Table T7	0	64	32	16	8	4	2	1	7Fh
5Dh	R/W	Fan Control Look-Up Table S7	-	-	32	16	8	4	2	1	3Fh
5Eh	R/W	Fan Control Look-Up Table T8	0	64	32	16	8	4	2	1	7Fh
5Fh	R/W	Fan Control Look-Up Table S8	-	-	32	16	8	4	2	1	3Fh

Note 6.3 When the PROG bit in the Fan Configuration Register (see Section 6.16) is set to '0', these registers become read only.

The table should be loaded with the lowest temperature in the T1 register (50h) and increasing in temperature for all settings.

See Section 5.6.4 for description of the Fan Control Look Up Table operation. The fan speed settings for each temperature threshold follow the same behavior as the Fan Setting Register (see Section 6.18).

6.23 Averaging Filter Register

Table 6.29 Averaging Filter Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
BFh	R/W	Averaging Filter	-	-	-	-	-	FILTER[1:0]		ALERT_ COMP	00h

The Averaging Filter Register controls the level of digital averaging that is used for the External Diode temperature measurements as well as the configuration of the $\overline{\text{ALERT}}$ / TACH pin functionality.

Bit 2 - 1 - FILTER[1:0] - control the level of digital filtering that is applied to the External Diode temperature measurements as shown in Table 6.30. See Figure 5.5 and Figure 5.6 for examples on the filter behavior.

Table 6.30 Averaging Settings

FILTER[1:0]		AVERAGING
1	**0**	
0	0	Disabled (default)
0	1	Level 1
1	0	Level 1
1	1	Level 2

Bit 0 - ALERT_COMP - determines the functionality of the $\overline{\text{ALERT}}$ / TACH pin.

- '0' (default) - the $\overline{\text{ALERT}}$ / TACH pin is configured to act as an interrupt (see Section 5.4.2).
- '1' - the $\overline{\text{ALERT}}$ / TACH pin is configured to operate as a temperature comparator (see Section 5.4.1).

6.24 Product ID Register

Table 6.31 Product ID Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FDh	R	Product ID Register	0	0	0	1	0	1	1	0	16h (EMC2101)
			0	0	1	0	1	0	0	0	28h (EMC2101-R)

The Product ID Register contains a unique 8 bit word that identifies the product.

6.25 Manufacturer ID Register (FEh)

Table 6.32 Manufacturer ID Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FEh	R	SMSC ID Register	0	1	0	1	1	1	0	1	5Dh

The Manufacturer ID register contains an 8 bit word that identifies the SMSC as the manufacturer of the EMC2101.

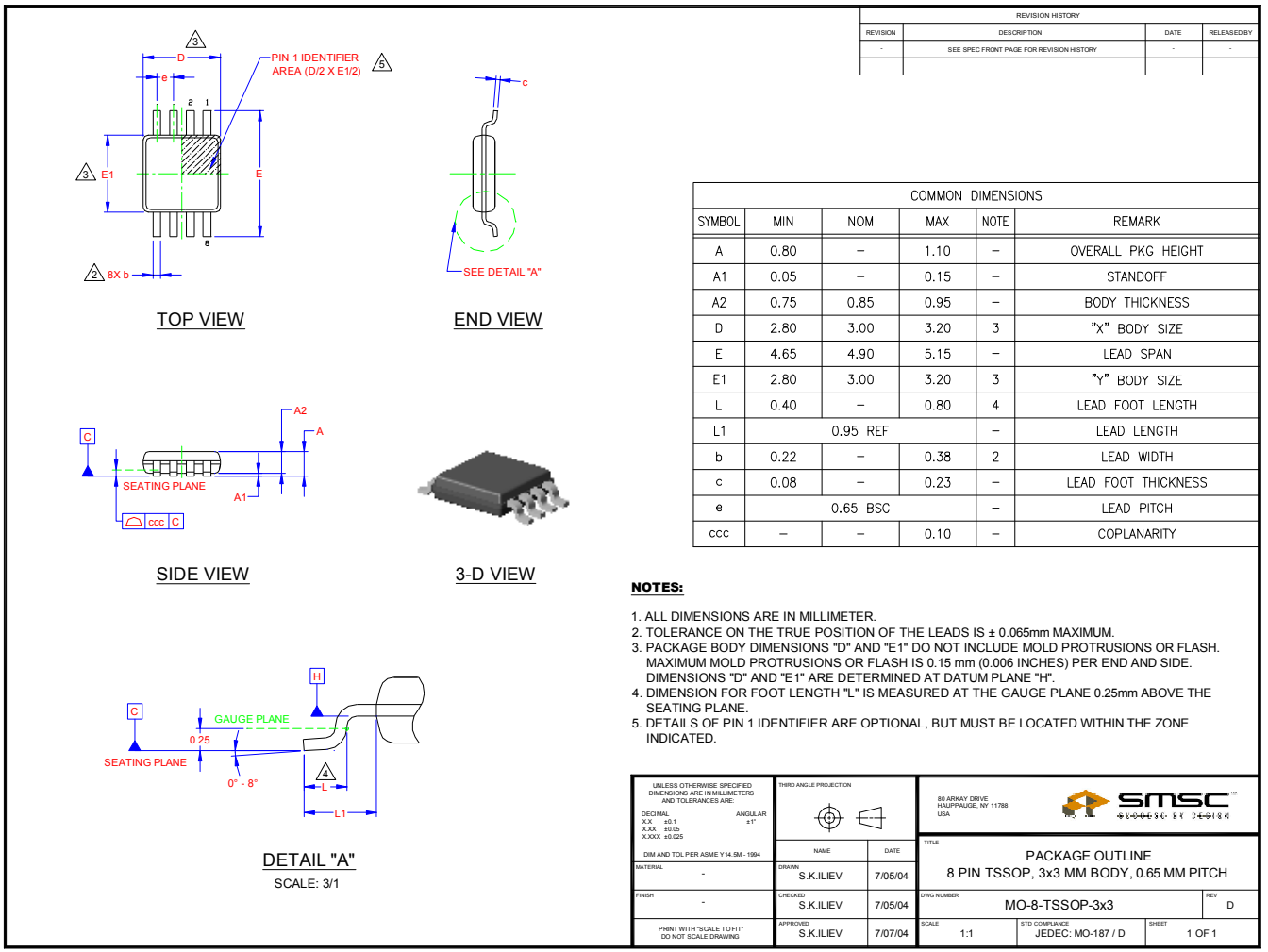
6.26 Revision Register (FFh)

Table 6.33 Revision Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FFh	R	Revision Register	0	0	0	0	0	0	0	1	01h

The Revision register contains an 8 bit word that identifies the die revision.

Chapter 7 Package Diagrams



REVISION HISTORY			
REVISION	DESCRIPTION	DATE	RELEASED BY
-	SEE SPEC FRONT PAGE FOR REVISION HISTORY	-	-

COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.80	–	1.10	–	OVERALL PKG HEIGHT
A1	0.05	–	0.15	–	STANDOFF
A2	0.75	0.85	0.95	–	BODY THICKNESS
D	2.80	3.00	3.20	3	"X" BODY SIZE
E	4.65	4.90	5.15	–	LEAD SPAN
E1	2.80	3.00	3.20	3	"Y" BODY SIZE
L	0.40	–	0.80	4	LEAD FOOT LENGTH
L1		0.95 REF		–	LEAD LENGTH
b	0.22	–	0.38	2	LEAD WIDTH
c	0.08	–	0.23	–	LEAD FOOT THICKNESS
e		0.65 BSC		–	LEAD PITCH
ccc	–	–	0.10	–	COPLANARITY

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETER.
2. TOLERANCE ON THE TRUE POSITION OF THE LEADS IS ± 0.065mm MAXIMUM.
3. PACKAGE BODY DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSIONS OR FLASH. MAXIMUM MOLD PROTRUSIONS OR FLASH IS 0.15 mm (0.006 INCHES) PER END AND SIDE. DIMENSIONS "D" AND "E1" ARE DETERMINED AT DATUM PLANE "H".
4. DIMENSION FOR FOOT LENGTH "L" IS MEASURED AT THE GAUGE PLANE 0.25mm ABOVE THE SEATING PLANE.
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS AND TOLERANCES ARE:
DECIMAL X.X ±0.1, X.XX ±0.05, X.XXX ±0.025 ANGULAR ±1°
DIM AND TOL PER ASME Y14.5M - 1994
MATERIAL -
FINISH -
PRINT WITH "SCALE TO FIT" DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

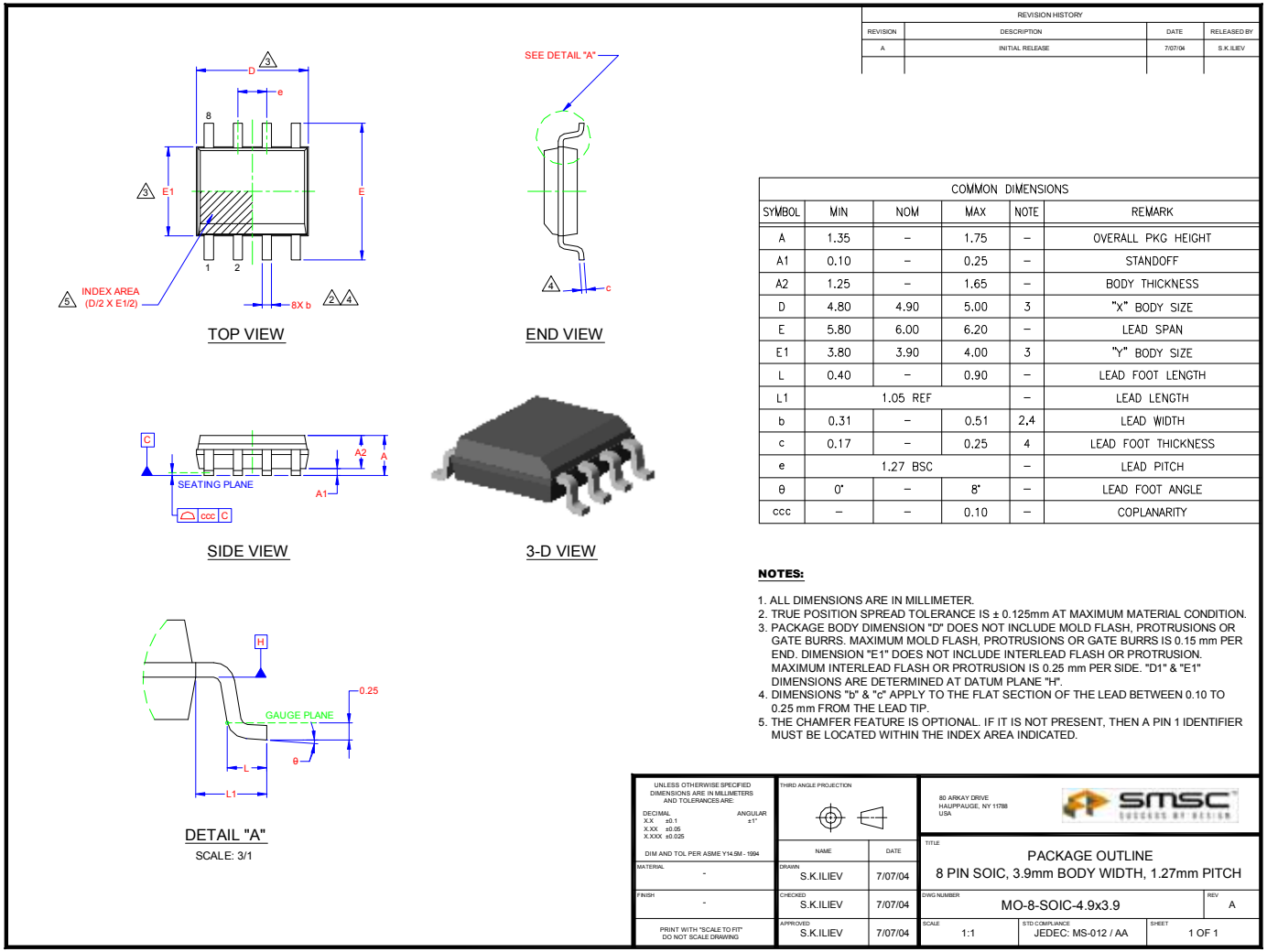
	NAME	DATE
DRAWN	S.K.ILIEV	7/05/04
CHECKED	S.K.ILIEV	7/05/04
APPROVED	S.K.ILIEV	7/07/04

80 ARKAY DRIVE
HAUPPAUGE, NY 11788
USA

TITLE: PACKAGE OUTLINE
8 PIN TSSOP, 3x3 MM BODY, 0.65 MM PITCH

DWG NUMBER: MO-8-TSSOP-3x3 REV: D
SCALE: 1:1 STD COMPLIANCE: JEDEC: MO-187 / D SHEET: 1 OF 1

Figure 9.1 8-PIN MSOP / TSSOP Package



REVISION HISTORY			
REVISION	DESCRIPTION	DATE	RELEASED BY
A	INITIAL RELEASE	7/07/04	S.K.ILIEV

COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	1.35	–	1.75	–	OVERALL PKG HEIGHT
A1	0.10	–	0.25	–	STANDOFF
A2	1.25	–	1.65	–	BODY THICKNESS
D	4.80	4.90	5.00	3	"X" BODY SIZE
E	5.80	6.00	6.20	–	LEAD SPAN
E1	3.80	3.90	4.00	3	"Y" BODY SIZE
L	0.40	–	0.90	–	LEAD FOOT LENGTH
L1		1.05 REF		–	LEAD LENGTH
b	0.31	–	0.51	2,4	LEAD WIDTH
c	0.17	–	0.25	4	LEAD FOOT THICKNESS
e		1.27 BSC		–	LEAD PITCH
θ	0°	–	8°	–	LEAD FOOT ANGLE
ccc	–	–	0.10	–	COPLANARITY

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETER.
2. TRUE POSITION SPREAD TOLERANCE IS ± 0.125mm AT MAXIMUM MATERIAL CONDITION.
3. PACKAGE BODY DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MAXIMUM MOLD FLASH, PROTRUSIONS OR GATE BURRS IS 0.15 mm PER END. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. MAXIMUM INTERLEAD FLASH OR PROTRUSION IS 0.25 mm PER SIDE. "D1" & "E1" DIMENSIONS ARE DETERMINED AT DATUM PLANE "H".
4. DIMENSIONS "b" & "c" APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
5. THE CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS AND TOLERANCES ARE:
DECIMAL X.X ±0.1, X.XX ±0.05, X.XXX ±0.025 — ANGULAR ±1°
DIM AND TOL PER ASME Y14.5M - 1994
MATERIAL: -
FINISH: -
PRINT WITH "SCALE TO FIT" DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

	NAME	DATE
DRAWN	S.K.ILIEV	7/07/04
CHECKED	S.K.ILIEV	7/07/04
APPROVED	S.K.ILIEV	7/07/04

80 ARKAY DRIVE
HAUPPAUGE, NY 11788
USA

TITLE: PACKAGE OUTLINE
8 PIN SOIC, 3.9mm BODY WIDTH, 1.27mm PITCH

DWG NUMBER	REV
MO-8-SOIC-4.9x3.9	A

SCALE	STD COMPLIANCE	SHEET
1:1	JEDEC: MS-012 / AA	1 OF 1

Figure 9.2 8-PIN SOIC Package

Appendix A Advanced PWM Options

The PWM Frequency Register determines the number of clocks (set by the CLK_SEL bit or the PWM_D register settings) represent 1/2 of the period of the final PWM output waveform. Therefore, as the PWM Frequency Register is updated, the PWM frequency is likewise updated. However, it also directly affects the PWM Resolution and PWM duty cycle.

The PWM frequency is set according to Equation [8] or Equation [9] below or, if the PWM Divide Register is used, Equation [5] (see Section 6.20, "PWM Frequency Divide Register," on page 44).

The PWM Frequency Register does not affect the Fan Setting (either the Fan Setting Register or the Fan Setting entries in the Fan Control Look-up Table Registers).

The Fan Setting Register determines the number of clocks that the PWM output is high for is always based on 64 time steps for a PWM cycle. As the PWM Frequency Register changes (or the Fan Setting changes) the effective duty cycle will vary according to Equation [6] and the PWM resolution will vary according to Equation [7]. This is a result of the “on” time determined by Fan Setting changing with respect to the overall PWM period determined by the PWM Frequency Register.

APPLICATION NOTE: If the Fan Setting is set at a value that is higher than 2x the PWM Frequency Register settings, the PWM output will be at 100% duty cycle.

Table A.1 shows the effective resolution, duty cycle, and frequency as the PWM Frequency Register setting is changed.

$$EFFECTIVE_DUTY_CYCLE = \left(\frac{FAN_SETTING}{PWM_F \times 2}\right) \times 100\%$$

Where: PWM_F is the setting of the PWM Frequency Register (4Dh) **[6]**

$$EFFECTIVE_RESOLUTION = \frac{100\%}{PWM_F \times 2}$$

Where: PWM_F is the setting of the PWM Frequency Register (4Dh) **[7]**

$$PWM_FREQUENCY = \frac{360k}{2xPWM_F}$$

Where: PWM_F is the setting of the PWM Frequency register (4Dh)
PWM_D is the setting of the PWM Frequency Divide Register (4Eh)

CLK_SEL = ‘0’ **[8]**

$$PWM_FREQUENCY = \frac{1.4k}{2xPWM_F}$$

CLK_SEL = ‘1’ **[9]**

Table A.1 Fan Effective Duty Cycle Resolution and Frequency

PWM_F [4:0] SETTING	EFFECTIVE RESOLUTION (%)	EFFECTIVE DUTY CYCLE (AT 75% FAN_SETTING)	EFFECTIVE DUTY CYCLE (AT 50% FAN_SETTING)	FAN_SETTING TO GET 75% DUTY CYCLE	PWM FREQUENCY AT 360KHZ BASE FREQUENCY (KHZ)	PWM FREQUENCY AT 1.4KHZ BASE FREQUENCY (HZ)
00h	Setting 00h is mapped to setting 01h					
01h	50.00	100%	100%	01h (50%)	180.0	704.2
02h	25.00%	100%	100%	03h (75%)	90.0	350.0
03h	16.67%	100%	100%	04h (66.7%)	60.0	233.3
04h	12.50%	100%	100%	06h (75%)	45.0	175.0
05h	10.00%	100%	100%	07h (70%)	36.0	140.0
06h	8.33%	100%	100%	09h (75%)	30.0	116.7
07h	7.14%	100%	100%	0Ah (71.4%)	25.7	100.0
08h	6.25%	100%	100%	0Ch (75%)	22.5	87.5
09h	5.56%	100%	100%	0Dh (72.5)	20.0	77.8
0Ah	5.00%	100%	100%	0Fh (75%)	18.0	70.0
0Bh	4.54%	100%	100%	11h (77.3%)	16.4	63.7
0Ch	4.17%	100%	100%	12h (75%)	15.0	58.3
0Dh	3.84%	100%	100%	14h (76.9%)	13.8	53.8
0Eh	3.57%	100%	100%	15h (75%)	12.8	50.0
0Fh	3.33%	100%	100%	16h (73.3%)	12.0	46.7
10h	3.13	100%	100%	18h (75.0%)	11.25	44.0
11h	2.94	100%	94.1%	19h (73.5%)	10.68	41.4
12h	2.78	100%	88.9%	1Bh (75.0%)	10.00	39.1
13h	2.63	100%	84.2%	1Ch (73.7%)	9.47	37.1

Table A.1 Fan Effective Duty Cycle Resolution and Frequency (continued)

PWM_F [4:0] SETTING	EFFECTIVE RESOLUTION (%)	EFFECTIVE DUTY CYCLE (AT 75% FAN_SETTING)	EFFECTIVE DUTY CYCLE (AT 50% FAN_SETTING)	FAN_SETTING TO GET 75% DUTY CYCLE	PWM FREQUENCY AT 360KHZ BASE FREQUENCY (KHZ)	PWM FREQUENCY AT 1.4KHZ BASE FREQUENCY (HZ)
14h	2.50	100%	80.0%	1Eh (75.0%)	9.00	35.2
15h	2.38	100%	76.2%	1Fh (73.8%)	8.57	33.5
16h	2.27	100%	72.7%	21h (75.0%)	8.18	32.0
17h	2.17	100%	69.7%	22h (73.9%)	7.83	30.6
18h	2.08	100%	66.7%	24h (75.0%)	7.50	29.3
19h	2.00	96%	64.0%	25h (74.0%)	7.20	28.2
1Ah	1.92	92.3%	61.5%	27h (75.0%)	6.92	27.1
1Bh	1.85	88.9%	59.3%	28h (74.1%)	6.67	26.1
1Ch	1.79	85.7%	57.1%	2Ah (75.0%)	6.43	25.1
1Dh	1.72	82.8%	55.2%	2Bh (74.1%)	6.21	24.3
1Eh	1.67	80.0%	53.3%	2Dh (75.0%)	6.00	23.5
1Fh	1.61	77.4%	51.6%	2Eh (74.2%)	5.81	22.7

Appendix B TACH Reference Table

Table B.1 Example TACH Decode 10k RPM to 1k RPM

DEC	HEX	RPM	DEC	HEX	RPM	DEC	HEX	RPM	DEC	HEX	RPM	DEC	HEX	RPM	DEC	HEX	RPM
512	200h	10547	1280	500h	4219	2048	800h	2637	2816	B00h	1918	3584	E00h	1507	4352	1100h	1241
528	210h	10227	1296	510h	4167	2064	810h	2616	2832	B10h	1907	3600	E10h	1500	4368	1110h	1236
544	220h	9926	1312	520h	4116	2080	820h	2596	2848	B20h	1896	3616	E20h	1493	4384	1120h	1232
560	230h	9643	1328	530h	4066	2096	830h	2576	2864	B30h	1885	3632	E30h	1487	4400	1130h	1227
576	240h	9375	1344	540h	4018	2112	840h	2557	2880	B40h	1875	3648	E40h	1480	4416	1140h	1223
592	250h	9122	1360	550h	3971	2128	850h	2538	2896	B50h	1865	3664	E50h	1474	4432	1150h	1218
608	260h	8882	1376	560h	3924	2144	860h	2519	2912	B60h	1854	3680	E60h	1467	4448	1160h	1214
624	270h	8654	1392	570h	3879	2160	870h	2500	2928	B70h	1844	3696	E70h	1461	4464	1170h	1210
640	280h	8438	1408	580h	3835	2176	880h	2482	2944	B80h	1834	3712	E80h	1455	4480	1180h	1205
656	290h	8232	1424	590h	3792	2192	890h	2464	2960	B90h	1824	3728	E90h	1448	4496	1190h	1201
672	2A0h	8036	1440	5A0h	3750	2208	8A0h	2446	2976	BA0h	1815	3744	EA0h	1442	4512	11A0h	1197
688	2B0h	7849	1456	5B0h	3709	2224	8B0h	2428	2992	BB0h	1805	3760	EB0h	1436	4528	11B0h	1193
704	2C0h	7670	1472	5C0h	3668	2240	8C0h	2411	3008	BC0h	1795	3776	EC0h	1430	4544	11C0h	1188
720	2D0h	7500	1488	5D0h	3629	2256	8D0h	2394	3024	BD0h	1786	3792	ED0h	1424	4560	11D0h	1184
736	2E0h	7337	1504	5E0h	3590	2272	8E0h	2377	3040	BE0h	1776	3808	EE0h	1418	4576	11E0h	1180
752	2F0h	7181	1520	5F0h	3553	2288	8F0h	2360	3056	BF0h	1767	3824	EF0h	1412	4592	11F0h	1176
768	300h	7031	1536	600h	3516	2304	900h	2344	3072	C00h	1758	3840	F00h	1406	4608	1200h	1172
784	310h	6888	1552	610h	3479	2320	910h	2328	3088	C10h	1749	3856	F10h	1400	4624	1210h	1168
800	320h	6750	1568	620h	3444	2336	920h	2312	3104	C20h	1740	3872	F20h	1395	4640	1220h	1164
816	330h	6618	1584	630h	3409	2352	930h	2296	3120	C30h	1731	3888	F30h	1389	4656	1230h	1160

Table B.1 Example TACH Decode 10k RPM to 1k RPM (continued)

DEC	HEX	RPM	DEC	HEX	RPM	DEC	HEX	RPM	DEC	HEX	RPM	DEC	HEX	RPM	DEC	HEX	RPM
832	340h	6490	1600	640h	3375	2368	940h	2280	3136	C40h	1722	3904	F40h	1383	4672	1240h	1156
848	350h	6368	1616	650h	3342	2384	950h	2265	3152	C50h	1713	3920	F50h	1378	4688	1250h	1152
864	360h	6250	1632	660h	3309	2400	960h	2250	3168	C60h	1705	3936	F60h	1372	4704	1260h	1148
880	370h	6136	1648	670h	3277	2416	970h	2235	3184	C70h	1696	3952	F70h	1366	4720	1270h	1144
896	380h	6027	1664	680h	3245	2432	980h	2220	3200	C80h	1688	3968	F80h	1361	4736	1280h	1140
912	390h	5921	1680	690h	3214	2448	990h	2206	3216	C90h	1679	3984	F90h	1355	4752	1290h	1136
928	3A0h	5819	1696	6A0h	3184	2464	9A0h	2192	3232	CA0h	1671	4000	FA0h	1350	4768	12A0h	1133
944	3B0h	5720	1712	6B0h	3154	2480	9B0h	2177	3248	CB0h	1663	4016	FB0h	1345	4784	12B0h	1129
960	3C0h	5625	1728	6C0h	3125	2496	9C0h	2163	3264	CC0h	1654	4032	FC0h	1339	4800	12C0h	1125
976	3D0h	5533	1744	6D0h	3096	2512	9D0h	2150	3280	CD0h	1646	4048	FD0h	1334	4816	12D0h	1121
992	3E0h	5444	1760	6E0h	3068	2528	9E0h	2136	3296	CE0h	1638	4064	FE0h	1329	4832	12E0h	1118
1008	3F0h	5357	1776	6F0h	3041	2544	9F0h	2123	3312	CF0h	1630	4080	FF0h	1324	4848	12F0h	1114
1024	400h	5273	1792	700h	3013	2560	A00h	2109	3328	D00h	1623	4096	1000h	1318	4864	1300h	1110
1040	410h	5192	1808	710h	2987	2576	A10h	2096	3344	D10h	1615	4112	1010h	1313	4880	1310h	1107
1056	420h	5114	1824	720h	2961	2592	A20h	2083	3360	D20h	1607	4128	1020h	1308	4896	1320h	1103
1072	430h	5037	1840	730h	2935	2608	A30h	2071	3376	D30h	1600	4144	1030h	1303	4912	1330h	1099
1088	440h	4963	1856	740h	2909	2624	A40h	2058	3392	D40h	1592	4160	1040h	1298	4928	1340h	1096
1104	450h	4891	1872	750h	2885	2640	A50h	2045	3408	D50h	1585	4176	1050h	1293	4944	1350h	1092
1120	460h	4821	1888	760h	2860	2656	A60h	2033	3424	D60h	1577	4192	1060h	1288	4960	1360h	1089
1136	470h	4754	1904	770h	2836	2672	A70h	2021	3440	D70h	1570	4208	1070h	1283	4976	1370h	1085
1152	480h	4688	1920	780h	2813	2688	A80h	2009	3456	D80h	1563	4224	1080h	1278	4992	1380h	1082
1168	490h	4623	1936	790h	2789	2704	A90h	1997	3472	D90h	1555	4240	1090h	1274	5008	1390h	1078
1184	4A0h	4561	1952	7A0h	2766	2720	AA0h	1985	3488	DA0h	1548	4256	10A0h	1269	5024	13A0h	1075
1200	4B0h	4500	1968	7B0h	2744	2736	AB0h	1974	3504	DB0h	1541	4272	10B0h	1264	5040	13B0h	1071

Table B.1 Example TACH Decode 10k RPM to 1k RPM (continued)

DEC	HEX	RPM	DEC	HEX	RPM	DEC	HEX	RPM	DEC	HEX	RPM	DEC	HEX	RPM	DEC	HEX	RPM
1216	4C0h	4441	1984	7C0h	2722	2752	AC0h	1962	3520	DC0h	1534	4288	10C0h	1259	5056	13C0h	1068
1232	4D0h	4383	2000	7D0h	2700	2768	AD0h	1951	3536	DD0h	1527	4304	10D0h	1255	5072	13D0h	1065
1248	4E0h	4327	2016	7E0h	2679	2784	AE0h	1940	3552	DE0h	1520	4320	10E0h	1250	5088	10E0h	1061
1264	4F0h	4272	2032	7F0h	2657	2800	AF0h	1929	3568	DF0h	1513	4336	10F0h	1245	5104	13F0h	1058

Revision History

Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Revision 2.54 (06-16-09)	Table 2.2, "Pin Types"	Added table and the following application note above the table: “For the 5V tolerant pins that have a pull-up resistor, the voltage difference between VDD and the pull-up voltage must never exceed 3.6V.”
	Table 3.1, "Absolute Maximum Ratings"	Updated voltage limits for 5V tolerant pins with pull-up resistors. Added the following note below table: “For the 5V tolerant pins that have a pull-up resistor, the pull-up voltage must not exceed 3.6V when the device is unpowered.”
	Table 3.2, "Electrical Specifications"	Updated supply current max TBD to 400. Updated Standby current from 180 to 270. Added conditions to the leakage current.