TC7109/A

12-Bit μA-Compatible Analog-to-Digital Converters

Features:

- Zero Integrator Cycle for Fast Recovery from Input Overloads
- Eliminates Cross-Talk in Multiplexed Systems
- 12-Bit Plus Sign Integrating A/D Converter with Over Range Indication
- Sign Magnitude Coding Format
- True Differential Signal Input and Differential Reference Input
- Low Noise: 15μV_{P-P} Typ.
- Input Current: 1pA Typ.
- No Zero Adjustment needed
- TTL Compatible, Byte Organized Tri-State Outputs
- UART Handshake Mode for simple Serial Data Transmissions

Device Selection Table

Part Number (TC7109X)*	Package	Temperature Range
TC7109CKW	44-Pin PQFP	0°C to +70°C
TC7109CLW	44-Pin PLCC	0°C to +70°C
TC7109CPL	40-Pin PDIP	0°C to +70°C
TC7109IJL	40-Pin CERDIP	-25°C to +85°C

*The “A” version has a higher I_{OUT} on the digital lines.

General Description:

The TC7109A is a 12-bit plus sign, CMOS low power Analog-to-Digital Converter (ADC). Only eight passive components and a crystal are required to form a complete dual slope integrating ADC.

The improved V_{OH} source current and other TC7109A features make it an attractive per-channel alternative to analog multiplexing for many data acquisition applications. These features include typical input bias current of 1pA, drift of less than 1μV/°C, input noise typically 15μV_{P-P}, and auto-zero. True differential input and reference allow measurement of bridge type transducers, such as load cells, strain gauges and temperature transducers.

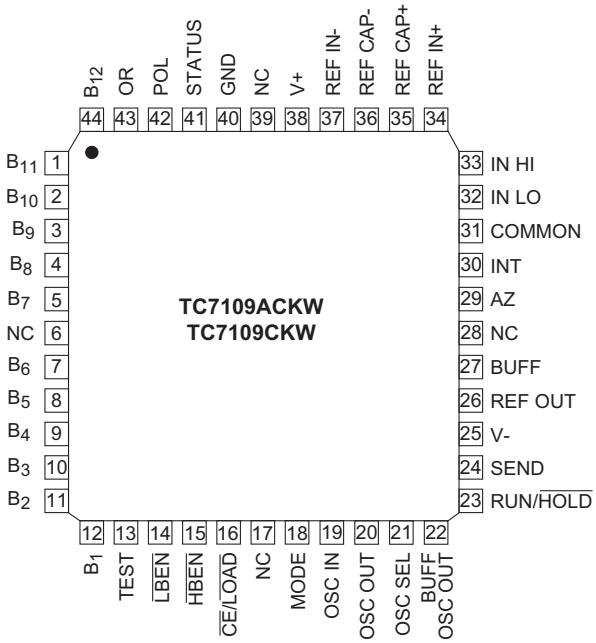
The TC7109A provides a versatile digital interface. In the Direct mode, Chip Select and HIGH/LOW byte enable control parallel bus interface. In the Handshake mode, the TC7109A will operate with industry standard UARTs in controlling serial data transmission – ideal for remote data logging. Control and monitoring of conversion timing is provided by the RUN/HOLD input and Status output.

For applications requiring more resolution, see the TC500, 15-bit plus sign ADC data sheet. The TC7109A has improved over range recovery performance and higher output drive capability than the original TC7109. All new (or existing) designs should specify the TC7109A wherever possible.

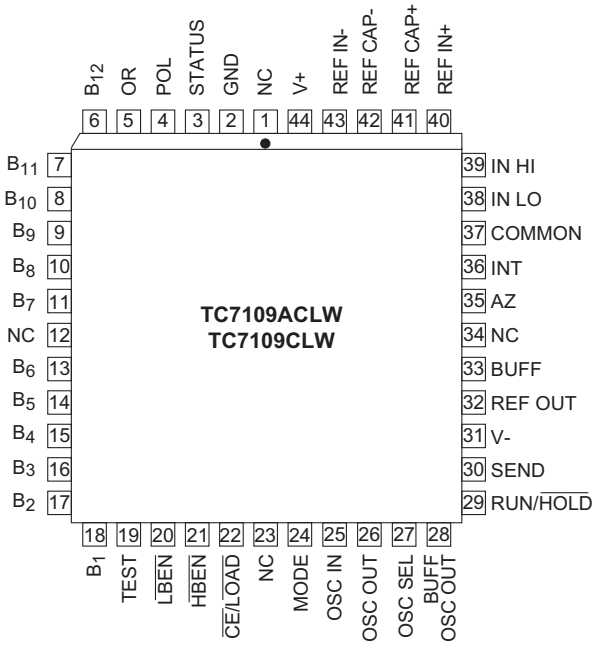
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Package Type

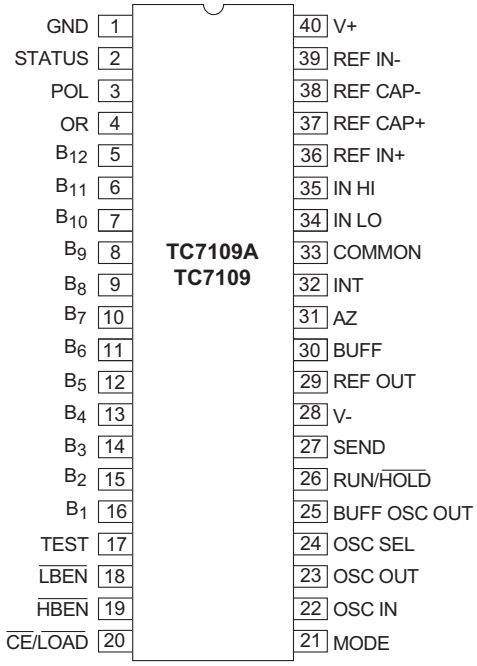
44-Pin PQFP



44-Pin PLCC



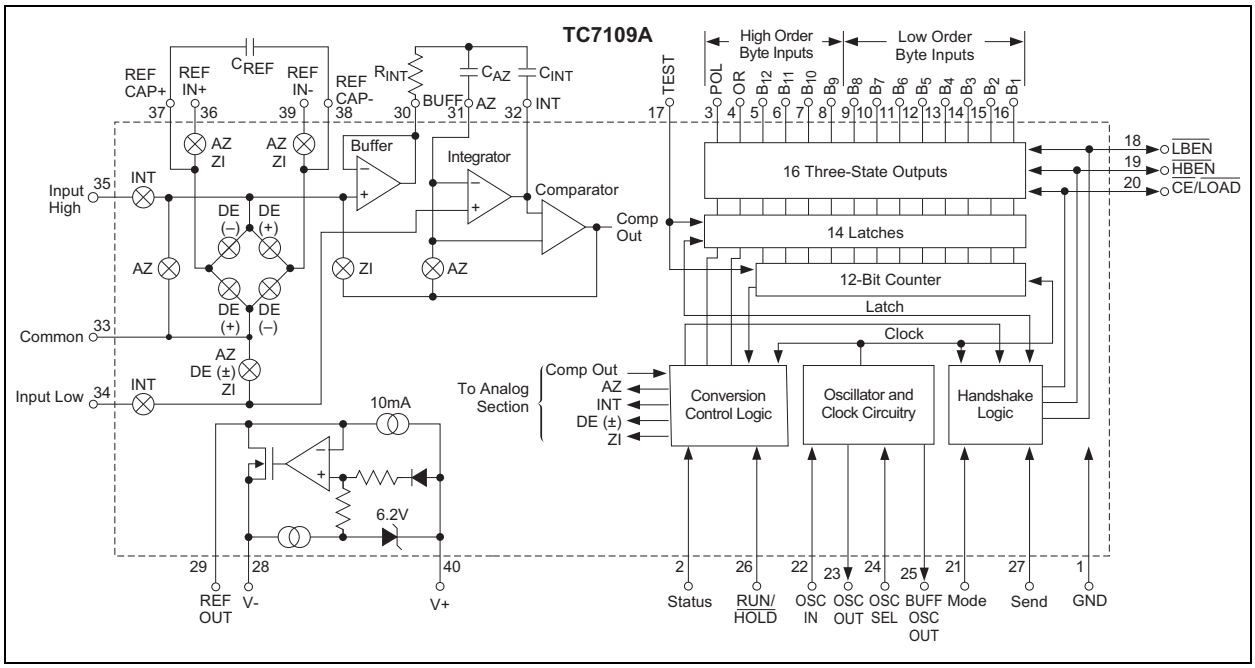
40-Pin PDIP/CERDIP



NC = No internal connection

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Typical Application



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Positive Supply Voltage (GND to V+) ..... +6.2V
Negative Supply Voltage (GND to V-) ..... -9V
Analog Input Voltage (Low to High) **(Note 1)** .... V+ to V-
Reference Input Voltage:
(Low to High) **(Note 1)** ..... V+ to V-
Digital Input Voltage:
(Pins 2-27) **(Note 2)** ..... GND – 0.3V
Power Dissipation, $T_A \leq 70°C$ **(Note 3)**
CERDIP 2.29W
Plastic DIP 1.23W
PLCC 1.23W
PQFP 1.00W
Operating Temperature Range
Plastic Package (C) ..... 0°C to +70°C
Ceramic Package (I) ..... -25°C to +85°C
Storage Temperature Range ..... -65°C to +150°C

*Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC7109/TC7109A ELECTRICAL SPECIFICATIONS

Electrical Characteristics: All parameters with V+ = +5V, V- = -5V, GND = 0V, T_A = +25°C, unless otherwise indicated.						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Analog						
	Overload Recovery Time (TC7109A)	—	0	1	Measurement Cycle	
	Zero Input Reading	-0000_8	$\pm0000_8$	$+0000_8$	Octal Reading	V_{IN} = 0V; Full Scale = 409.6mV
	Ratio Metric Reading	3777_8	3777_8 4000_8	4000_8	Octal Reading	$V_{IN} = V_{REF}$ V_{REF} = 204.8mV
NL	Non-Linearity (Max Deviation from Best Straight Line Fit)	-1	±0.2	+1	Count	Full Scale = 409.6mV to 2.048V Over Full Operating Temperature Range
	Rollover Error (Difference in Reading for Equal Positive and Inputs near (Full Scale)	-1	±0.02	+1	Count	Full Scale = 409.6mV to 2.048V Over Full Operating Temperature Range
CMRR	Input Common Mode Rejection Ratio	—	50	—	µV/V	V_{CM} ±1V, V_{IN} = 0V Full Scale = 409.6mV
V_{CMR}	Common Mode Voltage Range	V- +1.5	—	V+ -1.5	V	Input High, Input Low and Common Pins
e_N	Noise (P-P Value Not Exceeded 95% of Time)	—	15	—	µV	V_{IN} = 0V, Full Scale = 409.6mV
I_{IN}	Leakage Current at Input	—	1	10	pA	V_{IN}, All Packages: +25°C
		—	20	100	pA	C Device: $0°C \leq T_A \leq +70°C$
		—	100	250	pA	I Device: $-25°C \leq T_A \leq +85°C$
TC_{ZS}	Zero Reading Drift	—	0.2	1	µV/°C	V_{IN} = 0V

Note 1: Input voltages may exceed supply voltages if input current is limited to ±100µA.
2: Connecting any digital inputs or outputs to voltages greater than V+ or less than GND may cause destructive device latch-up. Therefore, it is recommended that inputs from sources other than the same power supply should not be applied to the TC7109A before its power supply is established. In multiple supply systems, the supply to the device should be activated first.
3: This limit refers to that of the package and will not occur during normal operation.

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TC7109/TC7109A ELECTRICAL SPECIFICATIONS (Continued)

Electrical Characteristics: All parameters with V+ = +5V, V- = -5V, GND = 0V, T_A = +25°C, unless otherwise indicated.						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
TC_{FS}	Scale Factor Temperature Coefficient	—	1	5	µV/°C	V_{IN} = 408.9mV = $>7770_8$ Reading, Ext Ref = 0ppm/°C
I^+	Supply Current (V+ to GND)	—	700	1500	µA	V_{IN} = 0V, Crystal Oscillator 3.58MHz Test Circuit
I_S	Supply Current (V+ to V-)	—	700	1500	µA	Pins 2-21, 25, 26, 27, 29 Open
V_{REF}	Reference Out Voltage	-2.4	-2.8	-3.2	V	Referenced to V+, 25kΩ Between V+ and Ref Out
TC_{REF}	Ref Out Temperature Coefficient	—	80	—	ppm/°C	25kΩ Between V+ and Ref Out 0°C ≤ T_A ≤ +70°C
Digital						
V_{OH}	Output High Voltage I_{OUT} = 700µA	3.5	4.3	—	V	TC7109: I_{OUT} = 100µA Pins 3 -16, 18, 19, 20 TC7109A: I_{OUT} = 700µA
V_{OL}	Output Low Voltage	—	0.2	0.4	µA	I_{OUT} = 1.6mA
	Output Leakage Current	—	±0.01	±1	µA	Pins 3 -16 High-Impedance
	Control I/O Pull-up Current	—	5	—	µF	Pins 18, 19, 20 V_{OUT} = V+ – 3V Mode Input at GND
	Control I/O Loading	—	—	50	pF	$\overline{HBEN}$, Pin 19; $\overline{LBEN}$, Pin 18
V_{IH}	Input High Voltage	2.5	—	—	V	Pins 18 -21, 26, 27 Referenced to GND
V_{IL}	Input Low Voltage	—	—	1	V	Pins 18-21, 26, 27 Referenced to GND
	Input Pull-up Current	— —	5 25	— —	µA µA	Pins 26, 27; V_{OUT} = V+ – 3V Pins 17, 24; V_{OUT} = V+ – 3V
	Input Pull-down Current	—	1	—	µA	Pins 21, V_{OUT} = GND = +3V
	Oscillator Output Current, High	—	1	—	mA	V_{OUT} – 2.5V
	Oscillator Output Current, Low	—	1.5	—	mA	V_{OUT} – 2.5V
	Buffered Oscillator Output Current High	—	2	—	mA	V_{OUT} – 2.5V
	Buffered Oscillator Output Current Low	—	5	—	mA	V_{OUT} – 2.5V
t_W	Mode Input Pulse Width	60	—	—	nsec	

Note 1: Input voltages may exceed supply voltages if input current is limited to ±100µA.

2: Connecting any digital inputs or outputs to voltages greater than V+ or less than GND may cause destructive device latch-up. Therefore, it is recommended that inputs from sources other than the same power supply should not be applied to the TC7109A before its power supply is established. In multiple supply systems, the supply to the device should be activated first.

3: This limit refers to that of the package and will not occur during normal operation.

HANDLING PRECAUTIONS: These devices are CMOS and must be handled correctly to prevent damage. Package and store only in conductive foam, antistatic tubes, or other conducting material. Use proper antistatic handling procedures. Do not connect in circuits under “power-on” conditions, as high transients may cause permanent damage.

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2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number (40-Pin PDIP)	Symbol	Description
1	GND	Digital ground, 0V, ground return for all digital logic.
2	STATUS	Output HIGH during integrate and de-integrate until data is latched. Output LOW when analog section is in auto-zero or zero integrator configuration.
3	POL	Polarity – High for positive input.
4	OR	Over Range – High if over ranged (Three-State Data bit).
5	B_{12}	Bit 12 (Most Significant bit) (Three-State Data bit).
6	B_{11}	Bit 11 (Three-State Data bit).
7	B_{10}	Bit 10 (Three-State Data bit).
8	B_9	Bit 9 (Three-State Data bit).
9	B_8	Bit 8 (Three-State Data bit).
10	B_7	Bit 7 (Three-State Data bit).
11	B_6	Bit 6 (Three-State Data bit).
12	B_5	Bit 5 (Three-State Data bit).
13	B_4	Bit 4 (Three-State Data bit).
14	B_3	Bit 3 (Three-State Data bit).
15	B_2	Bit 2 (Three-State Data bit).
16	B_1	Bit 1 (Least Significant bit) (Three-State Data bit).
17	TEST	Input High – Normal operation. Input LOW – Forces all bit outputs HIGH. **Note:** This input is used for test purposes only.
18	$\overline{\text{LBEN}}$	Low Byte Enable – with MODE (Pin 21) LOW, and $\overline{\text{CE}}/\overline{\text{LOAD}}$ (Pin 20) LOW, taking this pin LOW activates low order byte outputs, B_1–B_8. With MODE (Pin 21) HIGH, this pin serves as low byte flag output used in Handshake mode. (See Figure 3-7, Figure , and Figure 3-9.)
19	$\overline{\text{HBEN}}$	High Byte Enable – with MODE (Pin 21) LOW, and $\overline{\text{CE}}/\overline{\text{LOAD}}$ (Pin 20) LOW, taking this pin LOW activates high order byte outputs, B_9–B_{12}, POL, OR. With MODE (Pin 21) HIGH, this pin serves as high byte flag output used in Handshake mode. See Figures 3-7, 3-8, and 3-9.
20	$\overline{\text{CE}}/\overline{\text{LOAD}}$	Chip Enable/Load – with MODE (Pin 21) LOW, $\overline{\text{CE}}/\overline{\text{LOAD}}$ serves as a master output enable. When HIGH, B_1–B_{12}, POL, OR outputs are disabled. When MODE (Pin 21) is HIGH, a load strobe is used in handshake mode. (See Figure 3-7, Figure , and Figure 3-9.)
21	MODE	Input LOW – Direct Output mode where $\overline{\text{CE}}/\overline{\text{LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19), and $\overline{\text{LBEN}}$ (Pin 18) act as inputs directly controlling byte outputs. Input Pulsed HIGH - Causes immediate entry into Handshake mode and output of data as in Figure 3-9. Input HIGH – enables $\overline{\text{CE}}/\overline{\text{LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19), and $\overline{\text{LBEN}}$ (Pin 18) as outputs, Handshake mode will be entered and data output as in Figure 3-7 and Figure 3-9 at conversions completion.
22	OSC IN	Oscillator Input.
23	OSC OUT	Oscillator Output.
24	OSC SEL	Oscillator Select – Input HIGH configures OSC IN, OSC OUT, BUFF OSC OUT as RC oscillator – clock will be same phase and duty cycle as BUFF OSC OUT. Input LOW configures OSC IN, OSC OUT for crystal oscillator - clock frequency will be 1/58 of frequency at BUFF OSC OUT.
25	BUFF OSC OUT	Buffered Oscillator Output.
26	RUN/$\overline{\text{HOLD}}$	Input HIGH – Conversions continuously performed every 8192 clock pulses. Input LOW – Conversion in progress completed; converter will stop in auto-zero seven counts before integrate.
27	SEND	Input - Used in Handshake mode to indicate ability of an external device to accept data. Connect to V+ if not used.
28	V-	Analog Negative Supply – Nominally -5V with respect to GND (Pin 1).
29	REF OUT	Reference Voltage Output – Nominally 2.8V down from V+ (Pin 40).

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TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number (40-Pin PDIP)	Symbol	Description
30	BUFF	Buffer Amplifier Output.
31	AZ	Auto-Zero Node – Inside foil of C_{AZ}.
32	INT	Integrator Output – Outside foil of C_{INT}.
33	COMMON	Analog Common – System is auto-zeroed to COMMON.
34	IN LO	Differential Input Low Side.
35	IN HI	Differential Input High Side.
36	REF IN+	Differential Reference Input Positive.
37	REF CAP+	Reference Capacitor Positive.
38	REF CAP-	Reference Capacitor Negative.
39	REF IN-	Differential Reference Input Negative.
40	V+	Positive Supply Voltage – Nominally +5V with respect to GND (Pin 1).

Note: All Digital levels are positive true.

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3.0 DETAILED DESCRIPTION

(All Pin Designations Refer to 40-Pin DIP.)

3.1 Analog Section

The Typical Application diagram on page 3 shows a block diagram of the analog section of the TC7109A. The circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle), when the RUN/$\overline{\text{HOLD}}$ input is left open or connected to V+. Each measurement cycle is divided into four phases, as shown in Figure 3-1. They are: (1) Auto-Zero (AZ), (2) Signal Integrate (INT), (3) Reference De-integrate (DE), and (4) Zero Integrator (ZI).

3.1.1 AUTO-ZERO PHASE

The buffer and the integrator inputs are disconnected from input high and input low and connected to analog common. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor, C_{AZ}, to compensate for offset voltage in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the AZ accuracy is limited only by the noise of the system. The offset referred to the input is less than 10μV.

3.1.2 SIGNAL INTEGRATE PHASE

The buffer and integrator inputs are removed from common and connected to input high and input low. The auto-zero loop is opened. The auto-zero capacitor is placed in series in the loop to provide an equal and opposite compensating offset voltage. The differential voltage between input high and input low is integrated for a fixed time of 2048 clock periods. At the end of this phase, the polarity of the integrated signal is determined. If the input signal has no return to the converter's power supply, input low can be tied to analog common to establish the correct Common mode voltage.

3.1.3 DE-INTEGRATE PHASE

Input high is connected across the previously charged reference capacitor and input low is internally connected to analog common. Circuitry within the chip ensures the capacitor will be connected with the correct polarity to cause the integrator output to return to the zero crossing (established by auto-zero), with a fixed slope. The time, represented by the number of clock periods counted for the output to return to zero, is proportional to the input signal.

3.1.4 ZERO INTEGRATOR PHASE

The ZI phase only occurs when an input over range condition exists. The function of the ZI phase is to eliminate residual charge on the integrator capacitor after an over range measurement. Unless removed, the residual charge will be transferred to the auto-zero capacitor and cause an error in the succeeding conversion.

The ZI phase virtually eliminates hysteresis, or "cross-talk" in multiplexed systems. An over range input on one channel will not cause an error on the next channel measured. This feature is especially useful in thermocouple measurements, where unused (or broken thermocouple) inputs are pulled to the positive supply rail.

During ZI, the reference capacitor is charged to the reference voltage. The signal inputs are disconnected from the buffer and integrator. The comparator output is connected to the buffer input, causing the integrator output to be driven rapidly to 0V (Figure 3-1). The ZI phase only occurs following an over range and lasts for a maximum of 1024 clock periods.

3.1.5 DIFFERENTIAL INPUT

The TC7109A has been optimized for operation with analog common near digital ground. With +5V and -5V power supplies, a full ±4V full scale integrator swing maximizes the analog section's performance.

A typical CMRR of 86dB is achieved for input differential voltages anywhere within the typical Common mode range of 1V below the positive supply, to 1.5V above the negative supply. However, for optimum performance, the IN HI and IN LO inputs should not come within 2V of either supply rail. Since the integrator also swings with the Common mode voltage, care must be exercised to ensure the integrator output does not saturate. A worst-case condition is near a full scale negative differential input voltage with a large positive Common mode voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive Common mode voltage. In such cases, the integrator swing can be reduced to less than the recommended ±4V full scale value, with some loss of accuracy. The integrator output can swing to within 0.3V of either supply without loss of linearity.

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3.1.6 DIFFERENTIAL REFERENCE

The reference voltage can be generated anywhere within the power supply voltage of the converter. Roll-over voltage is the main source of Common mode error, caused by the reference capacitor losing or gaining charge, due to stray capacity on its nodes. With a large Common mode voltage, the reference capacitor can gain charge (increase voltage) when called upon to de-integrate a positive signal and lose charge (decrease voltage) when called upon to de-integrate a negative input signal. This difference in reference for (+) or (–) input voltages will cause a rollover error. This error can be held to less than 0.5 count, worst-case, by using a large reference capacitor in comparison to the stray capacitance. To minimize rollover error from these sources, keep the reference Common mode voltage near or at analog common.

3.2 Digital Section

The digital section is shown in Figure 3-2 and includes the clock oscillator and scaling circuit, a 12-bit binary counter with output latches and TTL compatible three-state output drivers, UART handshake logic, polarity, over range, and control logic. Logic levels are referred to as LOW or HIGH.

Inputs driven from TTL gates should have 3kΩ to 5kΩ pull-up resistors added for maximum noise immunity. For minimum power consumption, all inputs should swing from GND (LOW) to V+ (HIGH).

3.2.1 STATUS OUTPUT

During a conversion cycle, the Status output goes high at the beginning of signal integrate and goes low one-half clock period after new data from the conversion has been stored in the output latches (see Figure 3-1). The signal may be used as a “data valid” flag to drive interrupts, or for monitoring the status of the converter. (Data will not change while status is low.)

3.2.2 MODE INPUT

The Output mode of the converter is controlled by the MODE input. The converter is in its “Direct” Output mode, when the MODE input is LOW or left open. The output data is directly accessible under the control of the chip and byte enable inputs (this input is provided with a pull-down resistor to ensure a LOW level when the pin is left open). When the MODE input is pulsed high, the converter enters the UART Handshake mode and outputs the data in 2 bytes, then returns to “Direct” mode. When the MODE input is kept HIGH, the converter will output data in the Handshake mode at the end of every conversion cycle. With MODE = 0 (direct bus transfer), the send input should be tied to V+. (See “Handshake Mode”.)

3.2.3 RUN/$\overline{\text{HOLD}}$ INPUT

With the RUN/$\overline{\text{HOLD}}$ input high, or open, the circuit operates normally as a dual slope ADC, as shown in Figure 3-1. Conversion cycles operate continuously with the output latches updated after zero crossing in the De-integrate mode. An internal pull-up resistor is provided to ensure a HIGH level with an open input.

The RUN/$\overline{\text{HOLD}}$ input may be used to shorten conversion time. If RUN/$\overline{\text{HOLD}}$ goes LOW any time after zero crossing in the De-integrate mode, the circuit will jump to auto-zero and eliminate that portion of time normally spent in de-integrate.

If RUN/$\overline{\text{HOLD}}$ stays or goes LOW, the conversion will complete with minimum time in de-integrate. It will stay in auto-zero for the minimum time and wait in auto-zero for a HIGH at the RUN/$\overline{\text{HOLD}}$ input. As shown in Figure 3-3, the Status output will go HIGH, 7 clock periods after RUN/$\overline{\text{HOLD}}$ is changed to HIGH, and the converter will begin the integrate phase of the next conversion.

The RUN/$\overline{\text{HOLD}}$ input allows controlled conversion interface. The converter may be held at Idle in auto-zero with RUN/$\overline{\text{HOLD}}$ LOW. The conversion is started when RUN/$\overline{\text{HOLD}}$ goes HIGH, and the new data is valid when the Status output goes LOW (or is transferred to the UART; see “Handshake Mode”). RUN/$\overline{\text{HOLD}}$ may now go LOW, terminating de-integrate and ensuring a minimum auto-zero time before stopping to wait for the next conversion. Conversion time can be minimized by ensuring RUN/$\overline{\text{HOLD}}$ goes LOW during de-integrate, after zero crossing, and goes HIGH after the hold point is reached.

The required activity on the RUN/$\overline{\text{HOLD}}$ input can be provided by connecting it to the buffered oscillator output. In this mode, the input value measured determines the conversion time.

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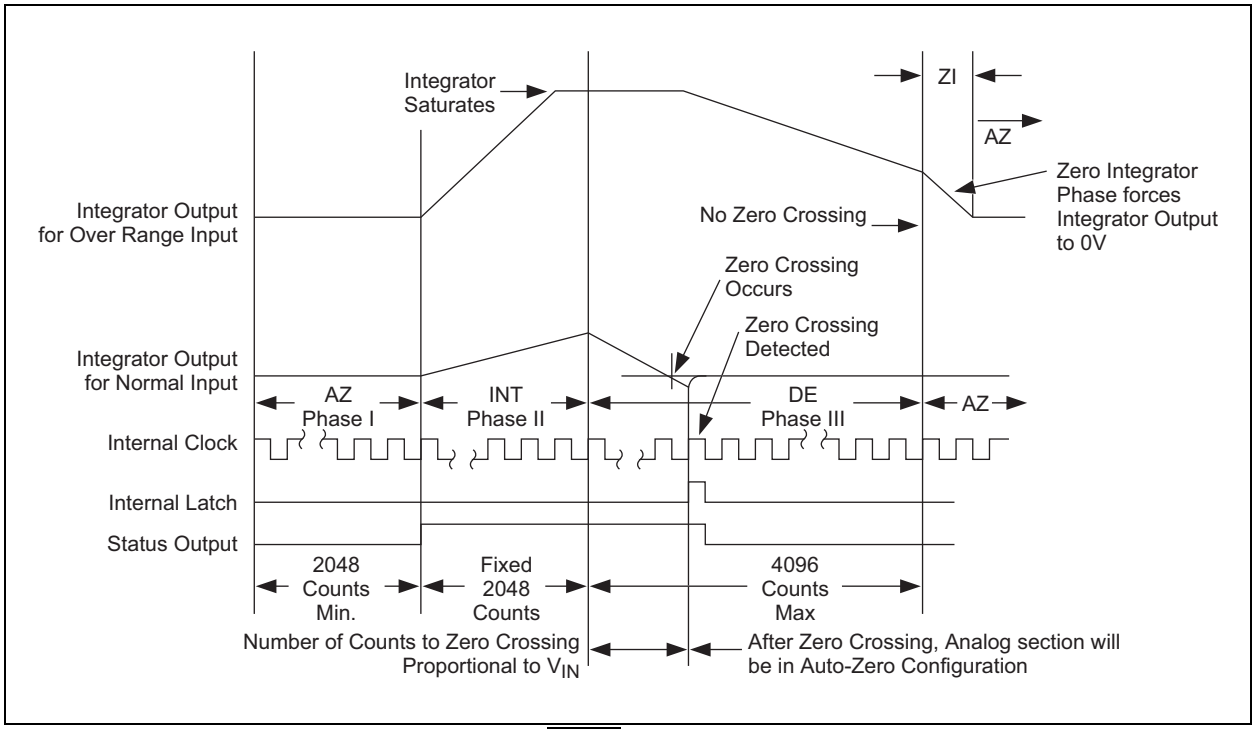


FIGURE 3-1: *Conversion Timing (RUN/$\overline{HOLD}$) Pin High*

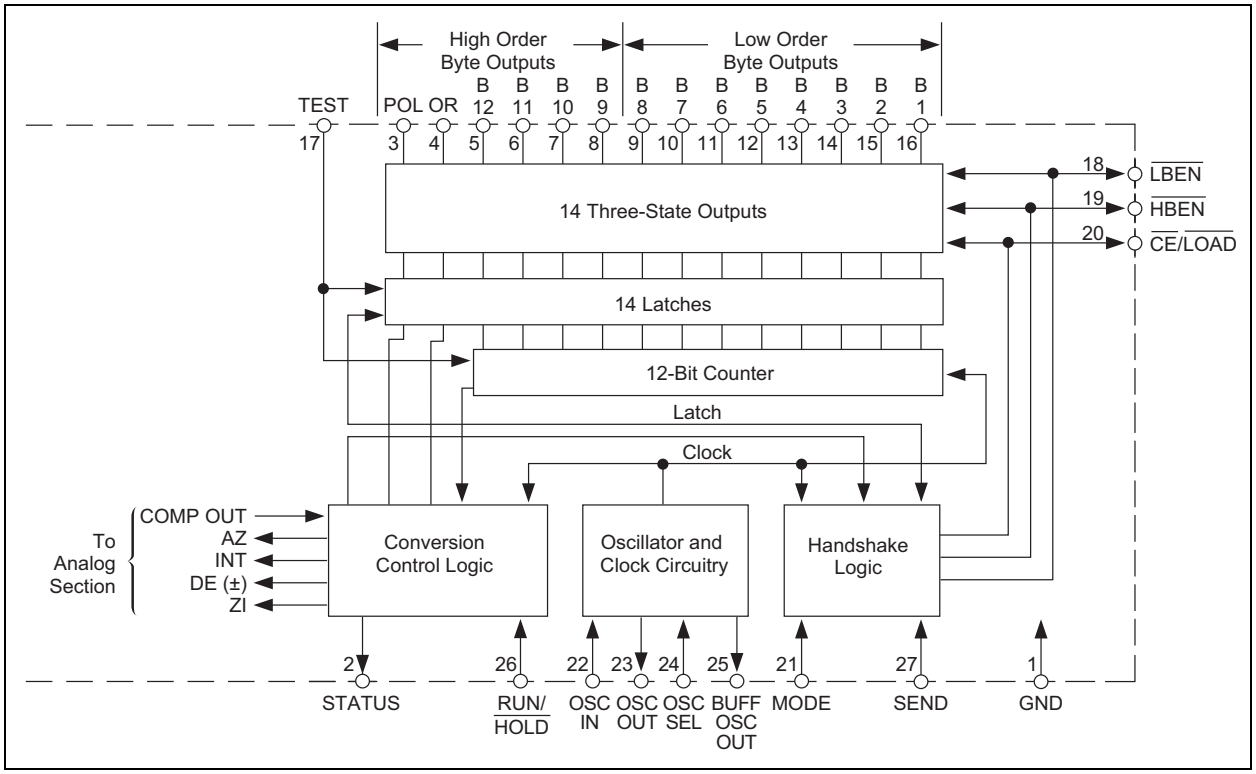


FIGURE 3-2: *Digital Section*

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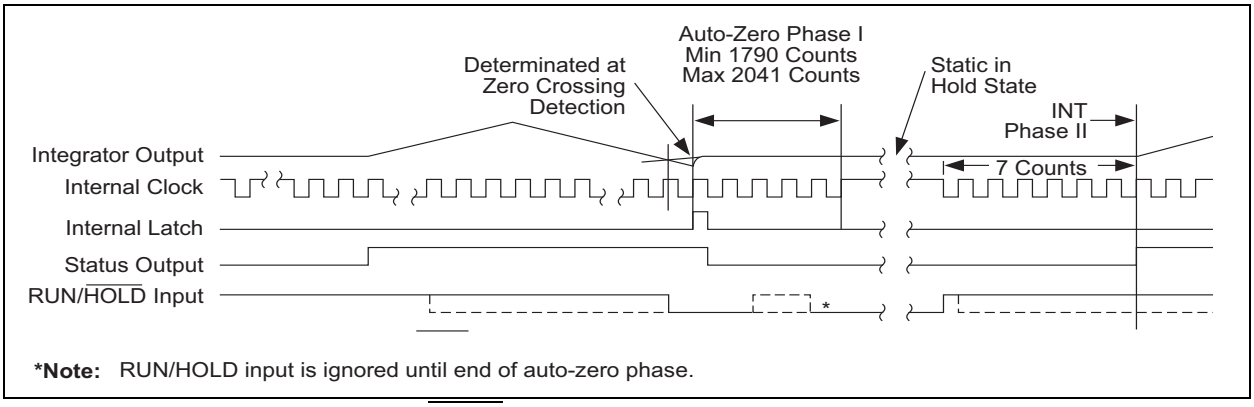


FIGURE 3-3: *TC7109A RUN/HOLD Operation*

3.2.4 DIRECT MODE

The data outputs (bits 1 through 8, low order bytes; bits 9 through 12, polarity and over range high order bytes) are accessible under control of the byte and chip enable terminals as inputs, with the MODE pin at a LOW level. These three inputs are all active LOW. Internal pull-up resistors are provided for an inactive HIGH level when left open. When chip enable is LOW, a byte enable input LOW will allow the outputs of the byte to become active. A variety of parallel data accessing techniques may be used, as shown in the "Interfacing" section. (See Figure 3-4 and Table 3-1.)

The access of data should be synchronized with the conversion cycle by monitoring the Status output. This prevents accessing data while it is being updated and eliminates the acquisition of erroneous data.

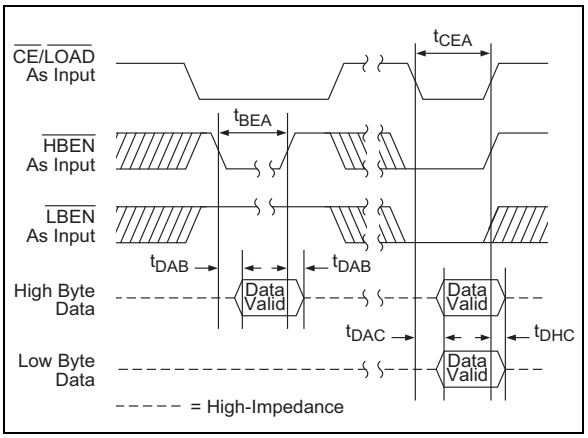


FIGURE 3-4: *TC7109A Direct Mode Output Timing*

TABLE 3-1: TC7109A DIRECT MODE TIMING REQUIREMENTS

Symbol	Description	Min	Typ	Max	Units
t_{BEA}	Byte Enable Width	200	500	—	nsec
t_{DAB}	Data Access Time from Byte Enable	—	150	300	nsec
t_{DHB}	Data Hold Time from Byte Enable	—	150	300	nsec
t_{CEA}	Chip Enable Width	300	500		nsec
t_{DAC}	Data Access Time from Chip Enable	—	200	400	nsec
t_{DHC}	Data Hold Time from Chip Enable	—	200	400	nsec

3.2.5 HANDSHAKE MODE

An alternative means of interfacing the TC7109A to digital systems is provided when the Handshake Output mode of the TC7109A becomes active in controlling the flow of data, instead of passively responding to chip and byte enable inputs. This mode allows a direct interface between the TC7109A and industry standard UARTs with no external logic required. The TC7109A provides all the control and flag signals necessary to sequence the two bytes of data into the UART and initiate their transmission in serial form when triggered into the Handshake mode. The cost of designing remote data acquisition stations is reduced using serial data transmission to minimize the number of lines to the central controlling processor.

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The MODE input controls the Handshake mode. When the MODE input is held HIGH, the TC7109A enters the Handshake mode after new data has been stored in the output latches at the end of every conversion performed (see Figure 3-7 and Figure). Entry into the Handshake mode may be triggered on demand by the MODE input. At any time during the conversion cycle, the LOW-to-HIGH transition of a short pulse at the MODE input will cause immediate entry into the Handshake mode. If this pulse occurs while new data is being stored, the entry into Handshake mode is delayed until the data is stable. The MODE input is ignored in the Handshake mode, and until the converter completes the output cycle and clears the Handshake mode, data updating will be inhibited (see Figure 3-9).

When the MODE input is HIGH, or when the converter enters the Handshake mode, the chip and byte enable inputs become TTL compatible outputs, which provide the output cycle control signals (see Figure 3-7, Figure and Figure 3-9). The SEND input is used by the converter as an indication of the ability of the receiving device (such as a UART) to accept data in the Handshake mode. The sequence of the output cycle with SEND held HIGH is shown in Figure 3-7. The Handshake mode (internal MODE HIGH) is entered after the data latch pulse (the $\overline{CE}$/LOAD, $\overline{LBEN}$ and $\overline{HBEN}$ terminals are active as outputs, since MODE remains HIGH).

The HIGH level at the SEND input is sensed on the same HIGH-to-LOW internal clock edge. On the next LOW-to-HIGH internal clock edge, the high order byte (bits 9 through 12, POL, and OR) outputs are enabled and the $\overline{CE}$/LOAD and the $\overline{HBEN}$ outputs assume a LOW level. The $\overline{CE}$/LOAD output remains LOW for one full internal clock period only; the data outputs remain active for 1-1/2 internal clock periods; and the high byte enable remains LOW for 2 clock periods.

The $\overline{CE}$/$\overline{LOAD}$ output LOW level, or LOW-to-HIGH edge, may be used as a synchronizing signal to ensure valid data, and the byte enable as an output may be used as a byte identification flag. With SEND remaining HIGH, the converter completes the output cycle using $\overline{CE}$/LOAD and $\overline{LBEN}$, while the low order byte outputs (bits 1 through 8) are activated. When both bytes are sent, the Handshake mode is terminated. The typical UART interfacing timing is shown in Figure .

The SEND input is used to delay portions of the sequence, or handshake, to ensure correct data transfer. This timing diagram shows an industry standard HD6403 or CDP1854 CMOS UART to interface to serial data channels. The SEND input to the TC7109A is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the $\overline{CE}$/LOAD input of the TC7109A drives the TBRL (Transmitter Buffer Register Load) input to the UART. The eight transmitter buffer register inputs accept the parallel data outputs. With the UART transmitter buffer register empty, the SEND input will be HIGH when the Handshake mode is entered, after new data is stored. The high order byte outputs become active and the $\overline{CE}$/LOAD and $\overline{HBEN}$ inputs will go LOW after SEND is sensed. When $\overline{CE}$/LOAD goes HIGH at the end of one clock period, the high order byte data is clocked into the UART transmitter buffer register. The UART TBRE output will go LOW, which halts the output cycle with the HBEN output LOW, and the high order byte outputs active. When the UART has transferred the data to the transmitter register and cleared the transmitter buffer register, the TBRE returns HIGH. The high order byte outputs are disabled on the next TC7109A internal clock HIGH-to-LOW edge, and one-half internal clock later, the $\overline{HBEN}$ output returns HIGH. The $\overline{CE}$/LOAD and $\overline{LBEN}$ outputs go LOW at the same time as the low order byte outputs become active. When the $\overline{CE}$/LOAD returns HIGH at the end of one clock period, the low order data is clocked into the UART transmitter buffer register, and TBRE again goes LOW. The next TC7109A internal clock HIGH-to-LOW edge will sense when TBRE returns to a HIGH, disabling the data inputs. One-half internal clock later, the Handshake mode is cleared, and the $\overline{CE}$/LOAD, $\overline{HBEN}$ and $\overline{LBEN}$ terminals return HIGH and stay active, if MODE still remains HIGH.

Handshake output sequences may be performed on demand by triggering the converter into Handshake mode with a LOW-to-HIGH edge on the MODE input. A handshake output sequence triggered is shown in Figure 3-9. The SEND input is LOW when the converter enters Handshake mode. The whole output sequence is controlled by the SEND input, and the sequence for the first (high order) byte is similar to the sequence for the second byte.

Figure 3-9 also shows that the output sequence can take longer than a conversion cycle. New data will not be latched when the Handshake mode is still in progress and is, therefore, lost.

3.3 Oscillator

The oscillator may be over driven, or may be operated as an RC or crystal oscillator. The OSCILLATOR SELECT input optimizes the internal configuration of the oscillator for RC or crystal operation. The OSCILLATOR SELECT input is provided with a pull-up resistor. When the OSCILLATOR SELECT input is HIGH or left open, the oscillator is configured for RC operation. The internal clock will be the same frequency and phase as the signal at the BUFFERED OSCILLATOR OUTPUT. Connect the resistor and capacitor as in Figure . The circuit will oscillate at a frequency given by $f = 0.45/RC$. A 100kΩ resistor is recommended for useful ranges of frequency. The capacitor value should be chosen such that 2048 clock periods are close to an integral multiple of the 60Hz period for optimum 60Hz line rejection.

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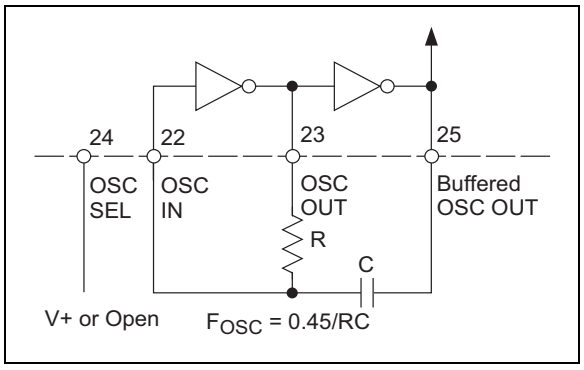


FIGURE 3-5: *TC7109A RC Oscillator*

With OSCILLATOR SELECT input LOW, two on-chip capacitors and a feedback device are added to the oscillator. In this configuration, the oscillator will operate with most crystals in the 1MHz to 5MHz range, with no external components (Figure). The OSCILLATOR SELECT input LOW inserts a fixed 458 divider circuit between the BUFFERED OSCILLATOR OUTPUT and the internal clock. A 3.58MHz TV crystal gives a division ratio, providing an integration time given by:

EQUATION 3-1:

$$t = (2048 \text{ clock periods}) \frac{58}{3.58 \text{ MHz}} = 33.18 \text{ msec}$$

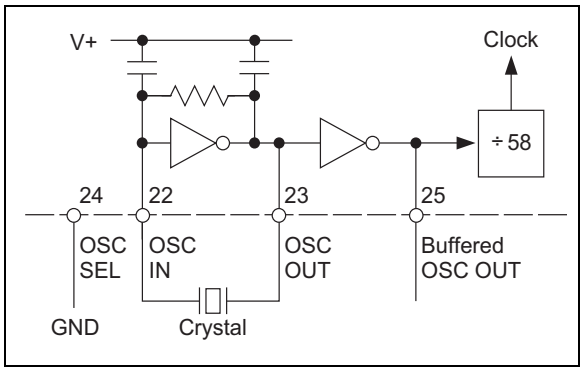


FIGURE 3-6: *Crystal Oscillator*

The error is less than 1% from two 60Hz periods, or 33.33msec, which will give better than 40dB, 60Hz rejection. The converter will operate reliably at conversion rates up to 30 per second, corresponding to a clock frequency of 245.8kHz.

When the oscillator is to be over driven, the OSCILLATOR OUTPUT should be left open, and the over driving signal should be applied at the OSCILLATOR INPUT.

The internal clock will be of the same duty cycle, frequency and phase as the input signal. When the OSCILLATOR SELECT is at GND, the clock will be 1/58 of the input frequency.

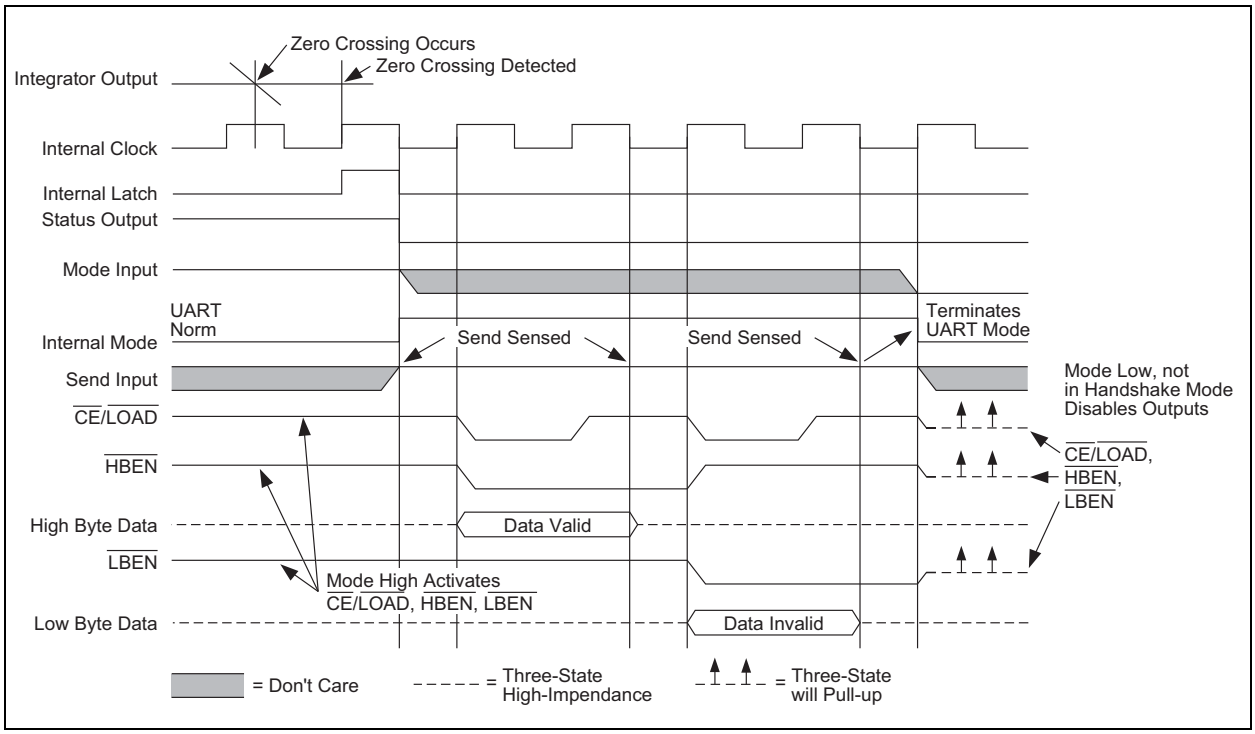


FIGURE 3-7: *TC7109A Handshake with Send Input Held Positive*

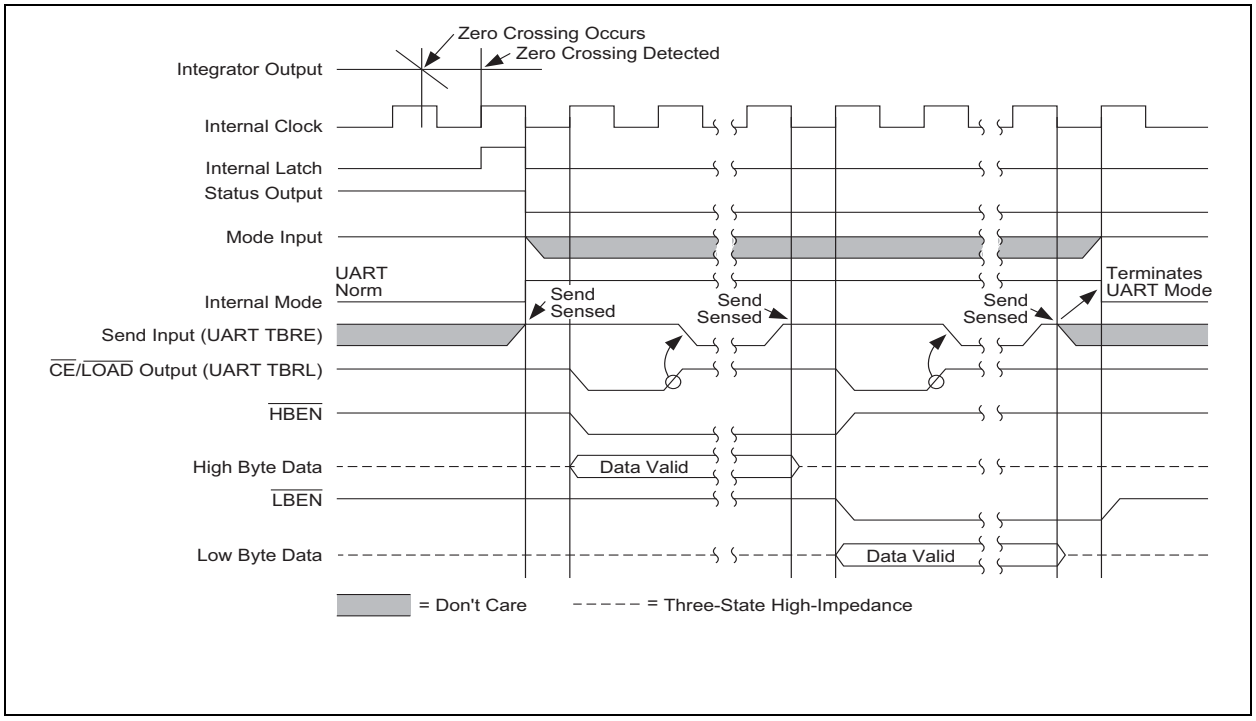


FIGURE 3-8: *TC7109A Handshake – Typical UART Interface Timing*

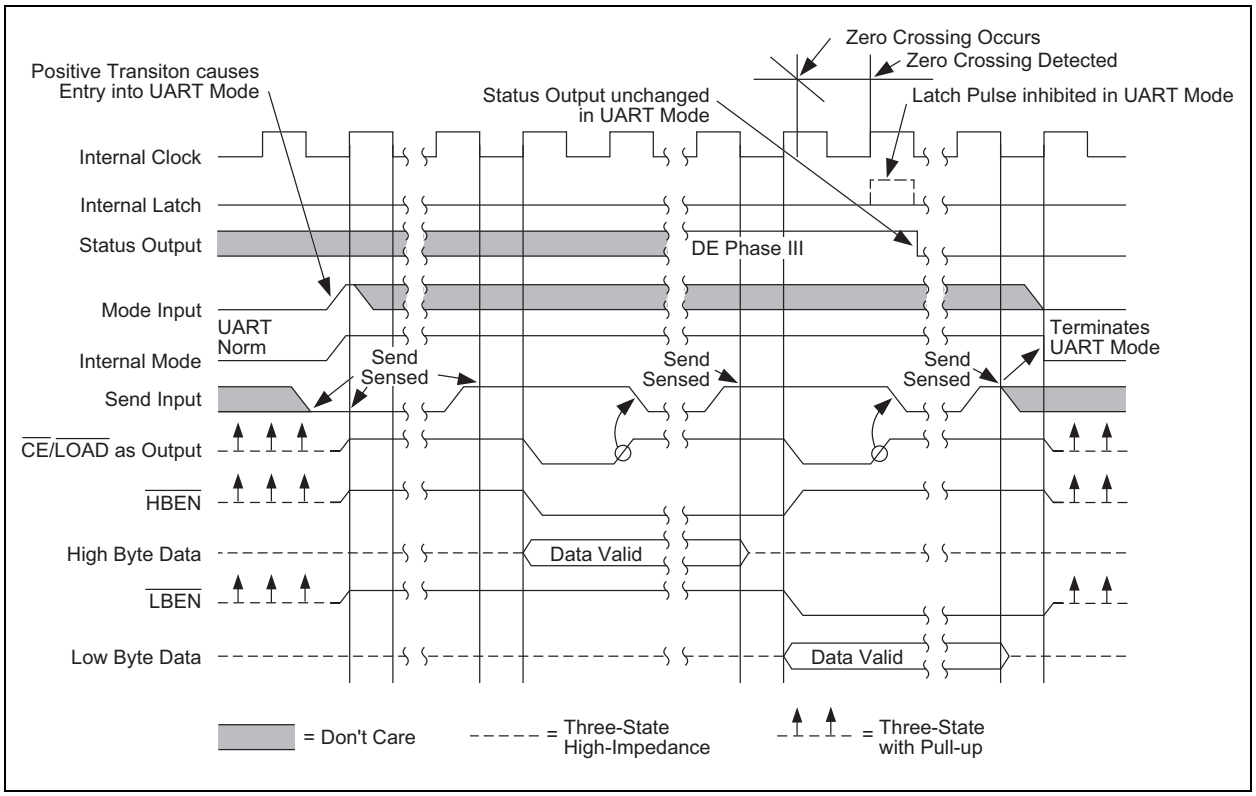


FIGURE 3-9: *TC7109A Handshake Triggered by Mode Input*

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3.4 Test Input

The counter and its outputs may be tested easily. When the TEST input is connected to GND, the internal clock is disabled and the counter outputs are all forced into the HIGH state. When the input returns to the 1/2 (V+ – GND) voltage or to V+ and one clock is input, the counter outputs will all be clocked to the LOW state.

The counter output latches are enabled when the TEST input is taken to a level halfway between V+ and GND, allowing the counter contents to be examined any time.

3.5 Component Value Selection

The integrator output swing for full scale should be as large as possible. For example, with ±5V supplies and COMMON connected to GND, the nominal integrator output swing at full scale is ±4V. Since the integrator output can go to 0.3V from either supply without significantly effecting linearity, a 4V integrator output swing allows 0.7V for variations in output swing, due to component value and oscillator tolerances. With ±5V supplies and a Common mode voltage range of ±1V required, the component values should be selected to provide ±3V integrator output swing. Noise and rollover errors will be slightly worse than in the ±4V case. For large Common mode voltage ranges, the integrator output swing must be reduced further. This will increase both noise and rollover errors. To improve performance, ±6V supplies may be used.

3.5.1 INTEGRATING CAPACITOR

The integrating capacitor, C_{INT}, should be selected to give the maximum integrator output voltage swing that will not saturate the integrator to within 0.3V from either supply. A ±3.5V to ±4V integrator output swing is nominal for the TC7109A, with ±5V supplies and analog common connected to GND. For 7-1/2 conversions per second (61.72kHz internal clock frequency), nominal values C_{INT} and C_{AZ} are 0.15μF and 0.33μF, respectively. These values should be changed if different clock frequencies are used to maintain the integrator output voltage swing. The value of C_{INT} is given by:

EQUATION 3-2:

$$C_{INT} = \frac{(2048 \text{ Clock Period})\ (20\ \mu A)}{\text{Integrator Output Voltage Swings}}$$

The integrating capacitor must have low dielectric absorption to prevent rollover errors. Polypropylene capacitors give undetectable errors, at reasonable cost, up to +85°C.

3.5.2 INTEGRATING RESISTOR

The integrator and buffer amplifiers have a class A output stage with 100μA of quiescent current. They supply 20μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2.048V full scale, a 100kΩ resistor is recommended and for 409.6mV full scale, a 20k resistor is recommended. R_{INT} may be selected for other values of full scale by:

EQUATION 3-3:

$$R_{INT} = \frac{\text{Full Scale Voltage}}{20\ \mu A}$$

3.5.3 AUTO-ZERO CAPACITOR

As the auto-zero capacitor is made large, the system noise is reduced. Since the TC7109A incorporates a zero integrator cycle, the size of the auto-zero capacitor does not affect overload recovery. The optimal value of the auto-zero capacitor is between 2 and 4 times C_{INT}. A typical value for C_{AZ} is 0.33μF.

The inner foil of C_{AZ} should be connected to Pin 31 and the outer foil to the RC summing junction. The inner foil of C_{INT} should be connected to the RC summing junction and the outer foil to Pin 32, for best rejection of stray pickups.

3.5.4 REFERENCE CAPACITOR

A 1μF capacitor is recommended for most circuits. However, where a large Common mode voltage exists, a larger value is required to prevent rollover error (e.g., the reference low is not analog common), and a 409.6mV scale is used. The rollover error will be held to 0.5 count with a 10μF capacitor.

3.5.5 REFERENCE VOLTAGE

To generate full scale output of 4096 counts, the analog input required is $V_{IN} = 2V_{REF}$. For 409.6mV full scale, use a reference of 204.8mV. In many applications, where the ADC is connected to a transducer, a scale factor will exist between the input voltage and the digital reading. For instance, in a measuring system, the designer might like to have a full scale reading when the voltage for the transducer is 700mV. Instead of dividing the input down to 409.6mV, the designer should use the input voltage directly and select V_{REF} = 350mV. Suitable values for integrating resistor and capacitor would be 34kΩ and 0.15μF. This makes the system slightly quieter and also avoids a divider network on the input. Another advantage of this system occurs when temperature and weight measurements, with an offset or tare, are desired for non-zero input. The offset may be introduced by connecting the voltage output of the transducer between common and analog high, and the offset voltage between common and analog low, observing polarities carefully. In processor based systems using the TC7109A, it may be more desirable to use software and perform this type of scaling or tare subtraction digitally.

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3.5.6 REFERENCE SOURCES

A major factor in the absolute accuracy of the ADC is the stability of the reference voltage. The 12-bit resolution of the TC7109A is one part in 4096, or 244 ppm. Thus, for the on-board reference temperature coefficient of 70ppm/°C, a temperature difference of 3°C will introduce a one-bit absolute error. Where the ambient temperature is not controlled, or where high accuracy absolute measurements are being made, it is recommended that an external high quality reference be used.

A reference output (Pin 29) is provided, which may be used with a resistive divider to generate a suitable reference voltage (20mA may be sunk without significant variation in output voltage). A pull-up bias device is provided, which sources about 10μA. The output voltage is nominally 2.8V below V+. When using the on-board reference, REF OUT (Pin 29) should be connected to REF IN- (pin 39), and REF IN+ should be connected to the wiper of a precision potentiometer between REF OUT and V+. The test circuit shows the circuit for a 204.8mV reference, generated by a 2kΩ precision potentiometer in series with a 24kΩ fixed resistor.

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4.0 INTERFACING

4.1 Direct Mode

Combinations of chip enable and byte enable control signals, which may be used when interfacing the TC7109A to parallel data lines, are shown in Figure . The CE/LOAD input may be tied low, allowing either byte to be controlled by its own enable (see Figure (A)). Figure (B) shows the HBEN and LBEN as flag inputs, and CE/LOAD as a master enable, which could be the READ strobe available from most microprocessors. Figure (C) shows a configuration where the two byte enables are connected together. The CE/LOAD is a chip enable, and the HBEN and LBEN may be used as a second chip enable, or connected to ground. The 14 data outputs will be enabled at the same time. In the direct MODE, SEND should be tied to V+.

Figure shows interfacing several TC7109A's to a bus, ganging the HBEN and LBEN signals to several converters together, and using the CE/LOAD input to select the desired converter.

Figure through Figure give practical circuits utilizing the parallel three-state output capabilities of the TC7109A. Figure shows parallel interface to the 8748/49 systems via an 8255 PPI, where the TC7109A data outputs are active at all times. This interface can be used in a read-after-update sequence, as shown in Figure . The data is accessed by the high-to-low transition of the Status driving an interrupt to the microcontroller.

The RUN/HOLD input is also used to initiate conversions under software control.

Direct interfacing to most microcontroller busses is easily accomplished through the three-state output of the TC7109A.

Figure 4-8 is a typical connection diagram. To ensure requirements for setup and hold times, minimum pulse widths, and the drive limitations on long busses are met, it is necessary to carefully consider the system timing in this type of interface. This type of interface is used when the memory peripheral address density is low, providing simple address decoding. Interrupt handling can be simplified by using an interface to reduce the component count.

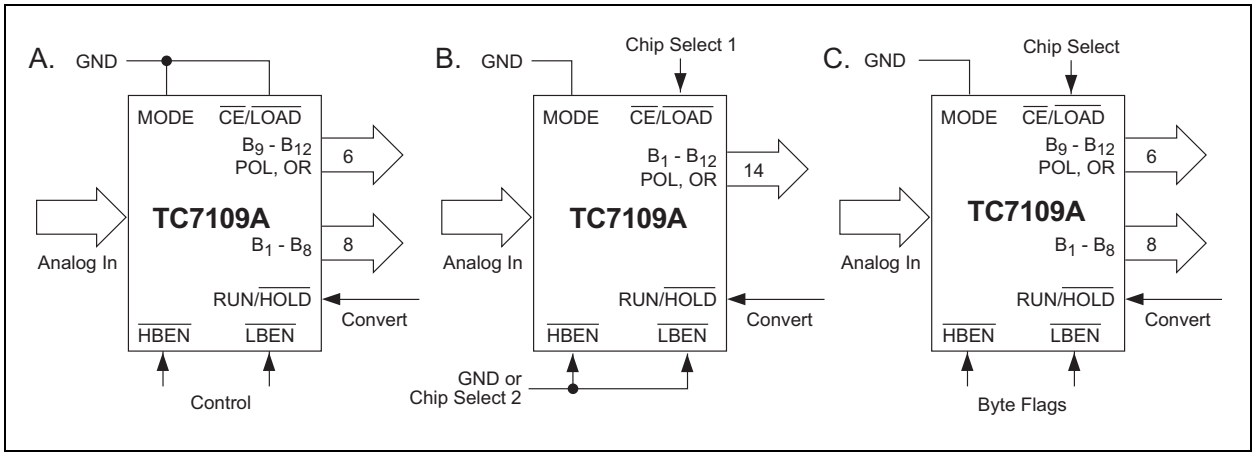


FIGURE 4-1: *Direct Mode Chip and Byte Enable Combination*

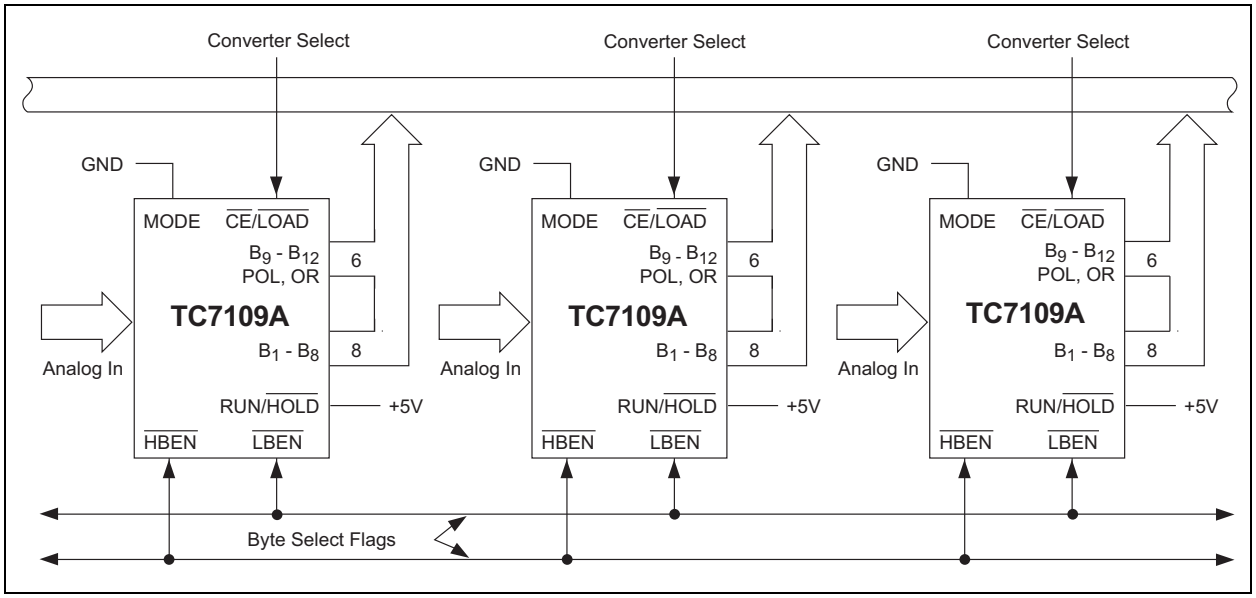


FIGURE 4-2: *Three-Stating Several TC7109As to a Small Bus*

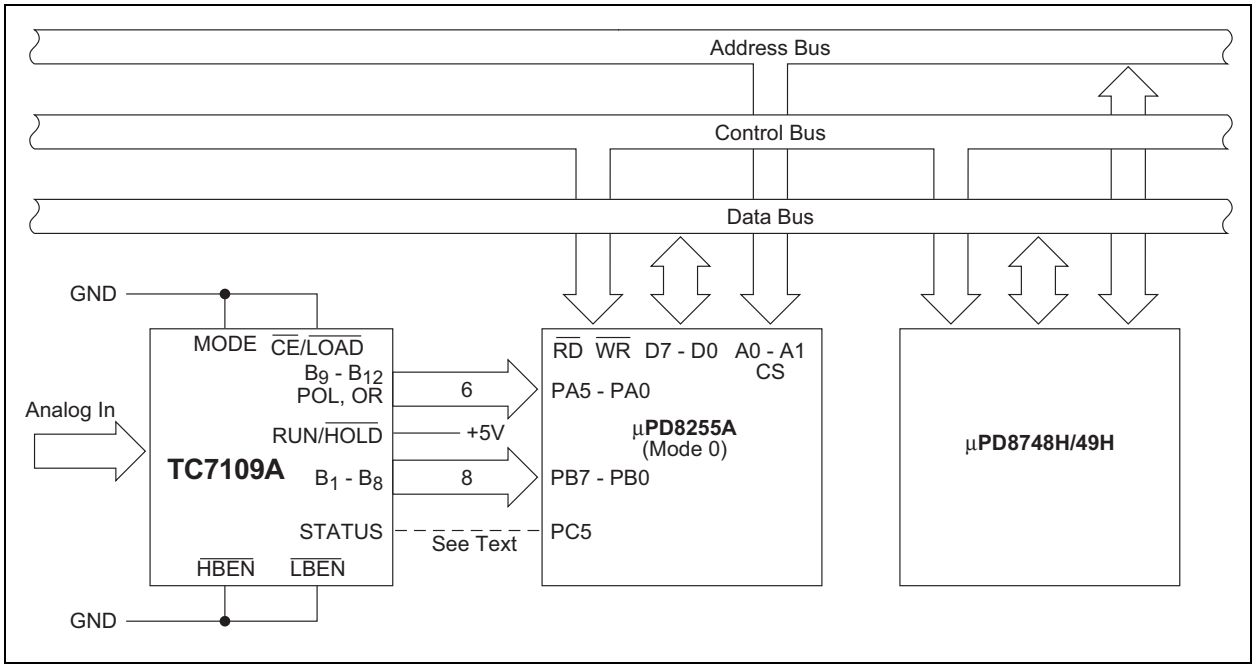


FIGURE 4-3: *Full Time Parallel Interface to µPD8748H/494 Microcontrollers*

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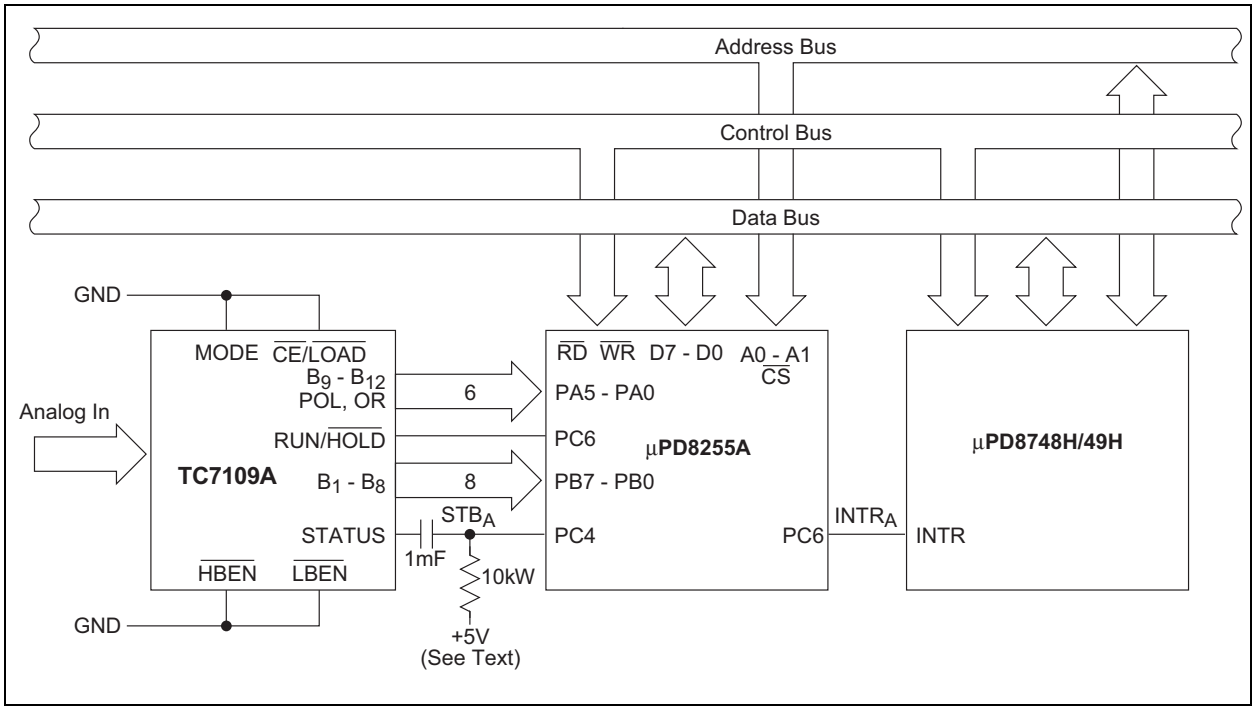


FIGURE 4-4: *Full Time Parallel Interface to µPD8748H/494 Microcontrollers*

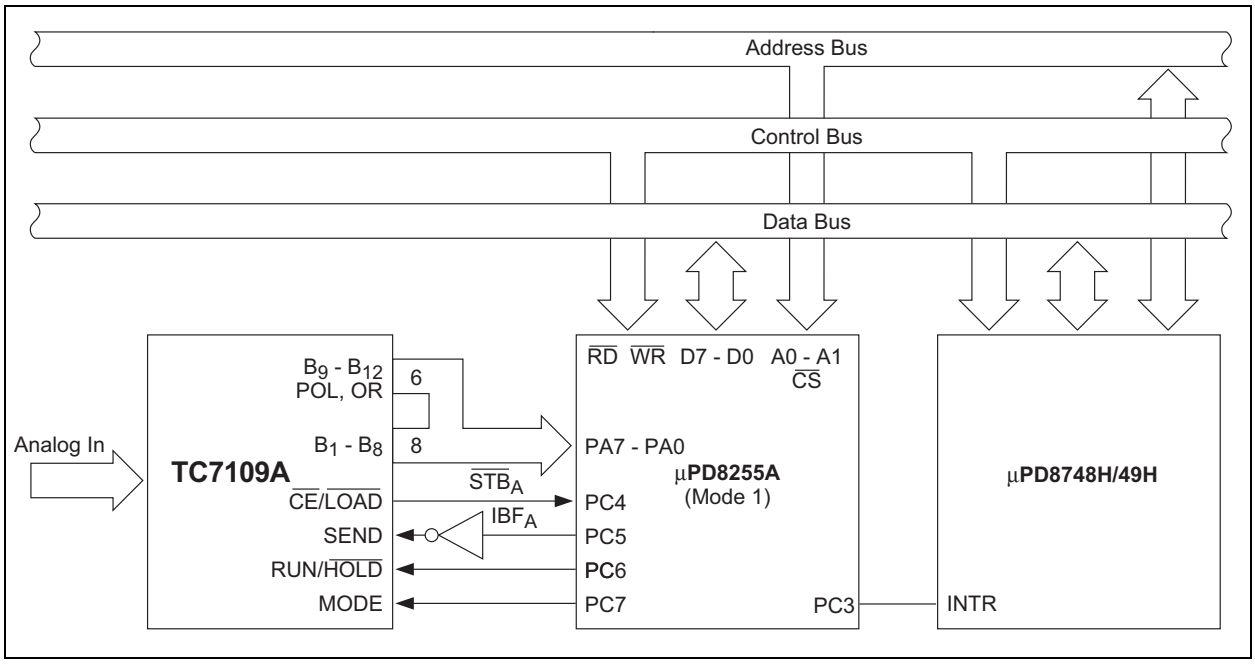


FIGURE 4-5: *TC7109A Handshake Interface to µPD8748H/494 Microcontrollers*

4.2 Handshake Mode

The Handshake mode provides an interface to a wide variety of external devices. The byte enables may be used as byte identification flags, or as load enables, and external latches may be clocked by the rising edge of $\overline{CE}/\overline{LOAD}$. A handshake interface to Intel® microprocessors using an 8255 PPI is shown in Figure . The handshake operation with the 8255 is controlled by inverting its Input Buffer Full (IBF) flag to drive the SEND input to the TC7109A, and using the $\overline{CE}/\overline{LOAD}$ to drive the 8255 strobe. The internal control register of the PPI should be set in MODE 1 for the port used. If the 8255 IBF flag is LOW and the TC7109A is in Handshake mode, the next word will be strobed into the port. The strobe will cause IBF to go HIGH (SEND goes LOW), which will keep the enabled byte outputs active. The PPI will generate an interrupt which, when executed, will result in the data being read. The IBF will be reset LOW when the byte is read, causing the TC7109A to sequence into the next byte. The MODE input to the TC7109A is connected to the control line on the PPI.

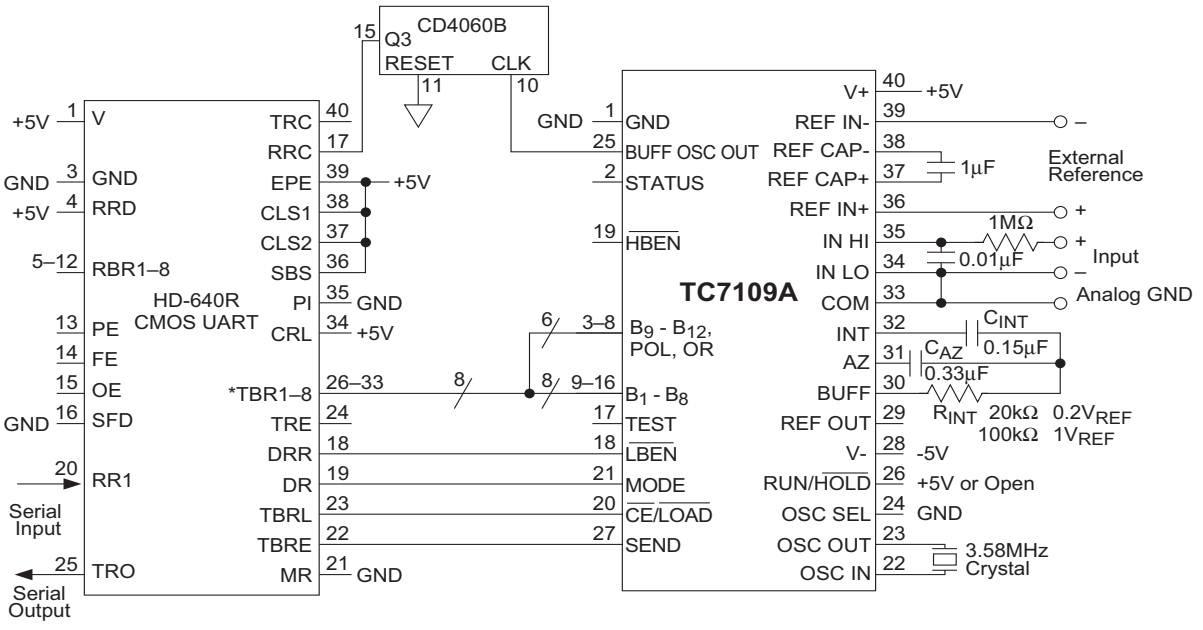
The data from every conversion will be sequenced in two bytes in the system, if this output is left HIGH, or tied HIGH separately. (The data access must take less time than a conversion.) The output sequence can be obtained on demand if this output is made to go from LOW to HIGH and the interrupt may be used to reset the MODE bit.

Conversions may be obtained on command under software control by driving the RUN/$\overline{HOLD}$ input to the TC7109A by a bit of the 8255. Another peripheral device may be serviced by the unused port of the 8255.

The Handshake mode is particularly useful for directly interfacing to industry standard UARTs (such as Intersil HD-6402), providing a means of serially transmitting converted data with minimum component count.

A typical UART connection is shown in Figure . In this circuit, any word received by the UART causes the UART DR (Data Ready) output to go HIGH. The MODE input to the TC7109A goes HIGH, triggering the TC7109A into Handshake mode. The high order byte is output to the UART and when the UART has transferred the data to the Transmitter register, TBRE (SEND) goes HIGH again, $\overline{LBEN}$ will go HIGH, driving the UART DRR (Data Ready Reset), which will signal the end of the transfer of data from the TC7109A to the UART.

An extension of the typical connection to several TC7109A's with one UART is shown in Figure 4-7. In this circuit, the word received by the UART (available at the RBR outputs when DR is HIGH) is used to select which converter will handshake with the UART. Up to eight TC7109A's may interface with one UART, with no external components. Up to 256 converters may be accessed on one serial line with additional components.



***Note:** For lowest power consumption, TBR1-TBR8 inputs should have 100kΩ pull-up resistors to +5V. Send any word to UART to transmit latest result.

FIGURE 4-6: *TC7109 Typical UART Interface*

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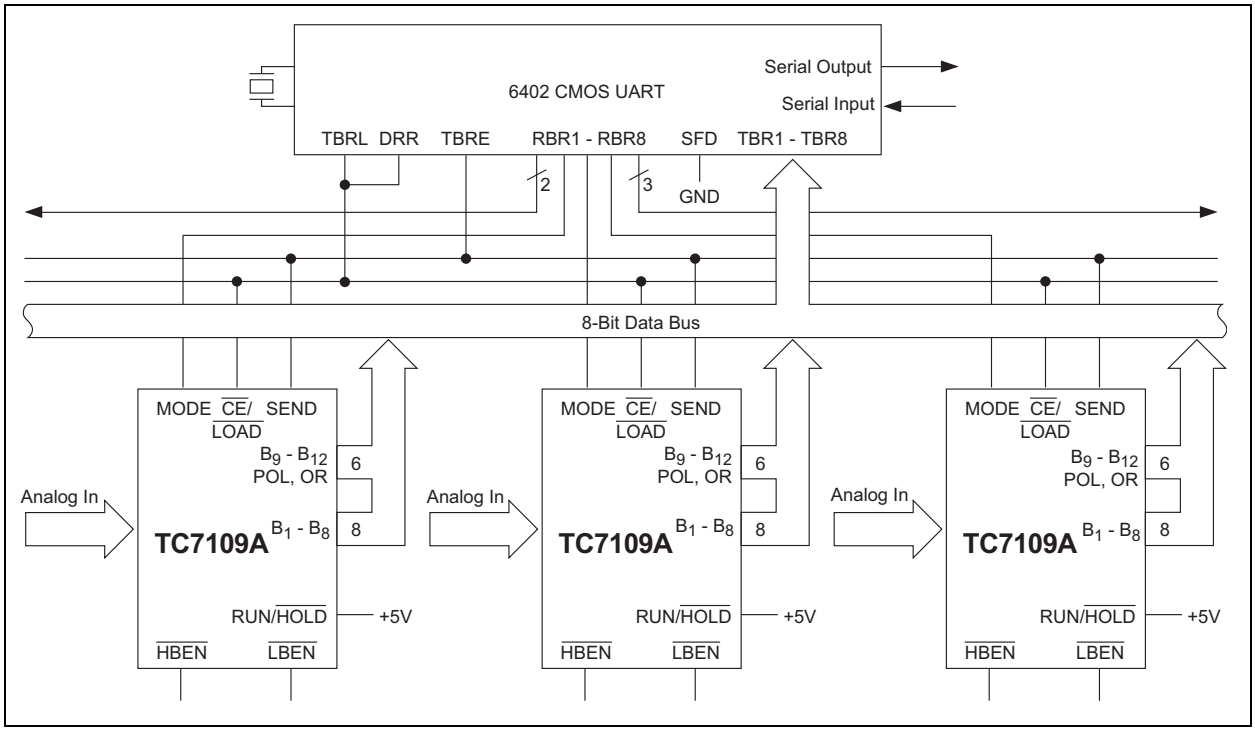


FIGURE 4-7: *Handshake Interface for Multiplexed Converters*

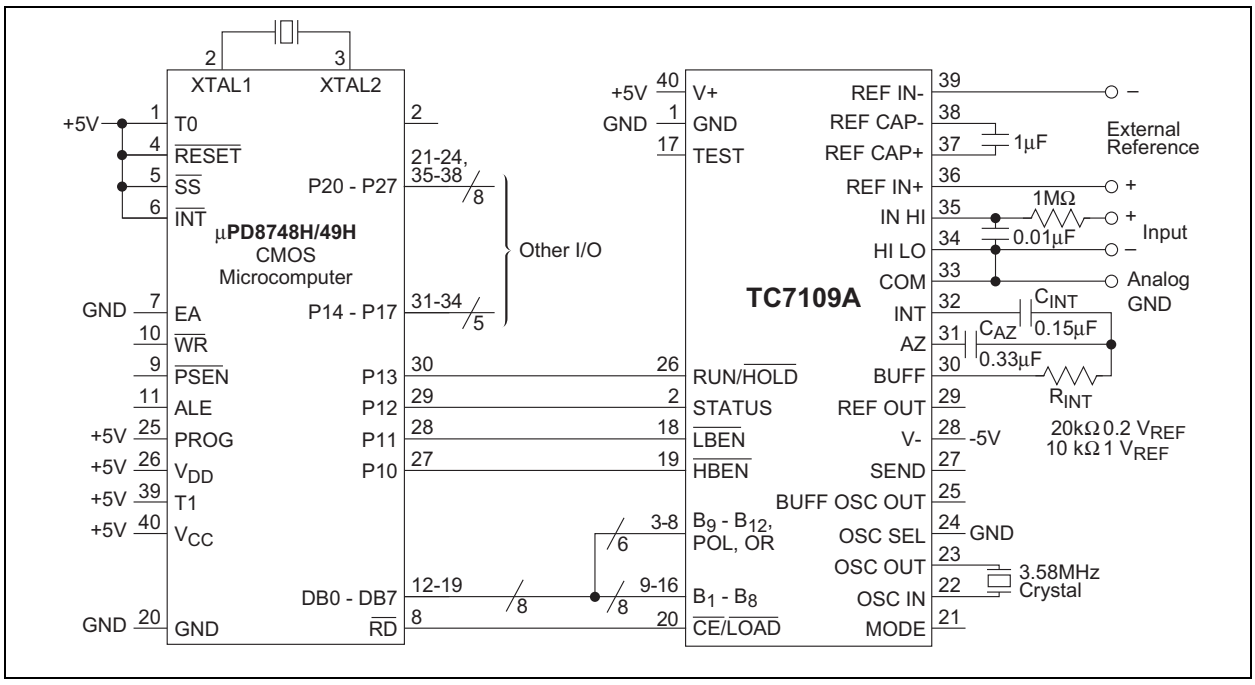


FIGURE 4-8: *Connection Diagram*

5.0 INTEGRATING CONVERTER FEATURES

The output of integrating ADCs represents the integral, or average, of an input voltage over a fixed period of time. Compared with techniques in which the input is sampled and held, the integrating converter averages the effects of noise. A second important characteristic is that time is used to quantize the answer, resulting in extremely small non-linearity errors and no missing output codes. The integrating converter also has very good rejection of frequencies whose periods are an integral multiple of the measurement period. This feature can be used to advantage in reducing line frequency noise (Figure).

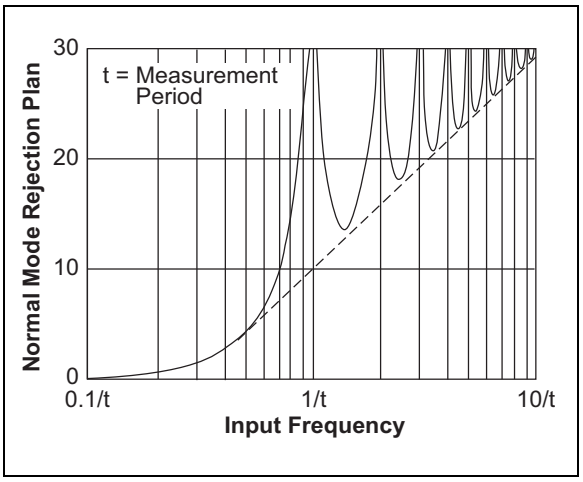


FIGURE 5-1: *Normal Mode Rejection of Dual Slope Converter as a Function of Frequency*

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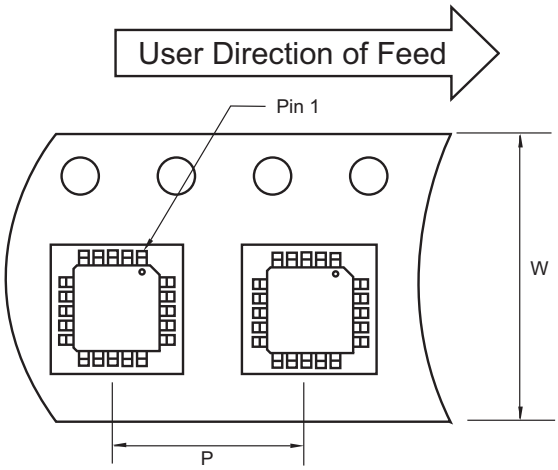
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

Package marking data not available at this time.

6.2 Taping Form

Component Taping Orientation for 44-Pin PQFP Devices



Standard Reel Component Orientation
for 713 Suffix Device

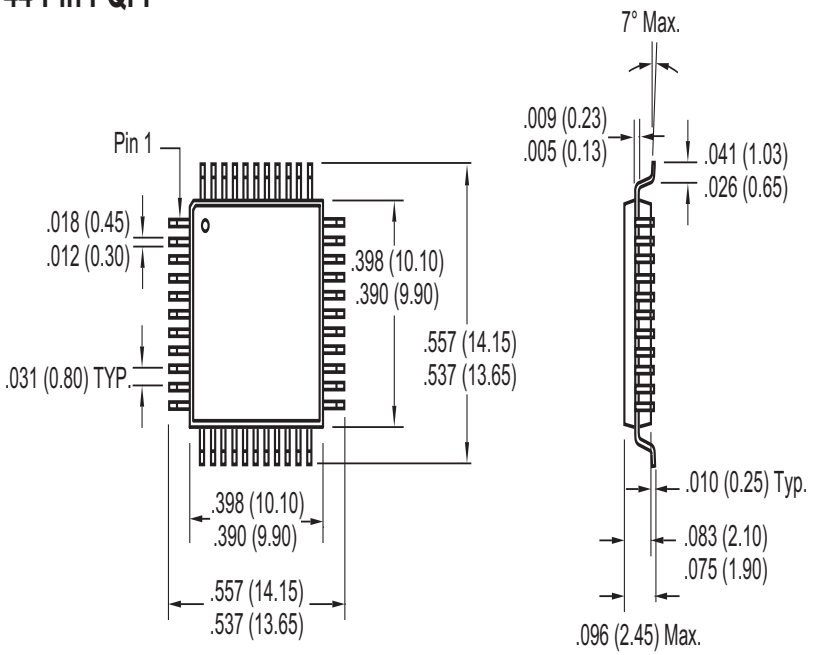
Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
44-Pin PQFP	24 mm	16 mm	500	13 in

Note: Drawing does not represent total number of pins.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

44-Pin PQFP

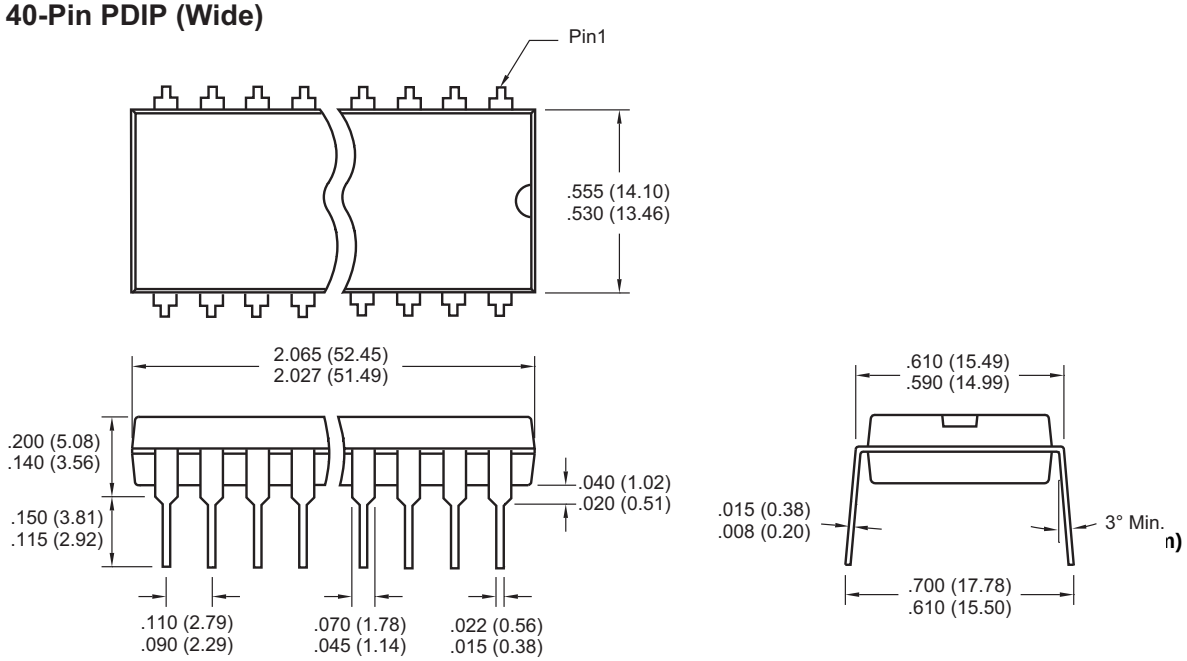


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6.3 Package Dimensions

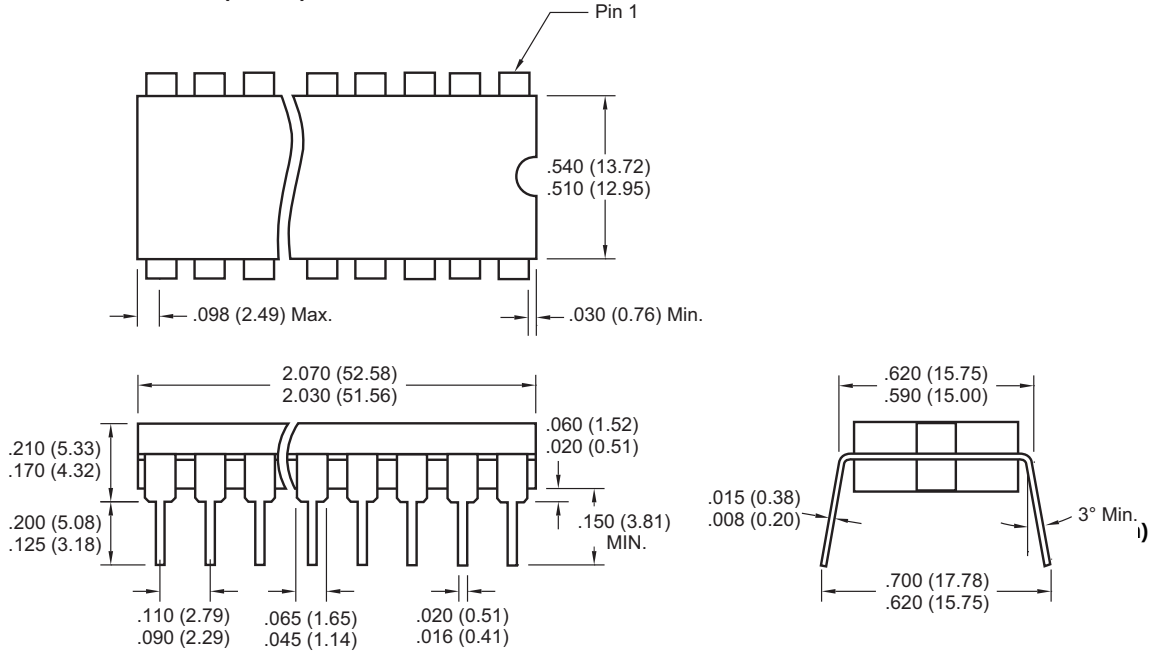
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

40-Pin PDIP (Wide)



Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

40-Pin CERDIP (Wide)

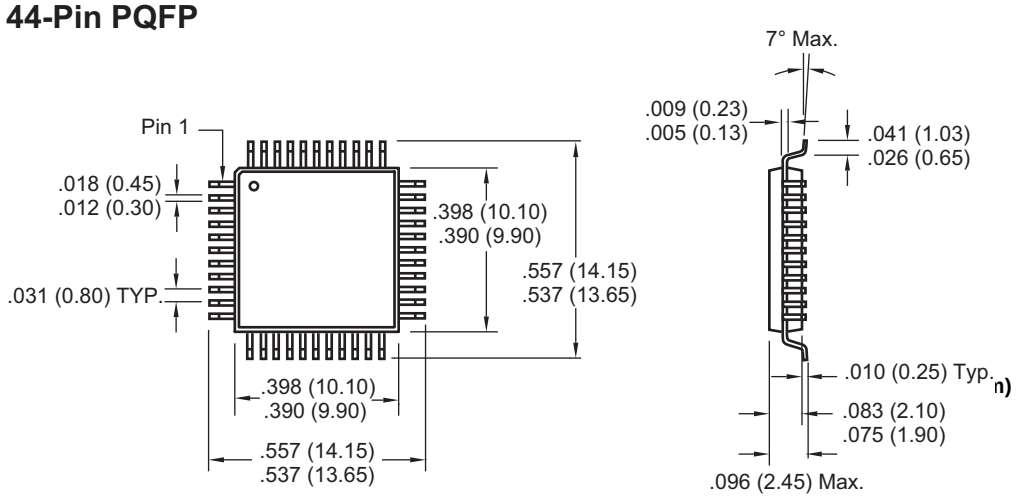


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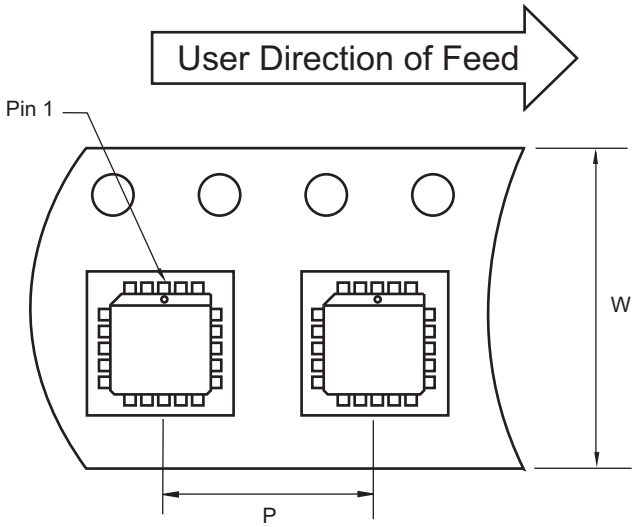
6.3 Package Dimensions (Continued)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

44-Pin PQFP



Component Taping Orientation for 44-Pin PLCC Devices



Standard Reel Component Orientation
for 713 Suffix Device

Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
44-Pin PLCC	32 mm	24 mm	500	13 in

Note: Drawing does not represent total number of pins.

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7.0 REVISION HISTORY

Revision D (December 2012)

Added a note to each package outline drawing.

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