TC7116/A/TC7117/A

3-1/2 Digit Analog-to-Digital Converters with Hold

Features:

- Low Temperature Drift Internal Reference:
  - TC7116/TC7117 80 ppm/°C, Typ.
  - TC7116A/TC7117A 20 ppm/°C, Typ.
- Display Hold Function
- Directly Drives LCD or LED Display
- Zero Reading with Zero Input
- Low Noise for Stable Display:
  - 2V or 200mV Full Scale Range (FSR)
- Auto-Zero Cycle Eliminates Need for Zero
- Adjustment Potentiometer
- True Polarity Indication for Precision Null Applications
- Convenient 9V Battery Operation: (TC7116/TC7116A)
- High-Impedance CMOS Differential Inputs: $10^{12}\Omega$
- Low-Power Operation: 10mW

Applications:

- Thermometry
- Bridge Readouts: Strain Gauges, Load Cells, Null Detectors
- Digital Meters: Voltage/Current/Ohms/Power, pH
- Digital Scales, Process Monitors
- Portable Instrumentation

Device Selection Table

Package Code	Package	Temperature Range
CPL	40-Pin PDIP	0°C to +70°C
IJL	40-Pin CERDIP	-25°C to +85°C
CKW	44-Pin PQFP	0°C to +70°C
CLW	44-Pin PLCC	0°C to +70°C

General Description:

The TC7116A/TC7117A are 3-1/2 digit CMOS Analog-to-Digital Converters (ADCs) containing all the active components necessary to construct a 0.05% resolution measurement system. Seven-segment decoders, polarity and digit drivers, voltage reference, and clock circuit are integrated on-chip. The TC7116A drives Liquid Crystal Displays (LCDs) and includes a back-plane driver. The TC7117A drives common anode Light Emitting Diode (LED) displays directly with an 8mA drive current per segment.

These devices incorporate a display hold (HLDR) function. The displayed reading remains indefinitely, as long as HLDR is held high. Conversions continue, but output data display latches are not updated. The reference low input (V_{REF}-) is not available, as it is with the TC7106/7107. V_{REF}- is tied internally to analog common in the TC7116A/7117A devices.

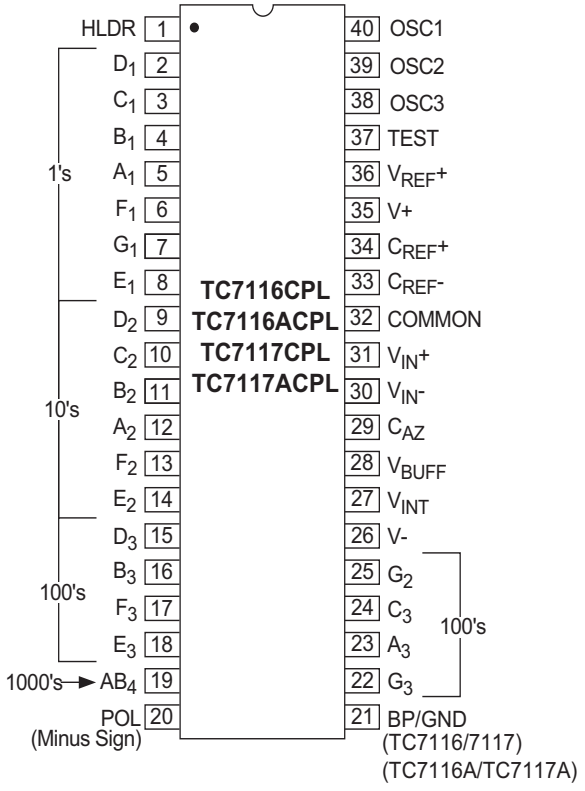
The TC7116A/7117A reduces linearity error to less than 1 count. Rollover error (the difference in readings for equal magnitude but opposite polarity input signals) is below ±1 count. High-impedance differential inputs offer 1pA leakage current and a $10^{12}\Omega$ input impedance. The $15\mu V_{P-P}$ noise performance enables a “rock solid” reading. The auto-zero cycle ensures a zero display reading with a 0V input.

The TC7116A and TC7117A feature a precision, low drift internal reference, and are functionally identical to the TC7116/TC7117. A low drift external reference is not normally required with the TC7116A/TC7117A.

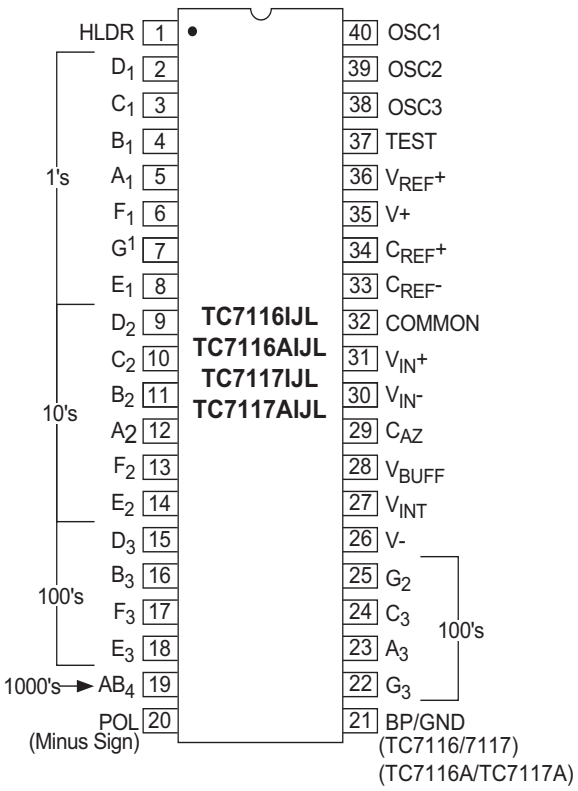
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Package Type

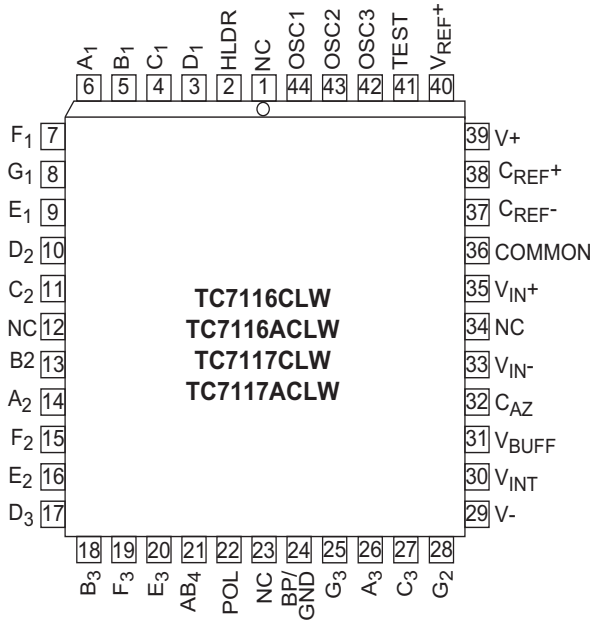
40-Pin PDIP



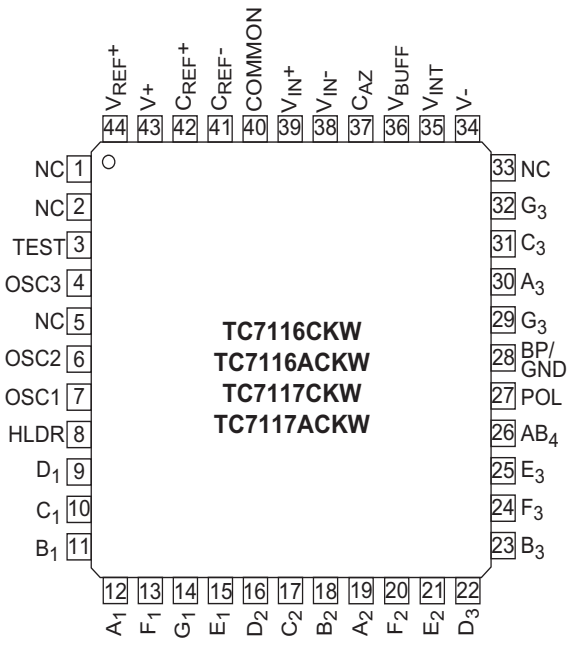
40-Pin CERDIP



44-Pin PLCC



44-Pin PQFP

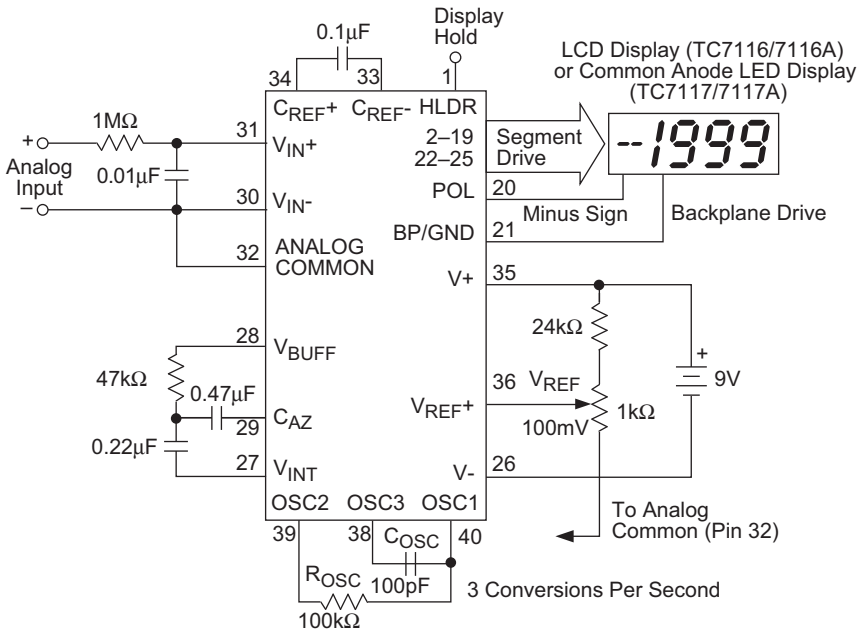


Note 1: NC = No internal connection.

2: Pins 9, 25, 40 and 56 are connected to the die substrate. The potential at these pins is approximately V+. No external connections should be made.

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Typical Application



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage:

TC7116/TC7116A (V+ to V-) 15V
TC7117/TC7117A (V+ to GND).....+6V
V- to GND.....-9V

Analog Input Voltage (Either Input) **(Note 1)**... V+ to V-

Reference Input Voltage (Either Input)..... V+ to V-

Clock Input:

TC7116/TC7116A..... TEST to V+
TC7117/TC7117A.....GND to V+

Package Power Dissipation; $T_A \leq 70°C$ **(Note 2)**

40-Pin CDIP.....2.29W
40-Pin PDIP 1.23W
44-Pin PLCC 1.23W
44-Pin PQFP.....1.00W

Operating Temperature:

C (Commercial) Device..... 0°C to +70°C
I (Commercial) Device..... 0°C to +70°C

Storage Temperature.....-65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TABLE 1-1: TC7116/A AND TC7117/A ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise noted, specifications apply to both the TC7116/A and TC7117/A at T_A = 25°C, f_{CLOCK} = 48kHz. Parts are tested in the circuit of the Typical Operating Circuit.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Z_{IR}	Zero Input Reading	—	±0	—	Digital Reading	V_{IN} = 0V Full Scale = 200mV
	Ratiometric Reading	999	999/1000	1000	Digital Reading	$V_{IN} = V_{REF}$ V_{REF} = 100mV
R/O	Rollover Error (Difference in Reading for Equal Positive and Negative Readings Near Full Scale)	-1	±0.2	+1	Counts	V_{IN}- = + V_{IN}+ ≅ 200mV or ≈ 2V
	Linearity (Maximum Deviation from Best Straight Line Fit)	-1	±0.2	+1	Counts	Full Scale = 200mV or 2V
CMRR	Common Mode Rejection Ratio **(Note 3)**	—	50	—	µV/V	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200mV
e_N	Noise (Peak to Peak 95% of Time)	—	15	—	µV	V_{IN} = 0V Full Scale = 200mV
I_L	Leakage Current at Input	—	1	10	pA	V_{IN} = 0V
	Zero Reading Drift	—	0.2	1	µV/°C	V_{IN} = 0V "C" Device = 0°C to +70°C
		—	1.0	2	µV/°C	"I" Device = -25°C to +85°C

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100µA.

2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

3: Refer to "Differential Input" discussion.

4: Backplane drive is in phase with segment drive for "OFF" segment, 180° out of phase for "ON" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

5: The TC7116/TC7116A logic inputs have an internal pull-down resistor connected from HLDR, Pin 1 to TEST, Pin 37. The TC7117/TC7117A logic inputs have an internal pull-down resistor connected from HLDR, Pin 1 to GND, Pin 21.

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TABLE 1-1: TC7116/A AND TC7117/A ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise noted, specifications apply to both the TC7116/A and TC7117/A at T_A = 25°C, f_{CLOCK} = 48kHz. Parts are tested in the circuit of the Typical Operating Circuit.						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
TC_{SF}	Scale Factor Temperature Coefficient	—	1	5	ppm/°C	V_{IN} = 199mV, "C" Device = 0°C to +70°C (Ext. Ref = 0ppm°C)
		—	—	20	ppm/°C	"I" Device = -25°C to +85°C
	Input Resistance, Pin 1	30	70	—	kΩ	**(Note 5)**
	V_{IL}, Pin 1	—	—	Test + 1.5	V	TC7116/A Only
	V_{IL}, Pin 1	—	—	GND + 1.5	V	TC7117/A Only
	V_{IH}, Pin 1	V^+ - 1.5	—	—	V	Both
I_{DD}	Supply Current (Does not Include LED Current for TC7117/A)	—	0.8	1.8	mA	V_{IN} = 0V
V_C	Analog Common Voltage (with Respect to Positive Supply)	2.4	3.05	3.35	V	25kΩ Between Common and Positive Supply
V_{CTC}	Temperature Coefficient of Analog Common (with Respect to Positive Supply)	—	— 20 80	— 50 —	— ppm/°C ppm/°C	"C" Device: 0°C to +70°C TC7116A/TC7117A TC7116/TC7117
V_{SD}	TC7116/TC7117A ONLY Peak to Peak Segment Drive Voltage	4	5	6	V	V+ to V- = 9V **(Note 4)**
V_{BD}	TC7116A/TC7116A ONLY Peak to Peak Backplane Drive Voltage	4	5	6	V	V+ to V- = 9V **(Note 4)**
	TC7117/TC7117A ONLY Segment Sinking Current (Except Pin 19)	5	8	—	mA	V+ = 5.0V Segment Voltage = 3V
	TC7117/TC7117A ONLY Segment Sinking Current (Pin 19 Only)	10	16	—	mA	V+ = 5.0V Segment Voltage = 3V

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.

2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

3: Refer to "Differential Input" discussion.

4: Backplane drive is in phase with segment drive for "OFF" segment, 180° out of phase for "ON" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

5: The TC7116/TC7116A logic inputs have an internal pull-down resistor connected from HLDR, Pin 1 to TEST, Pin 37. The TC7117/TC7117A logic inputs have an internal pull-down resistor connected from HLDR, Pin 1 to GND, Pin 21.

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2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number (40-Pin PDIP) (40-Pin CERDIP)	Pin Number (44-Pin PQFP)	Symbol	Description
1	8	HLDR	Hold pin, Logic 1 holds present display reading.
2	9	D_1	Activates the D section of the units display.
3	10	C_1	Activates the C section of the units display.
4	11	B_1	Activates the B section of the units display.
5	12	A_1	Activates the A section of the units display.
6	13	F_1	Activates the F section of the units display.
7	14	G_1	Activates the G section of the units display.
8	15	E_1	Activates the E section of the units display.
9	16	D_2	Activates the D section of the tens display.
10	17	C_2	Activates the C section of the tens display.
11	18	B_2	Activates the B section of the tens display.
12	19	A_2	Activates the A section of the tens display.
13	20	F_2	Activates the F section of the tens display.
14	21	E_2	Activates the E section of the tens display.
15	22	D_3	Activates the D section of the hundreds display.
16	23	B_3	Activates the B section of the hundreds display.
17	24	F_3	Activates the F section of the hundreds display.
18	25	E_3	Activates the E section of the hundreds display.
19	26	AB_4	Activates both halves of the 1 in the thousands display.
20	27	POL	Activates the negative polarity display.
21	28	BP/ GND	LCD backplane drive output (TC7116/TC7116A). Digital ground (TC7117/TC7117A).
22	29	G_3	Activates the G section of the hundreds display.
23	30	A_3	Activates the A section of the hundreds display.
24	31	C_3	Activates the C section of the hundreds display.
25	32	G_2	Activates the G section of the tens display.
26	34	V-	Negative power supply voltage.
27	35	V_{INT}	Integrator output. Connection point for integration capacitor. See **Section 4.3 "Integrating Capacitor"**, Integrating Capacitor for more details.
28	36	V_{BUFF}	Integration resistor connection. Use a 47kΩ resistor for a 200mV full scale range and a 470kΩ resistor for 2V full scale range.
29	37	C_{AZ}	The size of the auto-zero capacitor influences system noise. Use a 0.47μF capacitor for 200mV full scale, and a 0.047μF capacitor for 2V full scale. See **Section 4.1 "Auto-Zero Capacitor"**, Auto-Zero Capacitor for more details.
30	38	V_{IN}-	The analog LOW input is connected to this pin.
31	39	V_{IN}+	The analog HIGH input signal is connected to this pin.
32	40	COMMON	This pin is primarily used to set the Analog Common mode voltage for battery operation, or in systems where the input signal is referenced to the power supply. It also acts as a reference voltage source. See **Section 3.1.6 "Analog Common"**, Analog Common for more details.
33	41	C_{REF}-	See Pin 34.

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TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number (40-Pin PDIP) (40-Pin CERDIP)	Pin Number (44-Pin PQFP)	Symbol	Description
34	42	$C_{REF}+$	A 0.1μF capacitor is used in most applications. If a large Common mode voltage exists (for example, the $V_{IN}-$ pin is not at analog common), and a 200mV scale is used, a 1μF capacitor is recommended and will hold the rollover error to 0.5 count.
35	43	V+	Positive Power Supply Voltage.
36	44	$V_{REF}+$	The analog input required to generate a full scale output (1999 counts). Place 100mV between Pins 32 and 36 for 199.9mV full scale. Place 1V between Pins 35 and 36 for 2V full scale. See **Section 4.6 "Reference Voltage"**, Reference Voltage.
37	3	TEST	Lamp test. When pulled HIGH (to V+), all segments will be turned on and the display should read -1888. It may also be used as a negative supply for externally generated decimal points. See **Section 3.1.7 "Test"**, TEST for additional information.
38	4	OSC3	See Pin 40.
39	6	OSC2	See Pin 40.
40	7	OSC1	Pins 40, 39, 38 make up the oscillator section. For a 48kHz clock (3 readings per section), connect Pin 40 to the junction of a 100kΩ resistor and a 100pF capacitor. The 100kΩ resistor is tied to Pin 39 and the 100pF capacitor is tied to Pin 38.

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3.0 DETAILED DESCRIPTION

(All Pin Designations Refer to 40-Pin PDIP.)

3.1 Analog Section

Figure 3-1 shows the block diagram of the analog section for the TC7116/TC7116A and TC7117/TC7117A. Each measurement cycle is divided into three phases: (1) Auto-Zero (AZ), (2) Signal Integrate (INT), and (3) Reference Integrate (REF), or De-integrate (DE).

3.1.1 AUTO-ZERO PHASE

High and low inputs are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor (C_{AZ}) to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, AZ accuracy is limited only by system noise. The offset referred to the input is less than 10μV.

3.1.2 SIGNAL INTEGRATE PHASE

The auto-zero loop is opened, the internal short is removed, and the internal high and low inputs are connected to the external pins. The converter then integrates the differential voltages between $V_{IN}+$ and $V_{IN}-$ for a fixed time. This differential voltage can be within a wide Common mode range: 1V of either supply. However, if the input signal has no return with respect to the converter power supply, $V_{IN}-$ can be tied to analog common to establish the correct Common mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

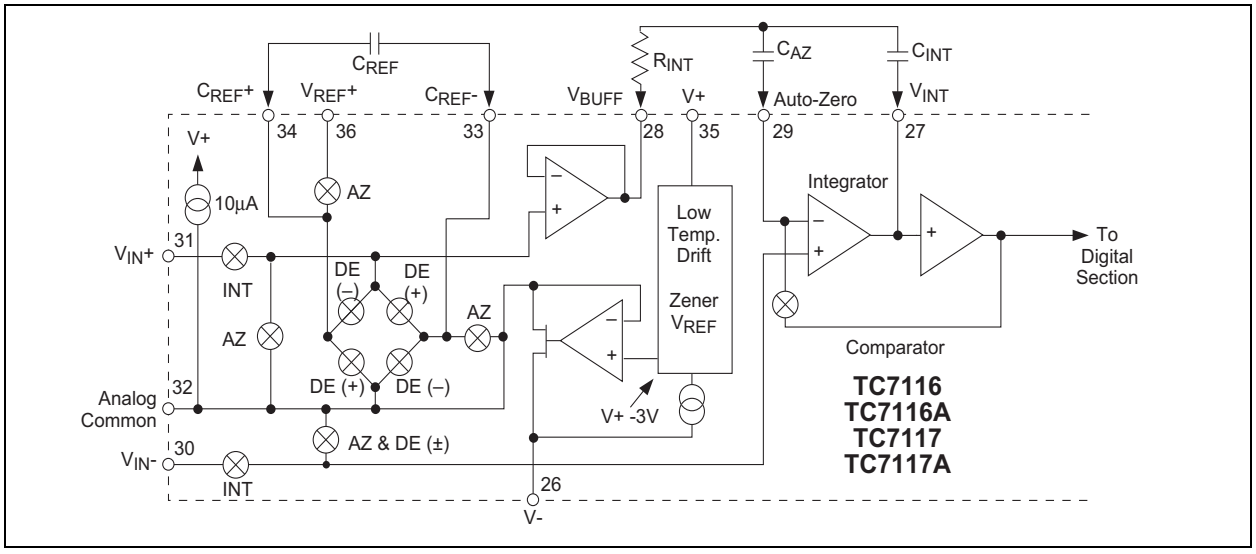


FIGURE 3-1: *Analog Section of TC7116/TC7116A and TC7117/TC7117A*

3.1.3 REFERENCE INTEGRATE PHASE

The final phase is reference integrate, or de-integrate. Input low is internally connected to analog common and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. The digital reading displayed is:

EQUATION 3-1:

$$1000 = \frac{V_{IN}}{V_{REF}}$$

3.1.4 REFERENCE

The positive reference voltage ($V_{REF}+$) is referred to analog common.

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3.1.5 DIFFERENTIAL INPUT

This input can accept differential voltages anywhere within the Common mode range of the input amplifier or, specifically, from 1V below the positive supply to 1V above the negative supply. In this range, the system has a CMRR of 86dB, typical. However, since the integrator also swings with the Common mode voltage, care must be exercised to ensure that the integrator output does not saturate. A worst-case condition would be a large, positive Common mode voltage with a near full scale negative differential input voltage. The negative input signal drives the integrator positive, when most of its swing has been used up by the positive Common mode voltage. For these critical applications, the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

3.1.6 ANALOG COMMON

This pin is included primarily to set the Common mode voltage for battery operation (TC7116/TC7116A), or for any system where the input signals are floating, with respect to the power supply. The analog common pin sets a voltage approximately 2.8V more negative than the positive supply. This is selected to give a minimum end of life battery voltage of about 6V. However, analog common has some attributes of a reference voltage. When the total supply voltage is large enough to cause the Zener to regulate (>7V), the analog common voltage will have a low voltage coefficient (0.001%), low output impedance (≅15Ω), and a temperature coefficient of less than 20ppm/°C, typically, and 50 ppm maximum. The TC7116/TC7117 temperature coefficients are typically 80ppm/°C.

An external reference may be used, if necessary, as shown in Figure 3-2.

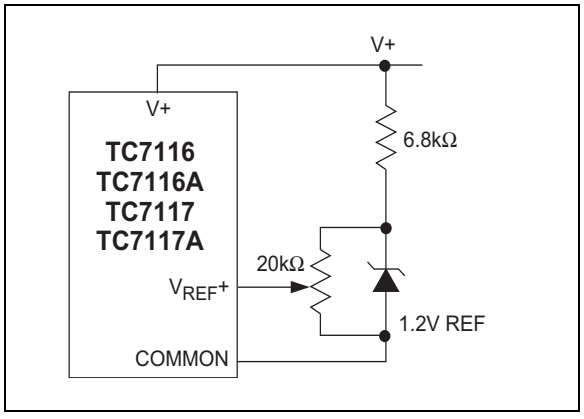


FIGURE 3-2: *Using an External Reference*

Analog common is also used as V_{IN}- return during auto-zero and de-integrate. If V_{IN}- is different from analog common, a Common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications, V_{IN}- will be set at a fixed, known voltage (power supply common for instance). In this application, analog common should be tied to the same point, thus removing the Common mode voltage from the converter. The same holds true for the reference voltage; if it can be conveniently referenced to analog common, it should be. This removes the Common mode voltage from the reference system.

Within the IC, analog common is tied to an N-channel FET, that can sink 30mA or more of current to hold the voltage 3V below the positive supply (when a load is trying to pull the analog common line positive). However, there is only 10μA of source current, so analog common may easily be tied to a more negative voltage, thus overriding the internal reference.

3.1.7 TEST

The TEST pin serves two functions. On the TC7117/TC7117A, it is coupled to the internally generated digital supply through a 500Ω resistor. Thus, it can be used as a negative supply for externally generated segment drivers, such as decimal points, or any other presentation the user may want to include on the LCD. (Figure 3-3 and Figure 3-4 show such an application.) No more than a 1mA load should be applied.

The second function is a “lamp test.” When TEST is pulled HIGH (to V+), all segments will be turned ON and the display should read -1888. The TEST pin will sink about 10mA under these conditions.

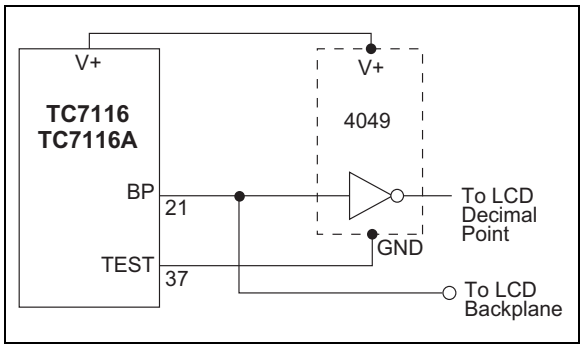


FIGURE 3-3: *Simple Inverter for Fixed Decimal Point*

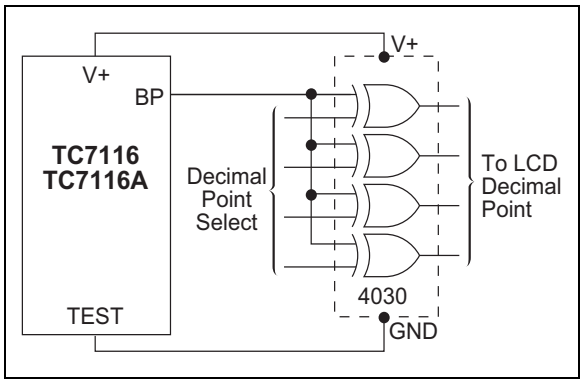


FIGURE 3-4: *Exclusive "OR" Gate for Decimal Point Drive*

3.2 Digital Section

Figure 3-5 and Figure show the digital section for TC7116/TC7116A and TC7117/TC7117A, respectively. For the TC7116/TC7116A (Figure 3-5), an internal digital ground is generated from a 6V Zener diode and a large P-channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the backplane (BP) voltage is switched. The BP frequency is the clock frequency 4800. For 3 readings per second, this is a 60Hz square wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude, and are in phase with BP when OFF, but out of phase when ON. In all cases, negligible DC voltage exists across the segments.

Figure is the digital section of the TC7117/TC7117A. It is identical to the TC7116/TC7116A, except that the regulated supply and BP drive have been eliminated, and the segment drive is typically 8mA. The 1000's output (Pin 19) sinks current from two LED segments, and has a 16mA drive capability. The TC7117/TC7117A are designed to drive common anode LED displays.

In both devices, the polarity indication is ON for analog inputs. If V_{IN}- and V_{IN}+ are reversed, this indication can be reversed also, if desired.

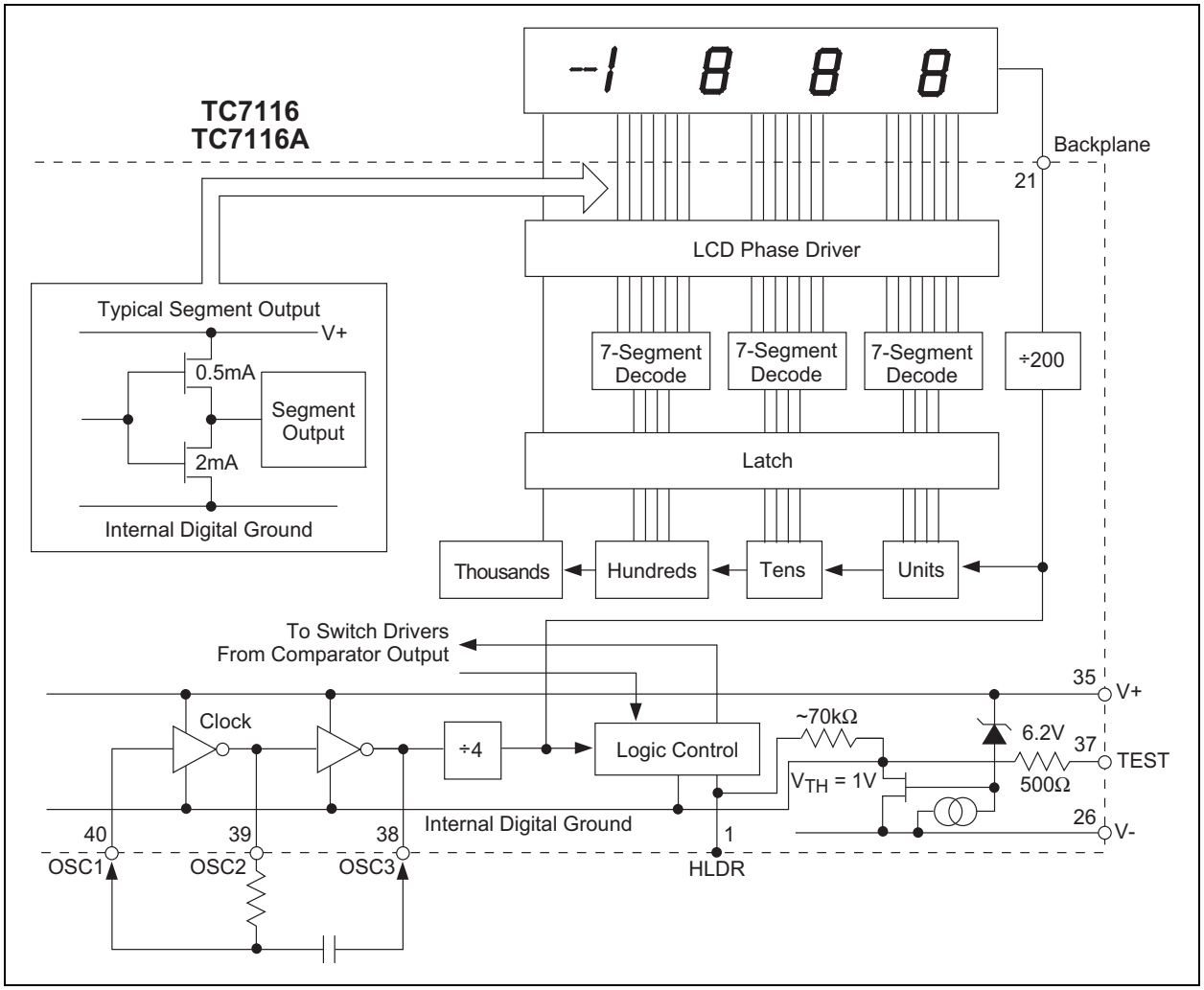


FIGURE 3-5: *TC7116/TC7116A Digital Section*

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3.2.1 SYSTEM TIMING

The clocking method used for the TC7116/TC7116A and TC7117/TC7117A is shown in Figure . Three clocking methods may be used:

1. An external oscillator connected to Pin 40.
2. A crystal between Pins 39 and 40.
3. An RC network using all three pins.

The oscillator frequency is ÷4 before it clocks the decade counters. It is then further divided to form the three convert cycle phases: Signal Integrate (1000 counts), Reference De-integrate (0 to 2000 counts), and Auto-Zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference de-integrate. This makes a complete measure cycle of 4000 (16,000 clock pulses), independent of input voltage. For 3 readings per second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 200kHz, 100kHz, 66-2/3kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings per second) will reject both 50Hz and 60Hz.

3.2.2 HOLD READING INPUT

When HLDR is at a logic HIGH, the latch will not be updated. Analog-to-Digital conversions will continue, but will not be updated until HLDR is returned to LOW. To continuously update the display, connect to TEST (TC7116/TC7116A) or GROUND (TC7117/TC7117A), or disconnect. This input is CMOS compatible with 70kΩ typical resistance to TEST (TC7116/TC7116A) or GROUND (TC7117/TC7117A).

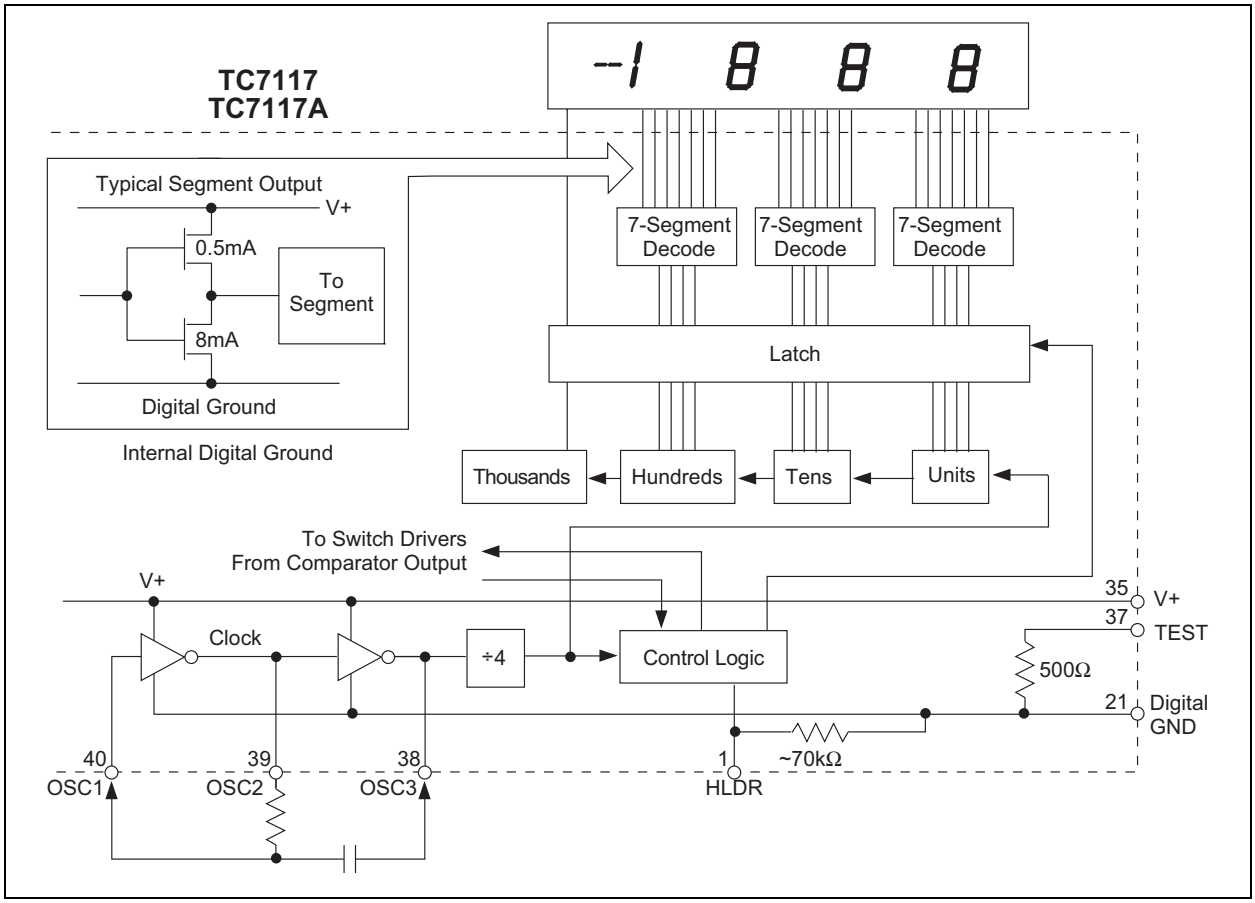


FIGURE 3-6: *TC7117/TC7117A Digital Section*

4.0 COMPONENT VALUE SELECTION

4.1 Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on system noise. For 200mV full scale, where noise is very important, a 0.47μF capacitor is recommended. On the 2V scale, a 0.047μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

4.2 Reference Capacitor

A 0.1μF capacitor is acceptable in most applications. However, where a large Common mode voltage exists (i.e., the V_{IN}- pin is not at analog common), and a 200mV scale is used, a larger value is required to prevent rollover error. Generally, 1μF will hold the rollover error to 0.5 count in this instance.

4.3 Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance buildup will not saturate the integrator swing (approximately 0.3V from either supply). In the TC7116/TC7116A or the TC7117/TC7117A, when the analog common is used as a reference, a nominal ±2V full scale integrator swing is acceptable. For the TC7117/TC7117A, with ±5V supplies and analog common tied to supply ground, a ±3.5V to ±4V swing is nominal. For 3 readings per second (48kHz clock), nominal values for C_{INT} are 0.22μ1F and 0.10μF, respectively. If different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the output swing. The integrating capacitor must have low dielectric absorption to prevent rollover errors. Polypropylene capacitors are recommended for this application.

4.4 Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They can supply 20μA of drive current with negligible nonlinearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full scale, 470kΩ is near optimum and, similarly, 47kΩ for 200mV full scale.

4.5 Oscillator Components

For all frequency ranges, a 100kΩ resistor is recommended; the capacitor is selected from the equation:

EQUATION 4-1:

$$f = \frac{0.45}{RC}$$

For a 48kHz clock (3 readings per second), C = 100pF.

4.6 Reference Voltage

To generate full scale output (2000 counts), the analog input requirement is $V_{IN} = 2V_{REF}$. Thus, for the 200mV and 2V scale, V_{REF} should equal 100mV and 1V, respectively. In many applications, where the ADC is connected to a transducer, a scale factor exists between the input voltage and the digital reading. For instance, in a measuring system, the designer might like to have a full scale reading when the voltage from the transducer is 700mV. Instead of dividing the input down to 200mV, the designer should use the input voltage directly and select V_{REF} = 350mV. Suitable values for integrating resistor and capacitor would be 120kW and 0.22μF. This makes the system slightly quieter and also avoids a divider network on the input. The TC7117/TC7117A, with ±5V supplies, can accept input signals up to ±4V. Another advantage of this system is when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between V_{IN}+ and analog common, and the variable (or fixed) offset voltage between analog common and V_{IN}-.

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5.0 TC7117/TC7117A POWER SUPPLIES

The TC7117/TC7117A are designed to operate from ±5V supplies. However, if a negative supply is not available, it can be generated with a TC7660 DC-to-DC converter and two capacitors. Figure 5-1 shows this application.

In selected applications, a negative supply is not required. The conditions for using a single +5V supply are:

1. The input signal can be referenced to the center of the Common mode range of the converter.
2. The signal is less than ±1.5V.
3. An external reference is used.

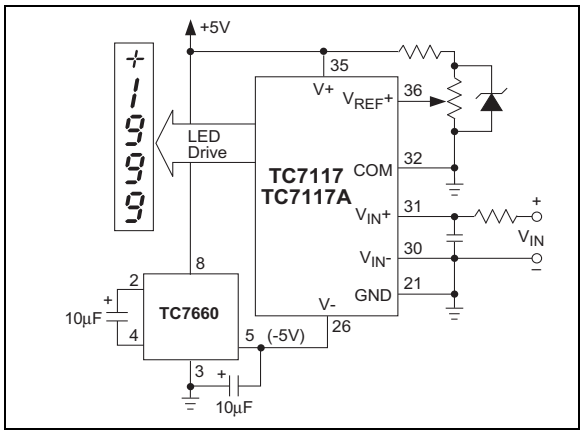


FIGURE 5-1: *Negative Power Supply Generation with TC7660*

6.0 TYPICAL APPLICATIONS

The TC7117/TC7117A sink the LED display current, causing heat to build up in the IC package. If the internal voltage reference is used, the changing chip temperature can cause the display to change reading. By reducing the LED common anode voltage, the TC7117/TC7117A package power dissipation is reduced.

Figure 6-1 is a curve tracer display showing the relationship between output current and output voltage for typical TC7117CPL/TC7117ACPL devices. Since a typical LED has 1.8V across it at 8mA and its common anode is connected to +5V, the TC7117/TC7117A output is at 3.2V (Point A, Figure 6-1). Maximum power dissipation is 8.1mA x 3.2V x 24 segments = 622mW.

However, notice that once the TC7117/TC7117A's output voltage is above 2V, the LED current is essentially constant as output voltage increases. Reducing the output voltage by 0.7V (Point B Figure 6-1) results in 7.7mA of LED current, only a 5% reduction. Maximum power dissipation is now only 7.7mA x 2.5V x 24 = 462mW, a reduction of 26%. An output voltage reduction of 1V (Point C) reduces LED current by 10% (7.3mA), but power dissipation by 38% (7.3mA x 2.2V x 24 = 385mW).

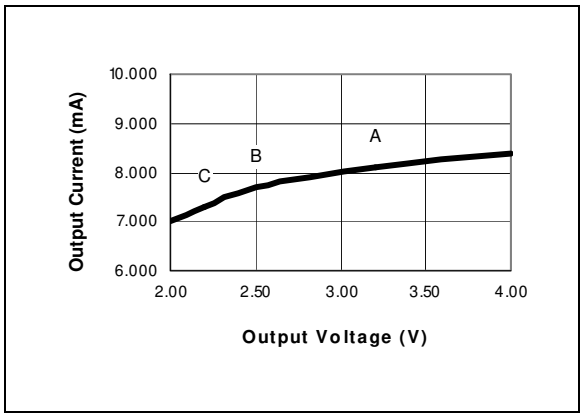


FIGURE 6-1: *TC7117/TC7117A Output vs. Output Voltage*

Reduced power dissipation is very easy to obtain. Figure 6-2 shows two ways: either a 5.1Ω, 1/4W resistor, or a 1A diode placed in series with the display (but not in series with the TC7117/TC7117A). The resistor reduces the TC7117/TC7117A's output voltage (when all 24 segments are ON) to Point C of Figure 6-1. When segments turn off, the output voltage will increase. The diode, however, will result in a relatively steady output voltage, around Point B.

In addition to limiting maximum power dissipation, the resistor reduces change in power dissipation as the display changes. The effect is caused by the fact that, as fewer segments are ON, each ON output drops more voltage and current. For the best-case of six segments (a "111" display) to worst-case (a "1888" display), the resistor circuit will change about 230mW, while a circuit without the resistor will change about 470mW. Therefore, the resistor will reduce the effect of display dissipation on reference voltage drift by about 50%.

The change in LED brightness caused by the resistor is almost unnoticeable as more segments turn off. If display brightness remaining steady is very important to the designer, a diode may be used instead of the resistor.

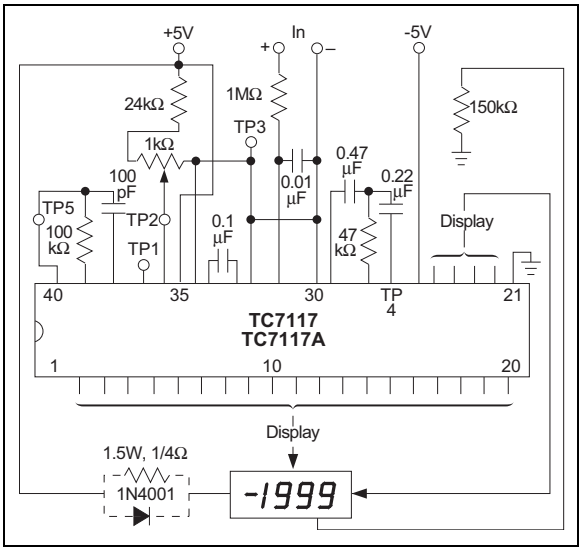


FIGURE 6-2: *Diode or Resistor Limits Package Power Dissipation*

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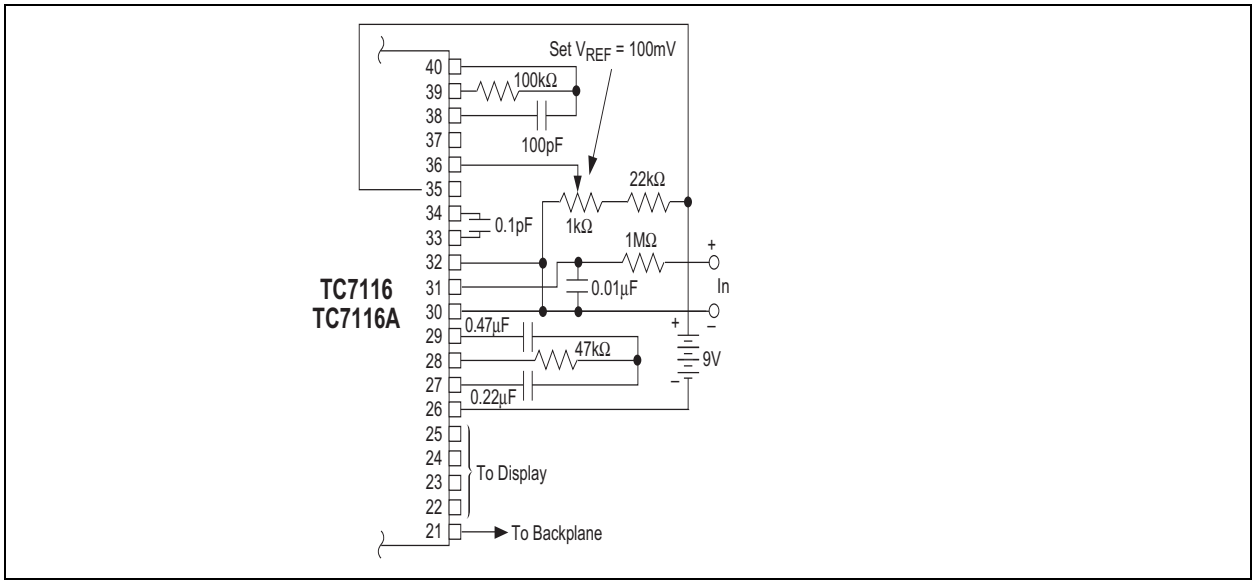


FIGURE 6-3: *TC7116/TC7117A Using the Internal Reference (200 mV Full Scale, 3 Readings Per Second – RPS)*

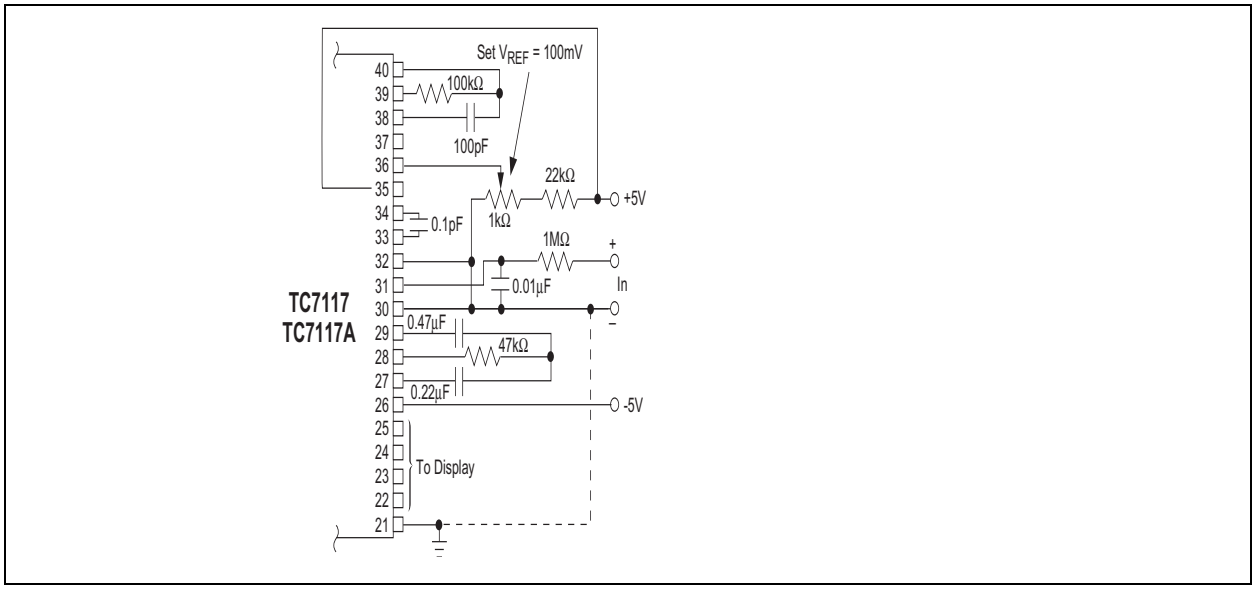


FIGURE 6-4: *TC7117/TC7117A Internal Reference (200 mV Full Scale, 3 RPS, V_{IN}- Tied to GND for Single Ended Inputs*

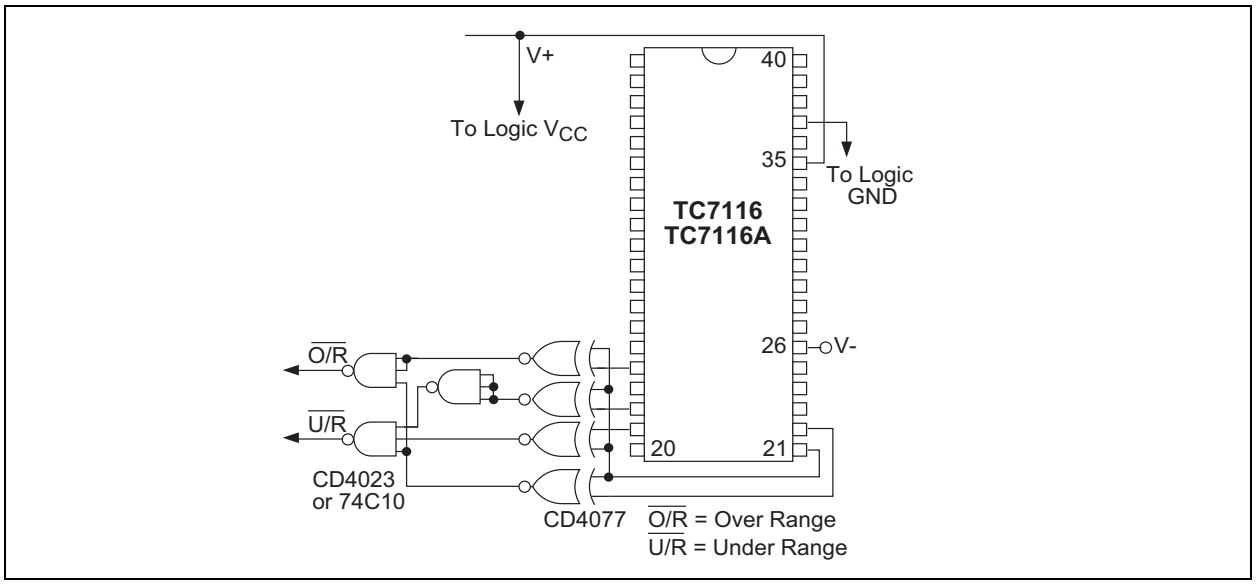


FIGURE 6-5: *Circuit for Developing Under Range and Over Range Signals From TC7116/TC7117A Outputs*

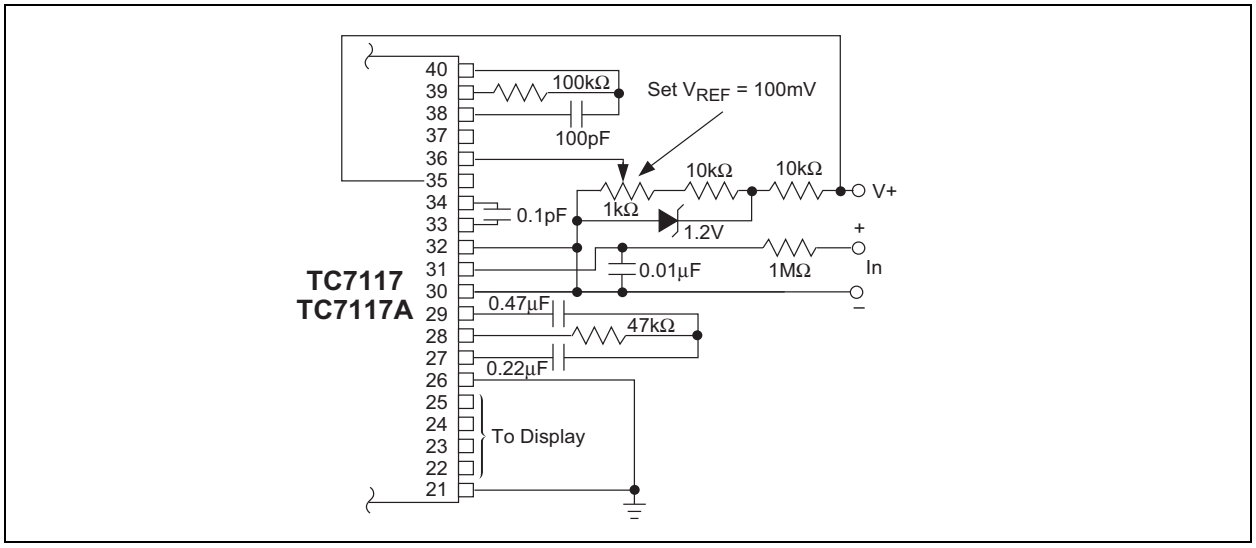


FIGURE 6-6: *TC7117/TC7117A With A 1.2 External Bandgap Reference (V_{IN}- Tied to Common)*

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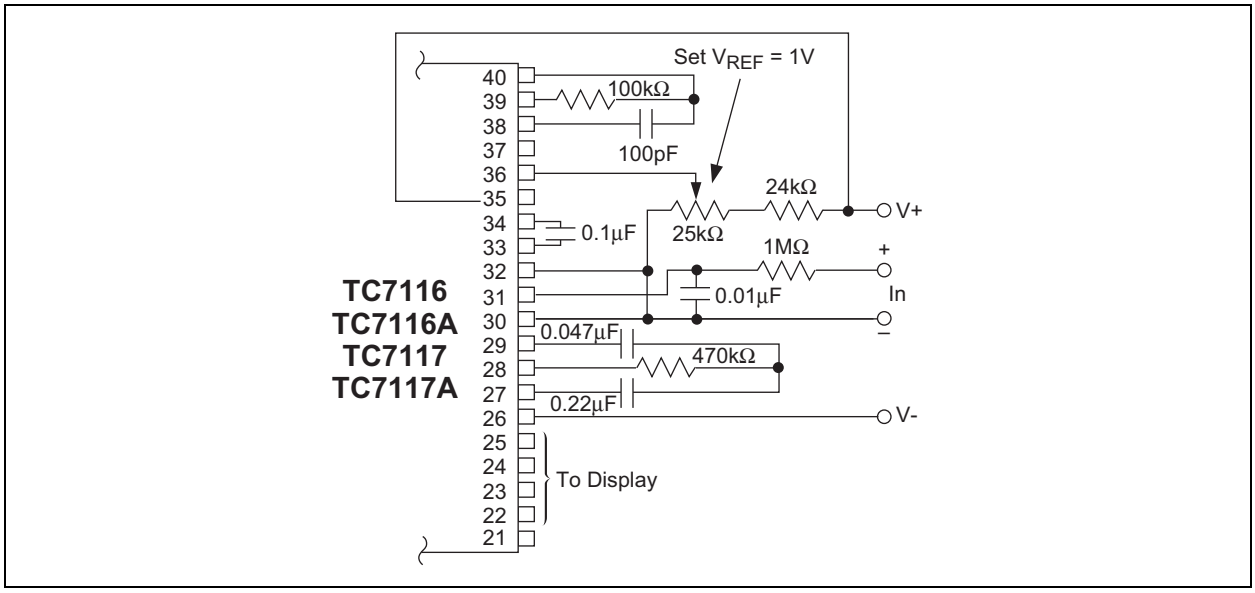


FIGURE 6-7: *Recommended Component Values for 2V Full Scale (TC7116/TC7116A and TC7117/TC7117A)*

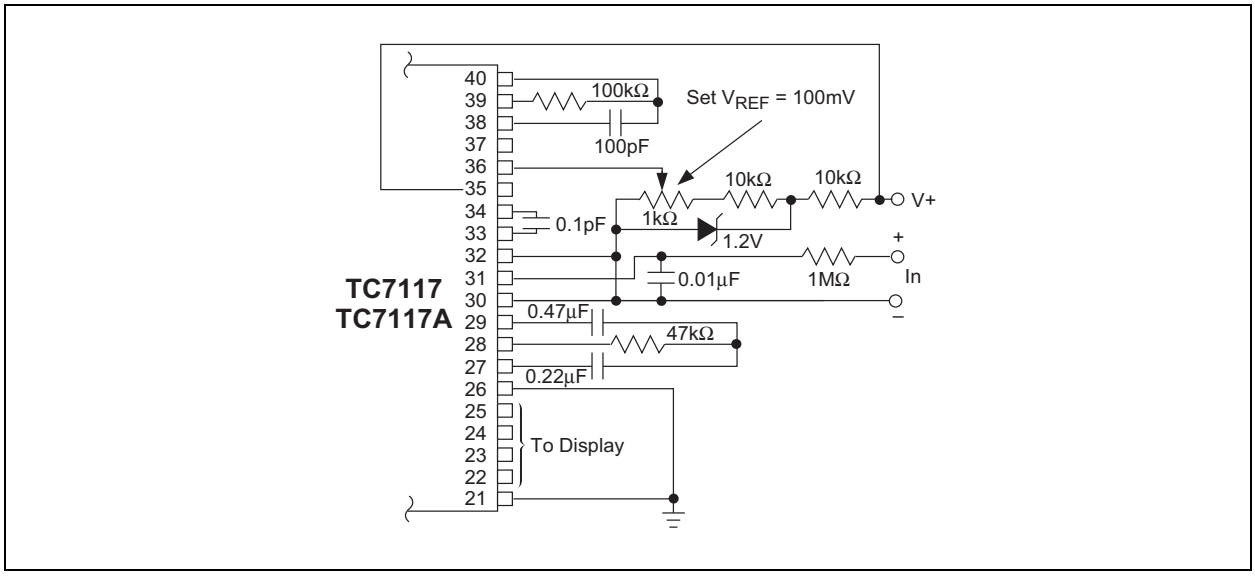


FIGURE 6-8: *TC7117/TC7117A Operated From Single +5V Supply (An External Reference Must be Used in This Application)*

7.0 PACKAGING INFORMATION

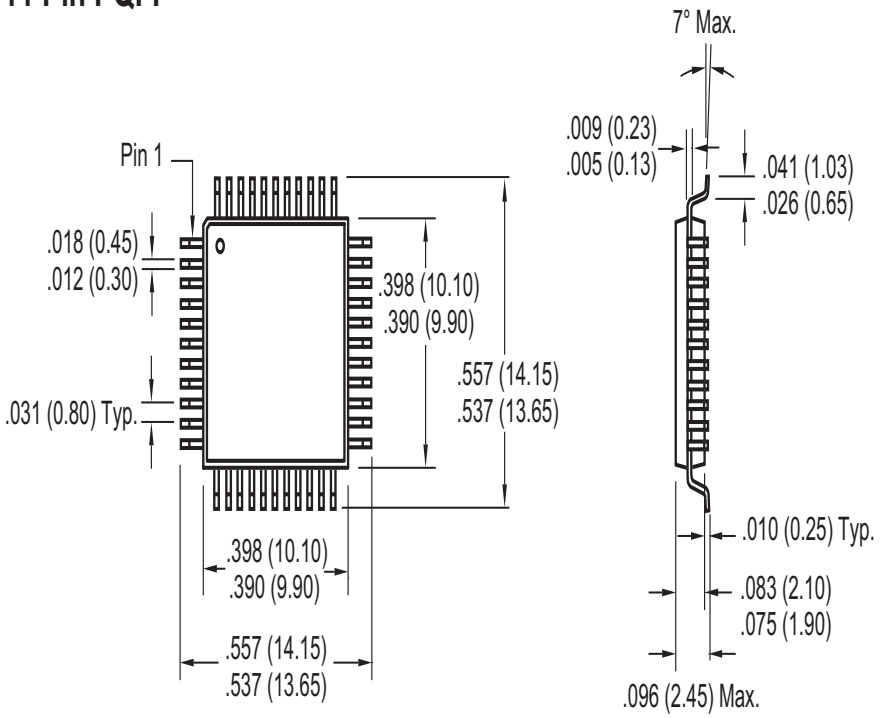
7.1 Package Marking Information

Package marking data not available at this time.

7.2 Taping Form

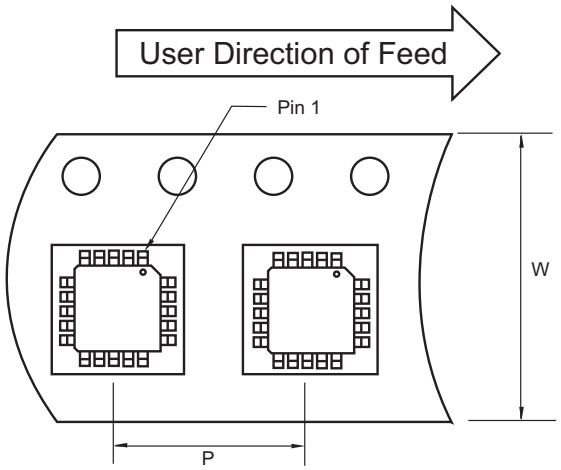
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

44-Pin PQFP



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Component Taping Orientation for 44-Pin PQFP Devices



Standard Reel Component Orientation
for 713 Suffix Device

Carrier Tape, Number of Components Per Reel and Reel Size

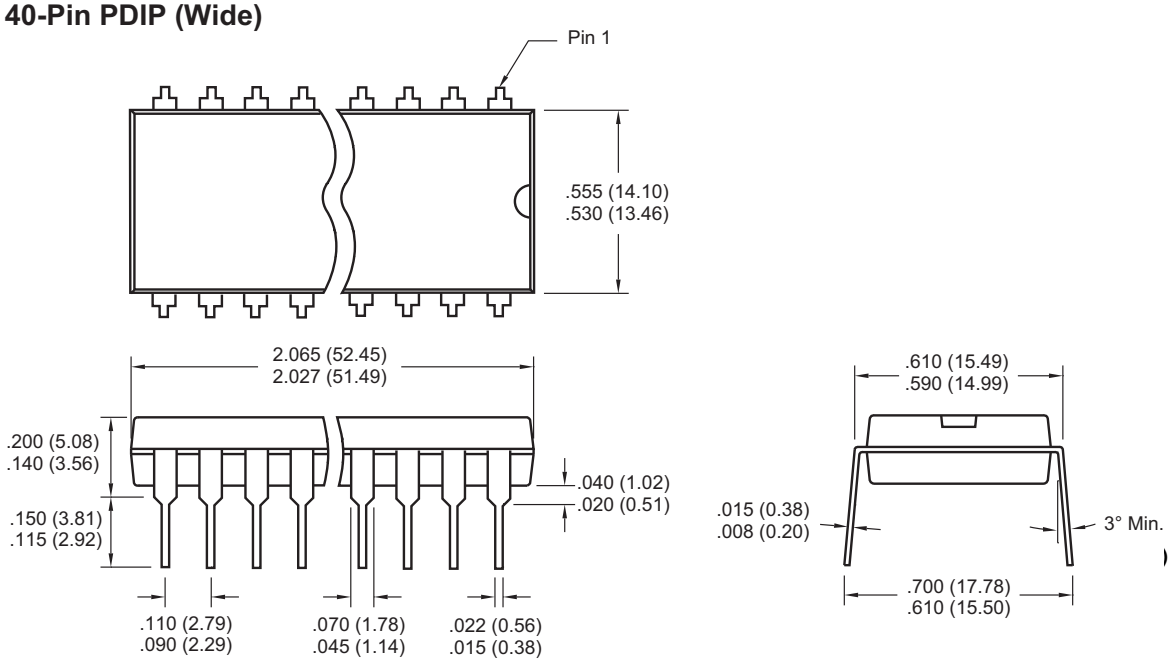
Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
44-Pin PQFP	24 mm	16 mm	500	13 in

Note: Drawing does not represent total number of pins.

7.3 Package Dimensions

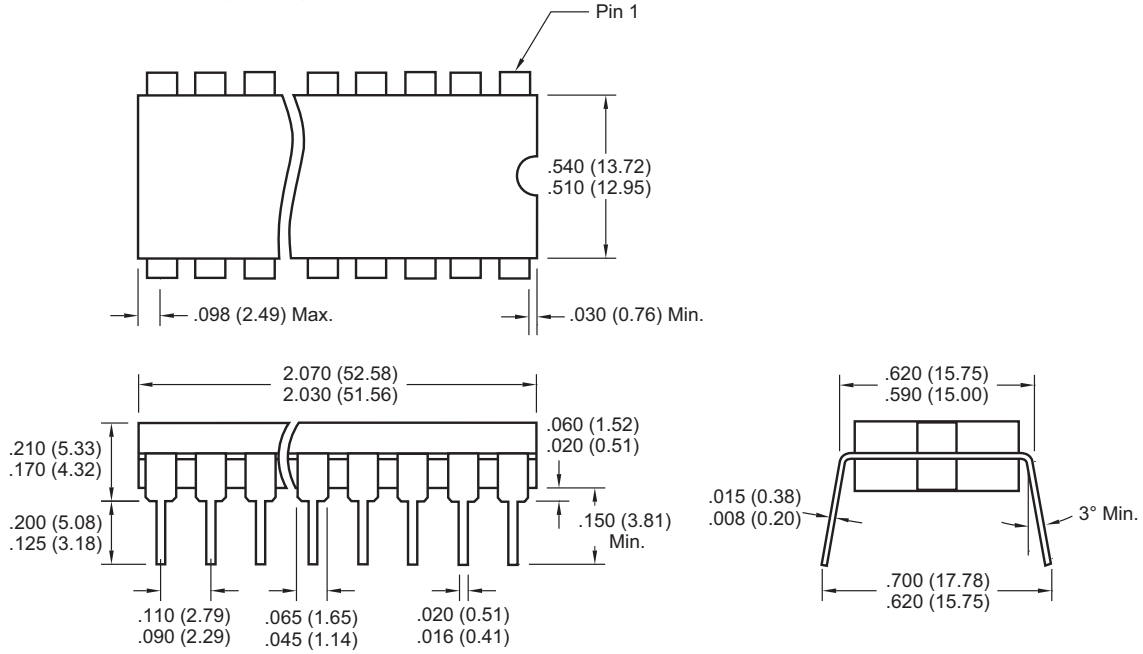
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

40-Pin PDIP (Wide)



Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

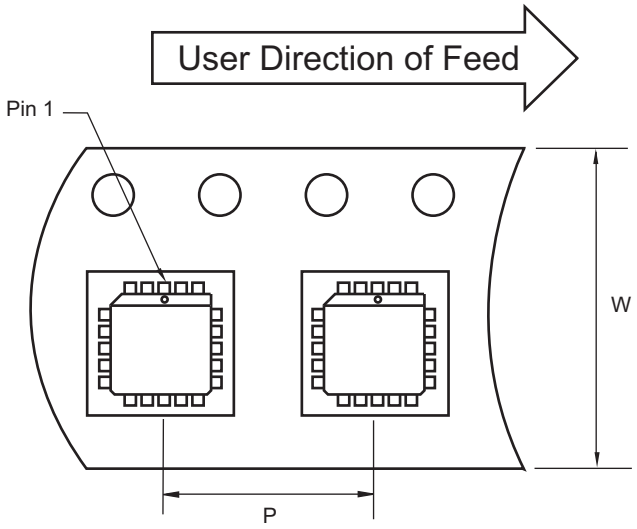
40-Pin CERDIP (Wide)



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7.3 Package Dimensions (Continued)

Component Taping Orientation for 44-Pin PLCC Devices



Standard Reel Component Orientation
for 713 Suffix Device

Carrier Tape, Number of Components Per Reel and Reel Size

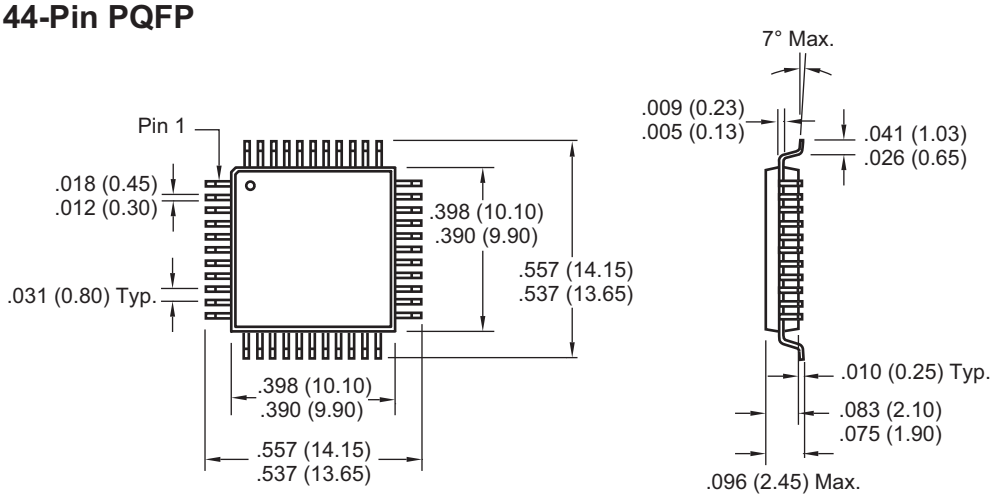
Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
44-Pin PLCC	32 mm	24 mm	500	13 in

Note: Drawing does not represent total number of pins.

Dimensions: inches (mm)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

44-Pin PQFP



Dimensions: inches (mm)

8.0 REVISION HISTORY

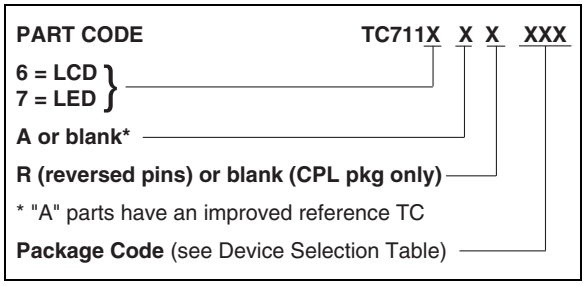
Revision D (December 2012)

Added a note to each package outline drawing.

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PRODUCT IDENTIFICATION SYSTEM

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ISBN: 9781620768365

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