TC9400/9401/9402

Voltage-to-Frequency / Frequency-to-Voltage Converters

Features:

VOLTAGE-TO-FREQUENCY

- Choice of Linearity:
  - TC9401: 0.01%
  - TC9400: 0.05%
  - TC9402: 0.25%
- DC to 100 kHz (F/V) or 1 Hz to 100 kHz (V/F)
- Low Power Dissipation: 27 mW (Typ.)
- Single/Dual Supply Operation:
  - +8V to +15V or ±4V to ±7.5V
- Gain Temperature Stability: ±25 ppm/°C (Typ.)
- Programmable Scale Factor

FREQUENCY-TO-VOLTAGE

- Operation: DC to 100 kHz
- Choice of Linearity:
  - TC9401: 0.02%
  - TC9400: 0.05%
  - TC9402: 0.25%
- Programmable Scale Factor

Applications:

- Microprocessor Data Acquisition
- 13-bit Analog-to-Digital Converters (ADC)
- Analog Data Transmission and Recording
- Phase Locked Loops
- Frequency Meters/Tachometer
- Motor Control
- FM Demodulation

General Description:

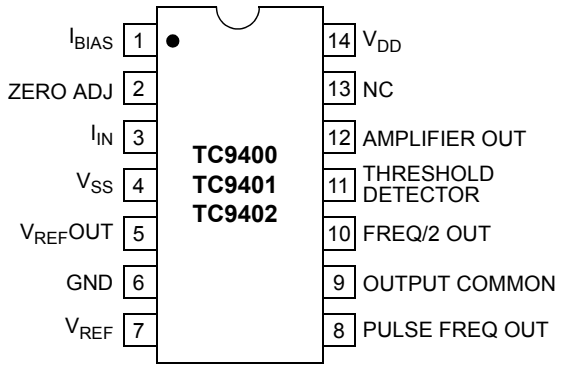
The TC9400/9401/9402 are low-cost Voltage-to-Frequency (V/F) converters, utilizing low-power CMOS technology. The converters accept a variable analog input signal and generate an output pulse train, whose frequency is linearly proportional to the input voltage.

The devices can also be used as highly accurate Frequency-to-Voltage (F/V) converters, accepting virtually any input frequency waveform and providing a linearly proportional voltage output.

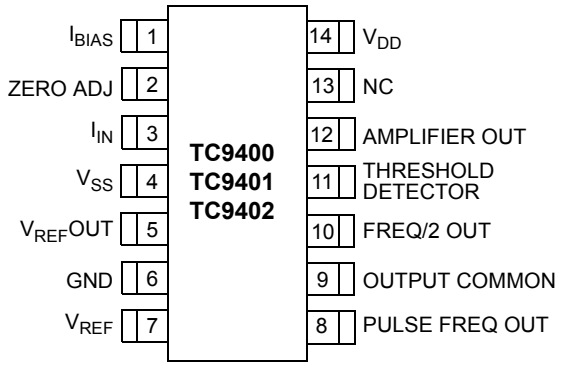
A complete V/F or F/V system only requires the addition of two capacitors, three resistors, and reference voltage.

Package Type

14-Pin Plastic DIP/CERDIP



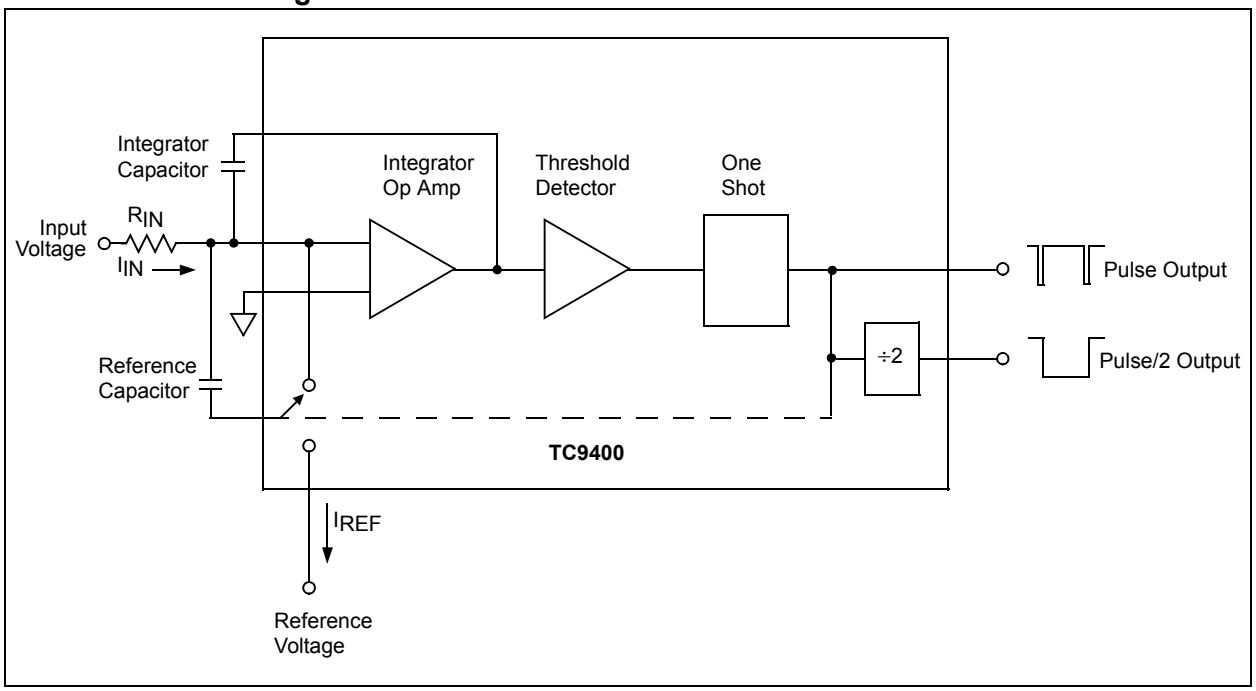
14-Pin SOIC



NC = No Internal Connection

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Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ .....+18V
I_{IN} .....10 mA
$V_{OUTMAX} - V_{OUT}$ Common.....23V
$V_{REF} - V_{SS}$ .....-1.5V
Storage Temperature Range.....-65°C to +150°C
Operating Temperature Range:
C Device .....0°C to +70°C
E Device.....-40°C to +85°C
Package Dissipation ($T_A \leq 70°C$):
8-Pin CerDIP.....800 mW
8-Pin Plastic DIP .....730 mW
8-Pin SOIC.....470 mW

† Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC940X ELECTRICAL SPECIFICATIONS

Electrical Characteristics: unless otherwise specified, V_{DD} = +5V, V_{SS} = -5V, V_{GND} = 0V, V_{REF} = -5V, R_{BIAS} = 100 kΩ, Full Scale = 10 kHz. T_A = +25°C, unless temperature range is specified (-40°C to +85°C for E device, 0°C to +70°C for C device).

Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units	Test Conditions
Voltage-to-Frequency											
Accuracy		**TC9400**			**TC9401**			**TC9402**			
Linearity 10 kHz	—	0.01	0.05	—	0.004	0.01	—	0.05	0.25	% Full Scale	Output Deviation from Straight Line Between Normalized Zero and Full Scale Input
Linearity 100 kHz	—	0.1	0.25	—	0.04	0.08	—	0.25	0.5	% Full Scale	Output Deviation from Straight Line Between Normalized Zero Reading and Full Scale Input
Gain Temperature Drift **(Note 1)**	—	±25	±40	—	±25	±40	—	±50	±100	ppm/°C Full Scale	Variation in Gain A due to Temperature Change
Gain Variance	—	±10	—	—	±10	—	—	±10	—	% of Nominal	Variation from Ideal Accuracy
Zero Offset **(Note 2)**	—	±10	±50	—	±10	±50	—	±20	±100	mV	Correction at Zero Adjust for Zero Output when Input is Zero
Zero Temperature Drift **(Note 1)**	—	±25	±50	—	±25	±50	—	±50	±100	µV/°C	Variation in Zero Offset Due to Temperature Change

Note 1: Full temperature range; not tested.
2: I_{IN} = 0.
3: Full temperature range, I_{OUT} = 10 mA.
4: I_{OUT} = 10 µA.
5: Threshold Detect = 5V, Amp Out = 0V, full temperature range.
6: 10 Hz to 100 kHz; not tested.
7: 5 µs minimum positive pulse width and 0.5 µs minimum negative pulse width.
8: $t_R = t_F$ = 20 ns.
9: $R_L \geq 2$ kΩ, tested @ 10 kΩ.
10: Full temperature range, V_{IN} = -0.1V.

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TC940X ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: unless otherwise specified, V_{DD} = +5V, V_{SS} = -5V, V_{GND} = 0V, V_{REF} = -5V, R_{BIAS} = 100 kΩ, Full Scale = 10 kHz. T_A = +25°C, unless temperature range is specified (-40°C to +85°C for E device, 0°C to +70°C for C device).

Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units	Test Conditions
Analog Input											
I_{IN} Full Scale	—	10	—	—	10	—	—	10	—	µA	Full Scale Analog Input Current to achieve Specified Accuracy
I_{IN} Over Range	—	—	50	—	—	50	—	—	50	µA	Over Range Current
Response Time	—	2	—	—	2	—	—	2	—	Cycle	Settling Time to 0.1% Full Scale
Digital Section	**TC9400**			**TC9401**			**TC9402**				
V_{SAT} @ I_{OL} = 10mA	—	0.2	0.4	—	0.2	0.4	—	0.2	0.4	V	Logic “0” Output Voltage **(Note 3)**
V_{OUTMAX} – V_{OUT} Common **(Note 4)**	—	—	18	—	—	18	—	—	18	V	Voltage Range Between Output and Common
Pulse Frequency Output Width	—	3	—	—	3	—	—	3	—	µs	
Frequency-to-Voltage											
Supply Current											
I_{DD} Quiescent **(Note 5)**	—	1.5	6	—	1.5	6	—	3	10	mA	Current Required from Positive Supply during Operation
I_{SS} Quiescent **(Note 5)**	—	-1.5	-6	—	-1.5	-6	—	-3	-10	mA	Current Required from Negative Supply during Operation
V_{DD} Supply	4	—	7.5	4	—	7.5	4	—	7.5	V	Operating Range of Positive Supply
V_{SS} Supply	-4	—	-7.5	-4	—	-7.5	-4	—	-7.5	V	Operating Range of Negative Supply
Reference Voltage											
V_{REF} – V_{SS}	-2.5	—	—	-2.5	—	—	-2.5	—	—	V	Range of Voltage Reference Input
Accuracy											
Non-Linearity **(Note 10)**	—	0.02	0.05	—	0.01	0.02	—	0.05	0.25	% Full Scale	Deviation from ideal Transfer Function as a Percentage Full Scale Voltage
Input Frequency Range **(Notes 7 and 8)**	10	—	100k	10	—	100k	10	—	100k	Hz	Frequency Range for Specified Non-Linearity

Note 1: Full temperature range; not tested.
2: I_{IN} = 0.
3: Full temperature range, I_{OUT} = 10 mA.
4: I_{OUT} = 10 µA.
5: Threshold Detect = 5V, Amp Out = 0V, full temperature range.
6: 10 Hz to 100 kHz; not tested.
7: 5 µs minimum positive pulse width and 0.5 µs minimum negative pulse width.
8: t_R = t_F = 20 ns.
9: $R_L \geq 2$ kΩ, tested @ 10 kΩ.
10: Full temperature range, V_{IN} = -0.1V.

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TC940X ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: unless otherwise specified, V_{DD} = +5V, V_{SS} = -5V, V_{GND} = 0V, V_{REF} = -5V, R_{BIAS} = 100 kΩ, Full Scale = 10 kHz. T_A = +25°C, unless temperature range is specified (-40°C to +85°C for E device, 0°C to +70°C for C device).

Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units	Test Conditions
Frequency Input											
Positive Excursion	0.4	—	V_{DD}	0.4	—	V_{DD}	0.4	—	V_{DD}	V	Voltage Required to Turn Threshold Detector On
Negative Excursion	-0.4		-2	-0.4	—	-2	-0.4	—	-2	V	Voltage Required to Turn Threshold Detector Off
Minimum Positive Pulse Width **(Note 8)**	—	5	—	—	5	—	—	5	—	µs	Time between Threshold Crossings
Minimum Negative Pulse Width **(Note 8)**	—	0.5	—	—	0.5	—	—	0.5	—	µs	Time Between Threshold Crossings
Input Impedance	—	10	—	—	10	—		—	10	MΩ	
Analog Outputs	**TC9400**			**TC9401**			**TC9402**				
Output Voltage **(Note 9)**	—	V_{DD} – 1	—	—	V_{DD} – 1	—	—	V_{DD} – 1	—	V	Voltage Range of Op Amp Output for Specified Non-Linearity
Output Loading	2	—	—	2	—	—	2	—	—	kΩ	Resistive Loading at Output of Op Amp
Supply Current	**TC9400**			**TC9401**			**TC9402**				
I_{DD} Quiescent **(Note 10)**	—	1.5	6	—	1.5	6	—	3	10	mA	Current Required from Positive Supply During Operation
I_{SS} Quiescent **(Note 10)**	—	-1.5	-6		-1.5	-6	—	-3	-10	mA	Current Required from Negative Supply During Operation
V_{DD} Supply	4	—	7.5	4	—	7.5	4	—	7.5	V	Operating Range of Positive Supply
V_{SS} Supply	-4	—	-7.5	-4	—	-7.5	-4	—	-7.5	V	Operating Range of Negative Supply
Reference Voltage											
$V_{REF} – V_{SS}$	-2.5	—	—	-2.5	—	—	-2.5	—	—	V	Range of Voltage Reference Input

Note 1: Full temperature range; not tested.
2: I_{IN} = 0.
3: Full temperature range, I_{OUT} = 10 mA.
4: I_{OUT} = 10 µA.
5: Threshold Detect = 5V, Amp Out = 0V, full temperature range.
6: 10 Hz to 100 kHz; not tested.
7: 5 µs minimum positive pulse width and 0.5 µs minimum negative pulse width.
8: $t_R = t_F$ = 20 ns.
9: $R_L \geq$ 2 kΩ, tested @ 10 kΩ.
10: Full temperature range, V_{IN} = -0.1V.

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2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin No.	Symbol	Description
1	I_{BIAS}	This pin sets bias current in the TC9400. Connect to V_{SS} through a 100 kΩ resistor.
2	ZERO ADJ	Low frequency adjustment input.
3	I_{IN}	Input current connection for the V/F converter.
4	V_{SS}	Negative power supply voltage connection, typically -5V.
5	V_{REF} OUT	Reference capacitor connection.
6	GND	Analog ground.
7	V_{REF}	Voltage reference input, typically -5V.
8	PULSE FREQ OUT	Frequency output. This open drain output will pulse LOW each time the Freq. Threshold Detector limit is reached. The pulse rate is proportional to input voltage.
9	OUTPUT COMMON	Source connection for the open drain output FETs.
10	FREQ/2 OUT	This open drain output is a square wave at one-half the frequency of the pulse output (Pin 8). Output transitions of this pin occur on the rising edge of Pin 8.
11	THRESHOLD DETECTOR	Input to the Threshold Detector. This pin is the frequency input during F/V operation.
12	AMPLIFIER OUT	Output of the integrator amplifier.
13	NC	No internal connection.
14	V_{DD}	Positive power supply connection, typically +5V.

2.1 Bias Current (I_{BIAS})

An external resistor, connected to V_{SS}, sets the bias point for the TC9400. Specifications for the TC9400 are based on R_{BIAS} = 100 kΩ ±10%, unless otherwise noted.

Increasing the maximum frequency of the TC9400 beyond 100 kHz is limited by the pulse width of the pulse output (typically 3 µs). Reducing R_{BIAS} will decrease the pulse width and increase the maximum operating frequency, but linearity errors will also increase. R_{BIAS} can be reduced to 20 kΩ, which will typically produce a maximum full scale frequency of 500 kHz.

2.2 Zero Adjust

This pin is the non-inverting input of the operational amplifier. The low frequency set point is determined by adjusting the voltage at this pin.

2.3 Input Current (I_{IN})

The inverting input of the operational amplifier and the summing junction when connected in the V/F mode. An input current of 10 µA is specified, but an over range current up to 50 µA can be used without detrimental effect to the circuit operation. I_{IN} connects the summing junction of an operational amplifier. Voltage sources cannot be attached directly, but must be buffered by external resistors.

2.4 Voltage Capacitor (V_{REF} Out)

The charging current for C_{REF} is supplied through this pin. When the op amp output reaches the threshold level, this pin is internally connected to the reference voltage and a charge, equal to V_{REF} x C_{REF}, is removed from the integrator capacitor. After about 3µsec, this pin is internally connected to the summing junction of the op amp to discharge C_{REF}. Break-before-make switching ensures that the reference voltage is not directly applied to the summing junction.

2.5 Voltage Reference (V_{REF})

A reference voltage from either a precision source, or the V_{SS} supply is applied to this pin. Accuracy of the TC9400 is dependent on the voltage regulation and temperature characteristics of the reference circuitry.

Since the TC9400 is a charge balancing V/F converter, the reference current will be equal to the input current. For this reason, the DC impedance of the reference voltage source must be kept low enough to prevent linearity errors. For linearity of 0.01%, a reference impedance of 200Ω or less is recommended. A 0.1 µF bypass capacitor should be connected from V_{REF} to ground.

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2.6 Pulse Freq Out

This output is an open-drain N-channel FET, which provides a pulse waveform whose frequency is proportional to the input voltage. This output requires a pull-up resistor and interfaces directly with MOS, CMOS, and TTL logic (see Figure 2-1).

2.7 Output Common

The sources of both the FREQ/2 OUT and the PULSE FREQ OUT are connected to this pin. An output level swing from the drain voltage to ground, or to the V_{SS} supply, may be obtained by connecting this pin to the appropriate point.

2.8 Freq/2 Out

This output is an open-drain N-channel FET, which provides a square-wave one-half the frequency of the pulse frequency output. The FREQ/2 OUT output will change state on the rising edge of PULSE FREQ OUT. This output requires a pull-up resistor and interfaces directly with MOS, CMOS, and TTL logic.

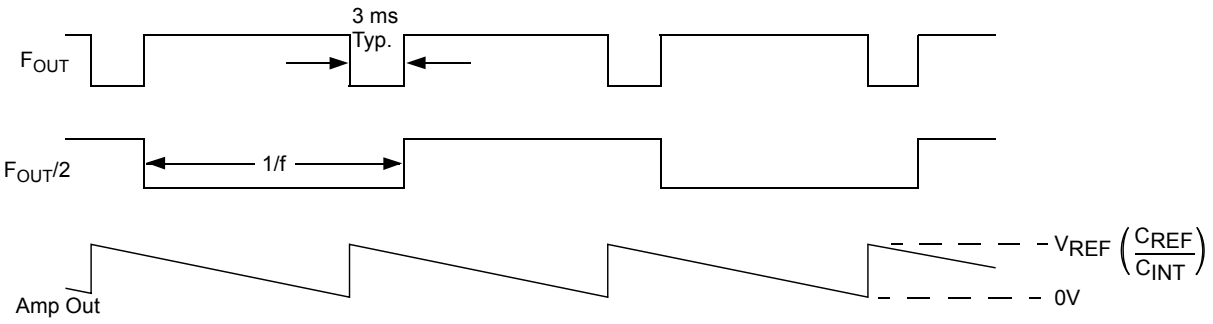
2.9 Threshold Detector Input

In the V/F mode, this input is connected to the AMPLIFIER OUT output (Pin 12) and triggers a 3 µs pulse when the input voltage passes through its threshold. In the F/V mode, the input frequency is applied to this input.

The nominal threshold of the detector is half way between the power supplies, or (V_{DD} + V_{SS})/2 ±400 mV. The TC9400's charge balancing V/F technique is not dependent on a precision comparator threshold, because the threshold only sets the lower limit of the op amp output. The op amp's peak-to-peak output swing, which determines the frequency, is only influenced by external capacitors and by V_{REF}.

2.10 Amplifier Out

This pin is the output stage of the operational amplifier. During V/F operation, a negative going ramp signal is available at this pin. In the F/V mode, a voltage proportional to the frequency input is generated.



Note 1: To adjust F_{MIN}, set V_{IN} = 10 mV and adjust the 50 kΩ offset for 10 Hz output.

2: To adjust F_{MAX}, set V_{IN} = 10V and adjust R_{IN} or V_{REF} for 10 kHz output.

3: To increase F_{OUTMAX} to 100 kHz, change C_{REF} to 2 pF and C_{INT} to 75 pF.

4: For high performance applications, use high stability components for R_{IN}, C_{REF}. V_{REF} (metal film resistors and glass capacitors). Also, separate output ground (Pin 9) from input ground (Pin 6).

FIGURE 2-1: *Output Waveforms.*

3.0 DETAILED DESCRIPTION

3.1 Voltage-to-Frequency (V/F) Circuit Description

The TC9400 V/F converter operates on the principal of charge balancing. The operation of the TC9400 is easily understood by referring to Figure 3-1. The input voltage (V_{IN}) is converted to a current (I_{IN}) by the input resistor. This current is then converted to a charge on the integrating capacitor and shows up as a linearly decreasing voltage at the output of the op amp. The lower limit of the output swing is set by the threshold detector, which causes the reference voltage to be applied to the reference capacitor for a time period long enough to charge the capacitor to the reference voltage. This action reduces the charge on the integrating capacitor by a fixed amount ($q = C_{REF} \times V_{REF}$), causing the op amp output to step up a finite amount.

At the end of the charging period, C_{REF} is shorted out. This dissipates the charge stored on the reference capacitor, so that when the output again crosses zero, the system is ready to recycle. In this manner, the continued discharging of the integrating capacitor by the input is balanced out by fixed charges from the reference voltage. As the input voltage is increased, the number of reference pulses required to maintain balance increases, which causes the output frequency to also increase. Since each charge increment is fixed, the increase in frequency with voltage is linear. In addition, the accuracy of the output pulse width does not directly affect the linearity of the V/F. The pulse must simply be long enough for full charge transfer to take place.

The TC9400 contains a “self-start” circuit to ensure the V/F converter always operates properly when power is first applied. In the event that, during power-on, the op amp output is below the threshold and C_{REF} is already charged, a positive voltage step will not occur. The op amp output will continue to decrease until it crosses the -3.0V threshold of the “self-start” comparator. When this happens, an internal resistor is connected to the op amp input, which forces the output to go positive until the TC9400 is in its normal Operating mode.

The TC9400 utilizes low-power CMOS processing for low input bias and offset currents, with very low power dissipation. The open drain N-channel output FETs provide high voltage and high current sink capability.

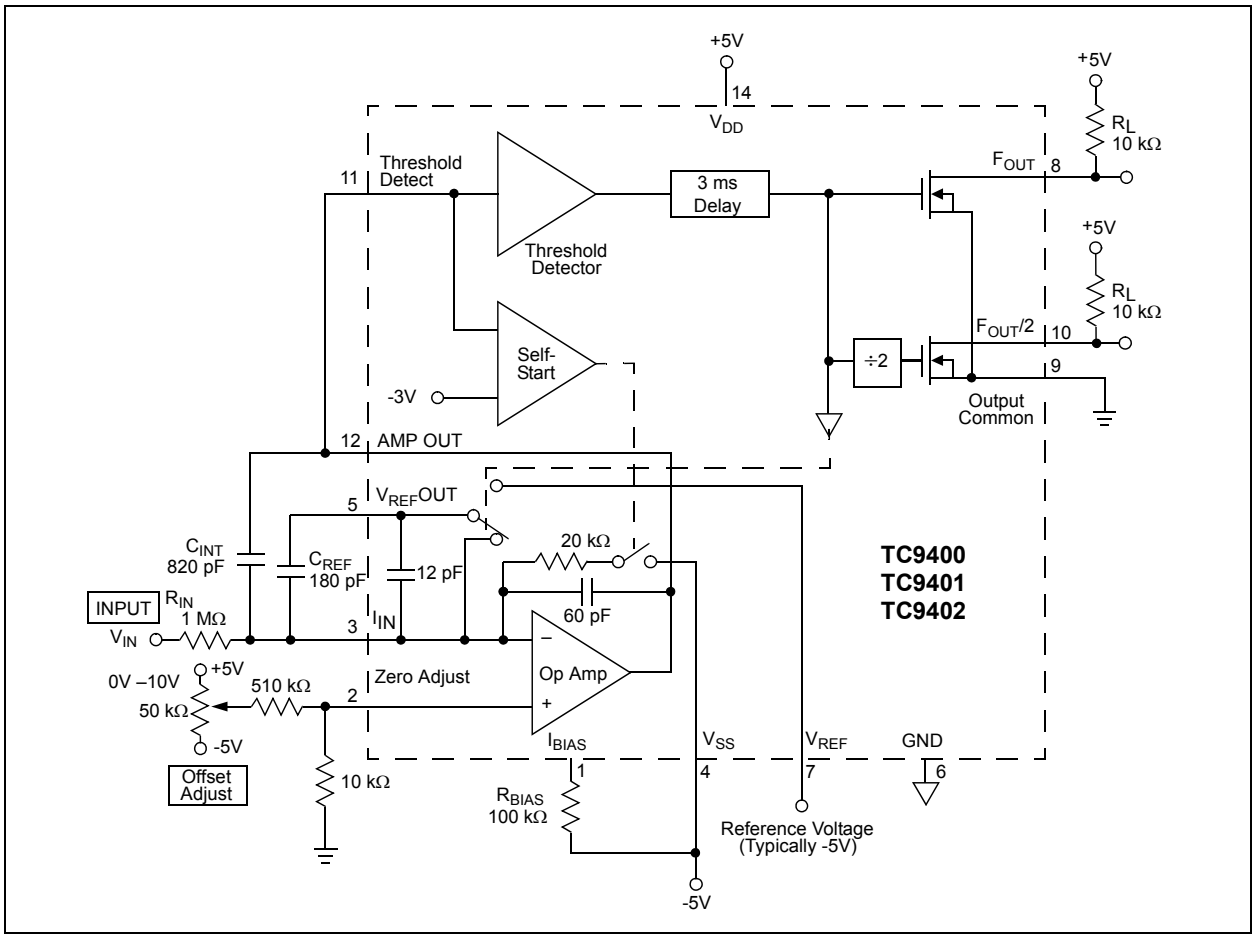


FIGURE 3-1: *10 Hz to 10 kHz V/F Converter.*

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3.2 Voltage-to-Time Measurements

The TC9400 output can be measured in the time domain as well as the frequency domain. Some microcomputers, for example, have extensive timing capability, but limited counter capability. Also, the response time of a time domain measurement is only the period between two output pulses, while the frequency measurement must accumulate pulses during the entire counter time-base period.

Time measurements can be made from either the TC9400's PULSE FREQ OUT output, or from the FREQ/2 OUT output. The FREQ/2 OUT output changes state on the rising edge of PULSE FREQ OUT, so FREQ/2 OUT is a symmetrical square wave at one-half the pulse output frequency. Timing measurements can, therefore, be made between successive PULSE FREQ OUT pulses, or while FREQ/2 OUT is high (or low).

4.0 VOLTAGE-TO-FREQUENCY (V/F) CONVERTER DESIGN INFORMATION

4.1 Input/Output Relationships

The output frequency (F_{OUT}) is related to the analog input voltage (V_{IN}) by the transfer equation:

EQUATION 4-1:

$$Frequency\ Out = \frac{V_{IN}}{R_{IN}} \bullet \frac{1}{(V_{REF})(C_{REF})}$$

4.2 External Component Selection

4.2.1 R_{IN}

The value of this component is chosen to give a full scale input current of approximately 10 µA:

EQUATION 4-2:

$$R_{IN} \cong \frac{V_{IN}{}^{FULL\ SCALE}}{10\ \mu A}$$

EQUATION 4-3:

$$R_{IN} \cong \frac{10V}{10\ \mu A} = 1\ M\Omega$$

Note that the value is an approximation and the exact relationship is defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed to obtain full scale frequency at V_{IN} full scale (see **Section 4.3 "Adjustment Procedure"**, Adjustment Procedure). Metal film resistors with 1% tolerance or better are recommended for high accuracy applications because of their thermal stability and low noise generation.

4.2.2 C_{INT}

The exact value is not critical but is related to C_{REF} by the relationship:

$$3C_{REF} \le C_{INT} \le 10C_{REF}$$

Improved stability and linearity are obtained when $C_{INT} \le 4C_{REF}$. Low leakage types are recommended, although mica and ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to Pins 12 and 13.

4.2.3 C_{REF}

The exact value is not critical and may be used to trim the full scale frequency (see **Section 6.1 "Input/Output Relationships"**, Input/Output Relationships). Glass film or air trimmer capacitors are recommended because of their stability and low leakage. Locate as close as possible to Pins 5 and 3 (see Figure 4-1).

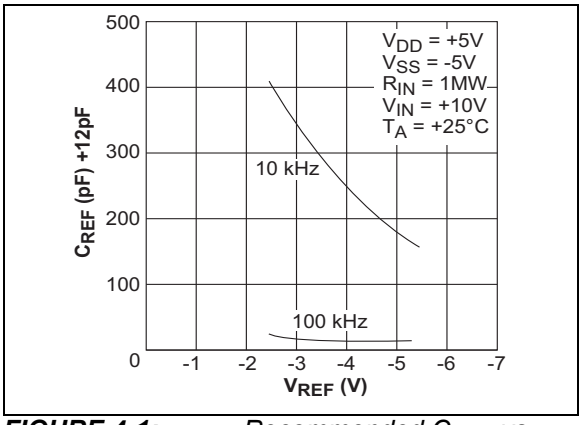


FIGURE 4-1: *Recommended C_{REF} vs. V_{REF}.*

4.2.4 V_{DD}, V_{SS}

Power supplies of ±5V are recommended. For high accuracy requirements, 0.05% line and load regulation and 0.1 µF disc decoupling capacitors, located near the pins, are recommended.

4.3 Adjustment Procedure

Figure 3-1 shows a circuit for trimming the zero location. Full scale may be trimmed by adjusting R_{IN}, V_{REF}, or C_{REF}. Recommended procedure for a 10 kHz full scale frequency is as follows:

1. Set V_{IN} to 10 mV and trim the zero adjust circuit to obtain a 10 Hz output frequency.
2. Set V_{IN} to 10V and trim either R_{IN}, V_{REF}, or C_{REF} to obtain a 10 kHz output frequency.

If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

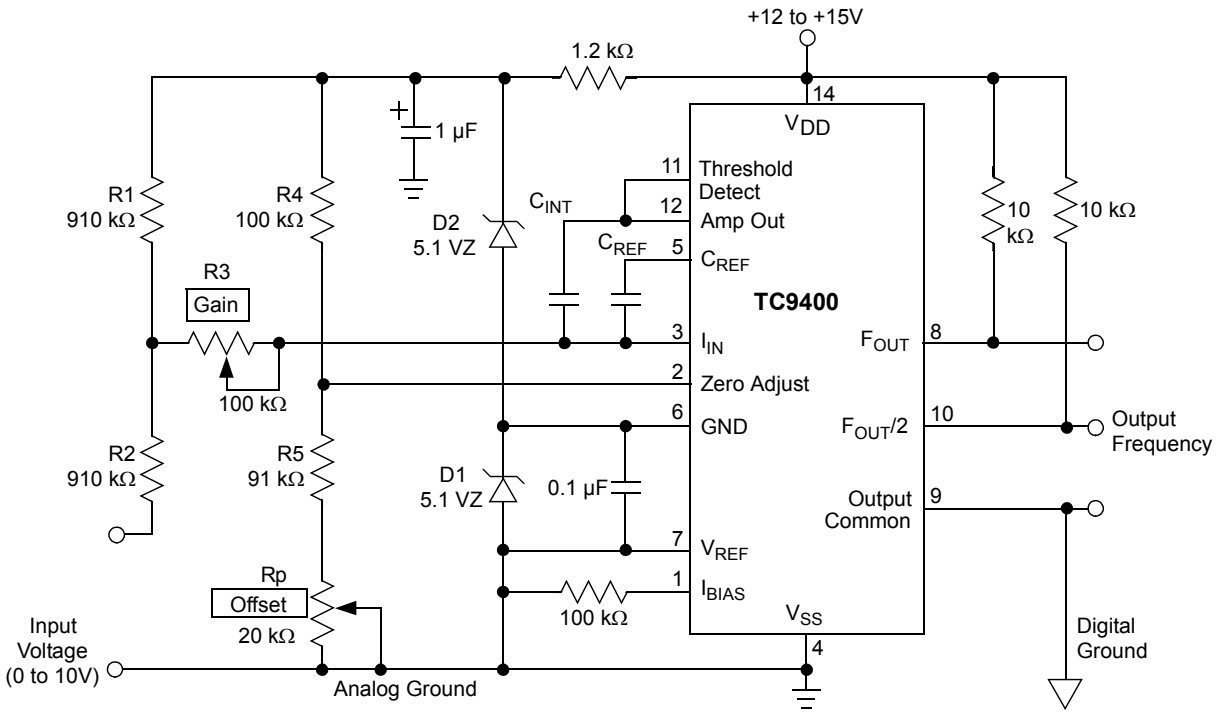
4.4 Improved Single Supply V/F Converter Operation

A TC9400, which operates from a single 12 to 15V variable power source, is shown in Figure 4-2. This circuit uses two Zener diodes to set stable biasing levels for the TC9400. The Zener diodes also provide the reference voltage, so the output impedance and temperature coefficient of the Zeners will directly affect power supply rejection and temperature performance. Full scale adjustment is accomplished by trimming the input current.

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Trimming the reference voltage is not recommended for high accuracy applications unless an op amp is used as a buffer, because the TC9400 requires a low-impedance reference (see **Section 2.5 "Voltage Reference (VREF)"**, V_{REF} pin description, for more information).

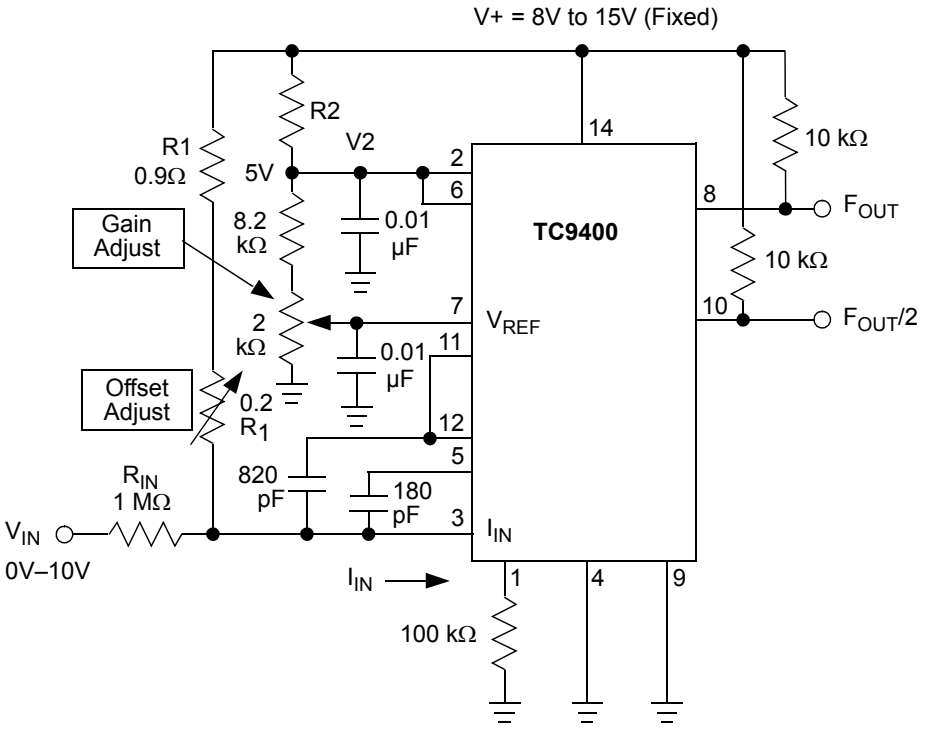
The circuit of Figure 4-2 will directly interface with CMOS logic operating at 12V to 15V. TTL or 5V CMOS logic can be accommodated by connecting the output pull-up resistors to the +5V supply. An optoisolator can also be used if an isolated output is required; also, see Figure 4-3.



Component Selection

F/S Freq.	C_{REF}	C_{INT}
1 kHz	2200 pF	4700 pF
10 kHz	180 pF	470 pF
100 kHz	27 pF	75 pF

FIGURE 4-2: *Voltage-to-Frequency.*



V+	R_1	R_2
10V	1 MΩ	10 kΩ
12V	1.4 MΩ	14 kΩ
15V	2 MΩ	20 kΩ

$$F_{OUT} = I_{IN}\frac{1}{(V_2 - V_7)(C_{REF})}$$

$$I_{IN} = \frac{(V_{IN} - V_2)}{R_{IN}} + \frac{(V+ - V_2)}{(0.9R_1 + 0.2R_1)}$$

FIGURE 4-3: *Fixed Voltage – Single Supply Operation.*

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5.0 FREQUENCY-TO-VOLTAGE (F/V) CIRCUIT DESCRIPTION

When used as an F/V converter, the TC9400 generates an output voltage linearly proportional to the input frequency waveform.

Each zero crossing at the threshold detector's input causes a precise amount of charge ($q = C_{REF} \times V_{REF}$) to be dispensed into the op amp's summing junction. This charge, in turn, flows through the feedback resistor, generating voltage pulses at the output of the op amp. A capacitor (C_{INT}) across R_{INT} averages these pulses into a DC voltage, which is linearly proportional to the input frequency.

6.0 F/V CONVERTER DESIGN INFORMATION

6.1 Input/Output Relationships

The output voltage is related to the input frequency (F_{IN}) by the transfer equation:

EQUATION 6-1:

$$V_{OUT} = [V_{REF}\, C_{REF}\, R_{INT}]\, F_{IN}$$

The response time to a change in F_{IN} is equal to (R_{INT} C_{INT}). The amount of ripple on V_{OUT} is inversely proportional to C_{INT} and the input frequency.

C_{INT} can be increased to lower the ripple. Values of 1 µF to 100 µF are perfectly acceptable for low frequencies.

When the TC9400 is used in the Single Supply mode, V_{REF} is defined as the voltage difference between Pin 7 and Pin 2.

6.2 Input Voltage Levels

The input frequency is applied to the Threshold Detector input (Pin 11). As discussed in the V/F circuit section of this data sheet, the threshold of Pin 11 is approximately (V_{DD} + V_{SS})/2 ±400 mV. Pin 11's input voltage range extends from V_{DD} to about 2.5V below the threshold. If the voltage on Pin 11 goes more than 2.5 volts below the threshold, the V/F mode start-up comparator will turn on and corrupt the output voltage. The Threshold Detector input has about 200 mV of hysteresis.

In ±5V applications, the input voltage levels for the TC9400 are ±400 mV, minimum. If the frequency source being measured is unipolar, such as TTL or CMOS operating from a +5V source, then an AC coupled level shifter should be used. One such circuit is shown in Figure 6-1(a).

The level shifter circuit in Figure 6-1(b) can be used in single supply F/V applications. The resistor divider ensures that the input threshold will track the supply voltages. The diode clamp prevents the input from going far enough in the negative direction to turn on the start-up comparator. The diode's forward voltage decreases by 2.1 mV/°C, so for high ambient temperature operation, two diodes in series are recommended.

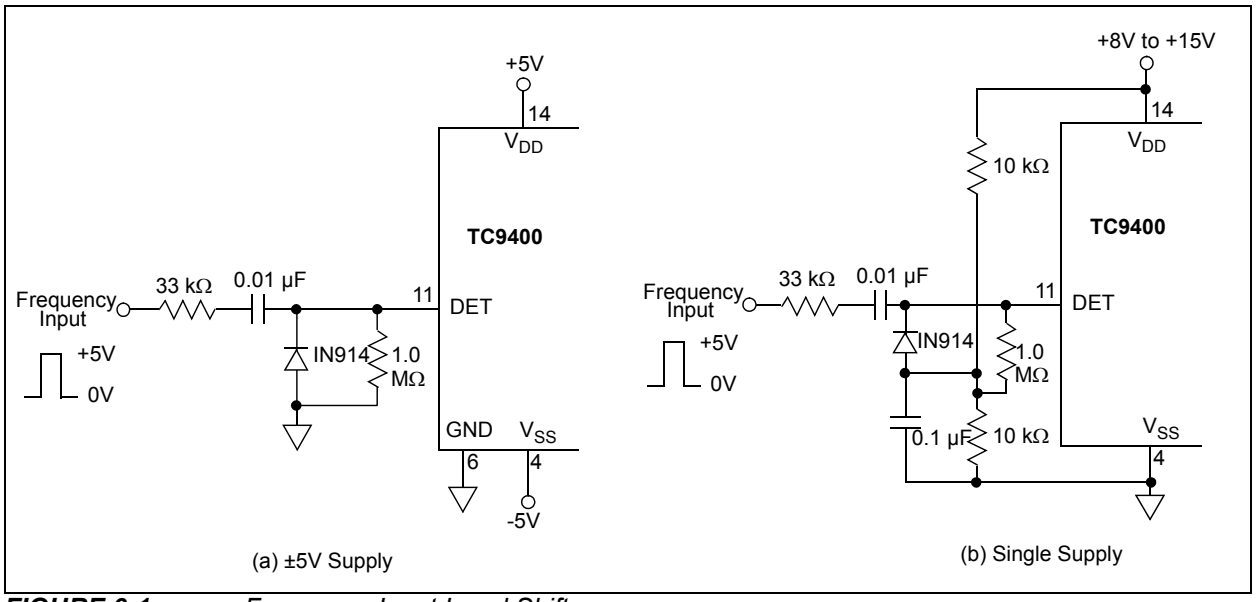
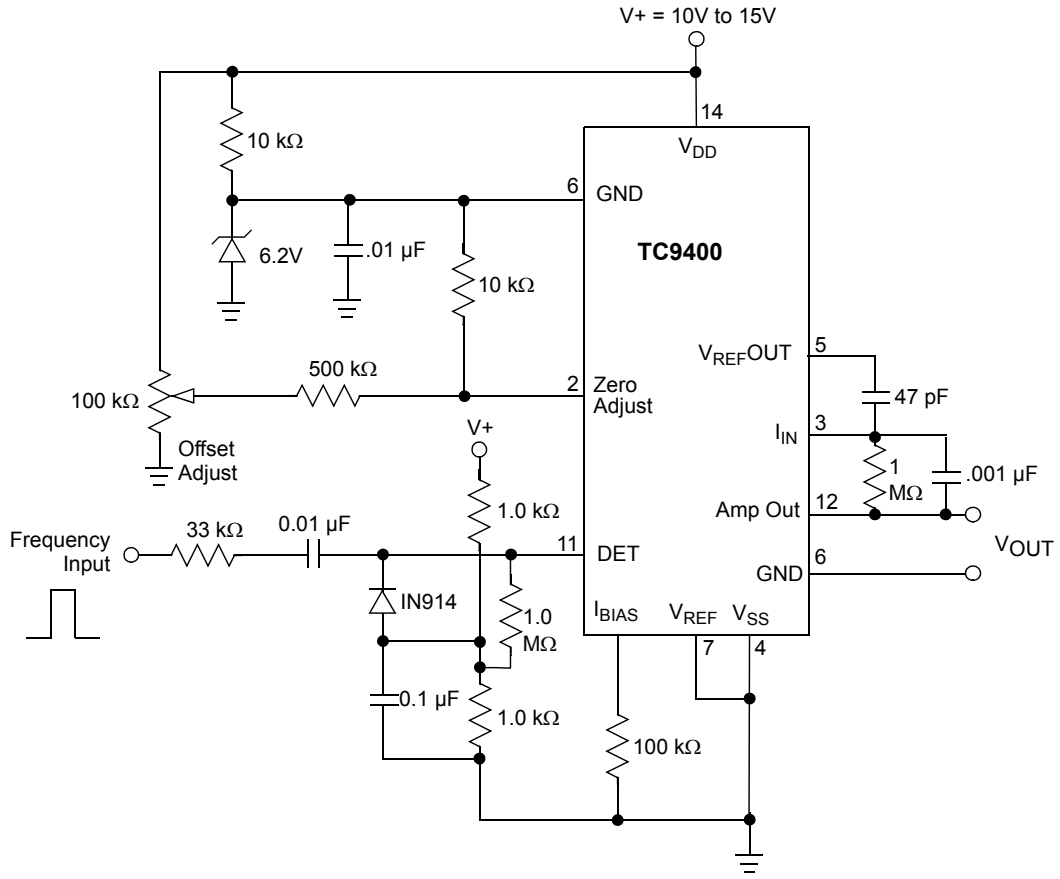


FIGURE 6-1: *Frequency Input Level Shifter.*

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Note: The output is referenced to Pin 6, which is at 6.2V (Vz). For frequency meter applications, a 1 mA meter with a series scaling resistor can be placed across Pins 6 and 12.

FIGURE 6-2: *F/V Single Supply F/V Converter.*

6.3 Input Buffer

F_{OUT} and $F_{OUT}/2$ are not used in the F/V mode. However, these outputs may be useful for some applications, such as a buffer to feed additional circuitry. Then, F_{OUT} will follow the input frequency waveform, except that F_{OUT} will go high 3 µs after F_{IN} goes high; $F_{OUT}/2$ will be square wave with a frequency of one-half F_{OUT}.

If these outputs are not used, Pins 8, 9 and 10 should be connected to ground (see Figure 6-3 and Figure 6-4).

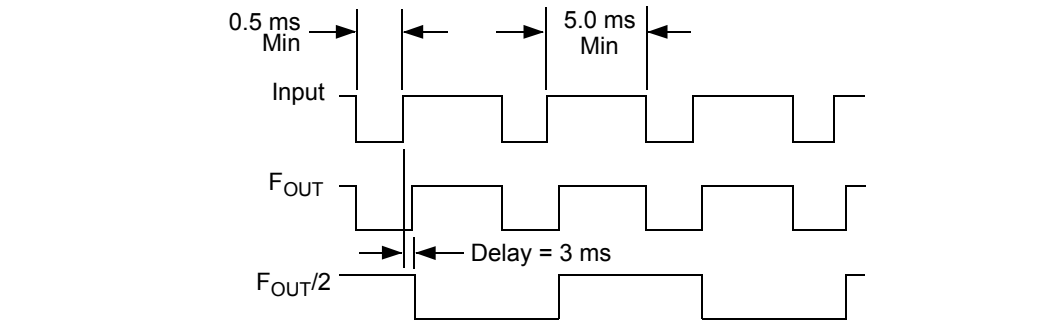


FIGURE 6-3: *F/V Digital Outputs.*

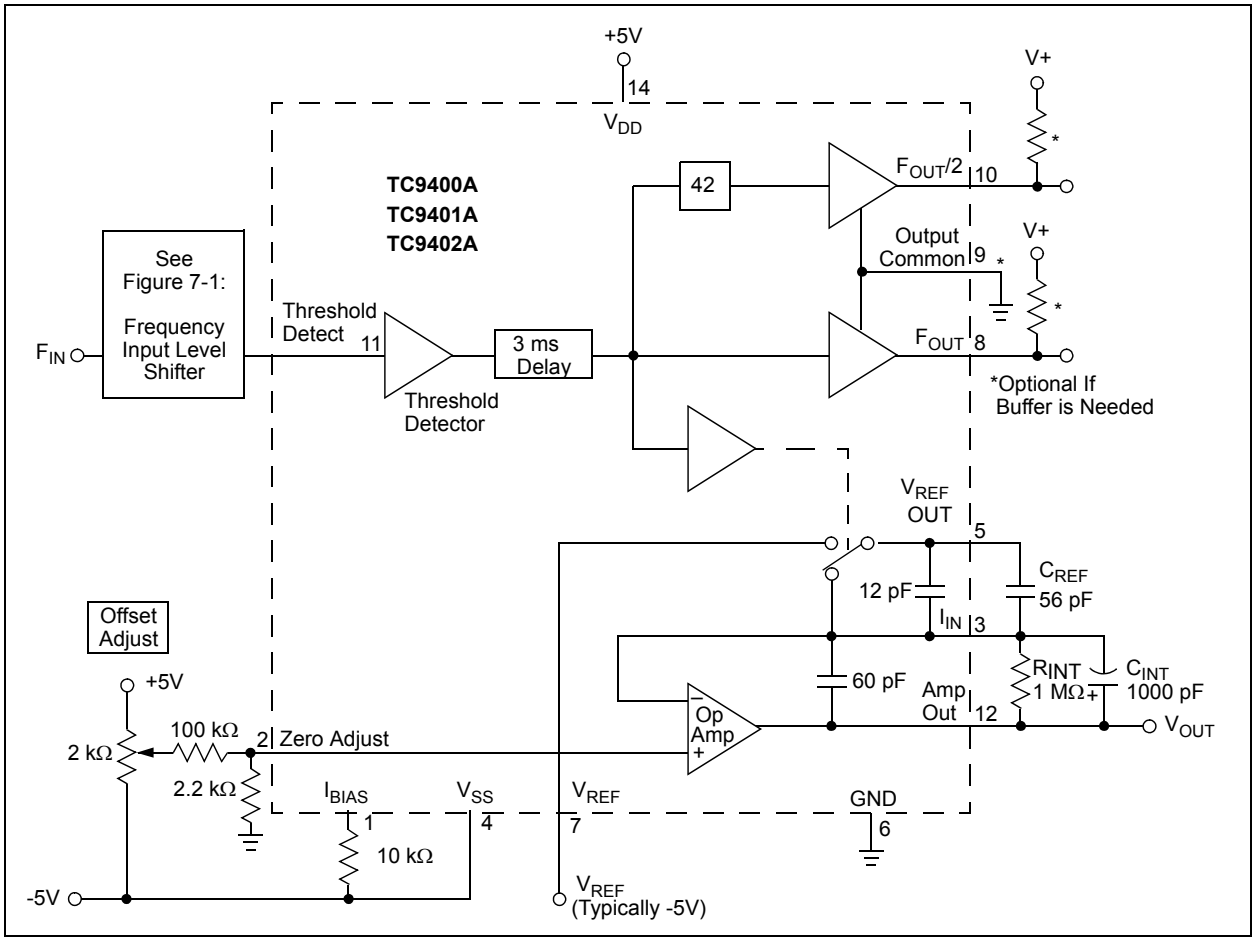


FIGURE 6-4: *DC – 10 kHz Converter.*

6.4 Output Filtering

The output of the TC9400 has a sawtooth ripple superimposed on a DC level. The ripple will be rejected if the TC9400 output is converted to a digital value by an integrating Analog-to-Digital Converter, such as the TC7107. The ripple can also be reduced by increasing the value of the integrating capacitor, although this will reduce the response time of the F/V converter.

The sawtooth ripple on the output of an F/V can be eliminated without affecting the F/V's response time by using the circuit in Figure 6-1. The circuit is a capacitance multiplier, where the output coupling capacitor is multiplied by the AC gain of the op amp. A moderately fast op amp, such as the TL071, should be used.

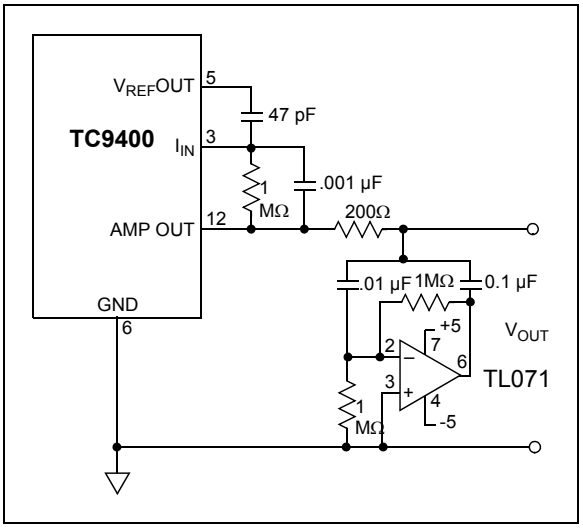


FIGURE 6-5: *Ripple Filter.*

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7.0 F/V POWER-ON RESET

In F/V mode, the TC9400 output voltage will occasionally be at its maximum value when power is first applied. This condition remains until the first pulse is applied to F_{IN}. In most frequency measurement applications, this is not a problem because proper operation begins as soon as the frequency input is applied.

In some cases, however, the TC9400 output must be zero at power-on without a frequency input. In such cases, a capacitor connected from Pin 11 to V_{DD} will usually be sufficient to pulse the TC9400 and provide a Power-on Reset (see Figure 7-1 (a) and (b)). Where predictable power-on operation is critical, a more complicated circuit, such as Figure 7-1 (b), may be required.

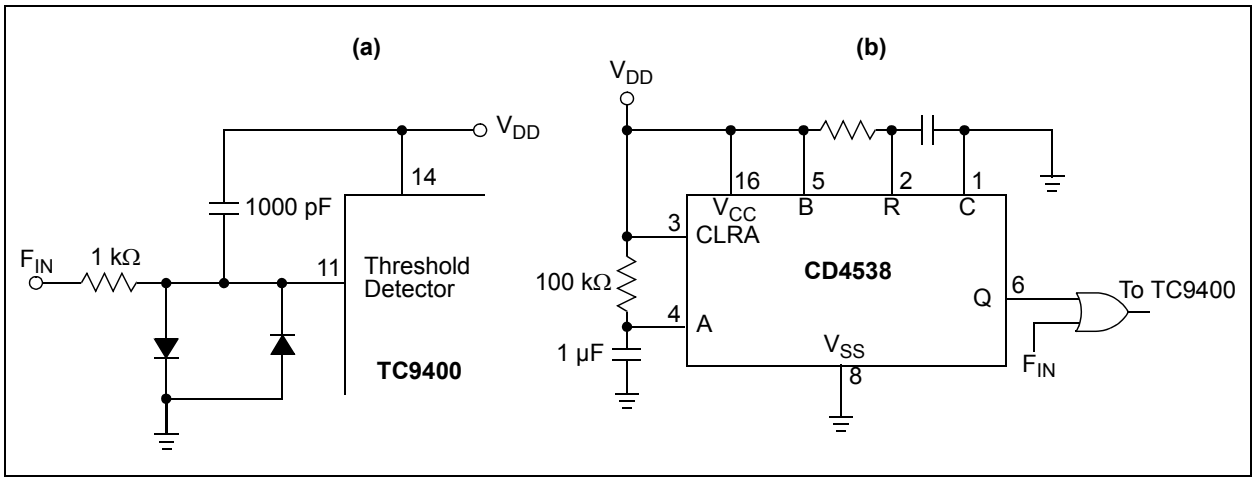
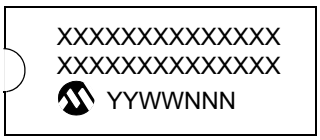


FIGURE 7-1: *Power-On Operation/Reset.*

8.0 PACKAGE INFORMATION

8.1 Package Marking Information

14-Lead CERDIP



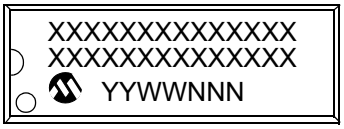
Example: (Front View)



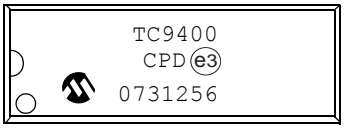
Example: (Back View)



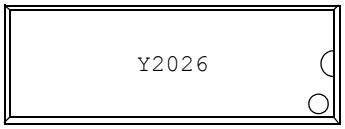
14-Lead PDIP



Example: (Front View)



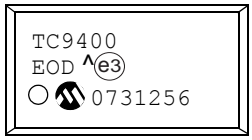
Example: (Back View)



14-Lead SOIC (.150")



Example: (Front View)



Example: (Back View)



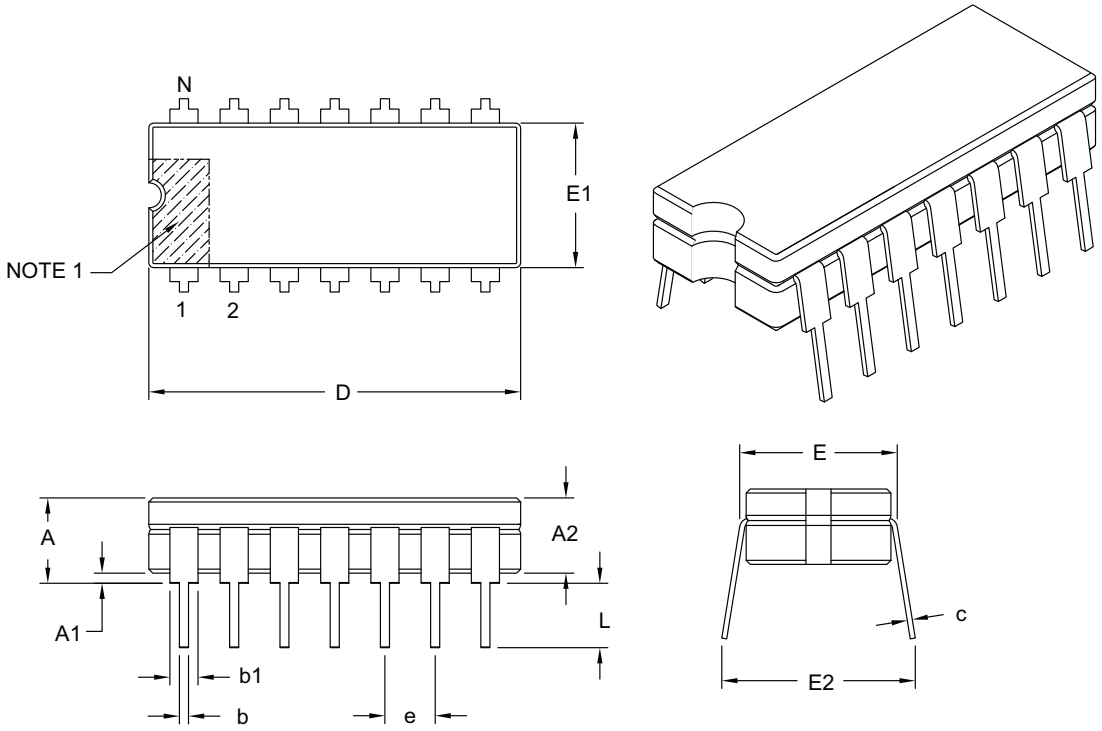
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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14-Lead Ceramic Dual In-Line (JD) – .300" Body [CERDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.200
Standoff §	A1	.015	–	–
Ceramic Package Height	A2	.140	–	.175
Shoulder to Shoulder Width	E	.290	–	.325
Ceramic Package Width	E1	.230	.288	.300
Overall Length	D	.740	.760	.780
Tip to Seating Plane	L	.125	–	.200
Lead Thickness	c	.008	–	.015
Upper Lead Width	b1	.045	–	.065
Lower Lead Width	b	.015	–	.023
Overall Row Spacing	E2	.320	–	.410

Notes:

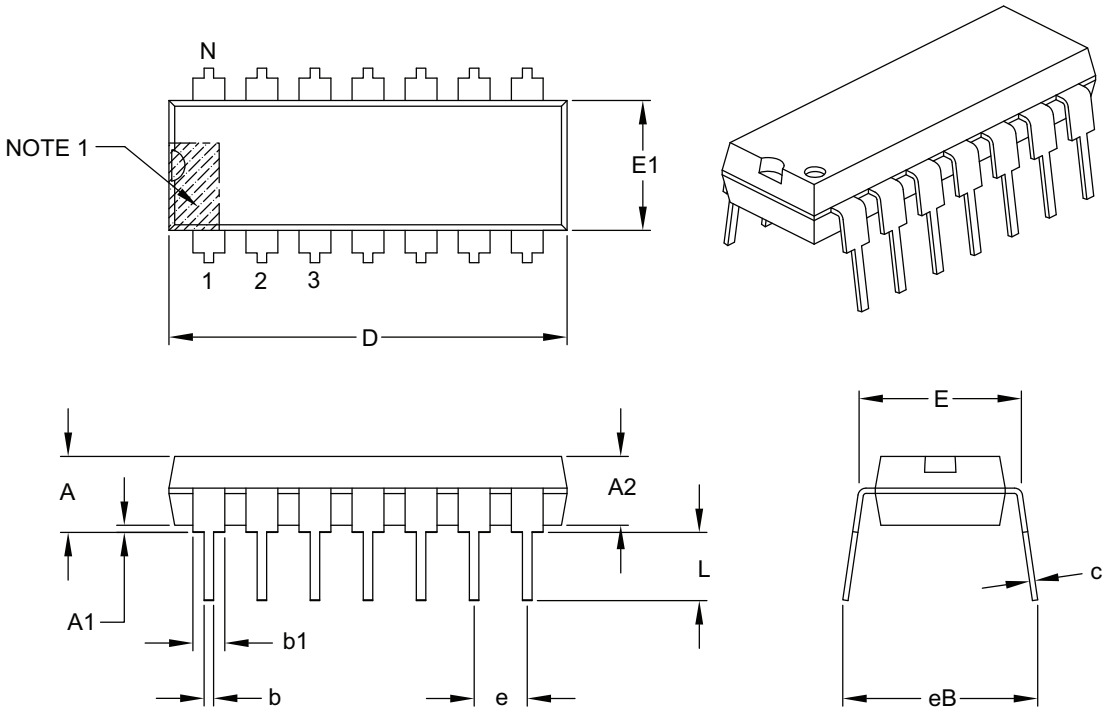
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-002B

14-Lead Plastic Dual In-Line (PD) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

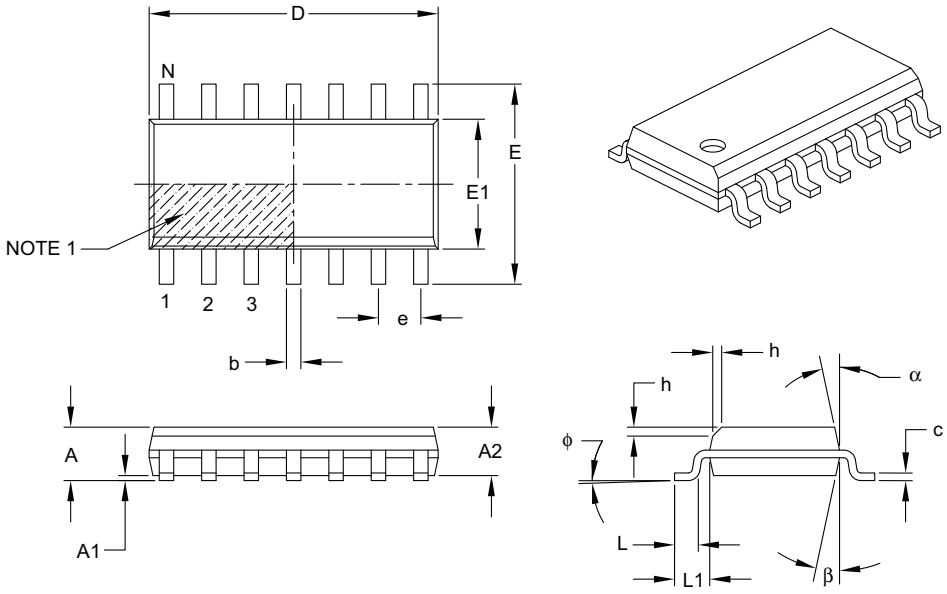
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

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14-Lead Plastic Small Outline (OD) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-065B

NOTES:

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APPENDIX A: REVISION HISTORY

Revision D (September 2007)

The following is the list of modifications:

1. Corrected Figure 6-1.
2. Added History section.
3. Updated package marking information and package outline drawings
4. Added Product identification System section.

Revision C (May 2006)

Revision B (May 2002)

Revision A (April 2002)

- Original Release of this Document.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device	TC9400: Voltage-to-Frequency Converter TC9401: Voltage-to-Frequency Converter TC9402: Voltage-to-Frequency Converter	
Temperature Range	E = -40°C to +85°C (Extended) C = 0°C to +70°C (Commercial)	
Package	JD = Ceramic Dual-Inline (.300” Body), 14-lead PD = Plastic Dual-Inline (300 mil Body), 14-lead OD = Plastic Small Outline (3.90 MM Body), 14-lead OD713 = Plastic Small Outline (3.90 MM Body), 14-lead Tape and Reel.	

Examples:

a) TC9400COD: 0°C to +70°C, 14LD SOIC package.

b) TC9400COD713: 0°C to +70°C, 14LD SOIC package, Tape and Reel

c) TC9400CPD: 0°C to +70°C, 14LD PDIP package.

d) TC9400EJD: -40°C to +85°C, 14LD PDIP package.

a) TC9401CPD: 0°C to +70°C, 14LD PDIP package.

b) TC9401EJD: -40°C to +85°C, 14LD CERDIP package.

a) TC9402CPD: 0°C to +70°C, 14LD PDIP package.

b) TC9402EJD: -40°C to +85°C, 14LD CERDIP package.

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