100ksps/250ksps/500ksps, 12-Bit Serial ADCs in TSOT-23

FEATURES

- **12-Bit Resolution**
- **Low Noise: 73dB SNR**
- **Low Power Dissipation: 1.5mW at 100ksps**
- **100ksps/250ksps/500ksps Sampling Rates**
- Single Supply 2.35V to 3.6V Operation
- No Data Latency
- Sleep Mode with 0.1µA Typical Supply Current
- Dedicated External Reference (TSOT23-8)
- 1V to 3.6V Digital Output Supply (TSOT23-8)
- SPI/MICROWIRE™ Compatible Serial I/O
- Guaranteed Operation from –40°C to 125°C
- Tiny 6- and 8-Lead TSOT-23 Packages

APPLICATIONS

- Communication Systems
- Data Acquisition Systems
- Handheld Portable Devices
- Uninterrupted Power Supplies
- Battery-Operated Systems
- Automotive

DESCRIPTION

The LTC®2360/LTC2361/LTC2362 are 100ksps/250ksps/500ksps, 12-bit, sampling A/D converters that draw only 0.5mA, 0.75mA and 1.1mA, respectively, from a single 3V supply. The supply current drops at lower sampling rates because these devices automatically power down after conversions. The full-scale input of the LTC2360/LTC2361/LTC2362 is 0V to V_{DD} or V_{REF}. These ADCs are available in tiny 6- and 8-lead TSOT-23 packages.

The serial interface, tiny TSOT-23 package and extremely high sample rate-to-power ratio make the LTC2360/LTC2361/LTC2362 ideal for compact, low power, high speed systems.

The high impedance single-ended analog input and the ability to operate with reduced spans (down to 1.4V full scale) allow direct connection to sensors and transducers in many applications, eliminating the need for gain stages.

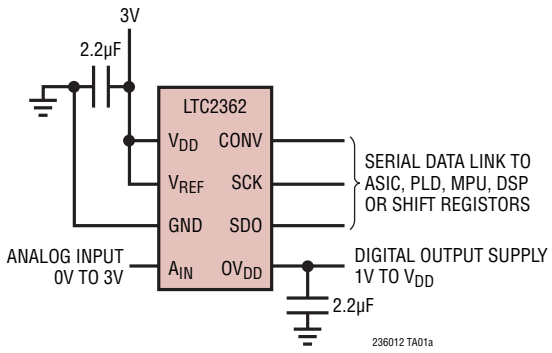
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TYPICAL APPLICATION

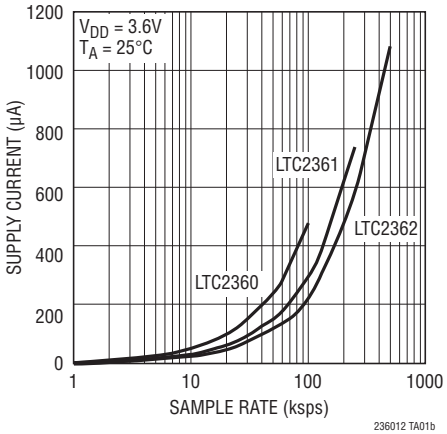
12-Bit TSOT23-6/-8 ADC Family

DATA OUTPUT RATE	3Msps	1Msps	500ksps	250ksps	100ksps
Part Number	LTC2366	LTC2365	LTC2362	LTC2361	LTC2360

Single 3V Supply, 500ksps, 12-Bit Sampling ADC



Supply Current vs Sample Rate

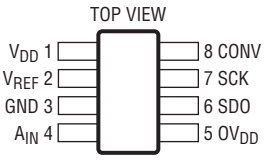


ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

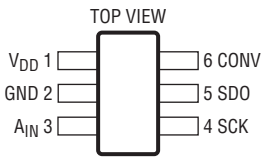
Supply Voltage (V_{DD}) 4V
Supply Voltage (OV_{DD})..... Min (V_{DD} + 0.3V, 4.0V)
V_{REF} and Analog Input Voltage
(Note 3).....–0.3V to (V_{DD} + 0.3V)
Digital Input Voltage.....–0.3V to (V_{DD} + 0.3V)
Digital Output Voltage .....–0.3V to (V_{DD} + 0.3V)
Power Dissipation 100mW

Operating Temperature Range
LTC2360C/LTC2361C/LTC2362C ..... 0°C to 70°C
LTC2360I/LTC2361I/LTC2362I..... –40°C to 85°C
LTC2360H/LTC2361H/LTC2362H (Note 12).. –40°C to 125°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C, θ_{JA} = 250°C/W



S6 PACKAGE
6-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C, θ_{JA} = 250°C/W

ORDER INFORMATION

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2362CTS8#TRMPBF	LTC2362CTS8#TRPBF	LTDBV	8-Lead Plastic TSOT23	0°C to 70°C
LTC2362ITS8#TRMPBF	LTC2362ITS8#TRPBF	LTDBV	8-Lead Plastic TSOT23	-40°C to 85°C
LTC2362HTS8#TRMPBF	LTC2362HTS8#TRPBF	LTDBV	8-Lead Plastic TSOT23	-40°C to 125°C
LTC2362CS6#TRMPBF	LTC2362CS6#TRPBF	LTDGP	6-Lead Plastic TSOT23	0°C to 70°C
LTC2362IS6#TRMPBF	LTC2362IS6#TRPBF	LTDGP	6-Lead Plastic TSOT23	-40°C to 85°C
LTC2362HS6#TRMPBF	LTC2362HS6#TRPBF	LTDGP	6-Lead Plastic TSOT23	-40°C to 125°C
LTC2361CTS8#TRMPBF	LTC2361CTS8#TRPBF	LTDGM	8-Lead Plastic TSOT23	0°C to 70°C
LTC2361ITS8#TRMPBF	LTC2361ITS8#TRPBF	LTDGM	8-Lead Plastic TSOT23	-40°C to 85°C
LTC2361HTS8#TRMPBF	LTC2361HTS8#TRPBF	LTDGM	8-Lead Plastic TSOT23	-40°C to 125°C
LTC2361CS6#TRMPBF	LTC2361CS6#TRPBF	LTDGN	6-Lead Plastic TSOT23	0°C to 70°C
LTC2361IS6#TRMPBF	LTC2361IS6#TRPBF	LTDGN	6-Lead Plastic TSOT23	-40°C to 85°C
LTC2361HS6#TRMPBF	LTC2361HS6#TRPBF	LTDGN	6-Lead Plastic TSOT23	-40°C to 125°C
LTC2360CTS8#TRMPBF	LTC2360CTS8#TRPBF	LTDGJ	8-Lead Plastic TSOT23	0°C to 70°C
LTC2360ITS8#TRMPBF	LTC2360ITS8#TRPBF	LTDGJ	8-Lead Plastic TSOT23	-40°C to 85°C
LTC2360HTS8#TRMPBF	LTC2360HTS8#TRPBF	LTDGJ	8-Lead Plastic TSOT23	-40°C to 125°C
LTC2360CS6#TRMPBF	LTC2360CS6#TRPBF	LTDGK	6-Lead Plastic TSOT23	0°C to 70°C
LTC2360IS6#TRMPBF	LTC2360IS6#TRPBF	LTDGK	6-Lead Plastic TSOT23	-40°C to 85°C
LTC2360HS6#TRMPBF	LTC2360HS6#TRPBF	LTDGK	6-Lead Plastic TSOT23	-40°C to 125°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			Bits
Integral Linearity Error	(Notes 5, 6)	●		±0.25	±1	LSB
Differential Linearity Error	(Note 6)	●		±0.25	±1	LSB
Transition Noise	(Note 7)			0.25		LSB_{RMS}
Offset Error	(Note 6)	●		1	±3.5	LSB
Gain Error	(Note 6)	●		0.1	±2	LSB
Total Unadjusted Error	(Note 6)	●		1.1	±3.5	LSB

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Voltage	S6 Package TS8 Package	● ●	–0.05 –0.05		V_{DD} + 0.05 V_{REF} + 0.05	V
I_{IN}	Analog Input Leakage Current	CONV = High	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions During Conversions			20 4		pF pF
V_{REF}	Reference Input Voltage	TS8 Package	●	1.4		V_{DD} + 0.05	V
I_{REF}	Reference Input Leakage Current	TS8 Package	●			±1	µA
C_{REF}	Reference Input Capacitance	TS8 Package			20		pF
t_{AP}	Sample-and-Hold Aperture Delay Time				1		ns
t_{JITTER}	Sample-and-Hold Aperture Delay Time Jitter				0.3		ns

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SINAD	Signal-to-(Noise + Distortion) Ratio	f_{IN} = 49kHz for LTC2360/LTC2361, f_{IN} = 100kHz for LTC2362			72		dB
SNR	Signal-to-Noise Ratio	f_{IN} = 49kHz for LTC2360/LTC2361, f_{IN} = 100kHz for LTC2362			73		dB
THD	Total Harmonic Distortion	f_{IN} = 49kHz for LTC2360/LTC2361, f_{IN} = 100kHz for LTC2362			–85		dB
SFDR	Spurious Free Dynamic Range	f_{IN} = 49kHz for LTC2360/LTC2361, f_{IN} = 100kHz for LTC2362			86		dB
IMD	Intermodulation Distortion	f_{IN1} = 97kHz, f_{IN2} = 100kHz for LTC2362 f_{IN1} = 47kHz, f_{IN2} = 49kHz for LTC2360/LTC2361			–75		dB
	Full-Power Bandwidth	at 3dB at 0.1dB			10 2		MHz MHz
	Full-Linear Bandwidth	SINAD ≥ 68dB			1		MHz

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	2.7V < V_{DD} ≤ 3.6V 2.35V ≤ V_{DD} ≤ 2.7V	● ●	2 1.7			V V
V_{IL}	Low Level Input Voltage	2.7V < V_{DD} ≤ 3.6V 2.35V ≤ V_{DD} ≤ 2.7V	● ●			0.8 0.7	V V
I_{IH}	High Level Input Current	V_{IN} = V_{DD}	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			–2.5	µA
C_{IN}	Digital Input Capacitance				2		pF
V_{OH}	High Level Output Voltage	V_{DD} = 2.35V to 3.6V, I_{SOURCE} = 200µA	●	V_{DD} – 0.2			V
V_{OL}	Low Level Output Voltage	V_{DD} = 2.35V to 3.6V, I_{SINK} = 200µA	●			0.2	V
I_{OZ}	Hi-Z Output Leakage	CONV = V_{DD}	●			±3	µA
C_{OZ}	Hi-Z Output Capacitance	CONV = V_{DD}			4		pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			10		mA

POWER REQUIREMENT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage		●	2.35	3.0	3.6	V
OV_{DD}	Digital Output Supply Voltage		●	1.0V		V_{DD}	V
I_{DD}	Supply Current						
	Operational Mode, LTC2362	f_{SMPL} = 500ksps	●		1.1	2	mA
	Operational Mode, LTC2361	f_{SMPL} = 250ksps	●		0.75	1.5	mA
	Operational Mode, LTC2360	f_{SMPL} = 100ksps	●		0.5	1	mA
	Sleep Mode	0°C to 70°C	●		0.1	2	µA
	Sleep Mode	–40°C to 85°C	●		0.1	2	µA
	Sleep Mode	–40°C to 125°C	●		0.1	5	µA
P_D	Power Dissipation						
	Operational Mode, LTC2362	f_{SMPL} = 500ksps	●		3.3	7.2	mW
	Operational Mode, LTC2361	f_{SMPL} = 250ksps	●		2.25	5.4	mW
	Operational Mode, LTC2360	f_{SMPL} = 100ksps	●		1.5	3.6	mW
	Sleep Mode	0°C to 70°C	●		0.3	7.2	µW
	Sleep Mode	–40°C to 85°C	●		0.3	7.2	µW
	Sleep Mode	–40°C to 125°C	●		0.3	18	µW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		LTC2360 MIN	LTC2360 TYP	LTC2360 MAX	LTC2361 MIN	LTC2361 TYP	LTC2361 MAX	LTC2362 MIN	LTC2362 TYP	LTC2362 MAX	UNITS
$f_{SMPL(MAX)}$	Maximum Sampling Frequency	(Notes 8, 9)	●	100			250			500			kHz
f_{SCK}	Shift Clock Frequency	(Notes 8, 9)	●			10			25			50	MHz
t_{SCK}	Shift Clock Period		●	100			40			20			ns
$t_{THROUGHPUT}$	Minimum Throughput Time, $t_{ACQ} + t_{CONV}$		●			10			4			2	µs
t_{ACQ}	Acquisition Time		●	2			1			0.5			µs
t_{CONV}	Conversion Time		●	8			3			1.5			µs
t_1	Minimum Positive CONV Pulse Width	(Note 8)	●	8			3			1.5			µs
t_2	SCK↑ Setup Time After CONV↓	(Note 8)	●	16			16			16			ns
t_3	SDO Enabled Time After CONV↓	(Notes 8, 9)	●			16			16			16	ns
t_4	SDO Data Valid Access Time After SCK↓	(Notes 8, 9, 10)	●			8			8			8	ns
t_5	SCK Low Time	(Note 11)	●	40%			40%			40%			t_{SCK}
t_6	SCK High Time	(Note 11)	●	40%			40%			40%			t_{SCK}
t_7	SDO Data Valid Hold Time After SCK↓	(Notes 8, 9, 10)	●	4			4			4			ns
t_8	SDO Into Hi-Z State Time After CONV↑	(Notes 8, 9)			6			6			6		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: When pins A_{IN} and V_{REF} are taken below GND or above V_{DD}, they will be clamped by internal diodes. These products can handle input currents greater than 100mA below GND or above V_{DD} without latch-up.

Note 4: V_{DD} = OV_{DD} = V_{REF} = 2.35V to 3.6V, f_{SMPL} = $f_{SMPL(MAX)}$ and f_{SCK} = $f_{SCK(MAX)}$ unless otherwise specified.

Note 5: Integral linearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 6: Linearity, offset and gain specifications apply for a single-ended A_{IN} input with respect to GND.

Note 7: Typical RMS noise at code transitions.

Note 8: Guaranteed by characterization. All input signals are specified with t_r = t_f = 2ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6V.

Note 9: All timing specifications given are with a 10pF capacitance load. With a capacitance load greater than this value, a digital buffer or latch must be used.

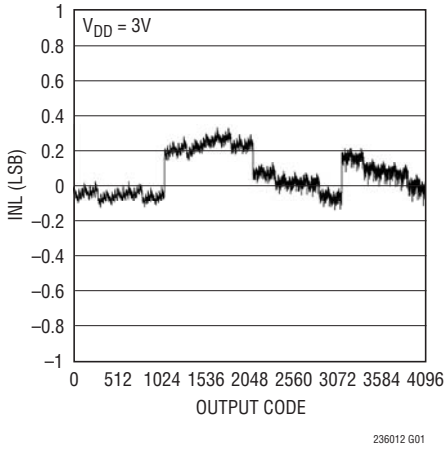
Note 10: The time required for the output to cross the V_{IH} or V_{IL} voltage.

Note 11: Guaranteed by design, not subject to test.

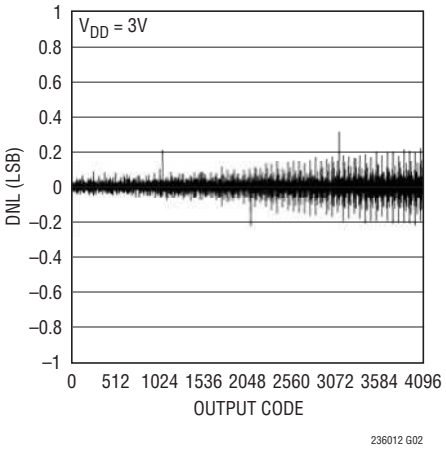
Note 12: High temperatures degrade operating lifetimes. Operating lifetime is derated at temperatures greater than 105°C.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, V_{DD} = OV_{DD} = V_{REF} (LTC2360, Note 4)

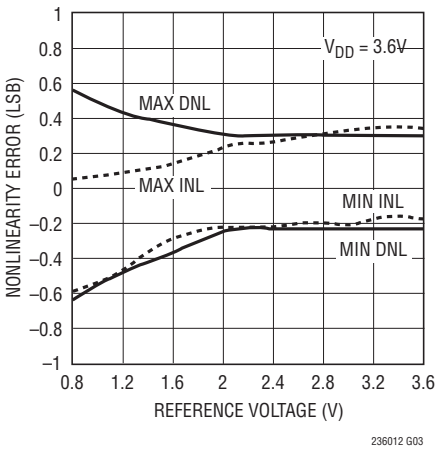
Integral Nonlinearity vs Output Code



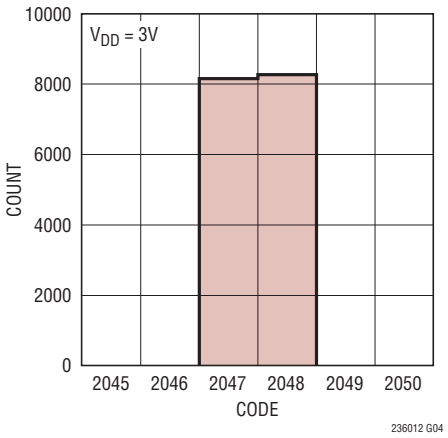
Differential Nonlinearity vs Output Code



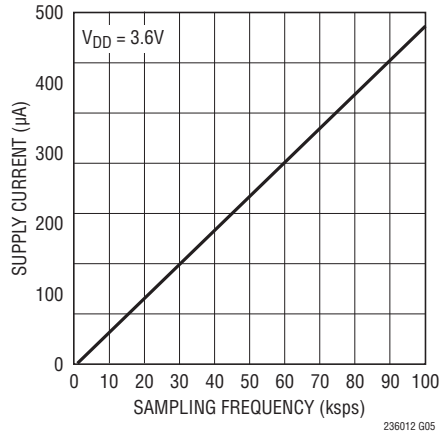
Integral and Differential Nonlinearity vs Reference Voltage (TS8 Package)



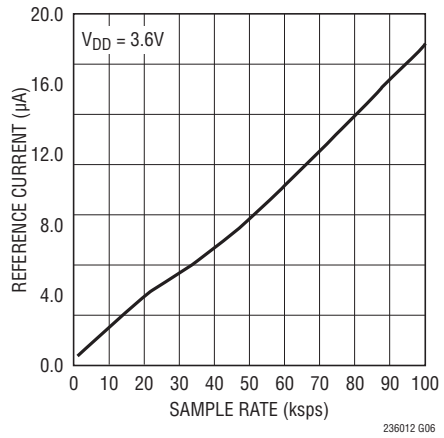
Histogram for 16384 Conversions



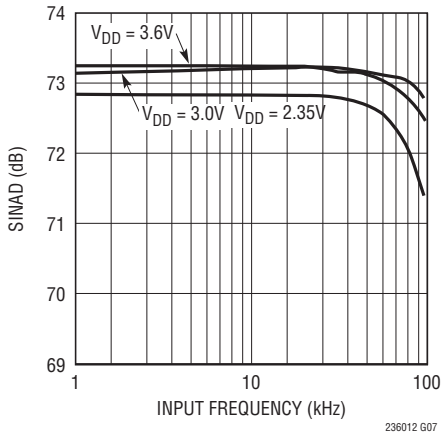
Supply Current vs Sample Rate



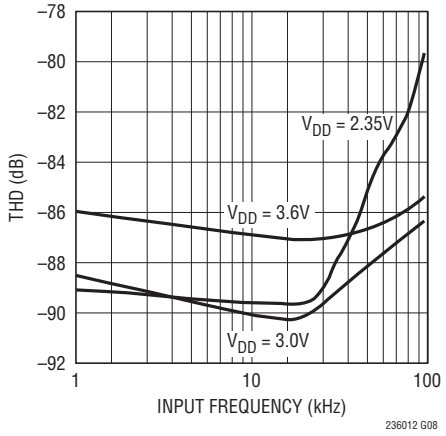
Reference Current vs Sample Rate (TS8 Package)



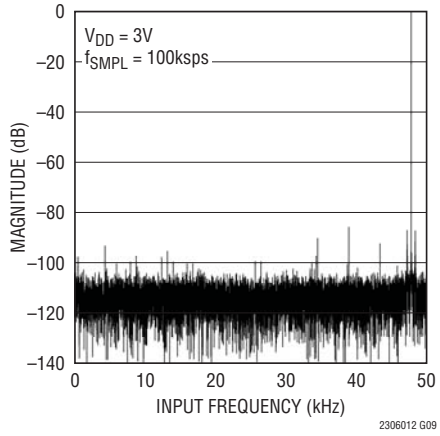
SINAD vs Input Frequency



THD vs Input Frequency

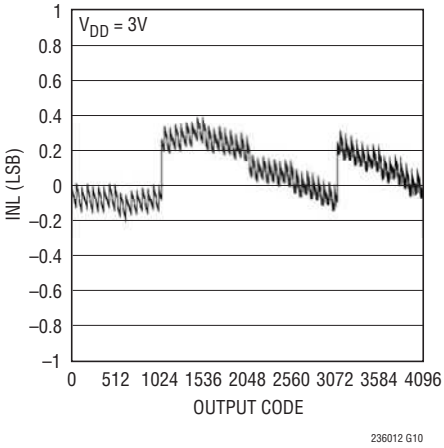


48kHz Sine Wave 8192 FFT Plot

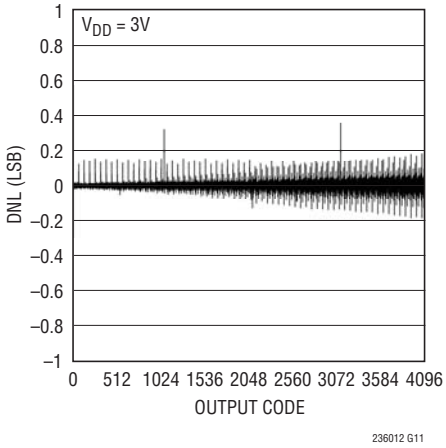


TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, $V_{DD} = OV_{DD} = V_{REF}$ (LTC2361, Note 4)

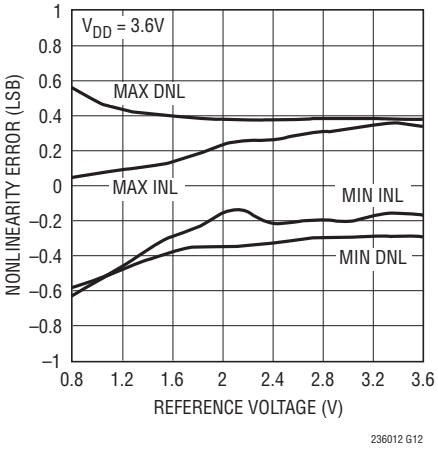
Integral Nonlinearity vs Output Code



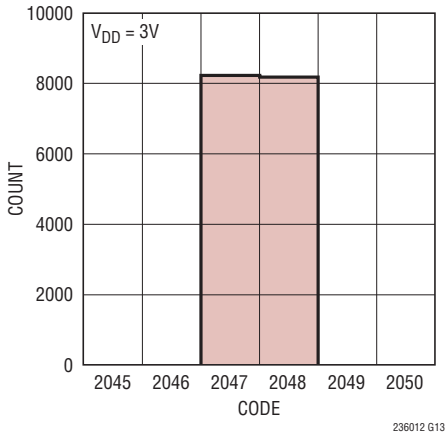
Differential Nonlinearity vs Output Code



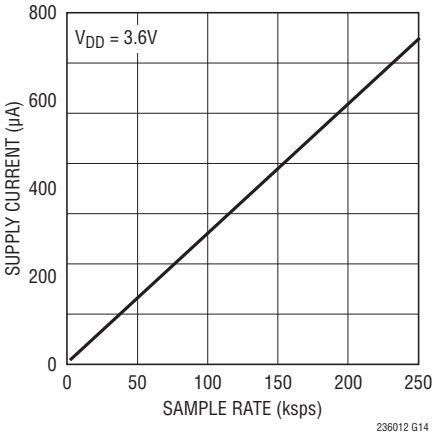
Integral and Differential Nonlinearity vs Reference Voltage (TS8 Package)



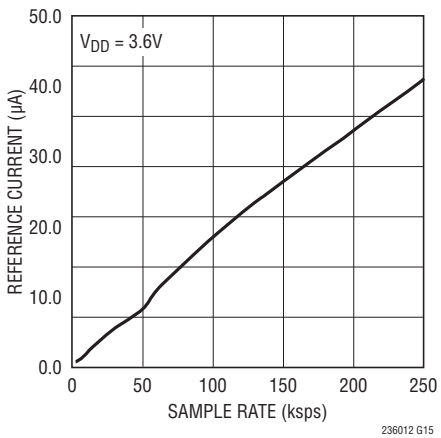
Histogram for 16384 Conversions



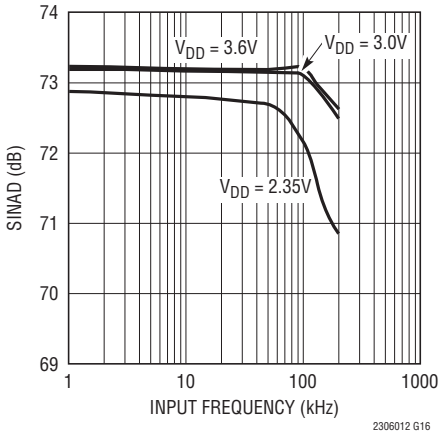
Supply Current vs Sample Rate



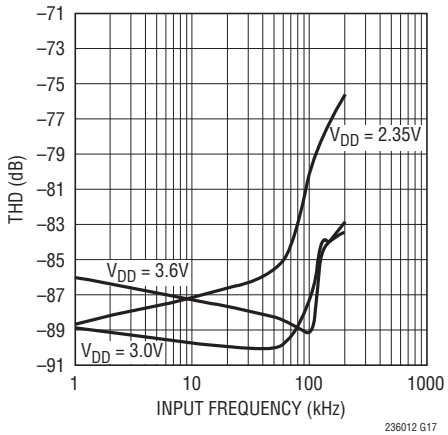
Reference Current vs Sample Rate (TS8 Package)



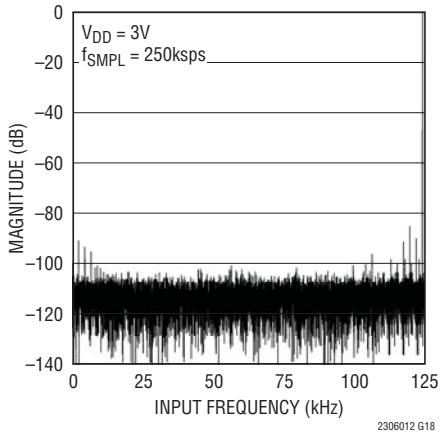
SINAD vs Input Frequency



THD vs Input Frequency

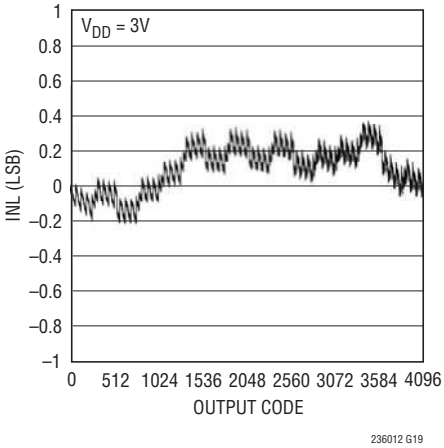


124kHz Sine Wave 8192 FFT Plot

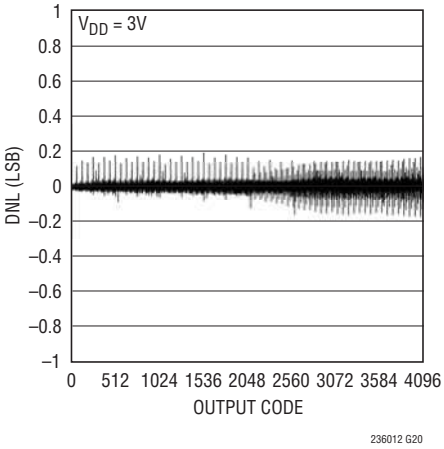


TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, $V_{DD} = OV_{DD} = V_{REF}$ (LTC2362, Note 4)

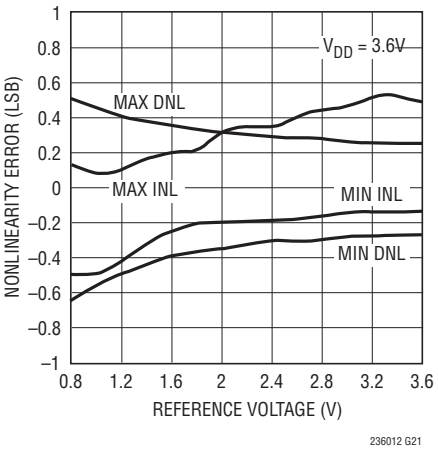
Integral Nonlinearity vs Output Code



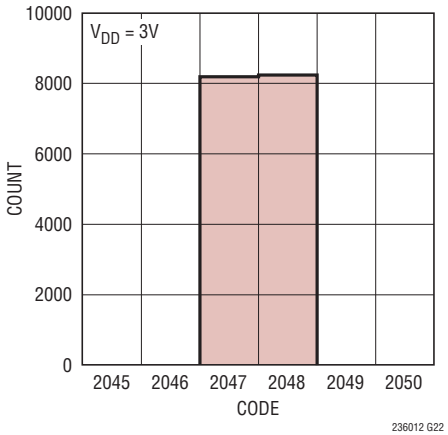
Differential Nonlinearity vs Output Code



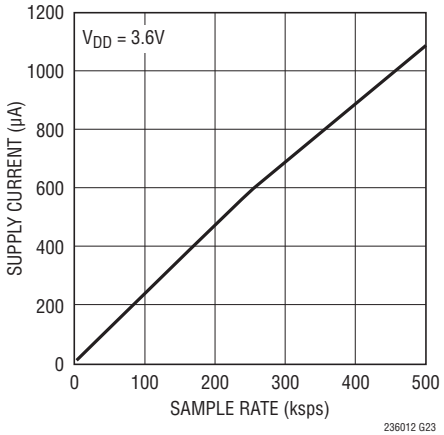
Integral and Differential Nonlinearity vs Reference Voltage (TS8 Package)



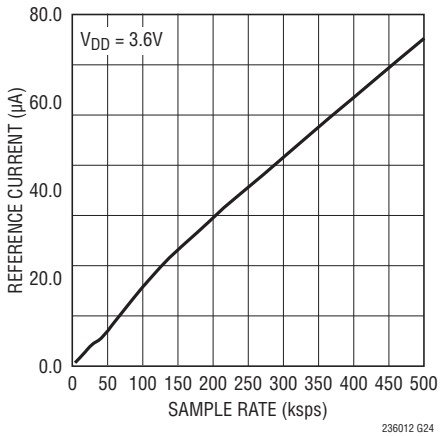
Histogram for 16384 Conversions



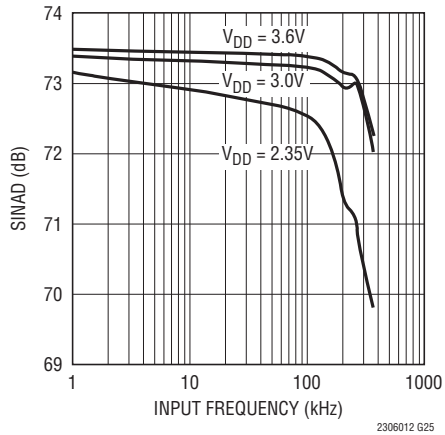
Supply Current vs Sample Rate



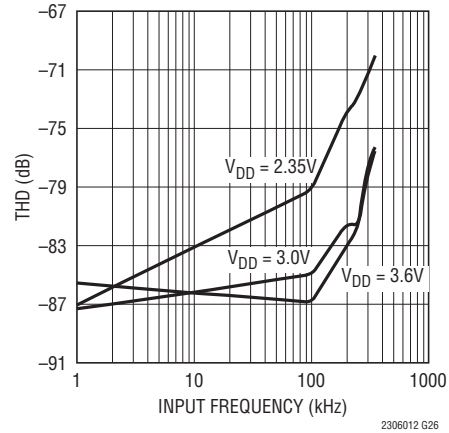
Reference Current vs Sample Rate (TS8 Package)



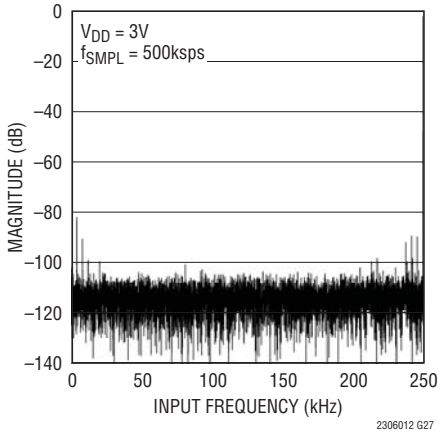
SINAD vs Input Frequency



THD vs Input Frequency



248kHz Sine Wave 8192 FFT Plot



PIN FUNCTIONS

S6 Package

V_{DD} (Pin 1): Positive Supply. The V_{DD} range is 2.35V to 3.6V. V_{DD} also defines the input span of the ADC, 0V to V_{DD}. Bypass to GND and to a solid ground plane with a 2.2µF ceramic capacitor (or 2.2µF tantalum in parallel with 0.1µF ceramic).

GND (Pin 2): Ground. The GND pin must be tied directly to a solid ground plane.

A_{IN} (Pin 3): Analog Input. A_{IN} is a single-ended input with respect to GND with a range from 0V to V_{DD}.

SCK (Pin 4): Shift Clock Input. The SCK serial clock synchronizes the serial data transfer. SDO data transitions on the falling edge of SCK.

SDO (Pin 5): Three-State Serial Data Output. The A/D conversion result is shifted out on SDO as a serial data stream with MSB first. The data stream consists of 12 bits of conversion data followed by trailing zeros.

CONV (Pin 6): Convert Input. This active high signal starts a conversion on the rising edge. The device automatically powers down after conversion. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

TS8 Package

V_{DD} (Pin 1): Positive Supply. The V_{DD} range is 2.35V to 3.6V. Bypass to GND and to a solid ground plane with a 2.2µF ceramic capacitor (or 2.2µF tantalum in parallel with 0.1µF ceramic).

V_{REF} (Pin 2): Reference Input. V_{REF} defines the input span of the ADC, 0V to V_{REF}. The V_{REF} range is 1.4V to V_{DD}. Bypass to GND and to a solid ground plane with a 2.2µF ceramic capacitor (or 2.2µF tantalum in parallel with 0.1µF ceramic).

GND (Pin 3): Ground. The GND pin must be tied directly to a solid ground plane.

A_{IN} (Pin 4): Analog Input. A_{IN} is a single-ended input with respect to GND with a range from 0V to V_{REF}.

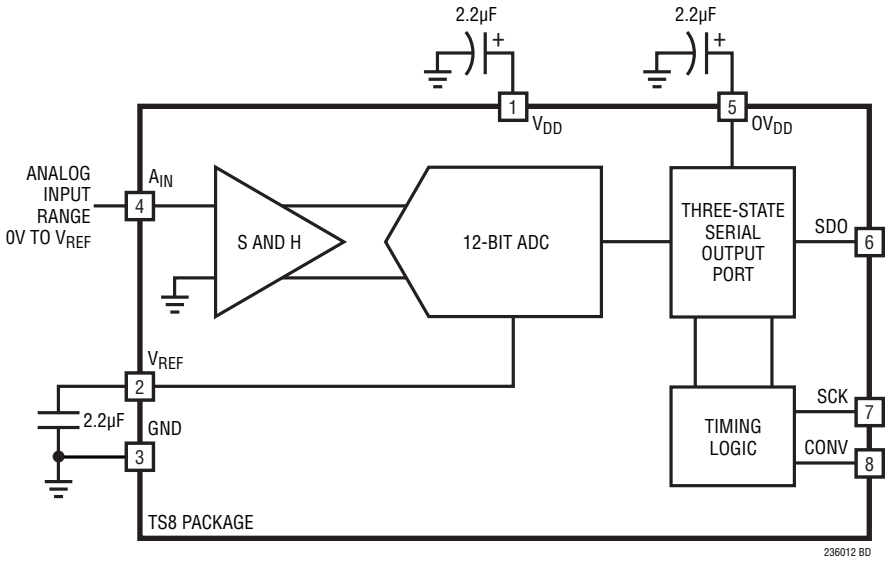
OV_{DD} (Pin 5): Output Driver Supply for SDO. The OV_{DD} range is 1V to V_{DD}. Bypass to GND and to a solid ground plane with a 2.2µF ceramic capacitor (or 2.2µF tantalum in parallel with 0.1µF ceramic). OV_{DD} can be driven separately from V_{DD} and OV_{DD} can be higher than V_{DD}.

SDO (Pin 6): Three-State Serial Data Output. The A/D conversion result is shifted out on SDO as a serial data stream with MSB first. The data stream consists of 12 bits of conversion data followed by trailing zeros.

SCK (Pin 7): Shift Clock Input. The SCK serial clock synchronizes the serial data transfer. SDO data transitions on the falling edge of SCK.

CONV (Pin 8): Convert Input. This active high signal starts a conversion on the rising edge. The device automatically powers down after conversion. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

BLOCK DIAGRAM



TIMING DIAGRAMS

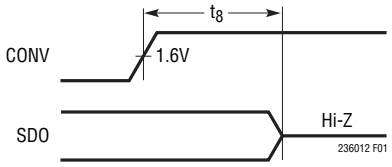


Figure 1. SDO Into Hi-Z State After CONV Rising Edge

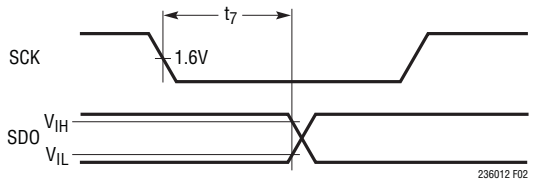


Figure 2. SDO Data Valid Hold Time After SCK Falling Edge

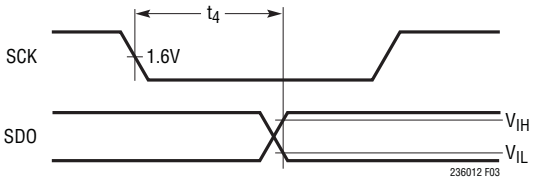


Figure 3. SDO Data Valid Acess Time After SCK Falling Edge

APPLICATIONS INFORMATION

DC PERFORMANCE

The noise of an ADC can be evaluated in two ways: signal-to-noise ratio (SNR) in the frequency domain and histogram in the time domain. The LTC2360/LTC2361/LTC2362 excel in both. Figure 5 demonstrates that the LTC2360/LTC2361/LTC2362 have an SNR of over 73dB. The noise in the time domain histogram is the transition noise associated with a 12-bit resolution ADC which can be measured with a fixed DC signal applied to the input of the ADC. The resulting output codes are collected over a large number of conversions. The shape of the distribution of codes will give an indication of the magnitude of the transition noise. In Figure 4, the distribution of output codes is shown for a DC input that has been digitized 16384 times. The distribution is Gaussian and the RMS code transition is about 0.32LSB. This corresponds to a noise level of 73dB relative to a full scale of 3V.

DYNAMIC PERFORMANCE

The LTC2360/LTC2361/LTC2362 have excellent high speed sampling capability. Fast fourier transform (FFT) test techniques are used to test the ADCs' frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADCs' spectral content can be examined for frequencies outside the fundamental. Figures 5 and 6 show typical LTC2361 and LTC2362 FFT plots respectively.

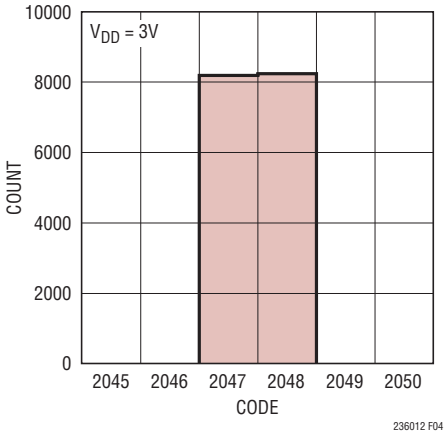


Figure 4. Histogram for 16384 Conversions

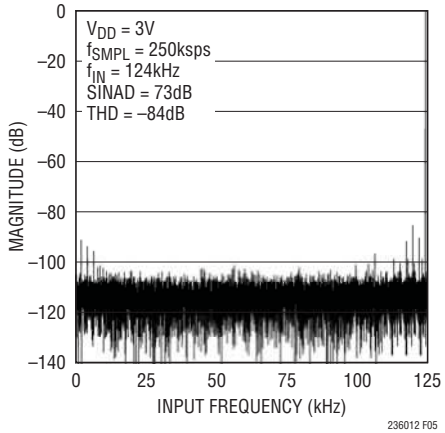


Figure 5. LTC2361 FFT Plot

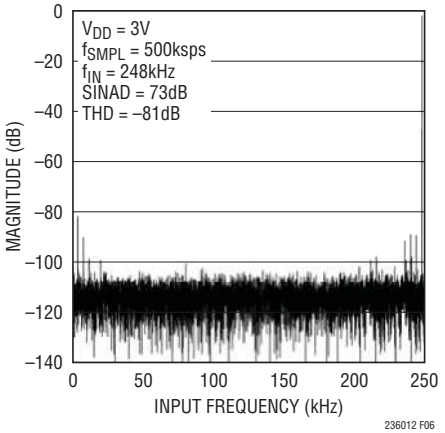


Figure 6. LTC2362 FFT Plot

APPLICATIONS INFORMATION

Signal-to-Noise plus Distortion Ratio

The signal-to-noise plus distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from above DC and below half the sampling frequency. Figure 6 shows a typical FFT with a 500kHz sampling rate and a 248kHz input. The dynamic performance is excellent for input frequencies up to and beyond the Nyquist frequency of 250kHz.

Effective Number of Bits

The effective number of bits (ENOB) is a measurement of the resolution of an ADC and is directly related to SINAD by the equation:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

where ENOB is the effective number of bits of resolution and SINAD is expressed in dB. At the maximum sampling rate of 500kHz, the LTC2362 maintains ENOB above 11 bits up to the Nyquist input frequency of 250kHz (refer to Figure 7).

Total Harmonic Distortion

The total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots V_n^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_n are the amplitudes of the second through nth harmonics. THD vs Input Frequency is shown in Figure 8. The LTC2362 has excellent distortion performance up to the Nyquist frequency and beyond.

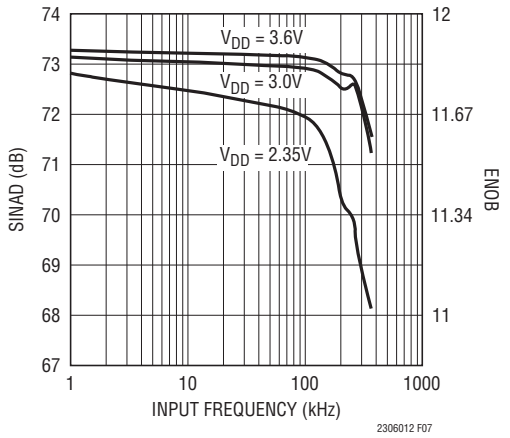


Figure 7. LTC2362 ENOB and SINAD vs Input Frequency

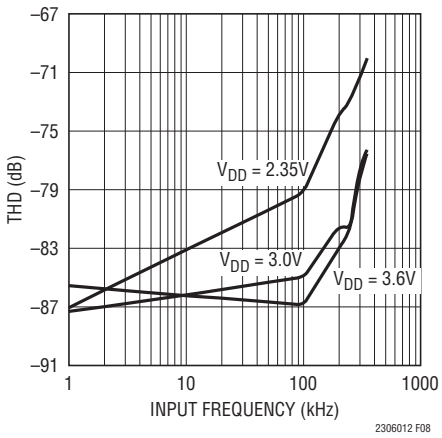


Figure 8. LTC2362 THD vs Input Frequency

APPLICATIONS INFORMATION

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermoduation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies f_a and f_b are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of $mf_a \pm nf_b$, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include $(f_a \pm f_b)$. If the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd order IMD products can be expressed by the following formula:

$$IMD\left(f_a \pm f_b\right) = 20\log\frac{\text{Amplitude at } \left(f_a \pm f_b\right)}{\text{Amplitude at } f_a}$$

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full-scale input signal.

Full-Power and Full-Linear Bandwidth

The full-power bandwidth is that input frequency at which the amplitude of reconstructed fundamental is reduced by 3dB for full-scale input signal.

The full-linear bandwidth is the input frequency at which the SINAD has dropped to 68dB (11 effective bits). The LTC2362 has been designed to optimize input bandwidth, allowing the ADC to undersample input signals with frequencies above the converter's Nyquist frequency. The noise floor stays very low at high frequencies; SINAD becomes dominated by distortion at frequencies far beyond Nyquist.

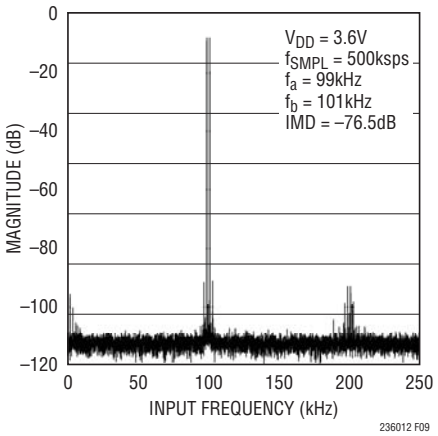


Figure 9. LTC2362 Intermodulation Distortion Plot

APPLICATIONS INFORMATION

OVERVIEW

The LTC2360/LTC2361/LTC2362 use a successive approximation algorithm and internal sample-and-hold circuit to convert an analog signal to a 12-bit serial output. All devices operate from a single 2.35V to 3.6V supply. The conversion time of the devices is controlled by an internal oscillator, which allows the LTC2360/LTC2361/LTC2362 to sample at a rate of 100ksps, 250ksps and 500ksps respectively.

The LTC2360/LTC2361/LTC2362 contain a 12-bit, switched-capacitor ADC, a sample-and-hold, a serial interface (see Block Diagram) and are available in tiny 6- or 8-lead TSOT-23 packages.

The S6 package of the LTC2360/LTC2361/LTC2362 uses V_{DD} as the reference and has an analog input range of 0V to V_{DD}. The ADC samples the analog input with respect to GND and outputs the result through the serial interface.

The TS8 package provides two additional pins: a reference pin, V_{REF}, and an output supply pin, OV_{DD}. The ADC can operate with reduced spans down to 1.4V and achieve 342µV resolution. OV_{DD} controls the output swing of the digital output pin, SDO, and allows the device to communicate with 1.8V, 2.5V or 3V digital systems.

SERIAL INTERFACE

The LTC2360/LTC2361/LTC2362 communicate with microcontrollers, DSPs and other external circuitry via a 3-wire interface. Figure 10 shows the operating sequence of the serial interface.

Data Transfer

A rising CONV edge starts a conversion and disables SDO. After the conversion, the ADC automatically goes into sleep mode, drawing only leakage current.

CONV going low enables SDO and clocks out the MSB bit, B11. SCK then synchronizes the data transfer with each bit being transmitted on the falling SCK edge and can be captured on the rising SCK edge. After completing the data transfer, if further SCK clocks are applied with CONV low, SDO will output zeros indefinitely (see Figure 10). For example, 16-clocks at SCK will produce the 12-bit data and four trailing zeros on SDO.

SLEEP MODE

The LTC2360/LTC2361/LTC2362 enter sleep mode to save power after each conversion if CONV remains high. In sleep mode, all bias currents are shut down and only leakage currents remain (about 0.1µA). The sample-and-hold is in hold mode while the ADC is in sleep mode. The ADC returns to sample mode after the falling edge of CONV during power-up (see Figure 10).

Exiting Sleep Mode and Power-Up Time

By taking CONV low, the ADC powers up and acquires an input signal completely after the aquisition time (t_{ACQ}). After t_{ACQ}, the ADC can perform a conversion as described in the Serial Interface section (see Figure 10).

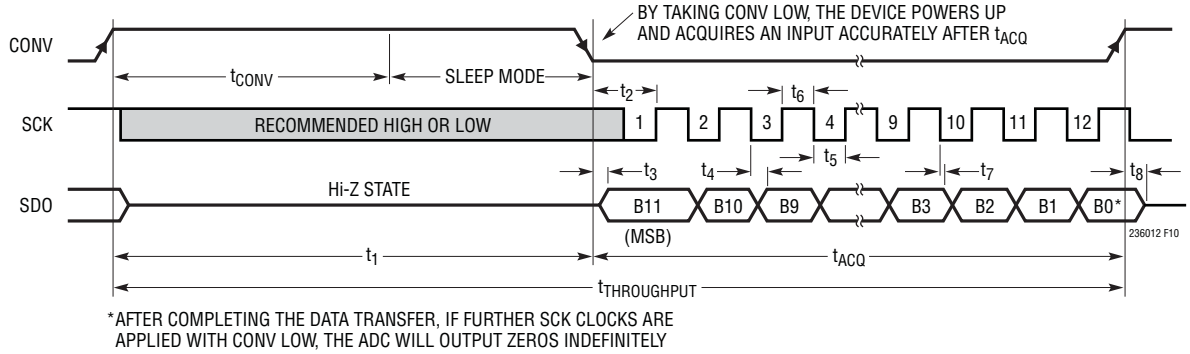


Figure 10. LTC2360/LTC2361/LTC2362 Serial Interface Timing Diagram

APPLICATIONS INFORMATION

ACHIEVING MICROPOWER PERFORMANCE

With typical operating currents of 0.5mA, 0.75mA and 1.1mA for the LTC2360/LTC2361/LTC2362 and automatically entering sleep mode right after a conversion, these devices achieve extremely low power consumption over a wide range of sample rates (see Figure 11). The sleep mode allows the supply current to drop with reduced sample rate. Several things must be taken into account to achieve such low power consumption.

Minimize Power Consumption in Sleep Mode

The LTC2360/LTC2361/LTC2362 enter sleep mode after each conversion if CONV remains high and draw only leakage current (see Figure 10). If the CONV input is not running rail-to-rail, the input logic buffer will draw current. This current may be large compared to the typical supply current. To obtain the lowest supply current, bring the CONV pin to GND when it is low and to V_{DD} when it is high.

After the conversion with CONV staying high, the converter is in sleep mode and draws only leakage current. The status of the SCK input has no effect on supply current during this time. For the best performance, hold SCK either high or low while the ADC is converting.

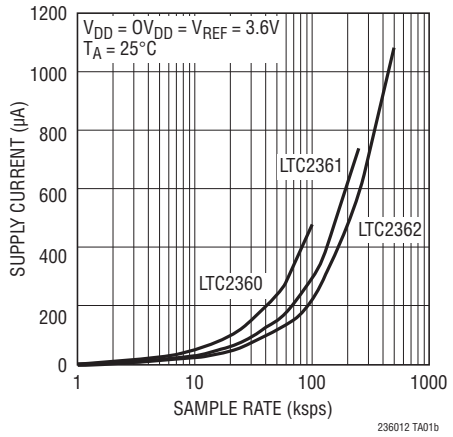


Figure 11. Supply Current vs Sample Rate

Minimize the Device Active Time

In systems that have significant time between conversions, the ADC draws a minimal amount of power. Figures 12 and 13 show two ways to minimize the amount of time the ADC draws power. In Figure 12, the ADC draws power during t_{ACQ} and t_{CONV} and is in sleep mode for the rest of the time. The conversion results are available at the next CONV falling edge. In Figure 13, the ADC draws twice the power than that in Figure 12, but the conversion results are available during t_{DATA}. The user can use the fastest SCK available in the system to shorten data transfer time, t_{DATA} as long as t_4 and t_7 are not violated.

SDO Loading

Capacitive loading on the digital output can increase power consumption. A 100pF capacitor on the SDO pin can add more than 50µA to the supply current at a 200kHz clock frequency. An extra 50µA or so of current goes into charging and discharging the load capacitor. The same goes for digital lines driven at a high frequency by any logic. The C • V • f currents must be evaluated with the troublesome ones minimized.

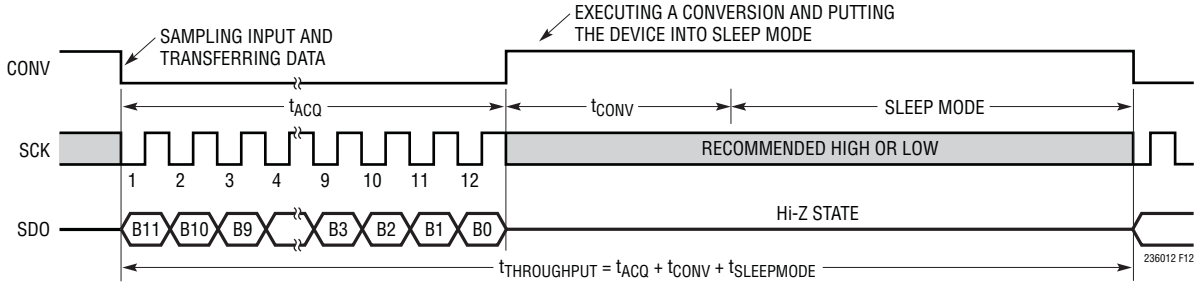


Figure 12. Minimize the Time When the Device Draws Power, While the Conversion Results are Available After the Device Wakes Up

APPLICATIONS INFORMATION

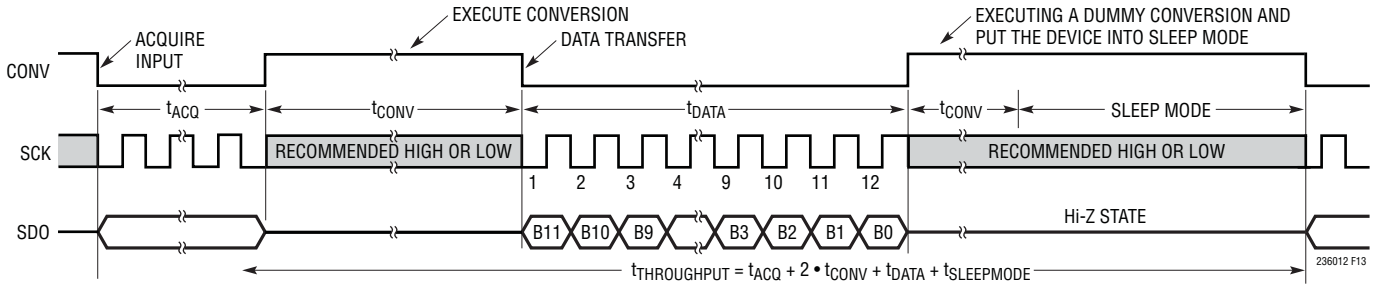


Figure 13. Minimize the Time When the Device Draws Power, While the Conversion Results are Available Right After Conversion

SINGLE-ENDED ANALOG INPUT

Driving the Analog Input

The analog input of the LTC2360/LTC2361/LTC2362 is easy to drive. The input draws only one small current spike while charging the sample-and-hold capacitor with the ADC going into track mode. During the conversion, the analog input draws only a small leakage current. If the source impedance of the driving circuit is low, then the input of the LTC2360/LTC2361/LTC2362 can be driven directly. As source impedance increases, so will acquisition time. For minimum acquisition time with high source impedance, a buffer amplifier should be used. The main requirement is that the amplifier driving the analog input must settle after the small current spike before the next conversion starts (settling time must be less than t_{ACQ} for full throughput rate). While choosing an input amplifier, also keep in mind the amount of noise and harmonic distortion the amplifier contributes.

Choosing an Input Amplifier

Choosing an input amplifier is easy if a few requirements are taken into consideration. First, to limit the magnitude of the voltage spike seen by the amplifier from charging the sampling capacitor, choose an amplifier that has a low output impedance (<100Ω) at the closed-loop bandwidth frequency. For example, if an amplifier is used in a gain of 1 and has a unity-gain bandwidth of 10MHz, then the output impedance at 10MHz must be less than 100Ω. The second requirement is that the closed-loop bandwidth must be greater than 8MHz to ensure adequate small-signal settling for full throughput rate. If slower op amps are used, more time for settling can be provided by increasing the time between conversions. The best choice for an op amp to drive the LTC2360/LTC2361/LTC2362 will depend on the application. Generally, applications fall into two categories: AC applications where dynamic specifications are most critical and time domain applications where DC accuracy and settling time are most critical. The following list is a summary of the op amps that are suitable for driving the LTC2360/LTC2361/LTC2362. (More detailed information is available on the Linear Technology website at www.linear.com.)

LTC1566-1: Low Noise 2.3MHz Continuous Time Low-pass Filter.

LT®1630: Dual 30MHz Rail-to-Rail Voltage FB Amplifier. 2.7V to ±15V supplies. Very high A_{VOL}, 500μV offset and 520ns settling to 0.5LSB for a 4V swing. THD and noise are –93dB to 40kHz and below 1LSB to 320kHz (A_V = 1, $2V_{P-P}$ into 1k, V_S = 5V), making the part excellent for AC applications (to 1/3 Nyquist) where rail-to-rail performance is desired. Quad version is available as LT1631.

LTC6241: Dual 18MHz, Low Noise, Rail-to-Rail, CMOS Voltage FB Amplifier. 2.8V to 6V supplies. Very high A_{VOL} and 125μV offset. It is suitable for applications with a single 5V supply. Quad version is available as LTC6242.

LT1797: Unity-Gain Stable 10MHz, Rail-to-Rail Voltage Feedback Amplifier.

LT1801: 180MHz GBWP, –75dBc at 500kHz, 2mA/Amplifier, 8.5nV/√Hz.

LT6203: 100MHz GBWP, –80dBc Distortion at 1MHz, Unity-Gain Stable, R-R In and Out, 3mA/Amplifier, 1.9nV/√Hz.

APPLICATIONS INFORMATION

Input Filtering and Source Impedance

The noise and the distortion of the input amplifier and other circuitry must be considered since they will add to the LTC2360/LTC2361/LTC2362 noise and distortion. The small-signal bandwidth of the sample-and-hold circuit is 10MHz. Any noise or distortion products that are present at the analog inputs will be summed over this entire bandwidth. Noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for many applications. For example, Figure 14 shows a 220pF capacitor from A_{IN} to ground and a 51Ω source resistor to limit the input bandwidth to 10MHz. The 220pF capacitor also acts as a charge reservoir for the input sample-and-hold and isolates the ADC input from sampling-glitch sensitive circuitry. High quality capacitors and resistors should be used since these components can add distortion. NPO and silvermica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems. When high amplitude unwanted signals are close in frequency to the desired signal frequency, a multiple pole filter is required. High external source resistance, combined with the 20pF of input capacitance, will reduce the rated 10MHz bandwidth and increase acquisition time beyond 500ns.

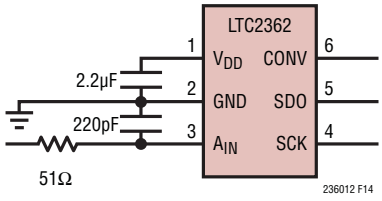


Figure 14. RC Input Filter

Reference Input

On the TS8 package of the LTC2360/LTC2361/LTC2362, the voltage on the V_{REF} pin defines the full-scale range of the ADC. The reference voltage can range from V_{DD} down to 1.4V.

Input Range

The analog input of the LTC2360/LTC2361/LTC2362 is driven single-ended with respect to GND from a single supply. The input may swing up to V_{DD} for the S6 package and to V_{REF} for the TS8 package. The 0V to 2.5V range is also ideally suited for single-ended input use with V_{DD} or V_{REF} = 2.5V for single supply applications. If the difference between the A_{IN} input and GND exceeds V_{DD} for the S6 package or V_{REF} for the TS8 package, the output code will stay fixed at all ones, and if this difference goes below 0V, the output code will stay fixed at all zeros.

Figure 15 shows the ideal input/output characteristics for the LTC2360/LTC2361/LTC2362. The code transitions occur midway between successive integer LSB values (i.e., 0.5LSB, 1.5LSB, 2.5LSB, …, FS – 1.5LSB). The output code is straight binary with 1LSB = V_{DD}/4096 for the S6 package and 1LSB = V_{REF}/4096 for the TS8 package.

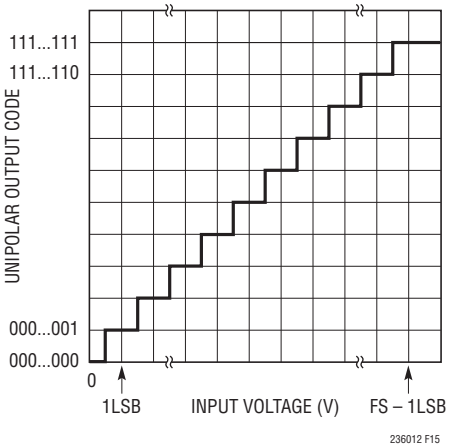


Figure 15. Transfer Characteristics

APPLICATIONS INFORMATION

BOARD LAYOUT AND BYPASSING

Wire wrap boards are not recommended for high resolution and/or high speed A/D converters. To obtain the best performance from the LTC2360/LTC2361/LTC2362, a printed circuit board with ground plane is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC. The analog input should be screened by the ground plane.

High quality tantalum and ceramic bypass capacitors should be used at the V_{DD} pin as shown in the Block Diagram on the first page of this data sheet. For optimum performance, a 2.2µF surface mount AVX capacitor with a 0.1µF ceramic is recommended for the V_{DD} and V_{REF} pins. Alternatively, 2.2µF ceramic chip capacitors such as Murata GRM235Y5V106Z016 may be used. The capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

Figure 16 shows the recommended system ground connections. All analog circuitry grounds should be terminated at the LTC2360/LTC2361/LTC2362. The ground return from the LTC2360/LTC2361/LTC2362 to the power supply should be low impedance for noise free operation. Digital circuitry grounds must be connected to the digital supply common.

In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in the conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a wait state during conversion or by using three-state buffers to isolate the ADC data bus.

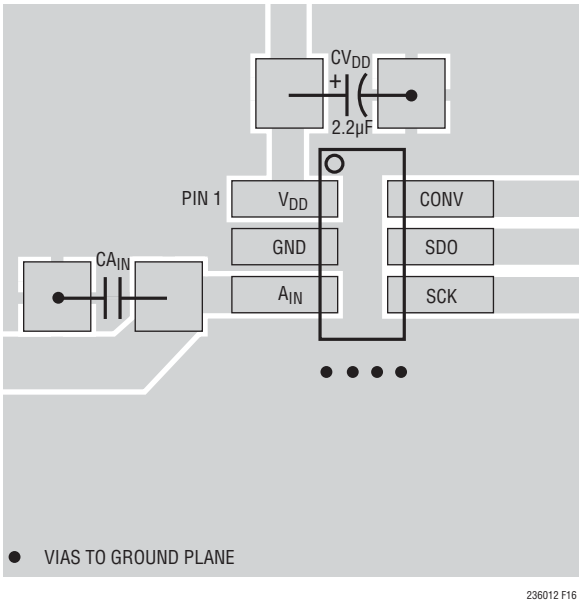
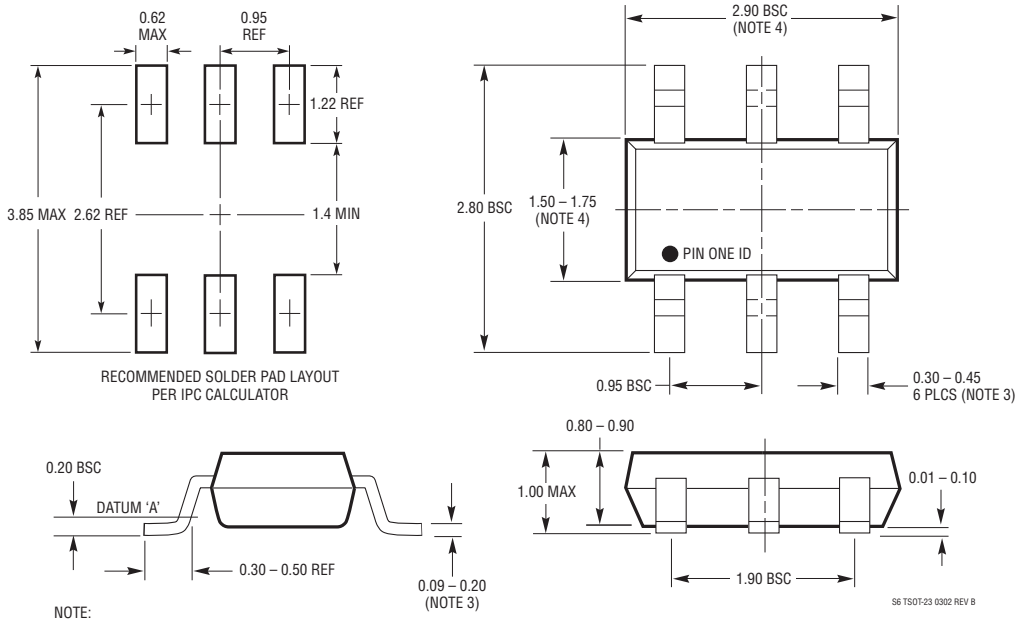


Figure 16. Power Supply Ground Practice

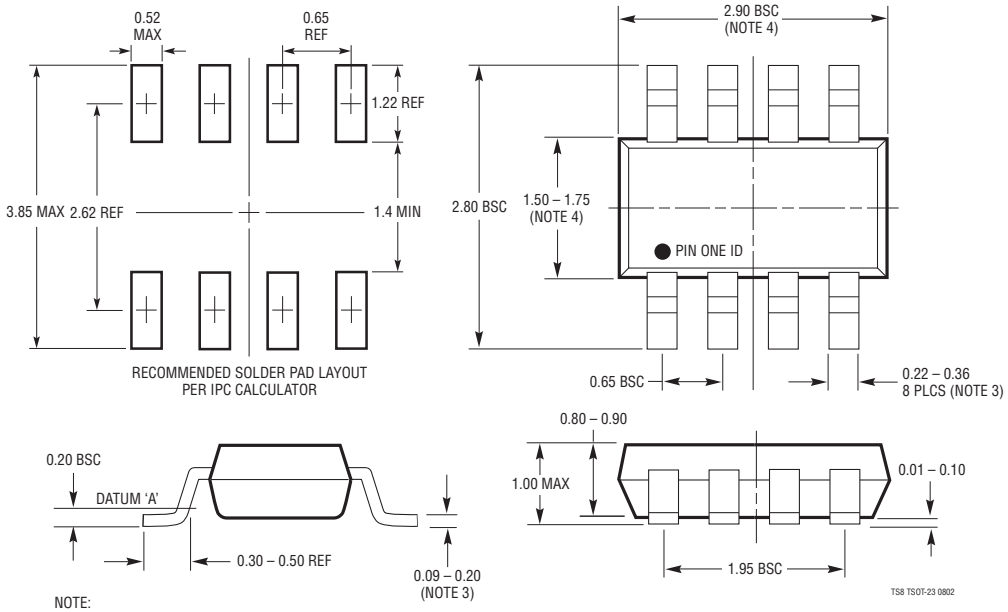
PACKAGE DESCRIPTION

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637)

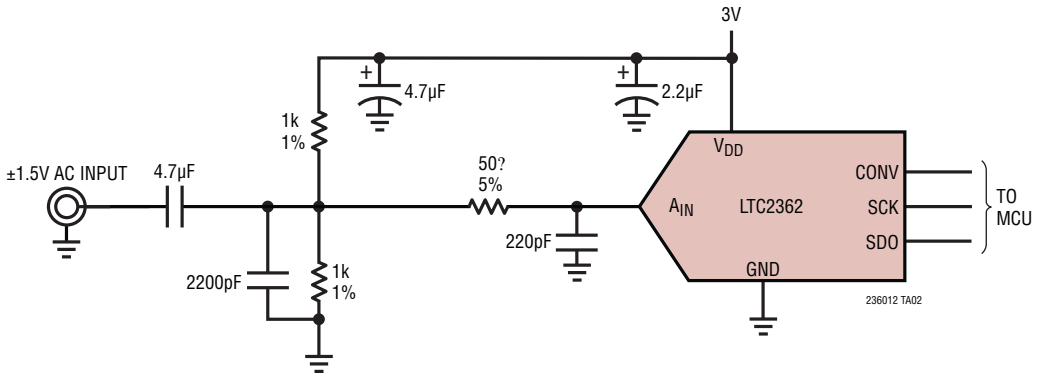


NOTE:
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Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Recommended AC Test Circuitry for the LTC2362



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADCs		
LTC1403/LTC1403A	12-/14-Bit, 2.8Msps Serial Sampling ADC	3V, Differential Input, 12mW, MSOP Package
LTC1407/LTC1407A	12-/14-Bit, 3Msps Simultaneous Sampling ADC	3V, 2-Channel Differential, 14mW, MSOP Package
LTC1860	12-Bit, 250ksps Serial ADC	5V Supply, 1-Channel, 4.3mW, MSOP-8 Package
LTC1860L	12-Bit, 150ksps Serial ADC	3V Supply, 1-Channel, 1.3mW, MSOP-8 Package
LTC1861	12-Bit, 250ksps Serial ADC	5V Supply, 2-Channel, 4.3mW, MSOP-8 Package
LTC1861L	12-Bit, 150ksps Serial ADC	3V Supply, 2-Channel, 1.3mW, MSOP-8 Package
LTC1863	12-Bit, 200ksps Serial ADC 8-Channel ADC	5V Supply, 6.5mW, SSOP-16 Package, Pin Compatible to LTC1863L, LTC1867
LTC1863L	12-Bit, 250ksps Serial ADC 8-Channel ADC	5V Supply, 2.2mW, SSOP-16 Package, Pin Compatible to LTC1863, LTC1867L
LTC1864/LTC1865	16-Bit, 250ksps Serial ADC	5V Supply, 1 and 2 Channel, 4.3mW, MSOP Package
LTC1867	16-Bit, 200ksps Serial ADC 8-Channel ADC	5V Supply, 6.5mW, SSOP-16 Package, Pin Compatible to LTC1863, LTC1867L
LTC1867L	16-Bit, 175ksps Serial ADC 8-Channel ADC	3V Supply, 2.2mW, SSOP-16 Package, Pin Compatible to LTC1863L, LTC1867
LTC2355/LTC2356	12-/14-Bit, 3.5Msps Serial ADCs	3.3V Supply, Differential Input, 18mW, MSOP Package
LTC2365/LTC2366	12-Bit, 1/3 Msps Serial ADCs in TSOT23	2.35V to 3.6V Supply, Pin and Software Compatible to LTC2360/LTC2361/LTC2362
DACs		
LTC1592	16-Bit, Serial SoftSpan™ I_{OUT} DAC	±1LSB INL/DNL, Software Selectable Spans
LTC1666/LTC1667/LTC1668	12-/14-/16-Bit, 50Msps DACs	87dB SFDR, 20ns Settling Time
LTC2630	12-/10-/8-Bit Single V_{OUT} DACs	SC70 6-Pin Package, Internal Reference, ±1LSB INL (12 Bits)
References		
LT1460-2.5	Micropower Series Voltage Reference	0.1% Initial Accuracy, 10ppm Drift
LT1461-2.5	Precision Voltage Reference	0.05% Initial Accuracy, 3ppm Drift
LT1790-2.5	Micropower Series Reference in SOT-23	0.05% Initial Accuracy, 10ppm Drift
LT6660	Ultra-Tiny Micropower Series Reference	2mm × 2mm DFN Package, 0.2% Initial Accuracy, 10ppm Drift

SoftSpan is a trademark of Linear Technology Corporation.

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