18-Bit, 1Msps, 8-Channel SAR ADC with 100dB SNR

FEATURES

- **1Msps Throughput Rate**
- **18-Bit Resolution with No Missing Codes**
- **8-Channel Multiplexer with Selectable Input Range**
  - **Fully Differential (±4.096V)**
  - **Pseudo-Differential Unipolar (0V to 4.096V)**
  - **Pseudo-Differential Bipolar (±2.048V)**
- **INL: ±2.75LSB (Maximum)**
- **SNR: 100dB (Fully Differential)/95dB (Pseudo-Differential) (Typical) at f_{IN} = 1kHz**
- **THD: –110dB (Typical) at f_{IN} = 1kHz**
- Programmable Sequencer
- Selectable Digital Gain Compression
- Single 5V Supply with 1.8V to 5V I/O Voltages
- SPI-Compatible Serial I/O
- Onboard 2.048V Reference and Reference Buffer
- No Pipeline Delay, No Cycle Latency
- Power Dissipation 40mW (Typical)
- Guaranteed Operation to 125°C
- 32-Lead 5mm × 5mm QFN Package

APPLICATIONS

- Programmable Logic Controllers
- Industrial Process Control
- High Speed Data Acquisition
- Portable or Compact Instrumentation
- ATE

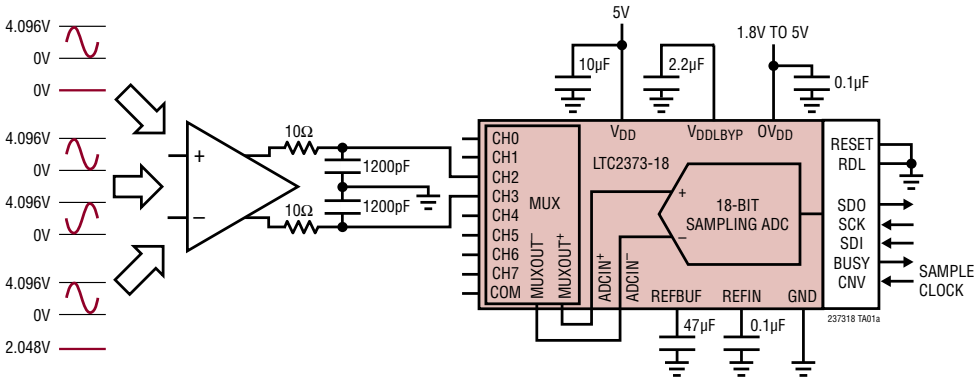
DESCRIPTION

The LTC®2373-18 is a low noise, high speed, 8-channel 18-bit successive approximation register (SAR) ADC. Operating from a single 5V supply, the LTC2373-18 has a highly configurable, low crosstalk 8-channel input multiplexer, supporting fully differential, pseudo-differential unipolar and pseudo-differential bipolar analog input ranges. The LTC2373-18 achieves ±2.75LSB INL (maximum) in all input ranges, no missing codes at 18-bits and 100dB (fully differential)/ 95dB (pseudo-differential) SNR (typical).

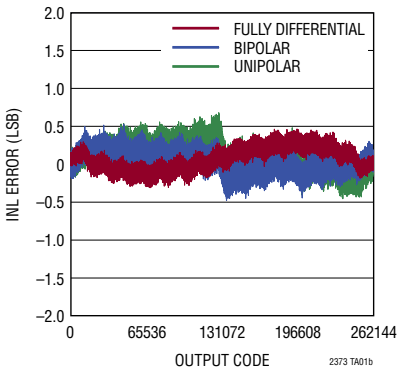
The LTC2373-18 has an onboard low drift (20ppm/°C max) 2.048V temperature-compensated reference and a single-shot capable reference buffer. The LTC2373-18 also has a high speed SPI-compatible serial interface that supports 1.8V, 2.5V, 3.3V and 5V logic through which a sequencer with a depth of 16 may be programmed. An internal oscillator sets the conversion time, easing external timing considerations. The LTC2373-18 dissipates only 40mW and automatically naps between conversions, leading to reduced power dissipation that scales with the sampling rate. A sleep mode is also provided to reduce the power consumption of the LTC2373-18 to 300µW for further power savings during inactive periods.

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TYPICAL APPLICATION



Integral Nonlinearity vs Output Code

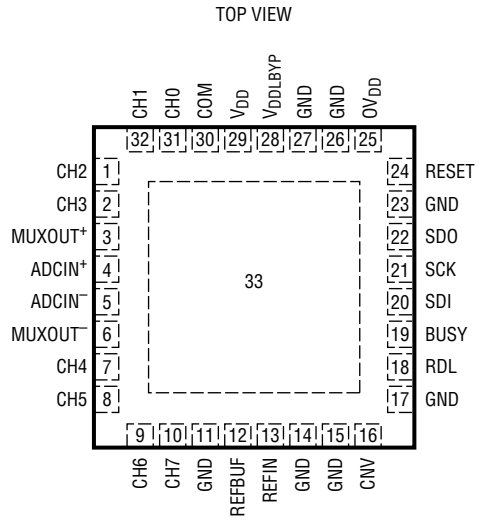


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD}) 6V
Supply Voltage (OV_{DD}) 6V
Analog Input Voltage (Note 3)
CH0 to CH7, COM ..... (GND – 0.3V) to (V_{DD} + 0.3V)
REFBUF ..... (GND – 0.3V) to (V_{DD} + 0.3V)
REFIN 2.8V
Digital Input Voltage
(Note 3) ..... (GND –0.3V) to (OV_{DD} + 0.3V)
Digital Output Voltage
(Note 3) ..... (GND –0.3V) to (OV_{DD} + 0.3V)
Power Dissipation 500mW
Operating Temperature Range
LTC2373C ..... 0°C to 70°C
LTC2373I ..... –40°C to 85°C
LTC2373H ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 44°C/W
EXPOSED PAD IS GND (PIN 33) MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2373CUH-18#PBF	LTC2373CUH-18#TRPBF	237318	32-Lead (5mm × 5mm) Plastic QFN	0°C to 70°C
LTC2373IUH-18#PBF	LTC2373IUH-18#TRPBF	237318	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 85°C
LTC2373HUH-18#PBF	LTC2373HUH-18#TRPBF	237318	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}^+	Absolute Input Range (CH0 to CH7)	(Note 5)	●	–0.1		V_{REFBUF} + 0.1	V
V_{IN}^-	Absolute Input Range (CH0 to CH7, COM)	Fully Differential (Note 5)	●	–0.1		V_{REFBUF} + 0.1	V
		Pseudo-Differential Unipolar (Note 5)	●	–0.1	0	0.1	V
		Pseudo-Differential Bipolar (Note 5)	●	$V_{REFBUF}/2$ – 0.1	$V_{REFBUF}/2$	$V_{REFBUF}/2$ + 0.1	V
$V_{IN}^+ – V_{IN}^-$	Input Differential Voltage Range	Fully Differential	●	$–V_{REFBUF}$		V_{REFBUF}	V
		Pseudo-Differential Unipolar	●	0		V_{REFBUF}	V
		Pseudo-Differential Bipolar	●	$–V_{REFBUF}/2$		$V_{REFBUF}/2$	V
V_{CM}	Common Mode Input Range	Pseudo-Differential Bipolar and Fully Differential (Note 6)	●	$–V_{REFBUF}/2$ – 0.1	$V_{REFBUF}/2$	$V_{REFBUF}/2$ + 0.1	V
I_{IN}	Analog Input Leakage Current		●	–1		1	µA
C_{IN}	Analog Input Capacitance	Sample Mode			75		pF
		Hold Mode			5		pF
CMRR	Input Common Mode Rejection Ratio	Fully Differential, f_{IN} = 500kHz			67		dB
		Pseudo-Differential Unipolar, f_{IN} = 500kHz			66		dB
		Pseudo-Differential Bipolar, f_{IN} = 500kHz			66		dB

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Resolution		●	18			Bits
	No Missing Codes		●	18			Bits
	Transition Noise	Fully Differential			0.85		LSB_{RMS}
		Pseudo-Differential Unipolar			1.5		LSB_{RMS}
		Pseudo-Differential Bipolar			1.5		LSB_{RMS}
INL	Integral Linearity Error	Fully Differential (Note 7)	●	–2	±0.5	2	LSB
		Pseudo-Differential Unipolar (Note 7)	●	–2.75	±0.8	2.75	LSB
		Pseudo-Differential Bipolar (Note 7)	●	–2.75	±0.8	2.75	LSB
DNL	Differential Linearity Error	Fully Differential (Note 6)	●	–0.9	±0.25	0.9	LSB
		Pseudo-Differential Unipolar (Note 6)	●	–0.9	±0.25	0.9	LSB
		Pseudo-Differential Bipolar (Note 6)	●	–0.9	±0.25	0.9	LSB
ZSE	Zero-Scale Error	Fully Differential (Note 8)	●	–15	±2	15	LSB
		Pseudo-Differential Unipolar (Note 8)	●	–30	±2	30	LSB
		Pseudo-Differential Bipolar (Note 8)	●	–30	±2	30	LSB
	Zero-Scale Error Drift	Fully Differential			20		mLSB/°C
		Pseudo-Differential Unipolar			30		mLSB/°C
		Pseudo-Differential Bipolar			30		mLSB/°C
	Zero-Scale Error Match	Fully Differential	●	–18	±2	18	LSB
		Pseudo-Differential Unipolar	●	–24	±4	24	LSB
		Pseudo-Differential Bipolar	●	–28	±4	28	LSB
FSE	Full-Scale Error	Fully Differential					
		REFBUF = 4.096V (REFBUF Overdriven) (Notes 8, 9)	●	–50	±7	50	LSB
		REFIN = 2.048V (REFIN Overdriven) (Note 8)	●	–100	±11	100	LSB
		Pseudo-Differential Unipolar					
		REFBUF = 4.096V (REFBUF Overdriven) (Notes 8, 9)	●	–75	±5	75	LSB
		REFIN = 2.048V (REFIN Overdriven) (Note 8)	●	–200	±14	200	LSB
		Pseudo-Differential Bipolar					
		REFBUF = 4.096V (REFBUF Overdriven) (Notes 8, 9)	●	–50	±8	50	LSB
		REFIN = 2.048V (REFIN Overdriven) (Note 8)	●	–120	±12	120	LSB

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Full-Scale Error Drift	Fully Differential REFBUF = 4.096V (REFBUF Overdriven) (Note 9) Pseudo-Differential Unipolar REFBUF = 4.096V (REFBUF Overdriven) (Note 9) Pseudo-Differential Bipolar REFBUF = 4.096V (REFBUF Overdriven) (Note 9)			0.2 0.2 0.2		ppm/°C ppm/°C ppm/°C
	Full-Scale Error Match	Fully Differential REFBUF = 4.096V (REFBUF Overdriven) (Note 9) Pseudo-Differential Unipolar REFBUF = 4.096V (REFBUF Overdriven) (Note 9) Pseudo-Differential Bipolar REFBUF = 4.096V (REFBUF Overdriven) (Note 9)	 ● ● ●	 –18 –24 –28	 ±2 ±4 ±4	 18 24 28	 LSB LSB LSB

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and A_{IN} = –1dBFS. (Notes 4, 10)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SINAD	Signal-to-(Noise + Distortion) Ratio	Fully Differential f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven) Pseudo-Differential Unipolar f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven) Pseudo-Differential Bipolar f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven)	 ● ● ●	 96 90.5 90.5	 99.5 94.8 94.8	 	 dB dB dB
		Fully Differential f_{IN} = 1kHz, REFBUF = 5V (REFBUF Overdriven) (Note 9) Pseudo-Differential Unipolar f_{IN} = 1kHz, REFBUF = 5V (REFBUF Overdriven) (Note 9) Pseudo-Differential Bipolar f_{IN} = 1kHz, REFBUF = 5V (REFBUF Overdriven) (Note 9)			101.4 96.6 96.6		dB dB dB
		Fully Differential f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven), SEL = 1 Pseudo-Differential Bipolar f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven), SEL = 1			98.4 93.3		dB dB
SNR	Signal-to-Noise Ratio	Fully Differential f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven) Pseudo-Differential Unipolar f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven) Pseudo-Differential Bipolar f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven)	 ● ● ●	 96.5 91 91	 100 95.0 95.0	 	 dB dB dB
		Fully Differential f_{IN} = 1kHz, REFBUF = 5V (REFBUF Overdriven) (Note 9) Pseudo-Differential Unipolar f_{IN} = 1kHz, REFBUF = 5V (REFBUF Overdriven) (Note 9) Pseudo-Differential Bipolar f_{IN} = 1kHz, REFBUF = 5V (REFBUF Overdriven) (Note 9)			102 96.8 96.8		dB dB dB
		Fully Differential f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven), SEL = 1 Pseudo-Differential Bipolar f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven), SEL = 1			98.5 93.4		dB dB

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and A_{IN} = –1dBFS. (Notes 4, 10)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
THD	Total Harmonic Distortion	Fully Differential					
		f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven)	●	–104	–114		dB
		Pseudo-Differential Unipolar					
		f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven)	●	–99	–110		dB
		Pseudo-Differential Bipolar					
		f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven)	●	–99	–110		dB
		Fully Differential					
		f_{IN} = 1kHz, REFBUF = 5V (REFBUF Overdriven) (Note 9)			–111		dB
		Pseudo-Differential Unipolar					
		f_{IN} = 1kHz, REFBUF = 5V (REFBUF Overdriven) (Note 9)			–110		dB
		Pseudo-Differential Bipolar					
		f_{IN} = 1kHz, REFBUF = 5V (REFBUF Overdriven) (Note 9)			–110		dB
		Fully Differential					
		f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven), SEL = 1			–113		dB
		Pseudo-Differential Bipolar					
		f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven), SEL = 1			–110		dB
SFDR	Spurious Free Dynamic Range	Fully Differential					
		f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven)	●	104	114		dB
		Pseudo-Differential Unipolar					
		f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven)	●	99	110		dB
		Pseudo-Differential Bipolar					
		f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven)	●	99	110		dB
		Fully Differential					
		f_{IN} = 1kHz, REFBUF = 5V (REFBUF Overdriven) (Note 9)			112		dB
		Pseudo-Differential Unipolar					
		f_{IN} = 1kHz, REFBUF = 5V (REFBUF Overdriven) (Note 9)			112		dB
		Pseudo-Differential Bipolar					
		f_{IN} = 1kHz, REFBUF = 5V (REFBUF Overdriven) (Note 9)			112		dB
		Fully Differential					
		f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven), SEL = 1			112.5		dB
		Pseudo-Differential Bipolar					
		f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven), SEL = 1			113.5		dB
	Channel-to-Channel Crosstalk	f_{IN} = 100kHz, Signal Applied to an OFF Channel			–107		dB
	–3dB Input Linear Bandwidth				22		MHz
	Aperture Delay				500		ps
	Aperture Jitter				4		ps_{RMS}
	Transient Response	Full-Scale Step			460		ns

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REFIN}	Internal Reference Output Voltage			2.043	2.048	2.053	V
	V_{REFIN} Temperature Coefficient	(Note 11)	●		4	20	ppm/°C
	REFIN Output Impedance				15		kΩ
	V_{REFIN} Line Regulation	V_{DD} = 4.75V to 5.25V			0.06		mV/V
	REFIN Input Voltage Range	(REFIN Overdriven) (Note 5)		1.25		2.4	V

REFERENCE BUFFER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REFBUF}	Reference Buffer Output Voltage	V_{REFIN} = 2.048V	●	4.088	4.096	4.104	V
	REFBUF Input Voltage Range	(REFBUF Overdriven) (Notes 5, 9)	●	2.5		5	V
	REFBUF Output Impedance	V_{REFIN} = 0V (Buffer Disabled)			13		kΩ
I_{REFBUF}	REFBUF Load Current	V_{REFBUF} = 5V (REFBUF Overdriven) (Notes 9, 12) V_{REFBUF} = 5V, Nap Mode (REFBUF Overdriven) (Note 9)	●		1.1 0.38	1.5	mA mA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage		●	0.8 • OV_{DD}			V
V_{IL}	Low Level Input Voltage		●			0.2 • OV_{DD}	V
I_{IN}	Digital Input Current	V_{IN} = 0V to OV_{DD}	●	–10		10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	I_O = –500µA	●	OV_{DD} – 0.2			V
V_{OL}	Low Level Output Voltage	I_O = 500µA	●			0.2	V
I_{OZ}	Hi-Z Output Leakage Current	V_{OUT} = 0V to OV_{DD}	●	–10		10	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = OV_{DD}			10		mA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage		●	4.75	5	5.25	V
OV_{DD}	Supply Voltage		●	1.71		5.25	V
I_{VDD}	Supply Current	1Msps Sample Rate	●		8.0	11	mA
I_{OVDD}	Supply Current	1Msps Sample Rate (C_L = 20pF)	●		0.7		mA
I_{NAP}	Nap Mode Current	Conversion Done (I_{VDD} + I_{OVDD})	●		1.25	1.5	mA
I_{SLEEP}	Sleep Mode Current	Sleep Mode (I_{VDD} + I_{OVDD})	●		60	120	µA
P_D	Power Dissipation	1Msps Sample Rate			40	55	mW
	Nap Mode	Conversion Done (I_{VDD} + I_{OVDD})			6.25	7.5	mW
	Sleep Mode	Sleep Mode (I_{VDD} + I_{OVDD})			300	600	µW

ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SMPL}	Maximum Sampling Frequency		●			1	Msps
t_{CONV}	Conversion Time		●	460		527	ns
t_{ACQ}	Acquisition Time	t_{ACQ} = t_{CYC} – t_{CONV} – t_{BUSYLH} (Note 6)	●	460			ns
t_{CYC}	Time Between Conversions		●	1			µs
t_{CNVH}	CNV High Time		●	20			ns
t_{CNVL}	Minimum Low Time for CNV	(Note 14)	●	20			ns
t_{BUSYLH}	CNV↑ to BUSY↑ Delay	C_L = 20pF	●			13	ns
t_{RESETH}	RESET Pulse Width		●	200			ns
t_{QUIET}	SCK, SDI and RDL Quiet Time from CNV↑	(Note 6)	●	20			ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

t_{SCK}	SCK Period	(Notes 13, 14)	●	10		ns
t_{SCKH}	SCK High Time		●	4		ns
t_{SCKL}	SCK Low Time		●	4		ns
$t_{SSDISCK}$	SDI Setup Time From SCK↑	(Note 13)	●	4		ns
$t_{HSDISCK}$	SDI Hold Time From SCK↑	(Note 13)	●	1		ns
t_{DSDO}	SDO Data Valid Delay from SCK↑	C_L = 20pF, OV_{DD} = 5.25V C_L = 20pF, OV_{DD} = 2.5V C_L = 20pF, OV_{DD} = 1.71V	● ● ●		7.5 8 9.5	ns ns ns
t_{HSDO}	SDO Data Remains Valid Delay from SCK↑	C_L = 20pF (Note 6)	●	1		ns
$t_{DSDOBUSYL}$	SDO Data Valid Delay from BUSY↓	C_L = 20pF (Note 6)	●		5	ns
t_{EN}	Bus Enable Time After RDL↓	(Note 13)	●		16	ns
t_{DIS}	Bus Relinquish Time After RDL↑	(Note 13)	●		13	ns
t_{WAKE}	REFBUF Wake-Up Time	C_{REFBUF} = 47µF, C_{REFIN} = 0.1µF		200		ms
$t_{CNVMRST}$	CNV↑ to MUX Starts Resetting Delay		●		38	ns
t_{MRST1}	MUX Reset Time During Conversion		●		36	ns
$t_{VLDMRST}$	8th SCK↑ to MUX Starts Resetting Delay After Programming 1st Valid Configuration Word		●		40	ns
t_{MRST2}	MUX Reset Time During Acquisition After Programming 1st Valid Configuration Word		●		42	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground.

Note 3: When these pin voltages are taken below ground or above V_{DD} or OV_{DD}, they will be clamped by internal diodes. This product can handle input currents up to 100mA below ground or above V_{DD} or OV_{DD} without latchup.

Note 4: V_{DD} = 5V, OV_{DD} = 2.5V, f_{SMPL} = 1MHz, REFIN = 2.048V unless otherwise noted.

Note 5: Recommended operating conditions.

Note 6: Guaranteed by design, not subject to test.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Fully differential zero-scale error is the offset voltage measured from –0.5LSB when the output code flickers between 01 1111 1111 1111 1111 and 10 0000 0000 0000 0000 in straight binary format and 00 0000 0000 0000 0000 and 11 1111 1111 1111 1111 in two's complement format. Unipolar zero-scale error is the offset voltage measured from 0.5LSB when the output code flickers between 00 0000 0000 0000 0000 and 00 0000 0000 0000 0001. Bipolar zero-scale error is the offset voltage measured from –0.5LSB when the output code flickers between 00 0000 0000 0000 0000 and 11 1111 1111 1111 1111. Fully differential full-scale error is the worst-case deviation of the first and last code transitions from ideal and includes the effect of offset error. Unipolar full-scale error is the deviation of the last code transition from the ideal and includes the effect of offset error. Bipolar full-scale error is the worst-case deviation of the first and last code transitions from ideal and includes the effect of offset error.

Note 9: When REFBUF is overdriven, the internal reference buffer must be turned off by setting REFIN=0V.

Note 10: All specifications in dB are referred to a full-scale $\pm V_{REFBUF}$ (fully differential), 0V to V_{REFBUF} (pseudo-differential unipolar), or $\pm V_{REFBUF}/2$ (pseudo-differential bipolar) input.

Note 11: Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

Note 12: f_{SMPL} = 1MHz, I_{REFBUF} varies proportionally with sample rate.

Note 13: Parameter tested and guaranteed at OV_{DD} = 1.71V, OV_{DD} = 2.5V and OV_{DD} = 5.25V.

Note 14: t_{SCK} of 10ns maximum allows a shift clock frequency up to 100MHz for rising edge capture.

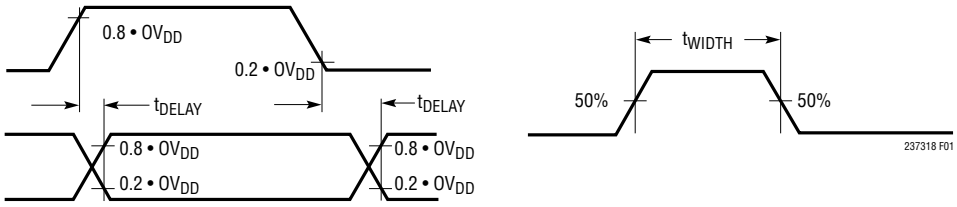
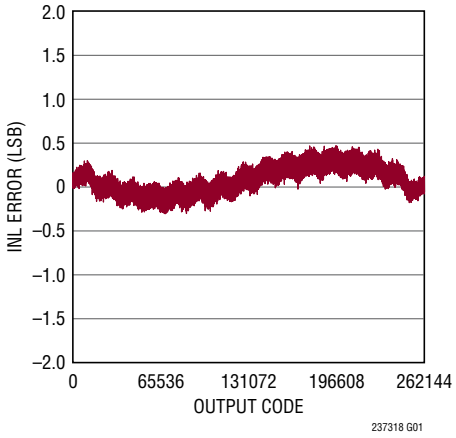


Figure 1. Voltage Levels for Timing Specifications

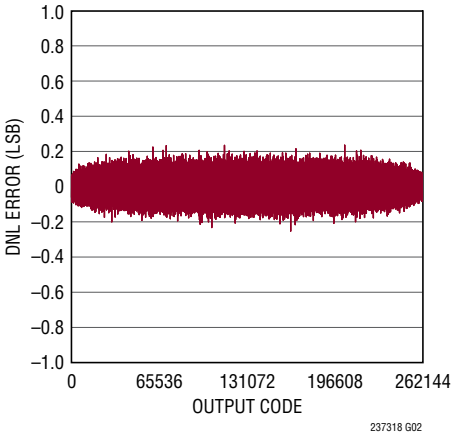
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, REFIN = 2.048V, Fully Differential Range, V_{CM} = 2.048V, f_{SMPL} = 1Msps, unless otherwise noted.

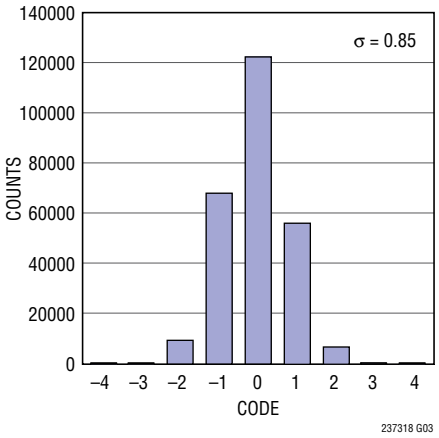
Integral Nonlinearity vs Output Code



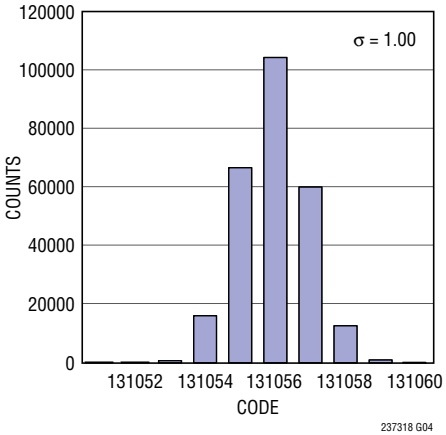
Differential Nonlinearity vs Output Code



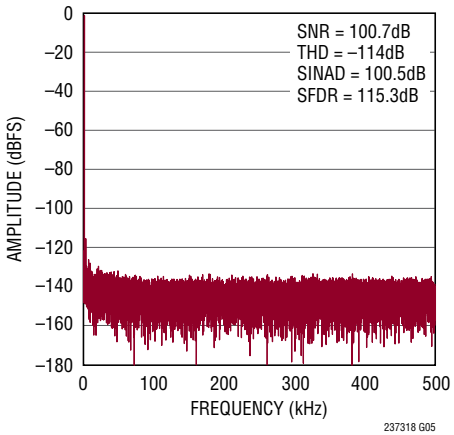
DC Histogram (Zero-Scale)



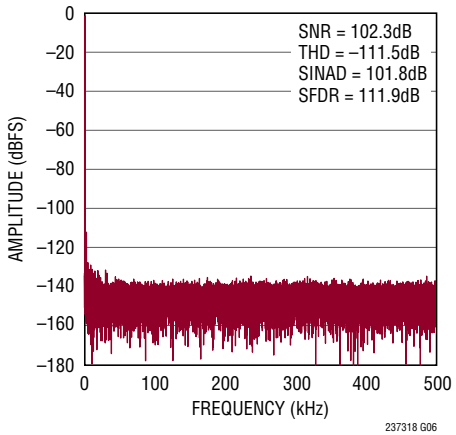
DC Histogram (Near Full-Scale)



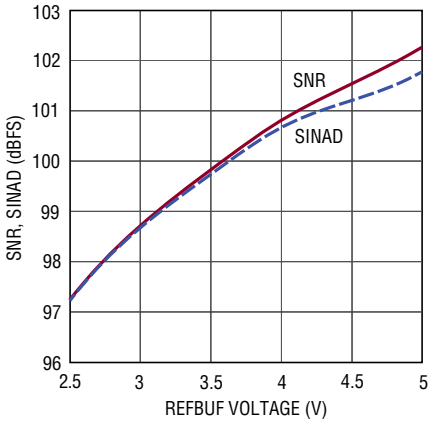
32k Point FFT f_{SMPL} = 1Msps, f_{IN} = 1kHz



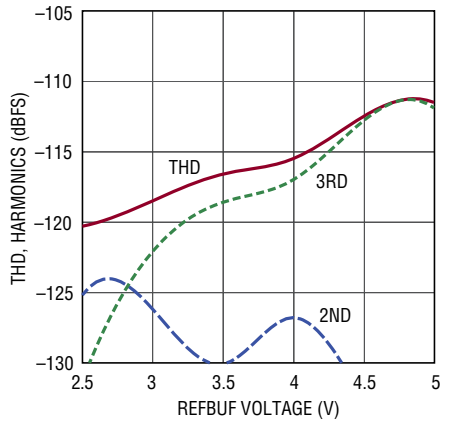
32k Point FFT f_{SMPL} = 1Msps, f_{IN} = 1kHz, REFBUF = 5V



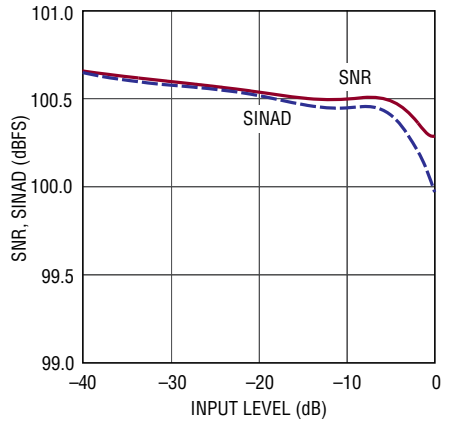
SNR, SINAD vs REFBUF, f_{IN} = 1kHz



THD, Harmonics vs REFBUF, f_{IN} = 1kHz



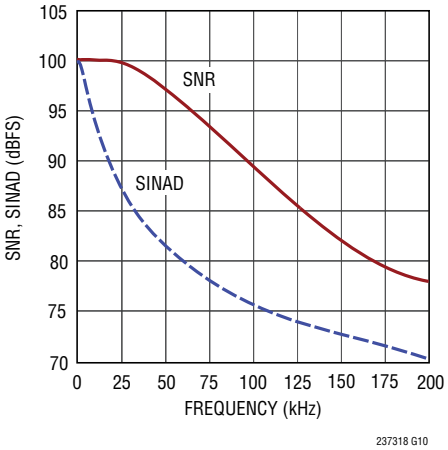
SNR, SINAD vs Input Level, f_{IN} = 1kHz



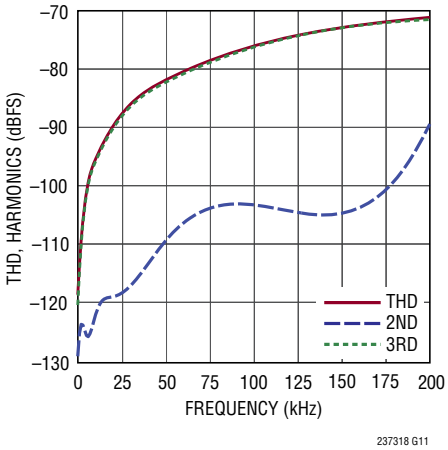
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, REFIN = 2.048V, Fully Differential Range, V_{CM} = 2.048V, f_{SMPL} = 1Msps, unless otherwise noted.

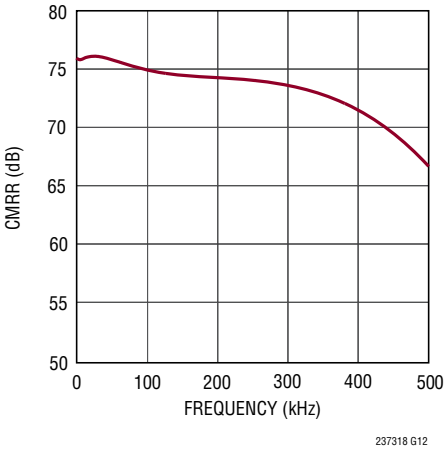
SNR, SINAD vs Input Frequency



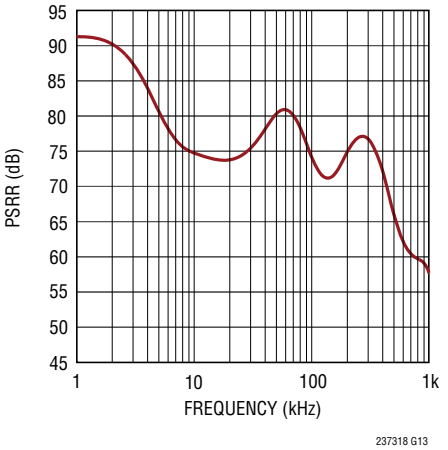
THD, Harmonics vs Input Frequency



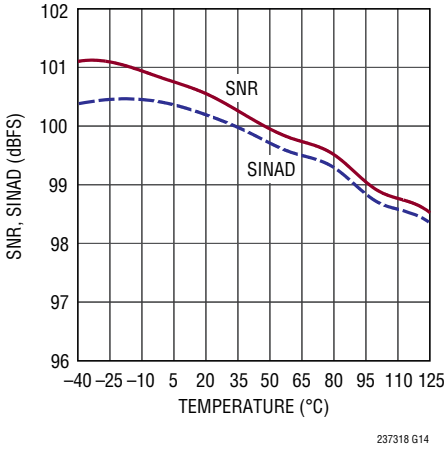
CMRR vs Input Frequency



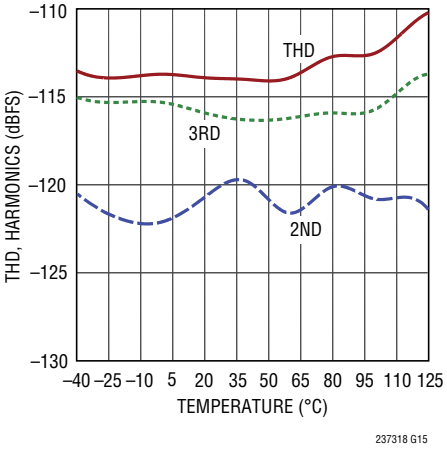
PSRR vs Frequency



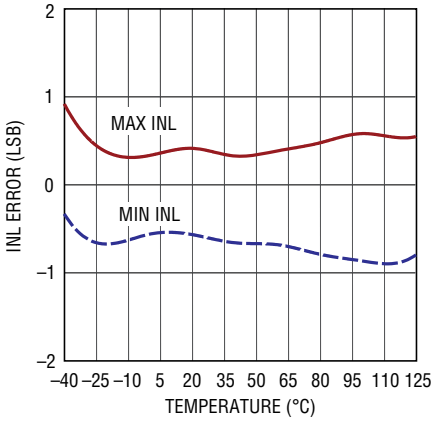
SNR, SINAD vs Temperature, f_{IN} = 1kHz



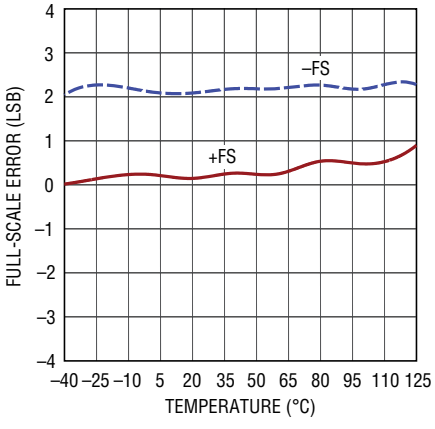
THD, Harmonics vs Temperature, f_{IN} = 1kHz



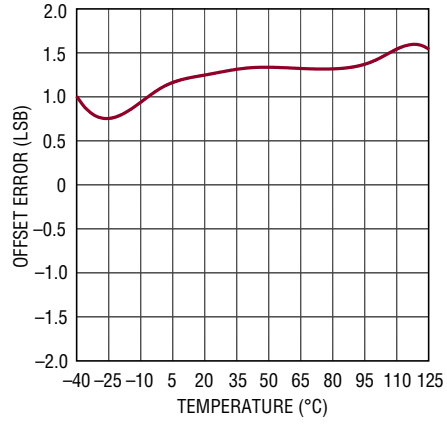
INL vs Temperature



Full-Scale Error vs Temperature REFBUF = 4.096V



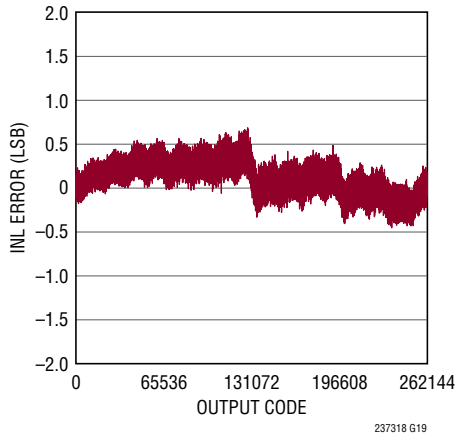
Zero-Scale Error vs Temperature



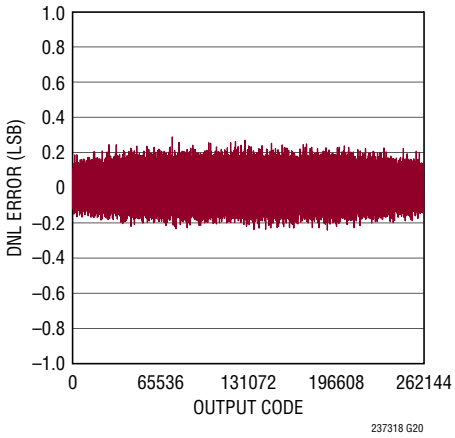
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, REFIN = 2.048V, Pseudo-Differential Unipolar Range, f_{SMPL} = 1Msps, unless otherwise noted.

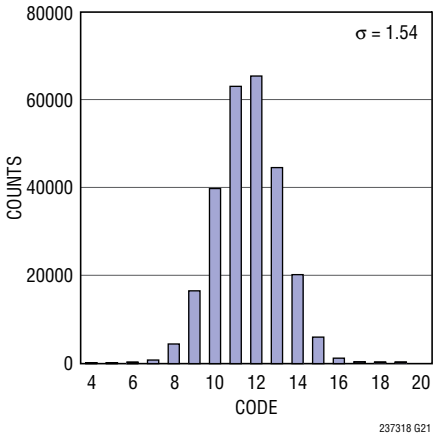
Integral Nonlinearity vs Output Code



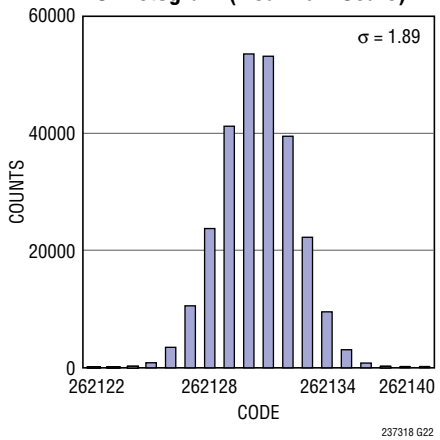
Differential Nonlinearity vs Output Code



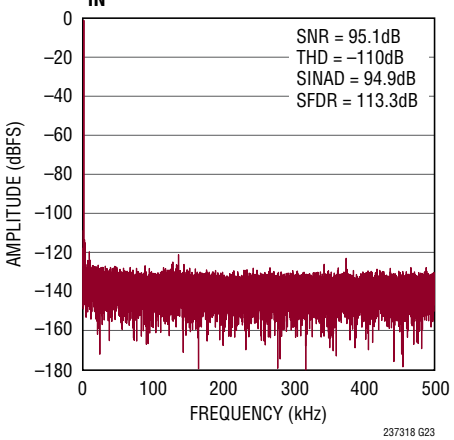
DC Histogram (Zero-Scale)



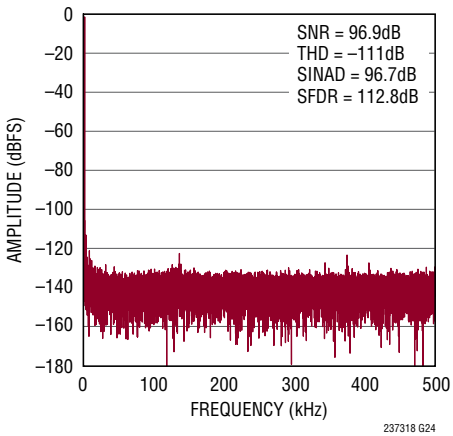
DC Histogram (Near Full-Scale)



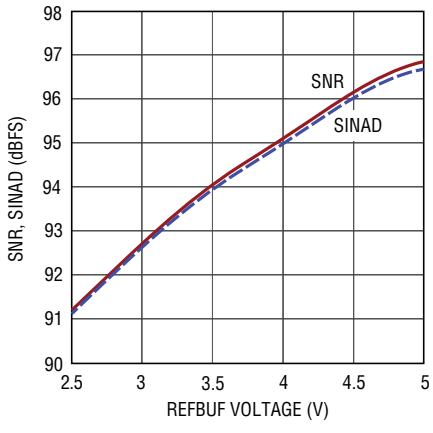
32k Point FFT f_{SMPL} = 1Msps, f_{IN} = 1kHz



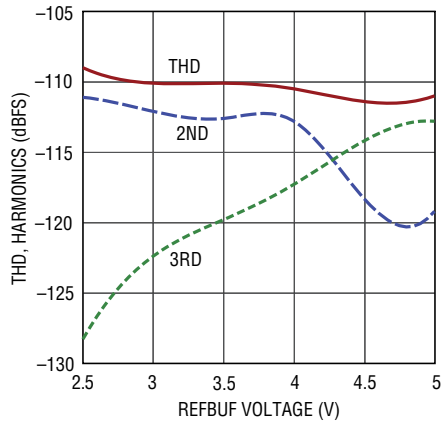
32k Point FFT f_{SMPL} = 1Msps, f_{IN} = 1kHz, REFBUF = 5V



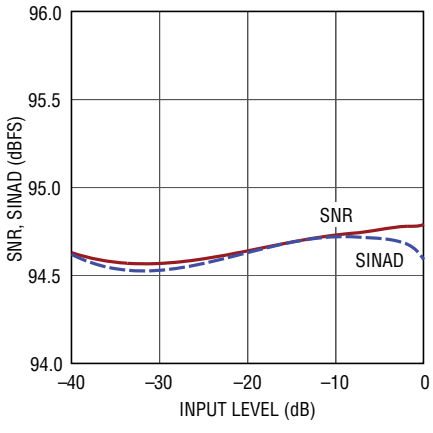
SNR, SINAD vs REFBUF, f_{IN} = 1kHz



THD, Harmonics vs REFBUF, f_{IN} = 1kHz



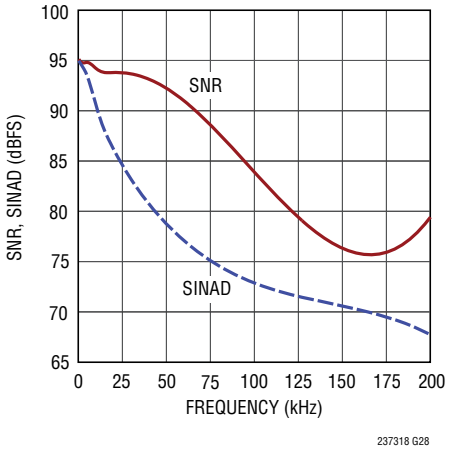
SNR, SINAD vs Input Level, f_{IN} = 1kHz



TYPICAL PERFORMANCE CHARACTERISTICS

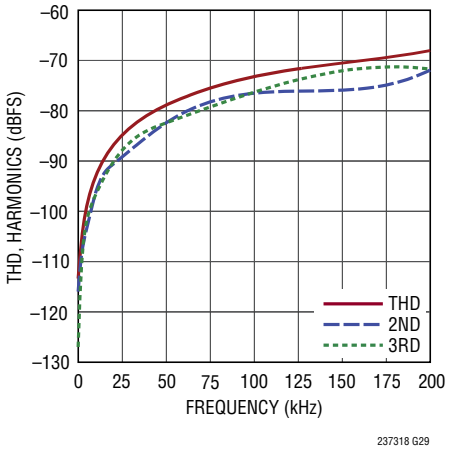
T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, REFIN = 2.048V, Pseudo-Differential Unipolar Range, f_{SMPL} = 1Msps, unless otherwise noted.

SNR, SINAD vs Input Frequency



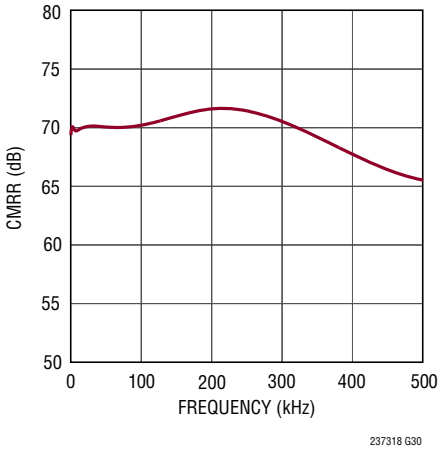
237318 G28

THD, Harmonics vs Input Frequency



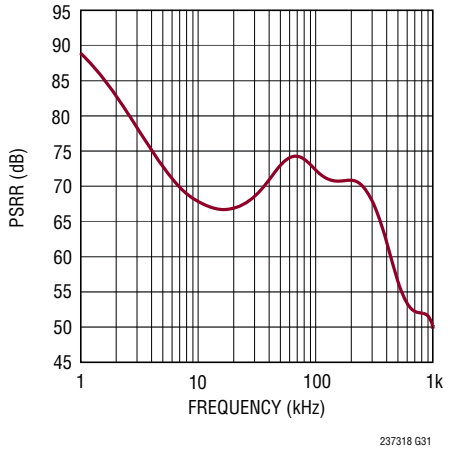
237318 G29

CMRR vs Input Frequency



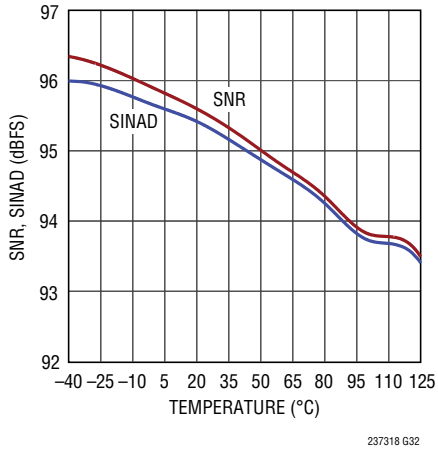
237318 G30

PSRR vs Frequency



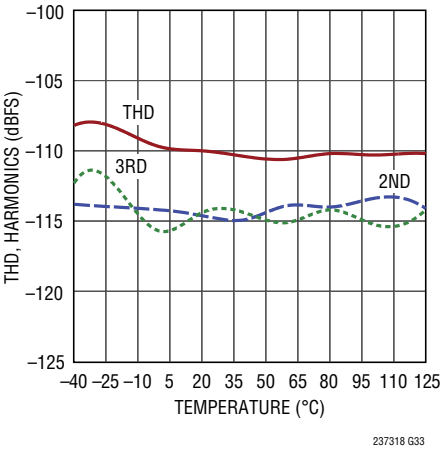
237318 G31

SNR, SINAD vs Temperature, f_{IN} = 1kHz



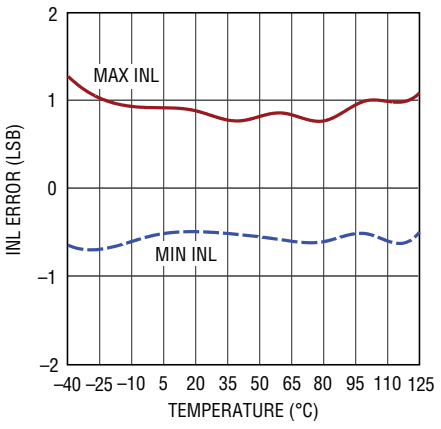
237318 G32

THD, Harmonics vs Temperature, f_{IN} = 1kHz



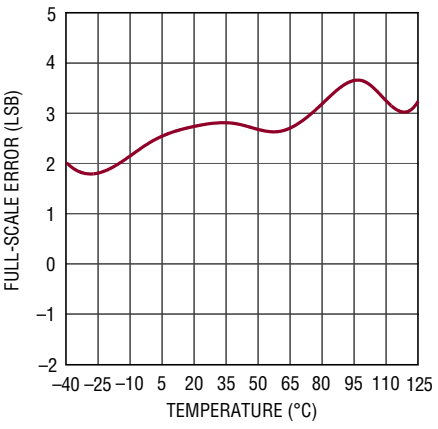
237318 G33

INL vs Temperature



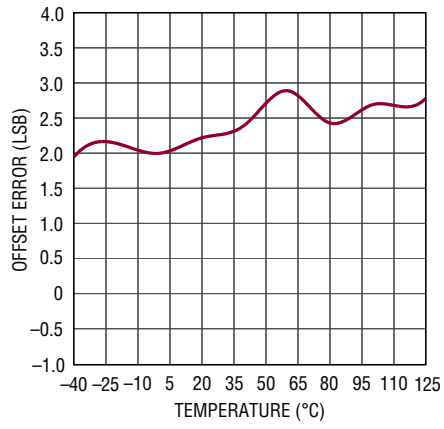
237318 G34

Full-Scale Error vs Temperature REFBUF = 4.096V



237318 G35

Zero-Scale Error vs Temperature

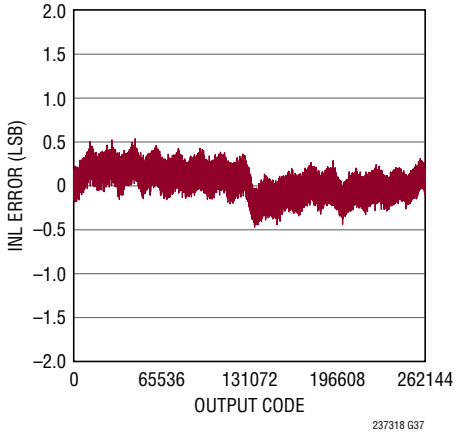


237318 G36

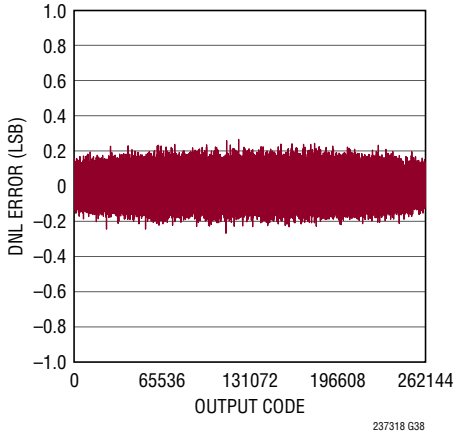
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, REFIN = 2.048V, Pseudo-Differential Bipolar Range, f_{SMPL} = 1Msps, unless otherwise noted.

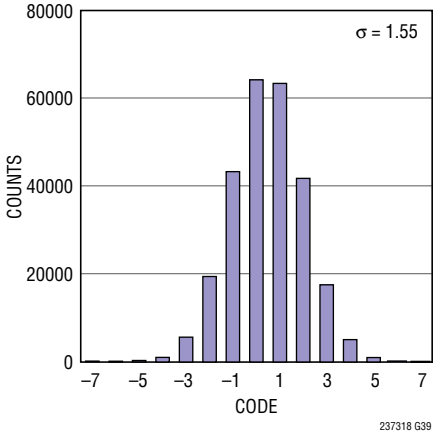
Integral Nonlinearity vs Output Code



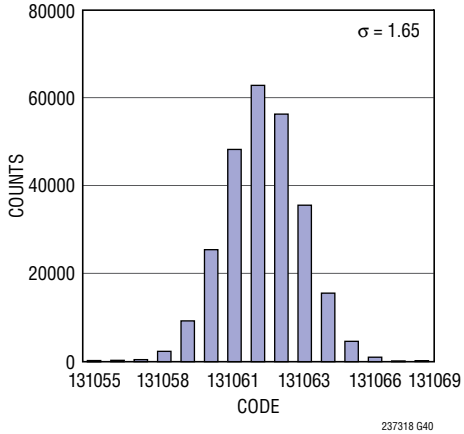
Differential Nonlinearity vs Output Code



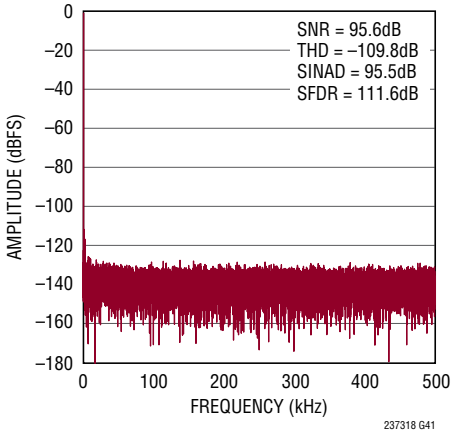
DC Histogram (Zero-Scale)



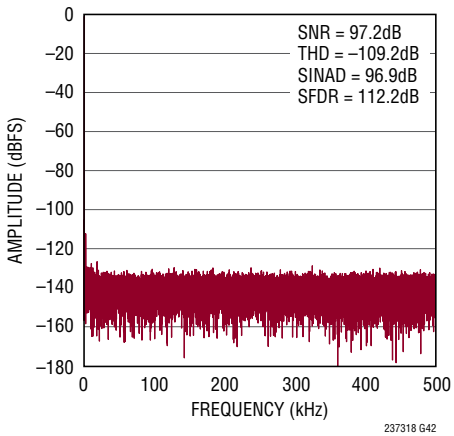
DC Histogram (Near Full-Scale)



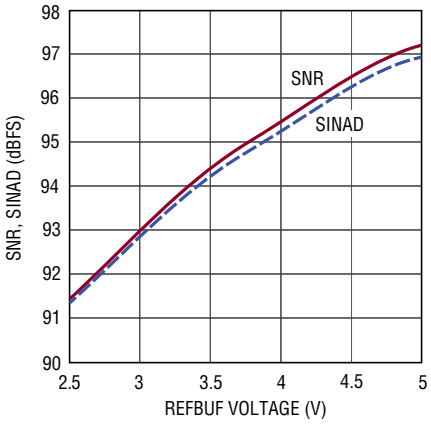
32k Point FFT f_{SMPL} = 1Msps, f_{IN} = 1kHz



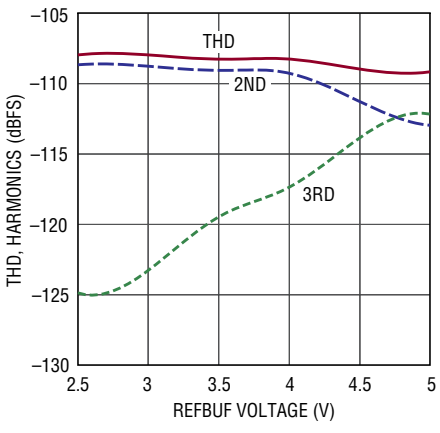
32k Point FFT f_{SMPL} = 1Msps, f_{IN} = 1kHz, REFBUF = 5V



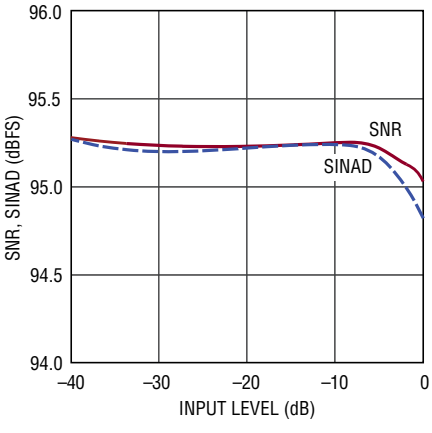
SNR, SINAD vs REFBUF, f_{IN} = 1kHz



THD, Harmonics vs REFBUF, f_{IN} = 1kHz



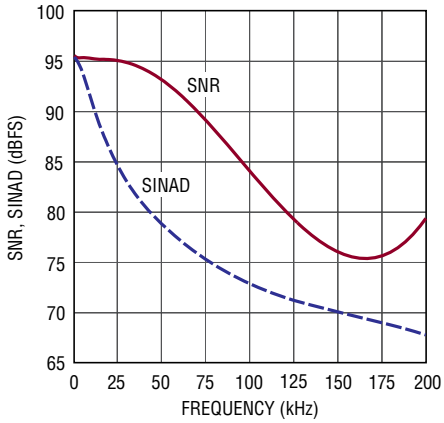
SNR, SINAD vs Input Level, f_{IN} = 1kHz



TYPICAL PERFORMANCE CHARACTERISTICS

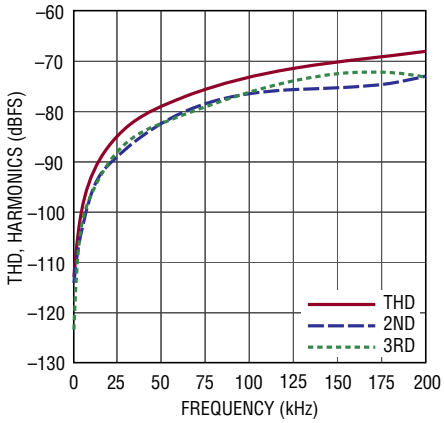
T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, REFIN = 2.048V, Pseudo-Differential Bipolar Range, f_{SMPL} = 1Msps, unless otherwise noted.

SNR, SINAD vs Input Frequency



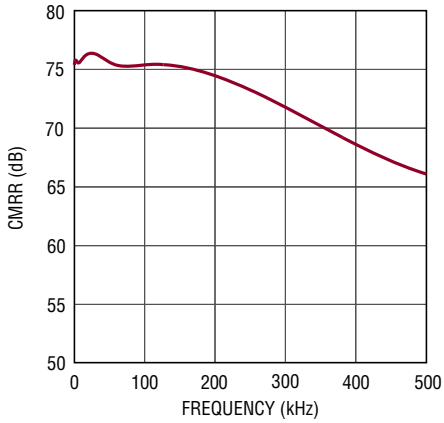
237318 G46

THD, Harmonics vs Input Frequency



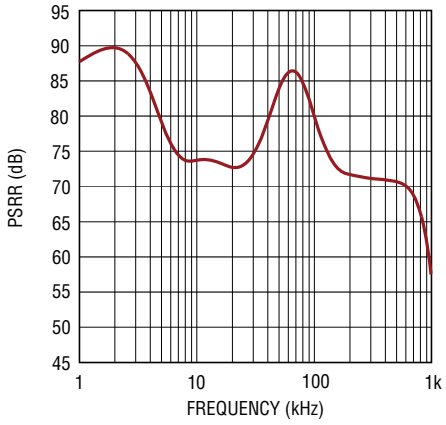
237318 G47

CMRR vs Input Frequency



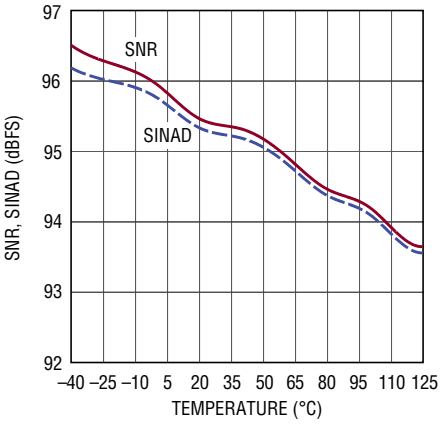
237318 G48

PSRR vs Frequency



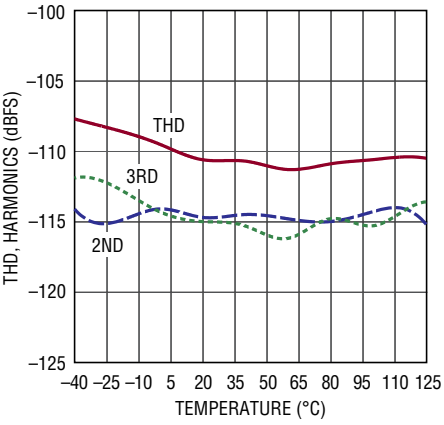
237318 G49

SNR, SINAD vs Temperature, f_{IN} = 1kHz



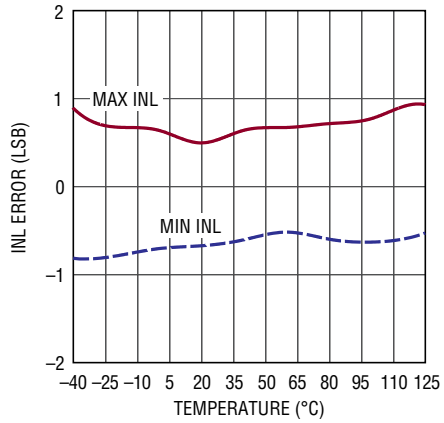
237318 G50

THD, Harmonics vs Temperature, f_{IN} = 1kHz



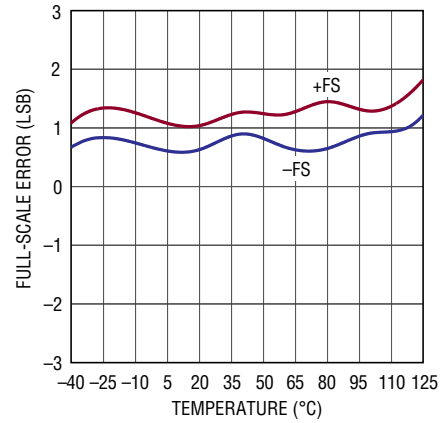
237318 G51

INL vs Temperature



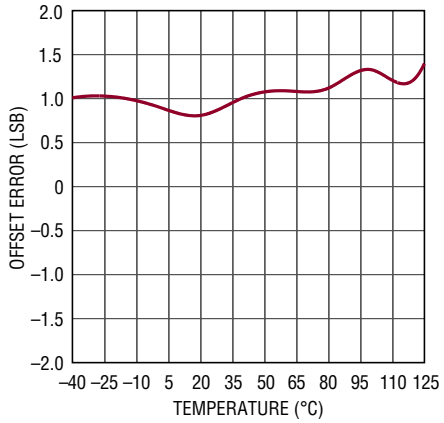
237318 G52

Full-Scale Error vs Temperature REFBUF = 4.096V



237318 G53

Zero-Scale Error vs Temperature

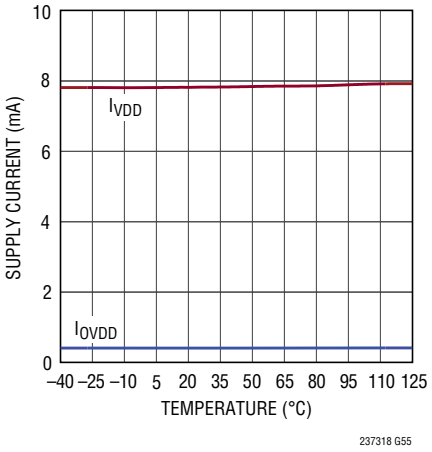


237318 G54

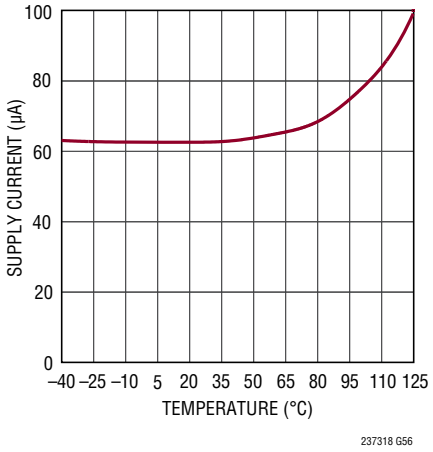
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, REFIN = 2.048V, f_{SMPL} = 1Msps, unless otherwise noted.

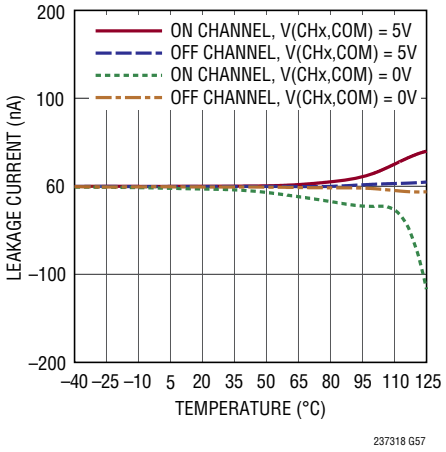
Supply Current vs Temperature



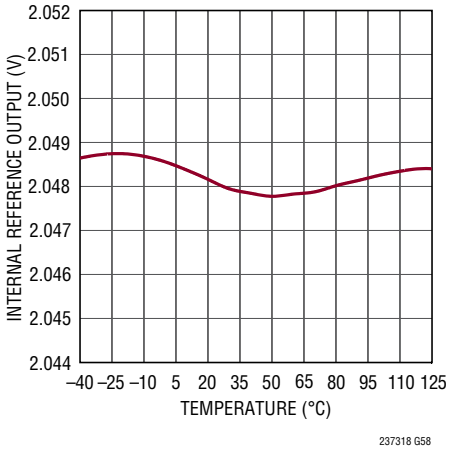
Sleep Current vs Temperature



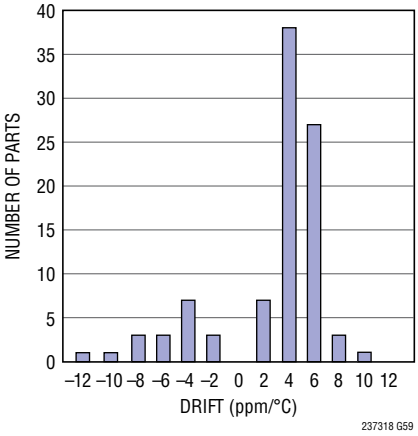
Input Leakage Current vs Temperature (MUXOUT± Shorted to ADCIN±)



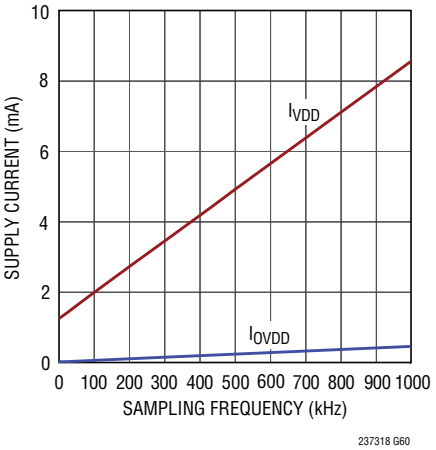
Internal Reference Output vs Temperature



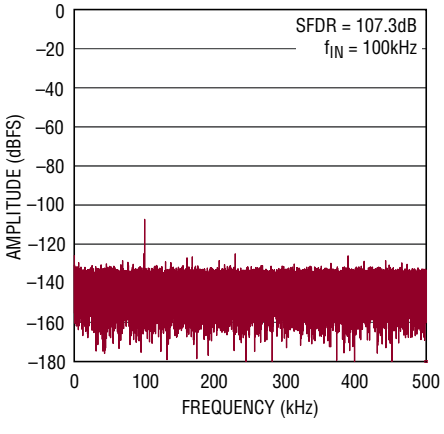
Internal Reference Output Temperature Coefficient Distribution



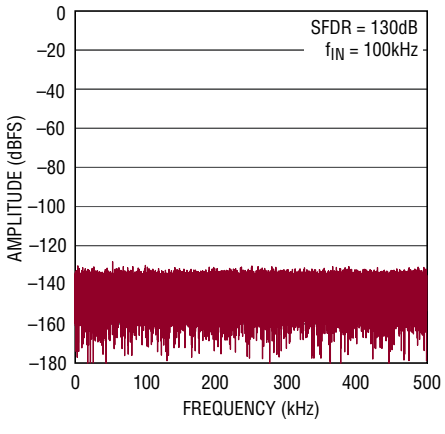
Supply Current vs Sampling Rate



Crosstalk FFT (AC Crosstalk- Channel Adjacent to MUXOUT)



Crosstalk FFT (AC Crosstalk- Channel NOT Adjacent to MUXOUT)



PIN FUNCTIONS

CH0 to CH7 (Pins 1, 2, 7, 8, 9, 10, 31 and 32): Analog Inputs. CH0 to CH7 can be configured as single-ended inputs relative to COM, or as pairs of differential input channels. See the Analog Input Multiplexer section. Unused analog inputs should be tied to a DC voltage within the analog input voltage range of (GND – 0.3V) to (V_{DD} + 0.3V) as specified in Absolute Maximum Ratings.

MUXOUT$^+$, MUXOUT$^-$ (Pin 3, Pin 6): Analog Output Pins of MUX.

ADCIN$^+$, ADCIN$^-$ (Pin 4, Pin 5): Analog Input Pins of ADC Core.

GND (Pins 11, 14, 15, 17, 23, 26, 27 and Exposed Pad Pin 33): Ground.

REFBUF (Pin 12): Reference Buffer Output. An onboard buffer nominally outputs 4.096V to this pin. This pin is referred to GND and should be decoupled closely to the pin with a 47µF ceramic capacitor. The internal buffer driving this pin may be disabled by grounding its input at REFIN. Once the buffer is disabled, an external reference may overdrive this pin in the range of 2.5V to 5V. A resistive load greater than 500k can be placed on the reference buffer output.

REFIN (Pin 13): Reference Output/Reference Buffer Input. An onboard bandgap reference nominally outputs 2.048V at this pin. Bypass this pin with a 0.1µF ceramic capacitor to GND to limit the reference output noise. If more accuracy is desired, this pin may be overdriven by an external reference in the range of 1.25V to 2.4V.

CNV (Pin 16): Convert Input. A rising edge on this input powers up the part and initiates a new conversion. Logic levels are determined by OV_{DD}.

RDL (Pin 18): Read Low Input. When RDL is low, the serial data I/O bus is enabled. When RDL is high, the serial data I/O bus becomes Hi-Z. RDL also gates the external shift clock. Logic levels are determined by OV_{DD}.

BUSY (Pin 19): BUSY Indicator. Goes high at the start of a new conversion and returns low when the conversion has finished. Logic levels are determined by OV_{DD}.

SDI (Pin 20): Serial Data Input. Data provided on this pin in synchrony with SCK can be used to program the MUX channel configuration, converter input range and digital gain compression setting via the sequencer. Input data on SDI is latched on rising edges of SCK when the serial data I/O bus is enabled. Logic levels are determined by OV_{DD}.

SCK (Pin 21): Serial Data Clock Input. When the serial data I/O bus is enabled, the conversion result followed by configuration information is shifted out at SDO on the rising edges of this clock MSB first. Serial input data is latched on the rising edges of this clock at SDI. Logic levels are determined by OV_{DD}.

SDO (Pin 22): Serial Data Output. The conversion result followed by configuration information is output on this pin on each rising edge of SCK MSB first when the serial data I/O bus is enabled. The output data format is determined by the converter operating mode. Logic levels are determined by OV_{DD}.

RESET (Pin 24): Reset Input. When this pin is brought high, the LTC2373-18 is reset. If this occurs during a conversion, the conversion is halted and the data bus becomes Hi-Z. Logic levels are determined by OV_{DD}.

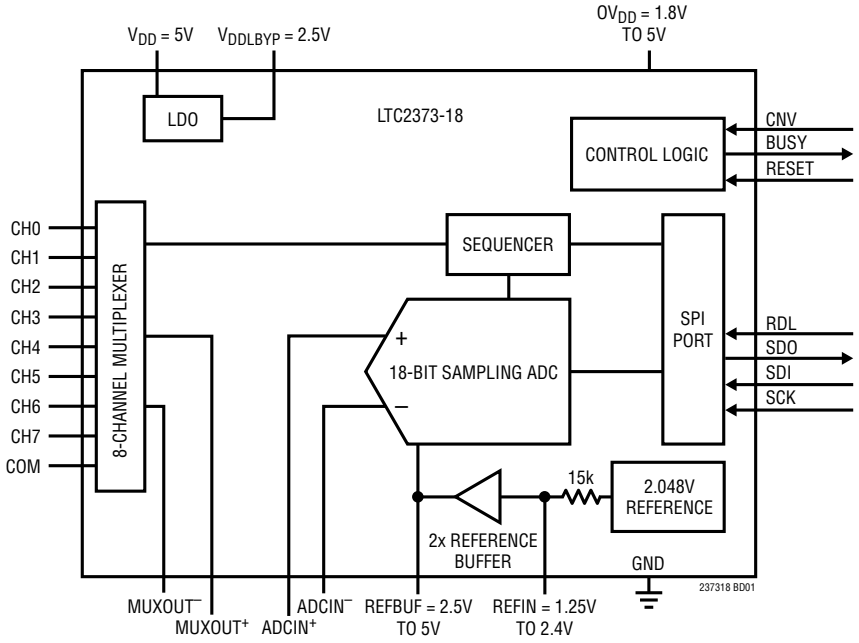
OV_{DD} (Pin 25): I/O Interface Digital Power. The range of OV_{DD} is 1.71V to 5.25V. This supply is nominally set to the same supply as the host interface (1.8V, 2.5V, 3.3V, or 5V). Bypass OV_{DD} to GND with a 0.1µF capacitor.

V_{DDLBYP} (Pin 28): 2.5V Supply Bypass Pin. The voltage on this pin is generated via an onboard regulator off of V_{DD}. This pin must be bypassed with a 2.2µF ceramic capacitor to GND. Applying an external voltage to this pin can cause damage to the IC or improper operation.

V_{DD} (Pin 29): 5V Power Supply. The range of V_{DD} is 4.75V to 5.25V. Bypass V_{DD} to GND with a 10µF ceramic capacitor.

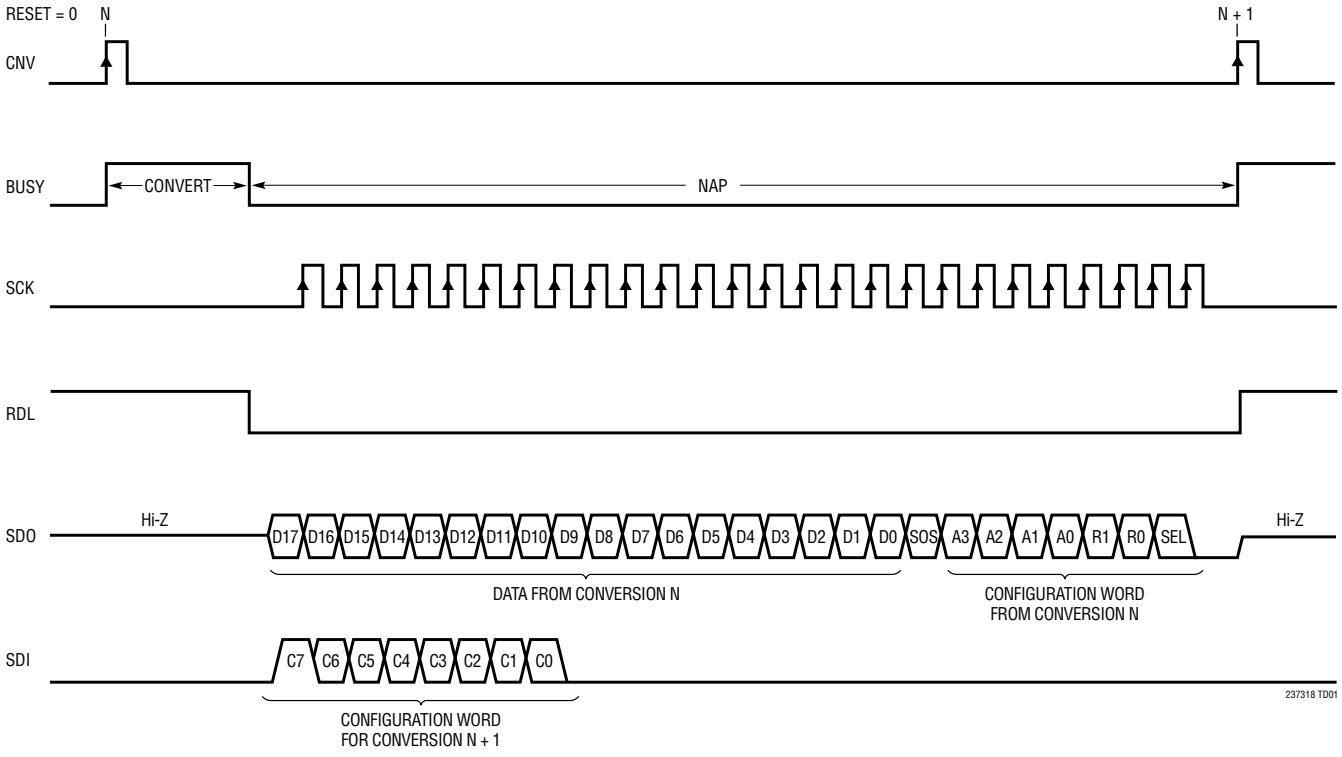
COM (Pin 30): Common Input. This is the reference point for all single-ended inputs. It must be free of noise and connected to GND for unipolar conversions and REFBUF/2 for bipolar conversions. If unused, this input should be tied to a DC voltage within the analog input voltage range of (GND – 0.3V) to (V_{DD} + 0.3V) as specified in Absolute Maximum Ratings.

FUNCTIONAL BLOCK DIAGRAM



TIMING DIAGRAM

Typical Conversion and Serial Interface Timing



APPLICATIONS INFORMATION

OVERVIEW

The LTC2373-18 is a low noise, high speed, highly configurable 8-channel 18-bit successive approximation register (SAR) ADC. The LTC2373-18 features a low crosstalk 8-channel input multiplexer (MUX) and a high performance 18-bit accurate ADC core that can be configured to accept fully-differential, pseudo-differential unipolar and pseudo-differential bipolar input signals. The input range of the ADC core can be set independently of the MUX input channel configuration. The outputs of the MUX and inputs of the ADC core are pinned out, allowing flexibility in how the MUX is connected to the ADC core. The MUX may be wired directly to the ADC core or signal conditioning circuitry may be inserted between the MUX and ADC core, depending on the application. The LTC2373-18 also has a selectable digital gain compression (DGC) feature. The LTC2373-18 has a programmable sequencer that can be programmed with configuration words ranging from a depth of one up to a maximum depth of 16 configuration words.

The LTC2373-18 has an onboard low drift reference and a single-shot capable reference buffer. The LTC2373-18 also has a high speed SPI-compatible serial interface that supports 1.8V, 2.5V, 3.3V and 5V logic. The LTC2373-18 automatically naps between conversions, leading to reduced power dissipation that scales with the sampling rate. A sleep mode is also provided for further power savings during inactive periods.

CONVERTER OPERATION

The LTC2373-18 operates in two phases. During the acquisition phase when $MUXOUT^{+/-}$ is wired to $ADCIN^{+/-}$, the charge redistribution capacitor D/A converter (CDAC) is connected through the MUX to the selected MUX analog input pins. A rising edge on the CNV pin initiates a conversion. During the conversion phase, the 18-bit CDAC is sequenced through a successive approximation algorithm, effectively comparing the sampled input with binary-weighted fractions of the reference voltage (e.g. $V_{REFBUF}/2$, $V_{REFBUF}/4$ … $V_{REFBUF}/262144$) using a differential comparator. At the end of conversion, the CDAC output approximates the sampled analog input. The ADC control logic then prepares the 18-bit digital output code for serial transfer.

TRANSFER FUNCTION

The LTC2373-18 digitizes the full-scale voltage of 2 × REFBUF in fully differential mode and REFBUF in pseudo-differential mode into 2^{18} levels. With REFBUF = 4.096V, the resulting LSB sizes in fully differential and pseudo-differential modes are 31.25µV and 15.625µV, respectively. The binary format of the conversion result depends on the converter input range as described in Table 6. The ideal two's complement transfer function is shown in Figure 2, while the ideal straight binary transfer function is shown in Figure 3. The ideal straight binary transfer function can be obtained from the two's complement transfer function by inverting the most significant bit (MSB) of each output code.

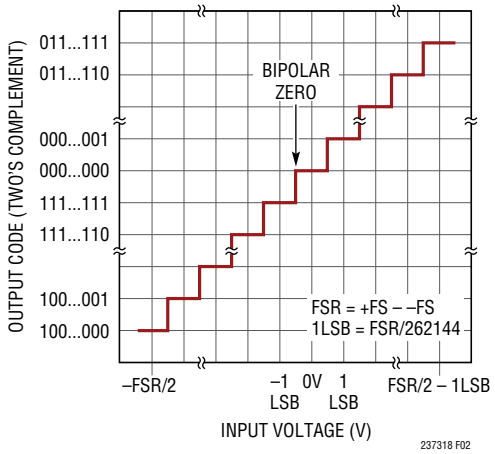


Figure 2. LTC2373-18 Two's Complement Transfer Function. Straight Binary Transfer Function Can Be Obtained by Inverting the Most Significant Bit (MSB) of Each Output Code

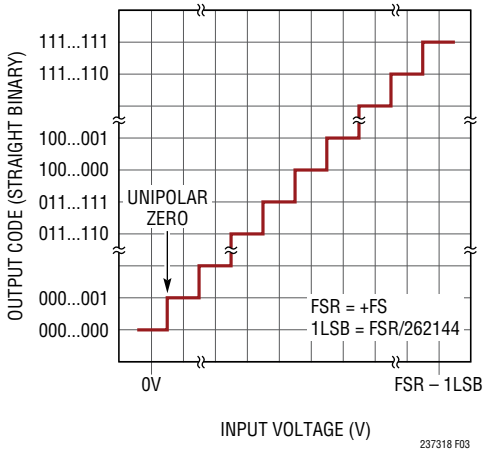


Figure 3. LTC2373-18 Straight Binary Transfer Function

APPLICATIONS INFORMATION

ANALOG INPUTS

The LTC2373-18 can be configured to accept one of three voltage ranges: fully differential (±4.096V), pseudo-differential unipolar (0V to 4.096V), and pseudo-differential bipolar (±2.048V). In all three ranges, the ADC samples and digitizes the voltage difference between the two ADC core analog input pins ($ADCIN^+ – ADCIN^–$), and any unwanted signal that is common to both inputs is reduced by the common mode rejection ratio (CMRR) of the ADC. The MUX outputs the voltages of the selected MUX analog input channels to $MUXOUT^{+/–}$, according to the MUX configuration. $MUXOUT^{+/–}$ may be wired directly to $ADCIN^{+/–}$ or connected through a buffer. Refer to the Configuring the LTC2373-18 section for details on how to select the analog input range and MUX channel configuration.

Independent of the selected range or channel configuration, the MUX analog inputs can be modeled by the equivalent circuit shown in Figure 4. CHx and CHy are distinct input pins selected from the CH0 to CH7 MUX analog inputs, depending on the MUX configuration. Each pin has ESD protection diodes. The ADC core analog inputs, $ADCIN^{+/–}$, each see a sampling network consisting of approximately 50pF (C_{IN}) from the sampling CDAC in series with 40Ω (R_{ON}) from the on-resistance of the sampling switch. The MUX is modeled by a 40Ω resistor representing the MUX switch on-resistance (R_{SW}) and a capacitance to ground, C_{PAR}, at the output summing node of the MUX. C_{PAR} is a lumped capacitance on the order of 20pF formed primarily by pin parasitics and diode junctions. Parasitic capacitances from the PCB will also contribute to C_{PAR}. This capacitance is discharged through a switch to ground every conversion cycle or when a first new configuration is programmed to minimize crosstalk due to charge sharing between channels.

During acquisition, each active MUX analog input sees a cascade of two first order lowpass filters formed by R_{SW}, C_{PAR} and the ADC sampling network when $MUXOUT^{+/–}$ is wired directly to $ADCIN^{+/–}$. If a buffer is inserted between $MUXOUT^{+/–}$ and $ADCIN^{+/–}$, then each active MUX analog input only sees a first order lowpass filter formed by R_{SW} and C_{PAR} that is loaded with the input impedance of the buffer.

Both C_{IN} and C_{PAR} draw current spikes while being charged during acquisition. If $MUXOUT^{+/–}$ is wired directly to $ADCIN^{+/–}$, the current spikes from the charging of both capacitors are drawn from the active MUX analog inputs. A buffer inserted between $MUXOUT^{+/–}$ and $ADCIN^{+/–}$ will absorb the current spike from C_{IN}, leaving the current spike from C_{PAR} to be drawn from the active MUX analog inputs. During conversion and sleep, the MUX analog inputs and ADC core analog inputs draw only a small leakage current.

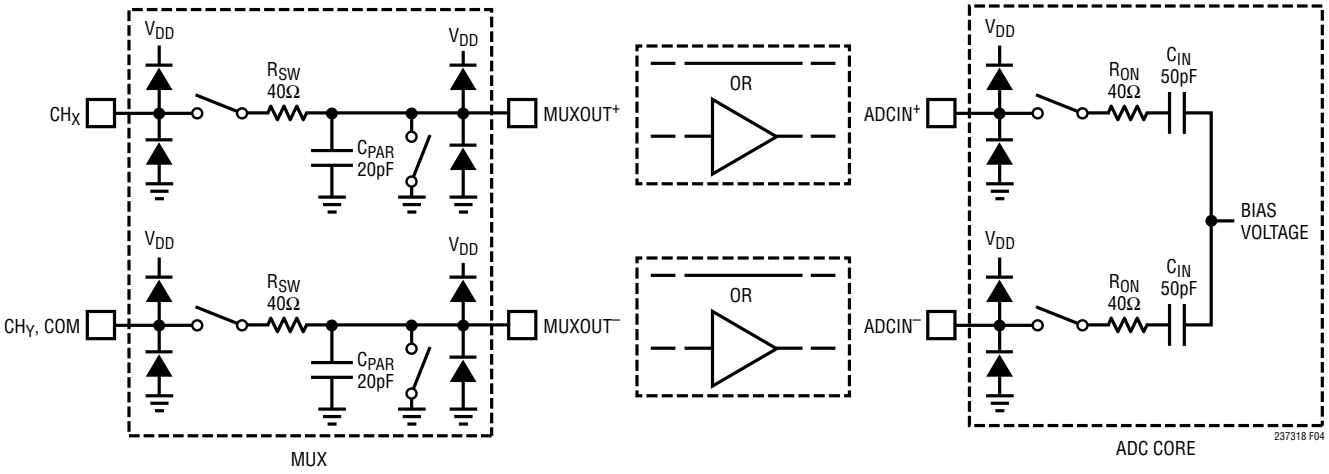


Figure 4. Equivalent Circuit for the Differential Analog Inputs of the LTC2373-18

APPLICATIONS INFORMATION

Fully Differential Input Range

The fully differential input range provides the widest input signal swing, configuring the ADC to digitize the differential analog input voltage to the ADC core ($ADCIN^+ - ADCIN^-$) provided through the selected MUX analog inputs over a span of $\pm V_{REFBUF}$. In this range, the $ADCIN^+$ and $ADCIN^-$ pins should be driven 180 degrees out-of-phase with respect to each other, centered around a common mode voltage ($(ADCIN^+ + ADCIN^-)/2$ that is restricted to ($V_{REFBUF}/2 \pm 0.1V$). Both the $ADCIN^+$ and $ADCIN^-$ pins are allowed to swing from (GND – 0.1V) to ($V_{REFBUF} + 0.1V$). Unwanted signals common to both inputs are reduced by the CMRR of the ADC. The output data format may be selected as straight binary or two's complement.

Pseudo-Differential Unipolar Input Range

In the pseudo-differential unipolar input range, the ADC digitizes the differential analog input voltage to the ADC core ($ADCIN^+ - ADCIN^-$) provided through the selected MUX analog inputs over a span of (0V to V_{REFBUF}). In this range, a single-ended unipolar input signal, driven on the $ADCIN^+$ pin, is measured with respect to the signal ground reference level, driven on the $ADCIN^-$ pin. The $ADCIN^+$ pin is allowed to swing from (GND – 0.1V) to ($V_{REFBUF} + 0.1V$), while the $ADCIN^-$ pin is restricted to (GND ± 0.1V). Unwanted signals common to both inputs are reduced by the CMRR of the ADC. The output data format is straight binary.

Pseudo-Differential Bipolar Input Range

In the pseudo-differential bipolar input range, the ADC digitizes the differential analog input voltage to the ADC core ($ADCIN^+ - ADCIN^-$) provided through the selected MUX analog inputs over a span of ($\pm V_{REFBUF}/2$). In this range, a single-ended bipolar input signal, driven on the $ADCIN^+$ pin, is measured with respect to the signal mid-scale reference level, driven on the $ADCIN^-$ pin. The $ADCIN^+$ pin is allowed to swing from (GND – 0.1V) to ($V_{REFBUF} + 0.1V$), while the $ADCIN^-$ pin is restricted to ($V_{REFBUF}/2 \pm 0.1V$). Unwanted signals common to both inputs are reduced by the CMRR of the ADC. The output data format is two's complement.

INPUT DRIVE CIRCUITS

Whether $MUXOUT^{+/-}$ is wired directly to $ADCIN^{+/-}$ or through a buffer with high input impedance, the MUX analog inputs of the LTC2373-18 are high impedance. In either case, a low impedance source can directly drive the MUX analog inputs without gain error. A high impedance source should be buffered in both cases to minimize settling time during acquisition and to optimize ADC linearity.

For best performance, a buffer amplifier should be used to drive the MUX analog inputs of the LTC2373-18 with $MUXOUT^{+/-}$ wired directly to $ADCIN^{+/-}$. The amplifier provides low output impedance, which produces fast settling of the analog signal during the acquisition phase. It also provides isolation between the signal source and the current spikes drawn by the MUX analog inputs when entering acquisition.

Noise and Distortion

The noise and distortion of the buffer amplifiers and signal sources must be considered since they add to the ADC noise and distortion. Noisy input signals should be filtered prior to the inputs of the buffers driving the MUX analog inputs with an appropriate filter to minimize noise. The simple 1-pole RC lowpass filter (LPF1) shown in Figure 5 is sufficient for many applications.

Buffer amplifiers with low noise density must be selected to minimize SNR degradation. Coupling filter networks (LPF2) should be placed between the buffer outputs and MUX analog inputs to both minimize the noise contribution of the buffers and reduce disturbances reflected into the buffer from MUX analog input sampling transients. If a buffer amplifier is used between $MUXOUT^{+/-}$ and $ADCIN^{+/-}$, a coupling filter network (LPF3) should be placed between the buffer output and ADC core analog inputs to both minimize the noise contribution of the buffer and reduce disturbances reflected into the buffer from the ADC core analog input sampling transients. Long RC time constants at the MUX or ADC core analog inputs will slow down the settling of those inputs. Therefore, LPF2 and LPF3 typically require wider bandwidths than LPF1.

APPLICATIONS INFORMATION

Table 1 lists typical recommended values for the R and C of each LPF mentioned.

Table 1. Recommended R and C Values for Each Lowpass Filter

	Rx(Ω)	Cx(pF)	BANDWIDTH
LPF1	50	100000	31.8kHz
LPF2	10	1200	13MHz
LPF3	25	2700	2.4MHz

High quality capacitors and resistors should be used in the RC filters since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

Input Currents

One of the biggest challenges in coupling an amplifier to the LTC2373-18 is in dealing with current spikes drawn by the MUX and ADC core analog inputs at the start of each acquisition phase. LPF2 and LPF3 are examples of coupling filters that are used to both filter noise and reduce sampling transients due to the current spikes.

The MUX and ADC core analog inputs may be modeled as a switched capacitor load on the drive circuit. A drive circuit may rely partially on attenuating switched-capacitor current spikes with small filter capacitors C_{FILT} placed directly at the ADC inputs and partially on the driver amplifier having sufficient bandwidth to recover from the residual disturbance. Amplifiers optimized for DC performance may not have sufficient bandwidth to fully recover at the ADC's maximum conversion rate, which can produce nonlinearity and other errors. Coupling filter circuits may be classified in three broad categories:

Fully Settled: This case is characterized by filter time constants and an overall settling time that are considerably shorter than the sample period. When acquisition begins, the coupling filter is disturbed. For a typical first order RC filter, the disturbance will look like an initial step with an exponential decay. The amplifier will have its own response to the disturbance, which may include ringing. If the input settles completely (to within the accuracy of the LTC2373-18), the disturbance will not contribute any error.

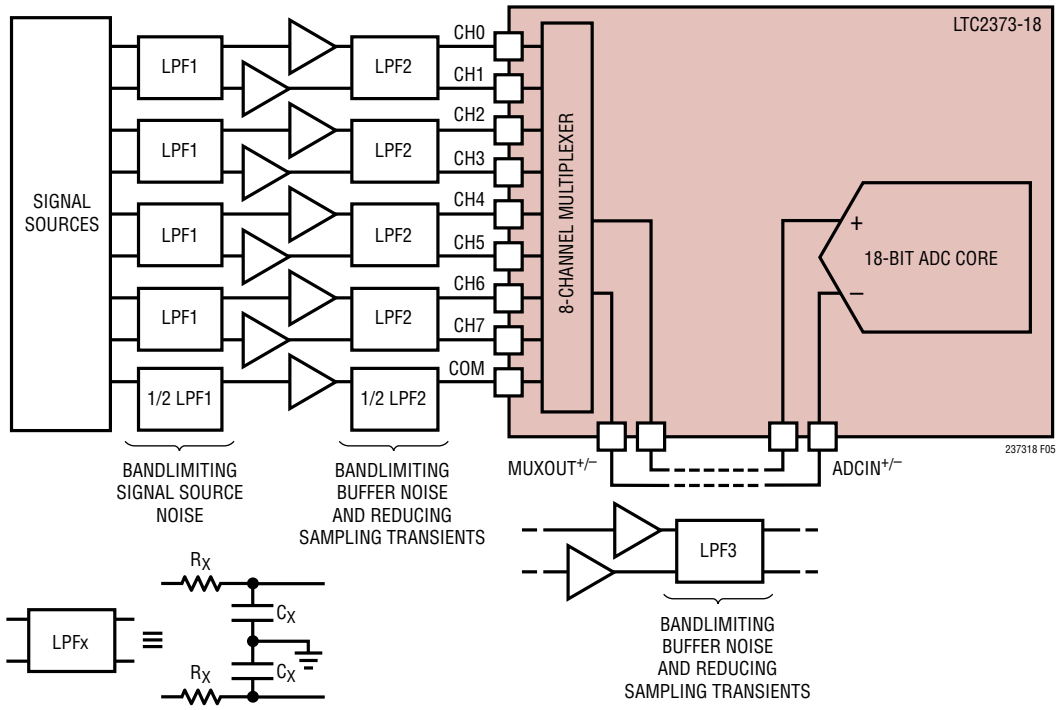


Figure 5. Input Signal Chain

APPLICATIONS INFORMATION

Partially Settled: In this case, the beginning of acquisition causes a disturbance of the coupling filter, which then begins to settle out towards the nominal input voltage. However, acquisition ends (and the conversion begins) before the input settles to its final value. This generally produces a gain error, but as long as the settling is linear, no distortion is produced. The coupling filter's response is affected by the amplifier's output impedance and other parameters. A linear settling response to fast switched-capacitor current spikes can NOT always be assumed for precision, low bandwidth amplifiers. The coupling filter serves to attenuate the current spikes' high frequency energy before it reaches the amplifier.

Fully Averaged: Consider the case where MUXOUT$^{+/-}$ is directly wired to ADCIN$^{+/-}$. If the coupling filter's capacitors (C_{FILT}) at the MUX analog inputs are much larger than the sum of the ADC's sample capacitors (50pF) and the MUX's output summing node capacitances (20pF), then the sampling glitch is greatly attenuated. The driving amplifier effectively only sees the average sampling current, which is quite small. At 1Msps, the equivalent input resistance is approximately 14k (as shown in Figure 6), a benign resistive load for most precision amplifiers. However, resistive voltage division will occur between the coupling filter's DC resistance and MUX's equivalent (switched-capacitor) input resistance, thus producing a gain error.

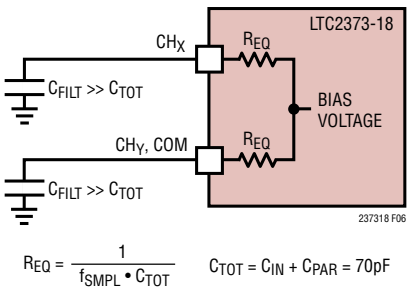


Figure 6. Equivalent Circuit for the MUX Analog Inputs of the LTC2373-18 at 1Msps

Crosstalk

Crosstalk is a typical concern in systems that employ multiplexers. The LTC2373-18 features a low crosstalk 8-channel MUX. There are two forms of crosstalk in the LTC2373-18 that potentially allow the signal from one channel to corrupt the signal from another channel being sampled.

The first form of crosstalk is often referred to as static crosstalk. In static crosstalk, a signal applied to an OFF channel, $V_{INTERFERER}$, couples capacitively into the input signal path, thus corrupting the input signal of the ON channel, V_{SIGNAL}. Figure 7 shows an RC model of two MUX input channels and the associated parasitic capacitances. Capacitive coupling from an OFF channel into the input signal path can occur through C_{SW} of an OFF switch to the MUXOUT$^{+/-}$ output pins or through C_{PIN} to an adjacent input pin or the MUXOUT$^{+/-}$ output pins. Coupling through C_{PIN} to the MUXOUT$^{+/-}$ pins is the dominant coupling mechanism that limits the crosstalk to –107dB with a 100kHz input signal applied to an OFF CH3 or CH4. These pins sit adjacent to the MUXOUT^{+} and MUXOUT^{-} pins, respectively.

The second form of crosstalk is referred to as adjacent channel crosstalk, which has to do with memory from the input of one channel affecting the sampled value of another channel. In this case, C_{PAR} at the output summing nodes of the MUX, MUXOUT$^{+/-}$, can act as memory storage elements if not dealt with properly. The potential crosstalk mechanism here is through charge sharing. C_{PAR} is charged approximately to the voltage of each channel that is sampled. If that charge is not cleared when switching from one channel to the next, then charge sharing between the charge on the filter capacitor (C_{FILT}) of one channel will occur with the charge from another channel stored on C_{PAR}. The unwanted charge from C_{PAR} can take a long time to settle out depending on the input filter bandwidth. C_{PAR} is discharged through a low impedance switch to ground every conversion cycle or when a first new configuration is programmed to mitigate this effect.

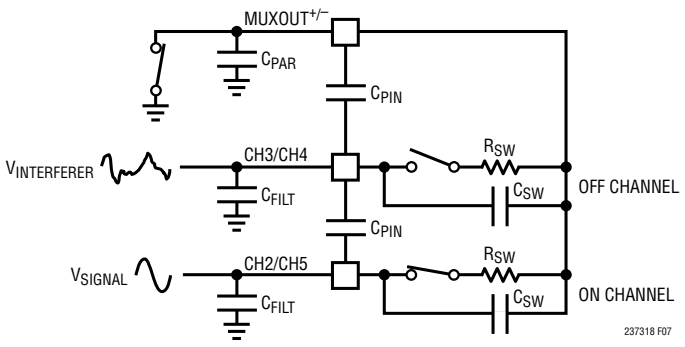


Figure 7. RC Equivalent Circuit for Two MUX Analog Input Channels

APPLICATIONS INFORMATION

Driving the MUX Analog Inputs

The LTC2373-18 can be programmed to accept fully differential or pseudo-differential input signals. In most applications, it is recommended that the LTC2373-18 be driven using the LT6237 ADC driver configured as two unity-gain buffers regardless of the input range, as shown in Figure 8a. The LT6237 combines fast settling and good DC linearity with a 1.1nV/$\sqrt{\text{Hz}}$ input-referred noise density, enabling it to achieve the full ADC data sheet SNR and THD specifications for all input ranges, as shown in the FFT plots in Figures 8b, 8c and 8d. The RC filter time constant is chosen to allow for sufficient transient settling of the LTC2373-18 MUX analog inputs during acquisition. With a maximum supply current of 7.8mA, the LT6237 is a perfect complement to the low power LTC2373-18.

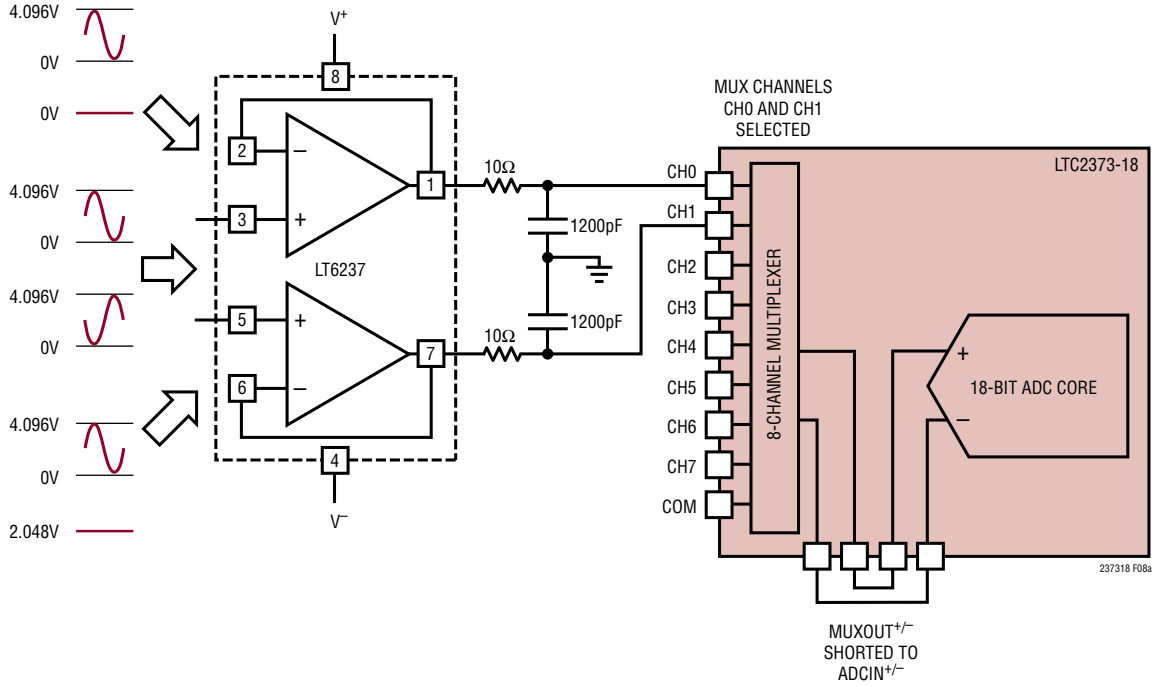


Figure 8a. LT6237 Buffering a Fully Differential or Pseudo-Differential Signal Source

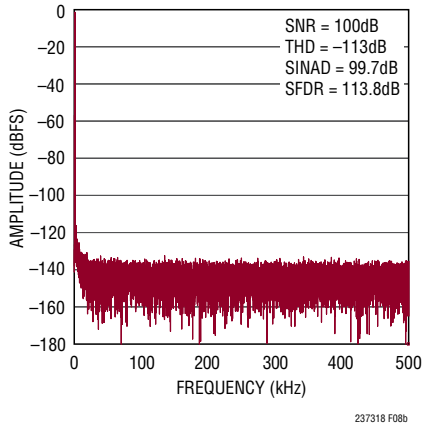


Figure 8b. 32k Point FFT f_{SMPL} = 1Msps, f_{IN} = 1kHz for Circuit Shown in Figure 8a; Driven with Fully Differential Inputs

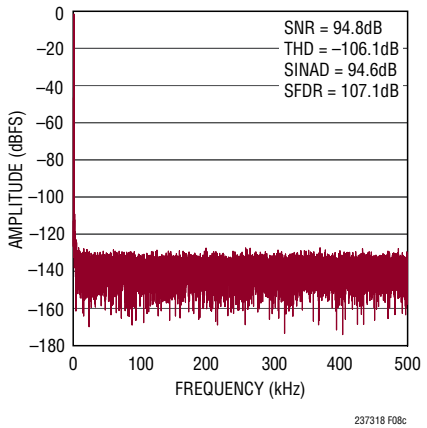


Figure 8c. 32k Point FFT f_{SMPL} = 1Msps, f_{IN} = 1kHz for Circuit Shown in Figure 8a; Driven with Unipolar Inputs

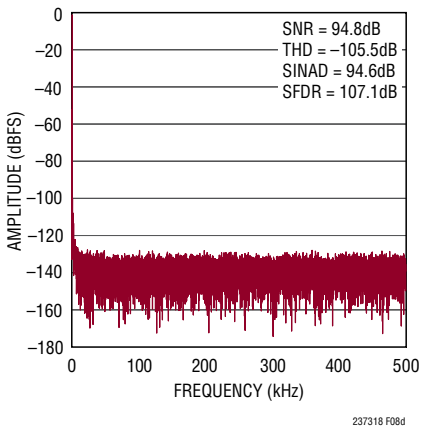


Figure 8d. 32k Point FFT f_{SMPL} = 1Msps, f_{IN} = 1kHz for Circuit Shown in Figure 8a; Driven with Bipolar Inputs

APPLICATIONS INFORMATION

Maximizing SNR with a Single-Ended to Differential Conversion

A single-ended input signal may be converted to a fully differential signal prior to driving the MUX analog inputs of the LTC2373-18 to take advantage of the higher SNR of the LTC2373-18 in the fully differential input range. The LT6350 ADC driver shown in Figure 9a can be used to convert a 0V to 4.096V input signal to a fully differential ±4.096V output signal. The RC time constant is larger in this case to limit the high frequency noise contribution of the LT6350. This topology provides a 5dB increase in SNR over single-ended operation and achieves the full data sheet SNR performance of the fully differential input range of 100dB as shown in the FFT plot in Figure 9b. The maximum supply current of 10.4mA makes the LT6350 a good companion to the low power LTC2373-18.

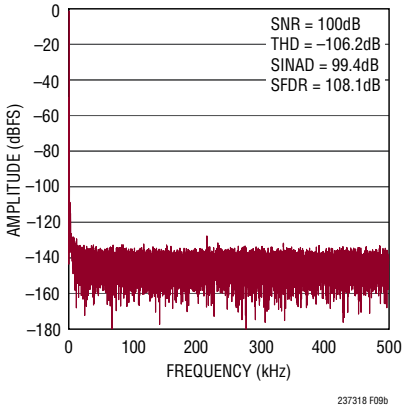


Figure 9b. 32k Point FFT f_{SMPL} = 1Msps, f_{IN} = 1kHz for Circuit Shown in Figure 9a

Maximizing SNR for Eight Single-Ended Inputs Using a Shared Amplifier Between MUXOUT+/– and ADCIN+/–

While converting a single-ended signal to a fully differential signal offers the benefit of higher SNR, two input channels are required per single-ended input, leading to a reduced number of single-ended input signals that can be interfaced to the LTC2373-18. Performing the single-ended to differential conversion using the LT6237

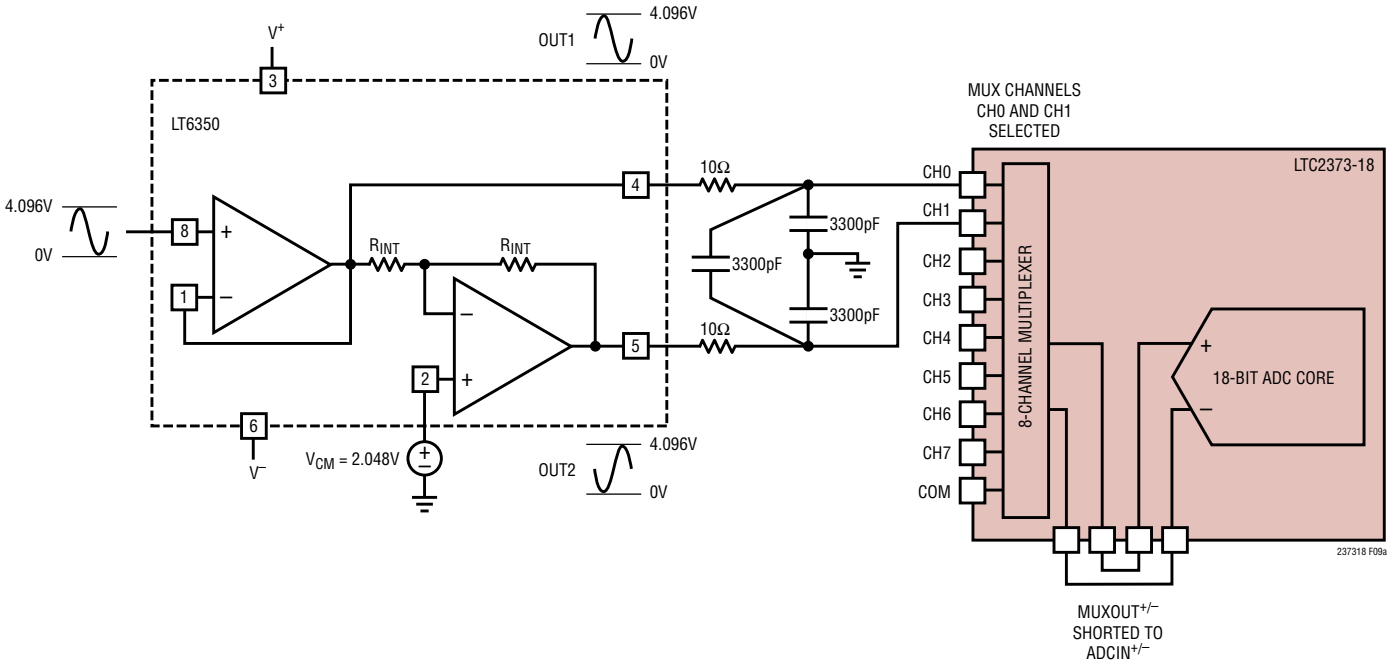


Figure 9a. LT6350 Converting a 0V to 4.096V Single-Ended Signal to a ±4.096V Fully Differential Signal

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between MUXOUT$^{+/-}$ and ADCIN$^{+/-}$ as shown in Figure 10a provides the SNR benefits of the fully differential range without sacrificing additional MUX inputs to do so. Using the MUX configurations where CH0 to CH7 is output to MUXOUT^{+} and COM to MUXOUT^{-} enables eight single-ended inputs to be converted with the fully differential input range. The COM MUX input channel is used in the feedback connection of the buffer amplifier connected in a follower configuration to improve the distortion performance of the circuit. THD degradation would otherwise occur due to the non-linear voltage drop across the MUX switch from the input current of the buffer and the non-linear on-resistance of the MUX switch. The 1k resistor between COM and MUXOUT^{-} maintains negative feedback around the buffer when the MUX turns OFF, so that the buffer output does not rail. Eight single-ended inputs achieve an SNR of 99dB with this circuit as shown in Figure 10b, which is a 4dB improvement in SNR over single-ended operation.

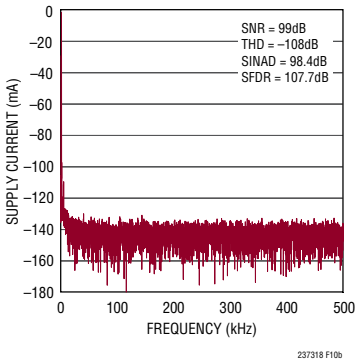


Figure 10b. 32k Point FFT f_{SMPL} = 1Msps, f_{IN} = 1kHz for Circuit Shown in Figure 10a

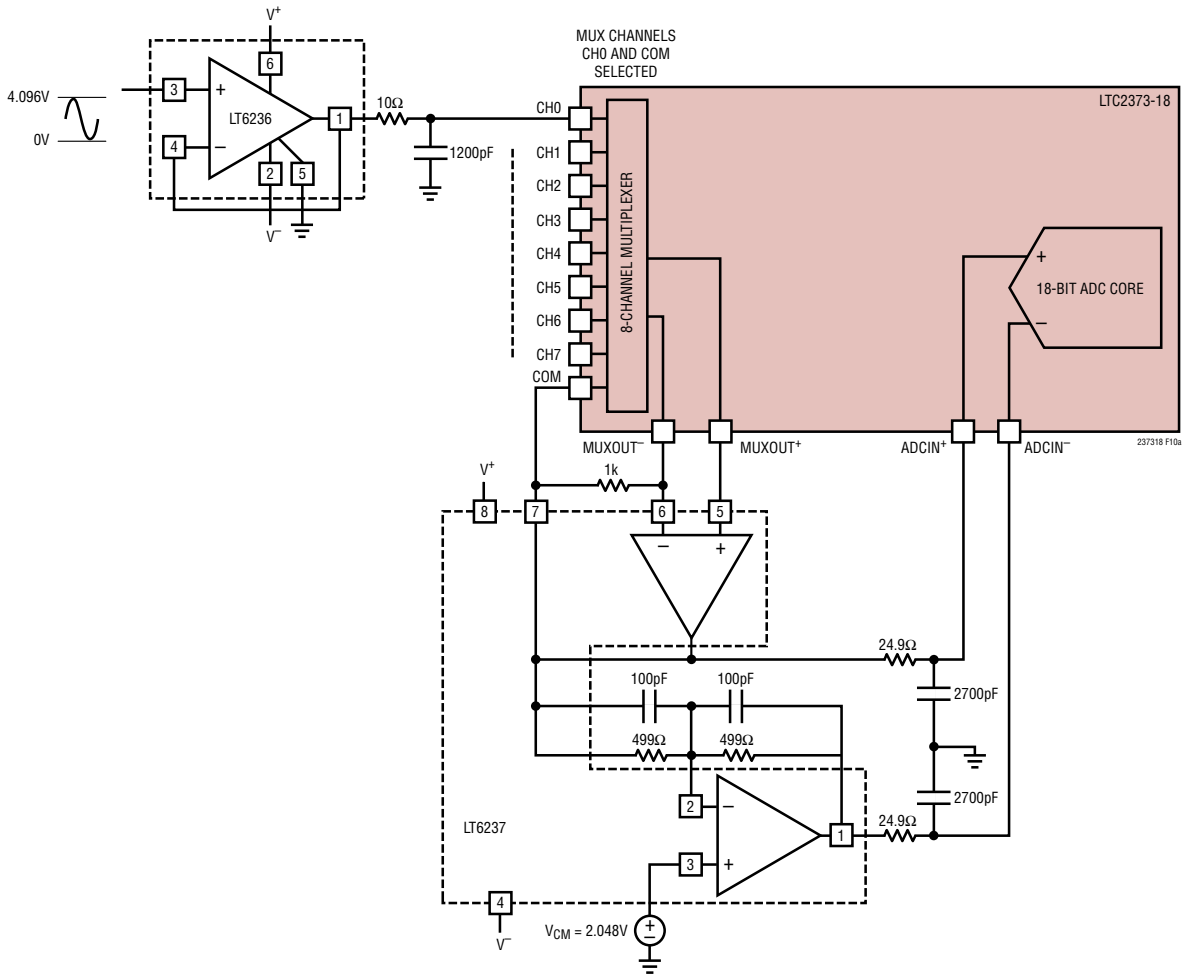


Figure 10a. LT6236 Buffering a Single-Ended 0V to 4.096V Input Signal and the LT6237 Configured to Perform a Single-Ended to Differential Conversion to the ±4.096V Fully Differential Input Range

APPLICATIONS INFORMATION

Using Digital Gain Compression for Single Supply Operation

The LTC2373-18 offers a digital gain compression (DGC) feature which defines the full-scale input swing to be between 10% and 90% of the $\pm V_{REFBUF}$ analog input range. This feature allows the ADC driver to be powered off of a single positive supply since each input swings between 0.41V and 3.69V with V_{REFBUF} = 4.096V as in Figure 11a. Needing only a positive supply and ground to power the ADC driver results in additional power savings for the entire system versus conventional systems that have a negative supply for the ADC driver.

With DGC enabled, the LTC2373-18 can be driven by the low power LTC6362 differential driver which is powered from a single 5V supply. Figure 11b shows how to configure the LTC6362 to accept a ±3.28V true bipolar single-ended input signal and level shift the signal to the reduced input range of the LTC2373-18 when digital gain compression is enabled. Using the LT6236 to buffer the resistor divider that creates V_{CM}, the entire signal chain solution can be powered from a single 5V supply, minimizing power consumption and reducing complexity. The reduced input signal swing of this single 5V supply solution limits the achievable SNR to 98dB, as shown in the FFT of Figure 11c. To enable DGC, set SEL=1 in the configuration word.

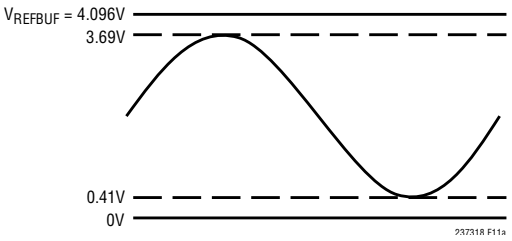


Figure 11a. Input Swing of the LTC2373-18 with Digital Gain Compression Enabled and V_{REFBUF} = 4.096V

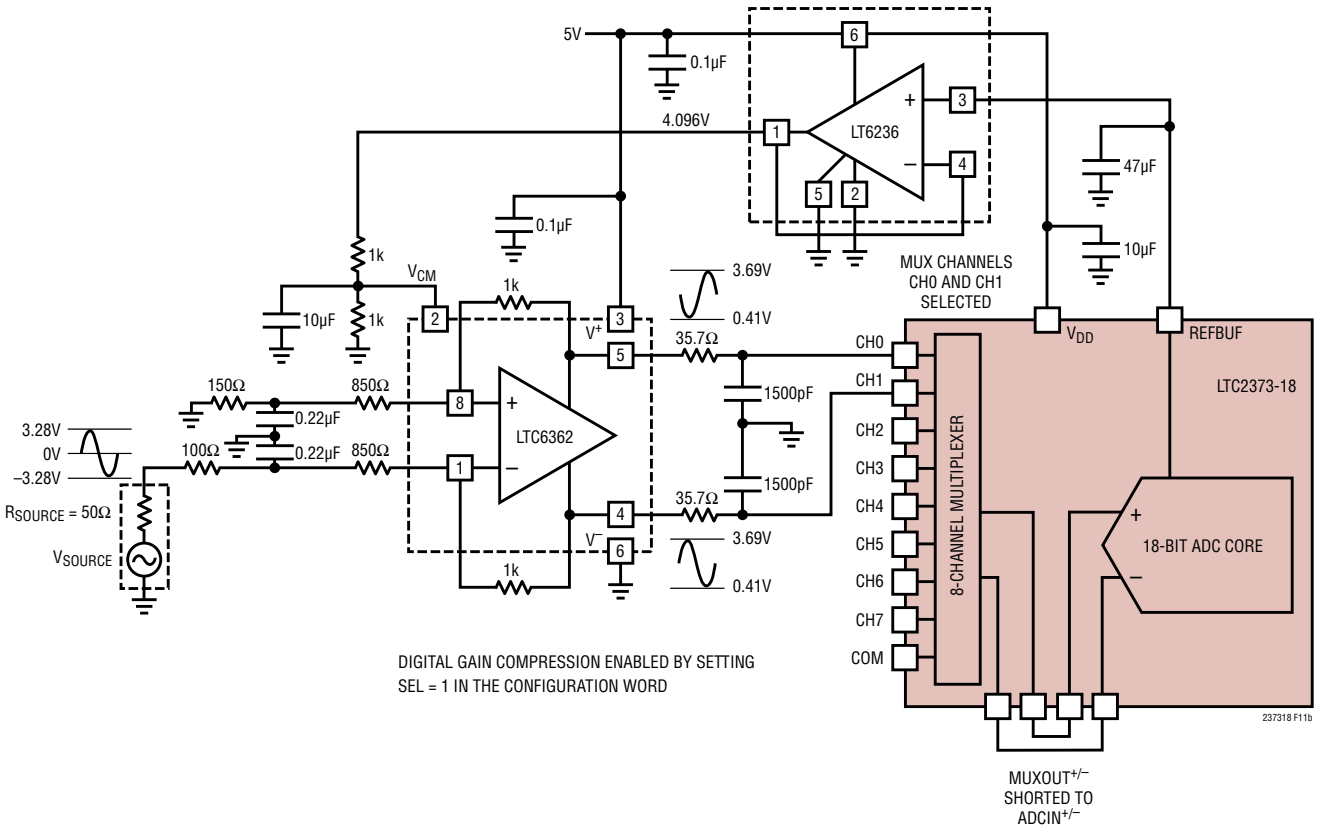


Figure 11b. LTC6362 Configured to Accept a ±3.28V Input Signal While Running from a Single 5V Supply When Digital Gain Compression is Enabled in the LTC2373-18

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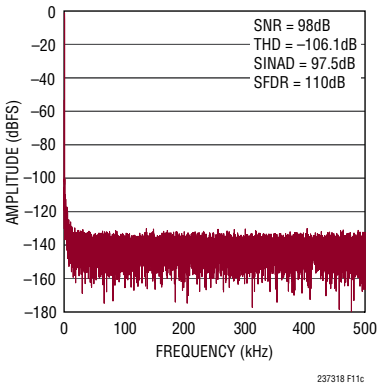


Figure 11c. 32k Point FFT f_{SMPL} = 1Msps, f_{IN} = 1kHz for Circuit Shown in Figure 11b

ADC REFERENCE

There are three ways of providing the ADC reference. The first is to use both the internal reference and reference buffer. The second is to externally overdrive the internal reference and use the internal reference buffer. The third is to disable the internal reference buffer and overdrive the REFBUF pin from an external source. The following tables give examples of these cases and the resulting fully differential, unipolar and bipolar input ranges.

Table 2. Internal Reference with Internal Buffer

REFIN	REFBUF	FULLY DIFFERENTIAL INPUT RANGE	UNIPOLAR INPUT RANGE	BIPOLAR INPUT RANGE
2.048V	4.096V	±4.096V	0V to 4.096V	±2.048V

Table 3. External Reference with Internal Buffer

REFIN (OVERDRIVE)	REFBUF	FULLY DIFFERENTIAL INPUT RANGE	UNIPOLAR INPUT RANGE	BIPOLAR INPUT RANGE
1.25 (Min)	2.5V	±2.5V	0V to 2.5V	±1.25V
2.048V	4.096V	±4.096V	0V to 4.096V	±2.048V
2.4V (Max)	4.8V	±4.8V	0V to 4.8V	±2.4V

Table 4. External Reference Unbuffered

REFIN	REFBUF	FULLY DIFFERENTIAL INPUT RANGE	UNIPOLAR INPUT RANGE	BIPOLAR INPUT RANGE
0V	2.5V (Min)	±2.5V	0V to 2.5V	±1.25V
0V	5V (Max)	±5V	0V to 5V	±2.5V

Internal Reference with Internal Buffer

The LTC2373-18 has an on-chip, low noise, low drift (20ppm/°C), temperature compensated bandgap reference that is factory trimmed to 2.048V. It is internally connected to a reference buffer as shown in Figure 12a and is available at REFIN (Pin 13). REFIN should be bypassed to GND with a 0.1µF ceramic capacitor to minimize noise. The reference buffer gains the REFIN voltage by 2 to 4.096V at REFBUF (Pin 12). Bypass REFBUF to GND with at least 47µF ceramic capacitor (X7R, 10V, 1210 size) to compensate the reference buffer and minimize noise.

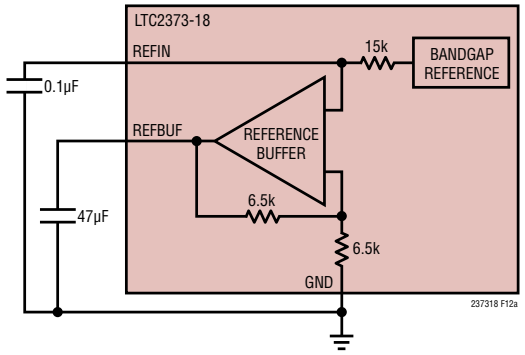


Figure 12a. LTC2373-18 Internal Reference Circuit

External Reference with Internal Buffer

If more accuracy and/or lower drift is desired, REFIN can be easily overdriven by an external reference since a 15k resistor is in series with the reference as shown in Figure 12b. REFIN can be overdriven in the range from 1.25V to 2.4V. The resulting voltage at REFBUF will be 2 × REFIN. Linear Technology offers a portfolio of high performance references designed to meet the needs of

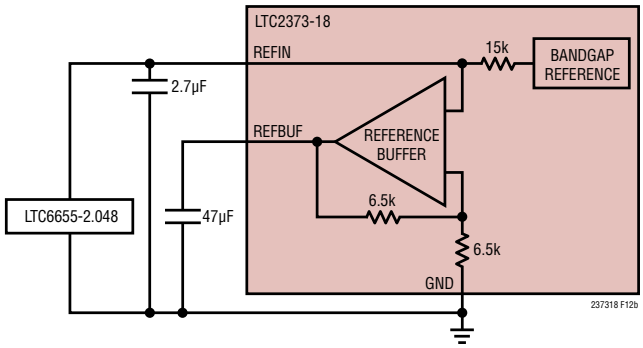


Figure 12b. Using the LTC6655-2.048 as an External Reference

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many applications. With its small size, low power, and high accuracy, the LTC6655-2.048 is well suited for use with the LTC2373-18 when overdriving the internal reference. The LTC6655-2.048 offers 0.025% (max) initial accuracy and 2ppm/°C (max) temperature coefficient for high precision applications. The LTC6655-2.048 is fully specified over the H-grade temperature range and complements the extended temperature range of the LTC2373-18 up to 125°C. Bypassing the LTC6655-2.048 with a 2.7µF to 100µF ceramic capacitor close to the REFIN pin is recommended.

External Reference Unbuffered

The internal reference buffer can also be overdriven from 2.5V to 5V with an external reference at REFBUF as shown in Figure 12c. To do so, REFIN must be grounded to disable the reference buffer. A 13k resistor loads the REFBUF pin when the reference buffer is disabled. To maximize the input signal swing and corresponding SNR, the LTC6655-5 is recommended when overdriving REFBUF. The LTC6655-5 offers the same small size, accuracy, drift and extended temperature range as the LTC6655-2.048. By using a 5V reference, an SNR of 102dB can be achieved. Bypassing the LTC6655-5 with a 47µF ceramic capacitor (X5R, 0805 size) close to the REFBUF pin is recommended.

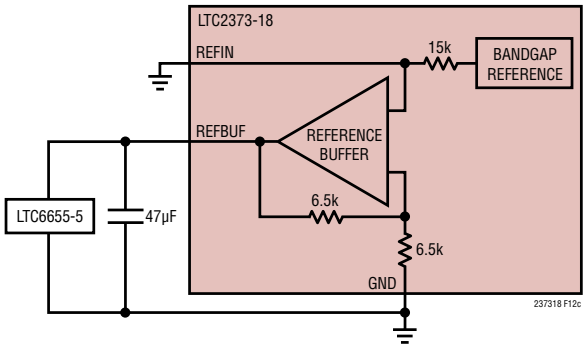


Figure 12c. Overdriving REFBUF Using the LTC6655-5

The REFBUF pin of the LTC2373-18 draws a charge (Q_{CONV}) from the external bypass capacitor during each conversion cycle. If the internal reference buffer is overdriven, the external reference must provide all of this charge with a DC current equivalent to $I_{REFBUF} = Q_{CONV}/t_{CYC}$. Thus, the DC current draw of REFBUF depends on the sampling rate and output code. In applications where a burst of samples is taken after idling for long periods, as shown in Figure 13, I_{REFBUF} quickly goes from approximately 380µA to a maximum of 1.5mA for REFBUF = 5V at 1Msps. This step in DC current draw triggers a transient response in the external reference that must be considered since any deviation in the voltage at REFBUF will affect the accuracy of the output code. If an external reference is used to overdrive REFBUF, the fast settling LTC6655-5 reference is recommended.

Internal Reference Buffer Transient Response

For optimum transient performance, the internal reference buffer should be used. The internal reference buffer uses a proprietary design that results in an output voltage change at REFBUF of less than 1LSB when responding to a sudden burst of conversions. This makes the internal reference buffer of the LTC2373-18 truly single-shot capable since the first sample taken after idling will yield the same result as a sample taken after the transient response of the internal reference buffer has settled. Figures 14a, 14b, and 14c show the transient responses of the LTC2373-18 with the internal reference buffer and with the internal reference buffer overdriven by the LTC6655-5, both with a bypass capacitance of 47µF in fully differential, pseudo-differential unipolar, and pseudo-differential bipolar input ranges, respectively.

DYNAMIC PERFORMANCE

Fast fourier transform (FFT) techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. The LTC2373-18 provides guaranteed tested limits for both AC distortion and noise measurements.

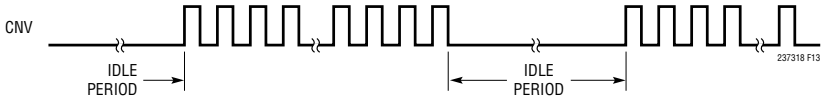


Figure 13. CNV Waveform Showing Burst Sampling

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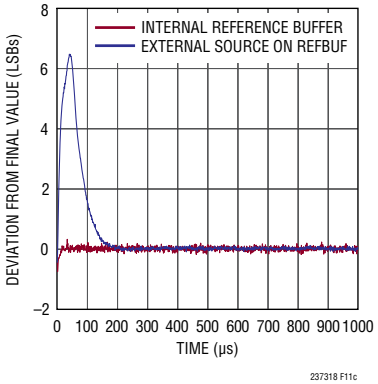


Figure 14a. Transient Response of the LTC2373-18 in the Fully Differential Input Range

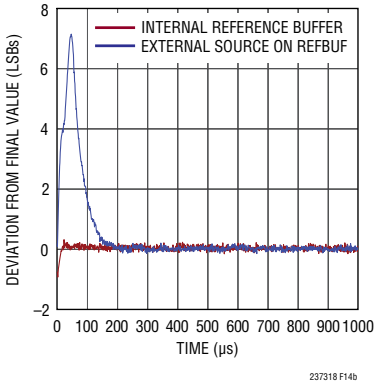


Figure 14b. Transient Response of the LTC2373-18 in the Pseudo-Differential Unipolar Input Range

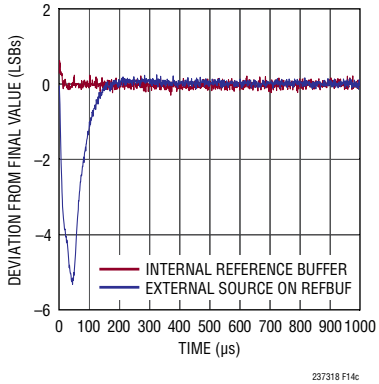


Figure 14c. Transient Response of the LTC2373-18 in the Pseudo-Differential Bipolar Input Range

Signal-to-Noise and Distortion Ratio (SINAD)

The signal-to-noise and distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from above DC and below half the sampling frequency. Figure 15 shows that the LTC2373-18 achieves a typical SINAD of 100dB (fully differential) at a 1MHz sampling rate with a 1kHz input.

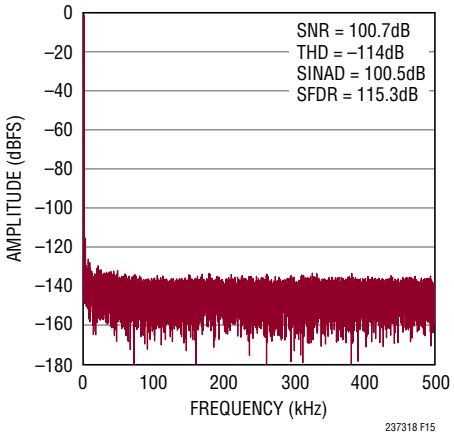


Figure 15. 32k Point FFT f_{SMPL} = 1Msps, f_{IN} = 1kHz

Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC. Figure 15 shows that the LTC2373-18 achieves a typical SNR of 100dB (fully differential) at a 1MHz sampling rate with a 1kHz input.

Total Harmonic Distortion (THD)

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency ($f_{SMPL}/2$). THD is expressed as:

$$THD = 20\log\frac{\sqrt{V2^2 + V3^2 + V4^2 + \ldots + V_N{}^2}}{V1}$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through V_N are the amplitudes of the second through Nth harmonics. Figure 15 shows that the LTC2373-18 achieves a typical THD of –114dB (fully differential) at a 1MHz sampling rate with a 1kHz input.

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POWER CONSIDERATIONS

The LTC2373-18 provides two power supply pins: the 5V power supply (V_{DD}), and the digital input/output interface power supply (OV_{DD}). The flexible OV_{DD} supply allows the LTC2373-18 to communicate with any digital logic operating between 1.8V and 5V, including 2.5V and 3.3V systems.

Power Supply Sequencing

The LTC2373-18 does not have any specific power supply sequencing requirements. Care should be taken to adhere to the maximum voltage relationships described in the Absolute Maximum Ratings section. The LTC2373-18 has a power-on-reset (POR) circuit that will reset the LTC2373-18 at initial power-up or whenever the power supply voltage drops below 2V. Once the supply voltage re-enters the nominal supply voltage range, the POR will reinitialize the ADC. No conversions should be initiated until 100ms after a POR event to ensure the reinitialization period has ended. Any conversions initiated before this time will produce invalid results.

TIMING AND CONTROL

CNV Timing

The LTC2373-18 conversion is controlled by CNV. A rising edge on CNV will start a conversion and power up the LTC2373-18. Once a conversion has been initiated, it cannot be restarted until the conversion is complete. For optimum performance, CNV should be driven by a clean low jitter signal. Converter status is indicated by the BUSY output which remains high while the conversion is in progress. To ensure that no errors occur in the digitized results, any additional transitions on CNV should occur within 40ns from the start of the conversion or after the conversion has been completed. Once the conversion has completed, the LTC2373-18 powers down and begins acquiring the input signal. It is not necessary to clock out all of the data and configuration bits before starting a new conversion.

Internal Conversion Clock

The LTC2373-18 has an internal clock that is trimmed to achieve a maximum conversion time of 527ns. With a minimum acquisition time of 460ns, throughput performance of 1Msps is guaranteed without any external adjustments.

Auto Nap Mode

The LTC2373-18 automatically enters nap mode after a conversion has been completed and completely powers up once a new conversion is initiated on the rising edge of CNV. During nap mode, only the ADC core powers down and all other circuits remain active. During nap, data from the last conversion can be clocked out. The auto nap mode feature will reduce the power dissipation of the LTC2373-18 as the sampling frequency is reduced. Since full power is consumed only during a conversion, the ADC core of the LTC2373-18 remains powered down for a larger fraction of the conversion cycle (t_{CYC}) at lower sample rates, thereby reducing the average power dissipation which scales with the sampling rate as shown in Figure 16.

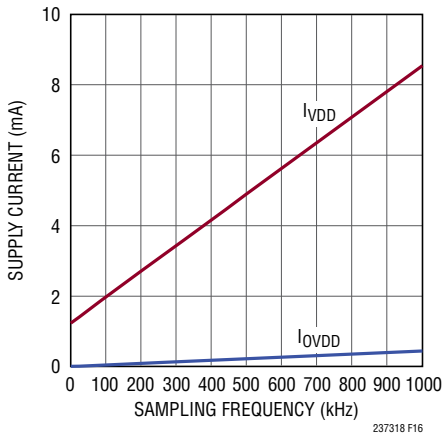


Figure 16. Power Supply Current of the LTC2373-18 vs Sampling Rate

Sleep Mode

The auto nap mode feature provides limited power savings since only the ADC core powers down. To obtain greater power savings, the LTC2373-18 provides a sleep mode. During sleep mode, the entire part is powered down except for a small standby current resulting in a power dissipation of 300µW. To enter sleep mode, toggle CNV twice with no intervening rising edge on SCK. The part will enter sleep mode on the falling edge of BUSY from the last conversion initiated. Once in sleep mode, a rising

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edge on SCK will wake the part up. Upon emerging from sleep mode, wait t_{WAKE} ms before initiating a conversion to allow the reference and reference buffer to wake-up and charge the bypass capacitors at REFIN and REFBUF. (Refer to the Timing Diagrams section for more detailed timing information about sleep mode.)

DIGITAL INTERFACE

The LTC2373-18 has a serial digital interface. The flexible OV_{DD} supply allows the LTC2373-18 to communicate with any digital logic operating between 1.8V and 5V, including 2.5V and 3.3V systems.

The serial data I/O bus is enabled when RDL is low. Serial output data is clocked out on the SDO pin and serial input configuration data is clocked in at the SDI pin when an external clock is applied to the SCK pin if the serial data I/O bus is enabled. Serial output data transitions on rising edges of SCK and serial input data is latched on rising edges of SCK. D17 remains valid till the first rising edge of SCK. After the 18 bits of the conversion result are shifted out, a start-of-sequence (SOS) bit followed by the 7-bit control word corresponding to the conversion result is shifted out. SDO will remain low after 26 SCK rising edges have been issued. Clocking out the data and configuration information after the conversion will yield the best performance. Table 5 lists the minimum shift clock frequency needed to achieve 1Msps throughput when shifting out a different number of bits.

Table 5. Minimum Shift Clock Frequency vs Number of Bits for 1Msps

	NUMBER OF BITS	f_{SCK}(MHz)
Conversion Result	18	41
Conversion Result + SOS Bit	19	44
Conversion Result + SOS Bit + Configuration Data	26	60

The configuration of the LTC2373-18 is programmed via a sequencer through the serial interface. The following sections describe the various ways the LTC2373-18 can be programmed, the operation of the sequencer and general use of the LTC2373-18.

Configuring the LTC2373-18

The various modes of operation of the LTC2373-18 are programmed by seven bits of an 8-bit control word, C[7:0]. The control word is shifted in at SDI on the rising edges of SCK, MSB first. The control word is defined as follows:

C[7]	C[6]	C[5]	C[4]	C[3]	C[2]	C[1]	C[0]
X	A[3]	A[2]	A[1]	A[0]	R[1]	R[0]	SEL

The MSB of the control word, C[7], is used during the programming of the sequencer and does not control the operating mode or configuration of the MUX or ADC (see Programming the Sequencer section). Referring to Table 6, bits A[3:0] (C[6:3]) control the analog input MUX channel configuration. Bits R[1:0] (C[2:1]) control the input range configuration of the ADC and the SEL (C[0]) bit enables/disables the digital gain compression feature (see Using Digital Gain Compression for Single Supply Operation section).

Table 6. Description of Decoded Configuration Bits

BITS	NAME	BEHAVIOR
[A3:A0]	MUX Channel Configuration Bits	See Table 7
[R1:R0]	Input Range Selection Bits	**00** – Pseudo-Differential Unipolar Input (Straight Binary Output Data Format) **01** – Pseudo-Differential Bipolar Input (Two's-Complement Output Data Format) **10** – Fully Differential Input (Straight Binary Output Data Format) **11** – Fully Differential Input (Two's-Complement Output Data Format)
SEL	Digital Gain Compression Bit	**0** – Digital Gain Compression Disabled **1** – Digital Gain Compression Enabled

Note: Digital gain compression feature always disabled for the pseudo-differential unipolar input range.

Analog Input Multiplexer

The analog input MUX is programmed by the A[3:0] (C[6:3]) bits of the input control word. Table 7 lists the MUX configurations for all combinations of the configuration bits. The selected positive (+) channel is output to $MUXOUT^+$ and the selected negative (–) channel is output to $MUXOUT^-$. Figure 17 shows an example of the MUX configuration being updated on successive conversions. Note how the voltages of the selected positive (+)

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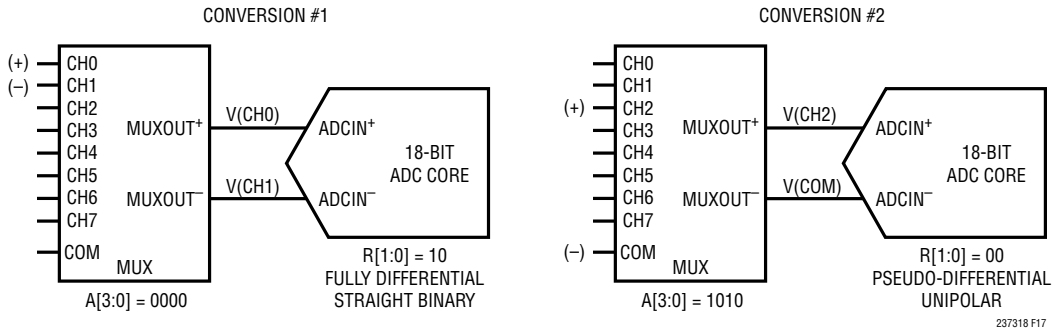


Figure 17. Changing the Configuration of the LTC2373-18 on Successive Conversions

and negative (–) channels are output at MUXOUT+ and MUXOUT–, respectively.

Table 7. Channel Configuration

MUX CONFIGURATION BITS				MULTIPLEXER CONFIGURATION								
A[3]	A[2]	A[1]	A[0]	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	0	+	–							
0	0	0	1			+	–					
0	0	1	0					+	–			
0	0	1	1							+	–	
0	1	0	0	–	+							
0	1	0	1			–	+					
0	1	1	0					–	+			
0	1	1	1							–	+	
1	0	0	0	+								–
1	0	0	1		+							–
1	0	1	0			+						–
1	0	1	1				+					–
1	1	0	0					+				–
1	1	0	1						+			–
1	1	1	0							+		–
1	1	1	1								+	–

Sequencer

The LTC2373-18 features a sequencer that can store up to 16 7-bit control words in internal memory. The 7-bit control word is defined in the Configuring the LTC2373-18 section. The sequencer repeatedly cycles through the control words stored in sequencer memory on successive conversions if no new valid control words are input to the part in a given transaction. The sequencer memory is shown in Figure 18a.

An internal memory pointer determines which of the up to 16 programmed control words is currently controlling the converter. The pointer is reset to point to the first programmed control word each time the sequencer memory is programmed. Upon reaching the final programmed control word stored in memory, the pointer is automatically reset to the first memory location and the sequence is restarted. At power-up or after resetting the LTC2373-18, the internal sequencer memory programming defaults to a depth of 1 with control word C0[6:0] = 0000000 (CH0+/CH1–, unipolar input range, digital gain compression disabled). Figure 18b shows the sequencer memory programmed with 8 configurations along with the memory pointer location for conversions run after programming.

Start of Sequence

The start of sequence (SOS) bit is output to SDO on the 19th SCK cycle during all SPI transactions and indicates whether the configuration for the conversion just performed corresponds to the control word stored in the first memory location of the sequencer memory. When SOS=1, the current configuration corresponds to the first memory location of the sequencer. The SOS bit can be used to align the conversion data with the corresponding control word when truncated SPI transactions are used to maximize throughput. Only one extra bit needs to be shifted out to maintain alignment of the configuration with the conversion data. This results in needing 19 SCK cycles instead of 26, which allows a higher throughput to be achieved while being able to keep the configuration information properly aligned with the conversion data.

APPLICATIONS INFORMATION

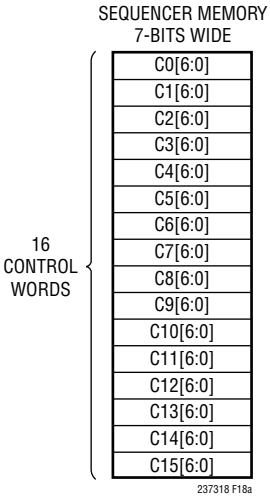


Figure 18a. Internal Sequencer Memory

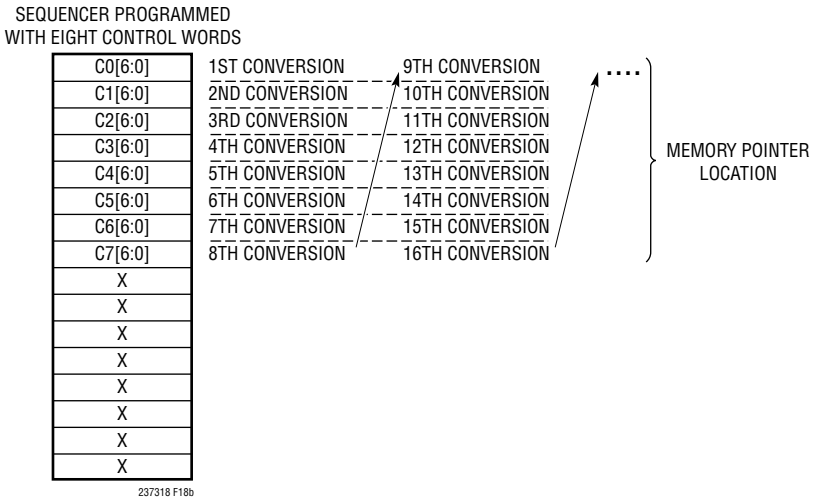


Figure 18b. Sequencer Programmed with Eight Control Words and the Memory Pointer Location for Conversions Run After Programming

Programming the Sequencer Transaction Window

A transaction window opens at power-up, after resetting the LTC2373-18, and every conversion cycle at the falling edge of BUSY, allowing the sequencer to be programmed. Once the transaction window opens, the state machine controlling the programming of the sequencer memory is in a reset state, waiting for control words to be shifted in at SDI. The transaction window closes at the start of the next conversion when BUSY transitions from low to high, as shown in Figure 19. Serial input data at SDI is ignored by the sequencer state machine when BUSY is high.

Input Control Word

The input control word is used to determine whether or not the sequencer is being programmed. In many cases the user will simply need to configure the converter once for their specific application after power-up or resetting the part, and then drive the SDI pin to GND. This will force the control word bits to all zeros and the converter will automatically sequence through the configurations stored in sequencer memory. The following sections provide further details on programming the sequencer.

The sequencer memory may be programmed by inputting one or more valid control words at SDI. Each control word is an 8-bit word as described in the Configuring the LTC2373-18 section. A valid input control word is one where C[7] = 1 and the remaining lower 7-bits, C[6:0], have been shifted in before the transaction window closes as shown in Figure 20a. When the 1st control word is successfully entered on the 8th rising edge of SCK, the sequencer memory is cleared, the new configuration, C[6:0], is written into the first memory location and is applied to the converter. At this point, a new acquisition window begins since the

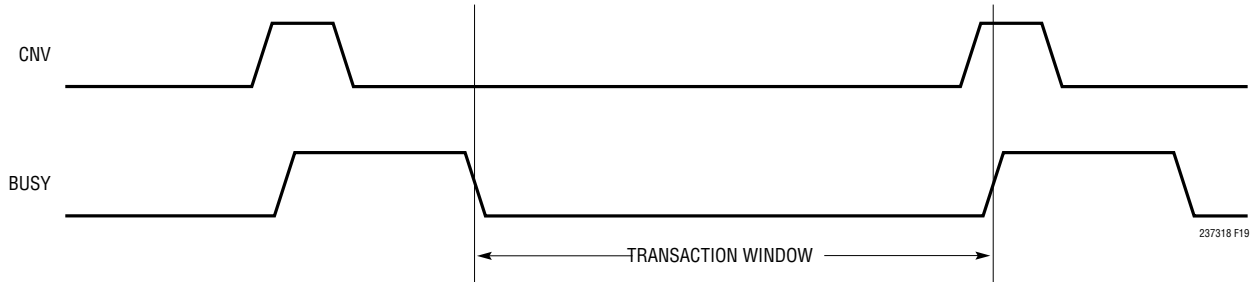


Figure 19. Sequencer Programming Transaction Window

APPLICATIONS INFORMATION

new configuration may result in a different channel being acquired. Additional valid input control words are written into subsequent memory locations. The sequencer only stores valid input control words and discards control words that are partially written or have C[7] = 0. If C[7] = 0 at any point during sequencer programming, the LTC2373-18 closes the input transaction window until the completion of the next conversion as shown in Figure 20b. Figure 21 shows a truncated programming transaction where the first partial input control word is discarded and the second complete input control word is successfully programmed. The transaction window also closes after 16 successive valid input control words have been written, since the sequencer memory has been filled.

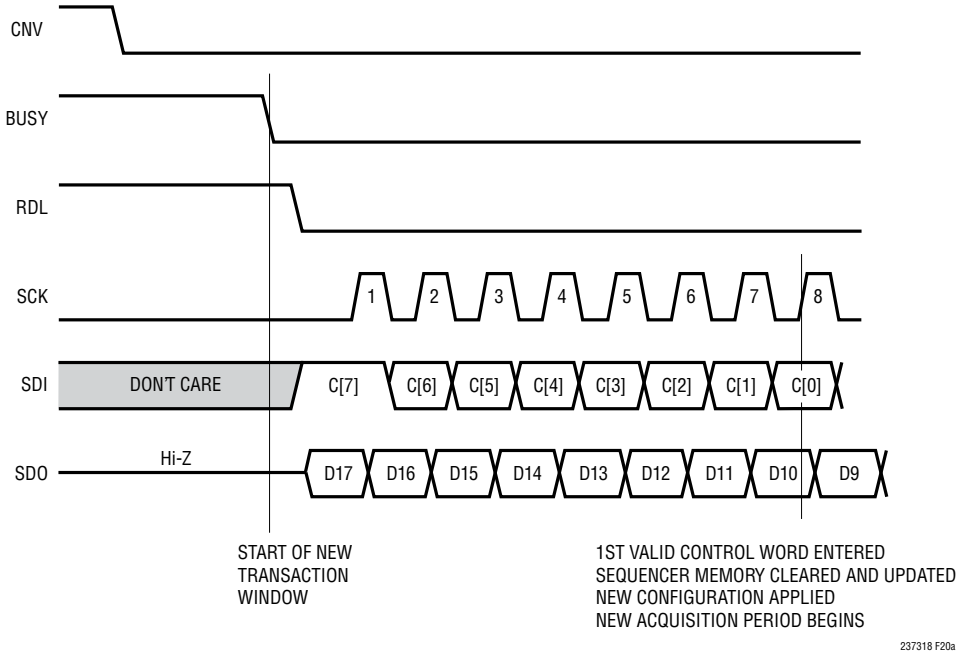


Figure 20a. Valid Control Word Successfully Programmed, C[7] = 1

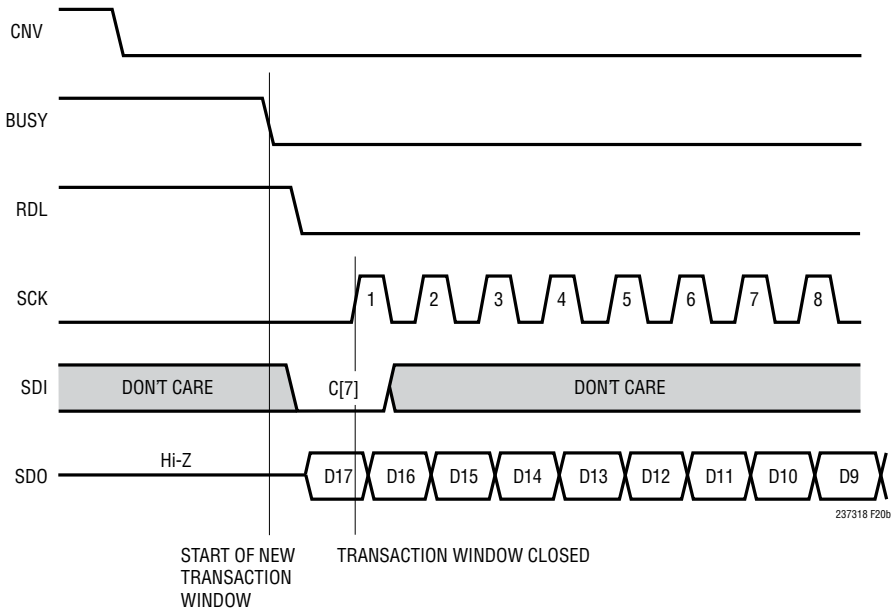


Figure 20b. Invalid Control Word Entered, C[7] = 0

APPLICATIONS INFORMATION

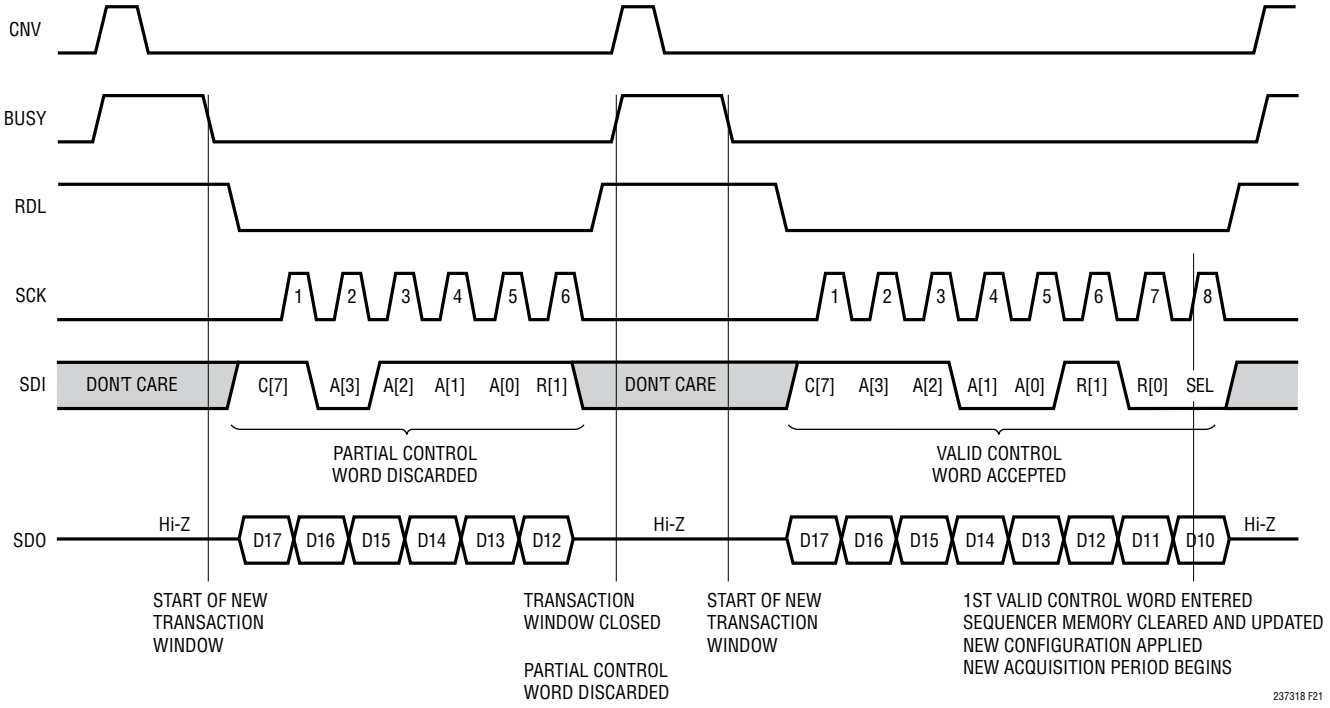


Figure 21. Truncated Programming Transaction Followed by the Successful Programming of One Configuration

APPLICATIONS INFORMATION

Programming the Sequencer with Two Configurations

Figure 22 illustrates the sequencer memory being programmed while reading out a conversion result. C[7] of the first two input control words is 1, so these control words are valid and are written to sequencer memory in succession. C[7] of the third control word is 0, so the input transaction is terminated at this point. Since there were only two valid control words entered, the sequencer memory is programmed with a depth of two. Figure 23 shows the state of the sequencer memory before, during and after the programming process. The first stored configuration will instruct the converter to sample a fully differential signal on the $CH7^+/CH6^-$ pair with digital gain compression disabled, and the second stored configuration will instruct the converter to sample a unipolar signal on the CH3/COM pair with digital gain compression disabled. The converter will then alternate between the two programmed configurations on successive conversions. Note that configurations stored in sequencer memory are retained until the power is cycled, the part is reset, or a new series of configuration programming words are input.

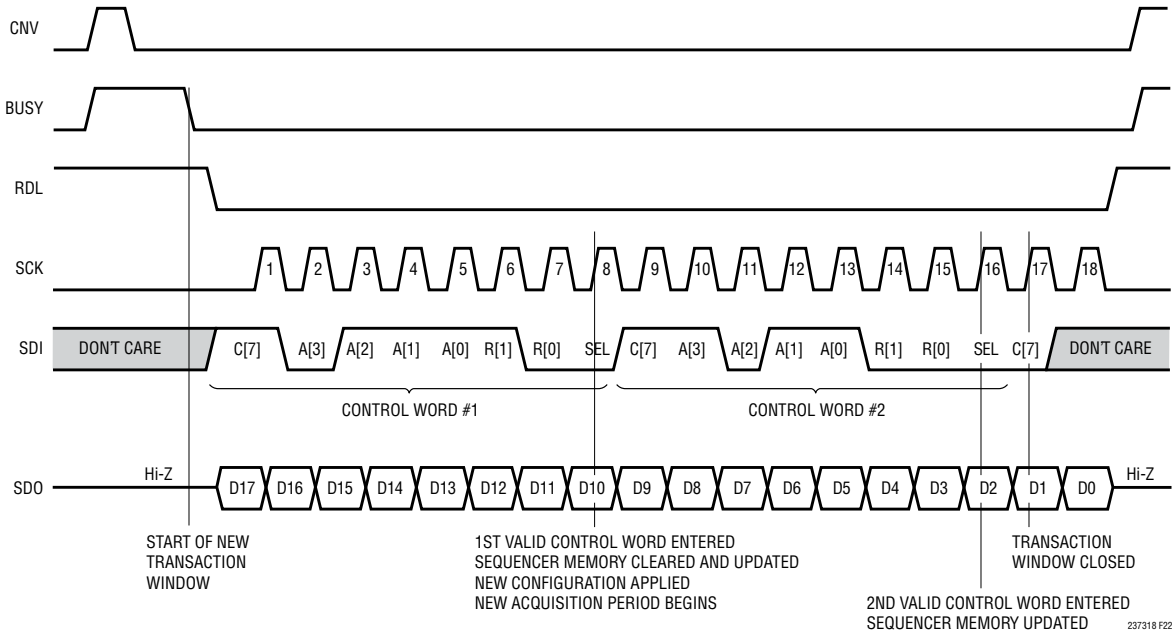


Figure 22. Sequencer Programmed with Two Control Words

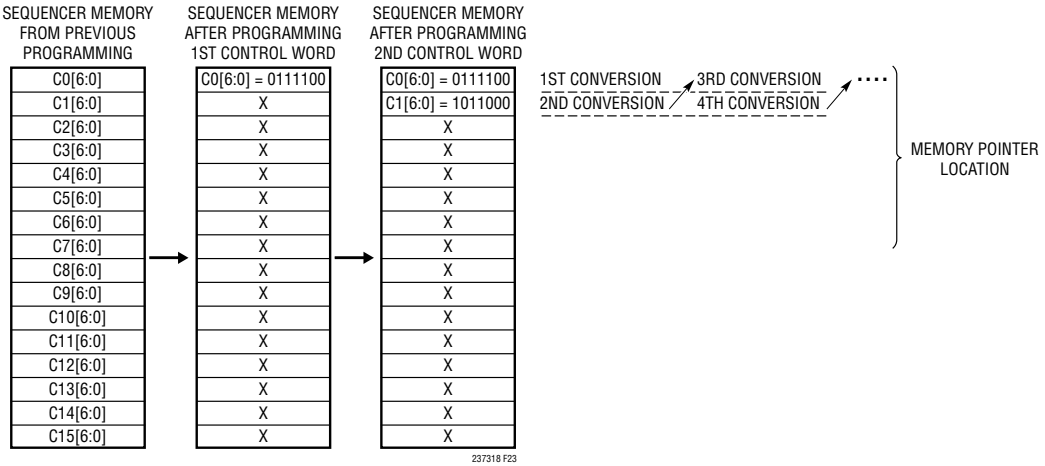


Figure 23. Sequencer Memory Before, During and After Programming

TIMING DIAGRAMS

MUX Reset Timing

The parasitic capacitances (C_{PAR}) on the output summing nodes of the MUX, MUXOUT$^{+/-}$, are discharged to ground every conversion cycle and when a first new valid configuration word is programmed into the sequencer. This is done to avoid crosstalk between input channels due to charge sharing from C_{PAR}. The bottom most waveform in Figure 24 represents the voltages of the MUX output nodes. The MUX is being reset when V(MUXOUT$^{+/-}$) sits at 0V.

The MUX turns OFF and begins resetting $t_{CNVMRST}$ ns after a conversion is initiated by the rising edge of CNV. After t_{MRST1} ns, the MUX turns ON to the next channel programmed in the sequencer.

The MUX also turns OFF and resets after $t_{VLDMRST}$ ns when a first new valid configuration word is programmed into the sequencer on the 8th rising edge of SCK. This is because the MUX may need to switch channels based on the newly input configuration, so memory of the previous channel needs to be cleared. A new acquisition period begins when the MUX is reconnected after t_{MRST2} ns.

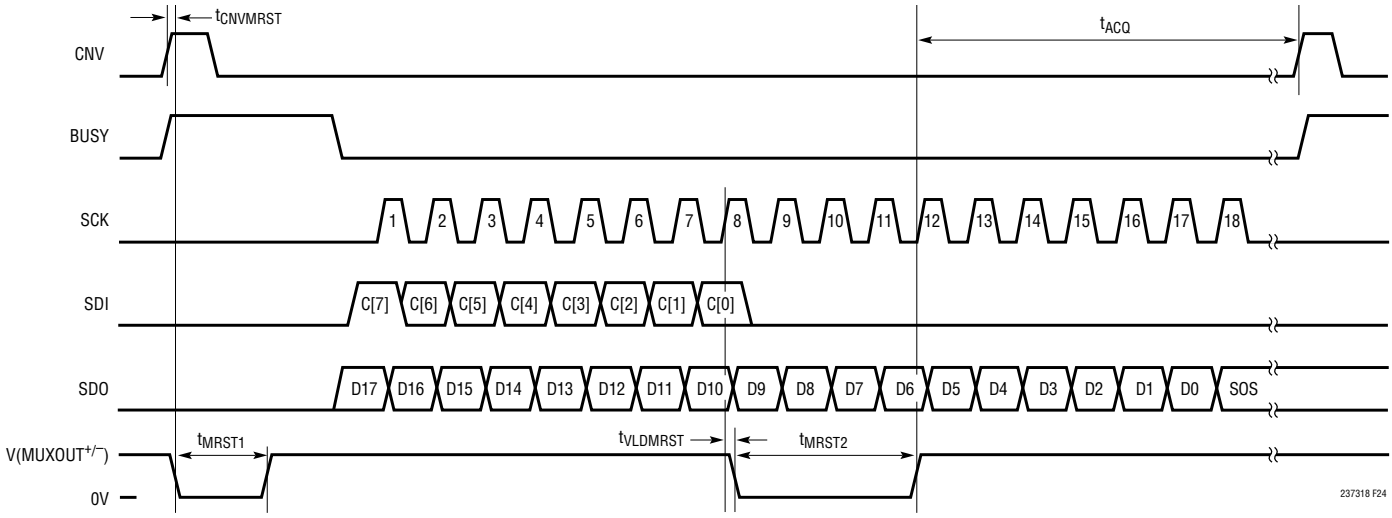


Figure 24. MUX Reset Timing

TIMING DIAGRAMS

Single Device, Sequencer Not Programmed

RDL enables or disables the serial data I/O bus. If RDL is high, the serial data I/O bus is disabled and the serial shift clock SCK is ignored. If RDL is low, SDO is driven and serial input data may be shifted in at SDI. Figure 25 shows a single LTC2373-18 operated with RDL and RESET tied to ground. With RDL grounded, the serial data I/O bus is enabled and the MSB(D17) of the new conversion data is available at the falling edge of BUSY. The start-of-sequence (SOS) bit followed by the current configuration is shifted out after the conversion data.

Bringing SDI low during data readback as shown closes the sequencer programming window at the first rising edge of SCK after the falling edge of BUSY since C[7] = 0. As a result, the sequencer is not programmed.

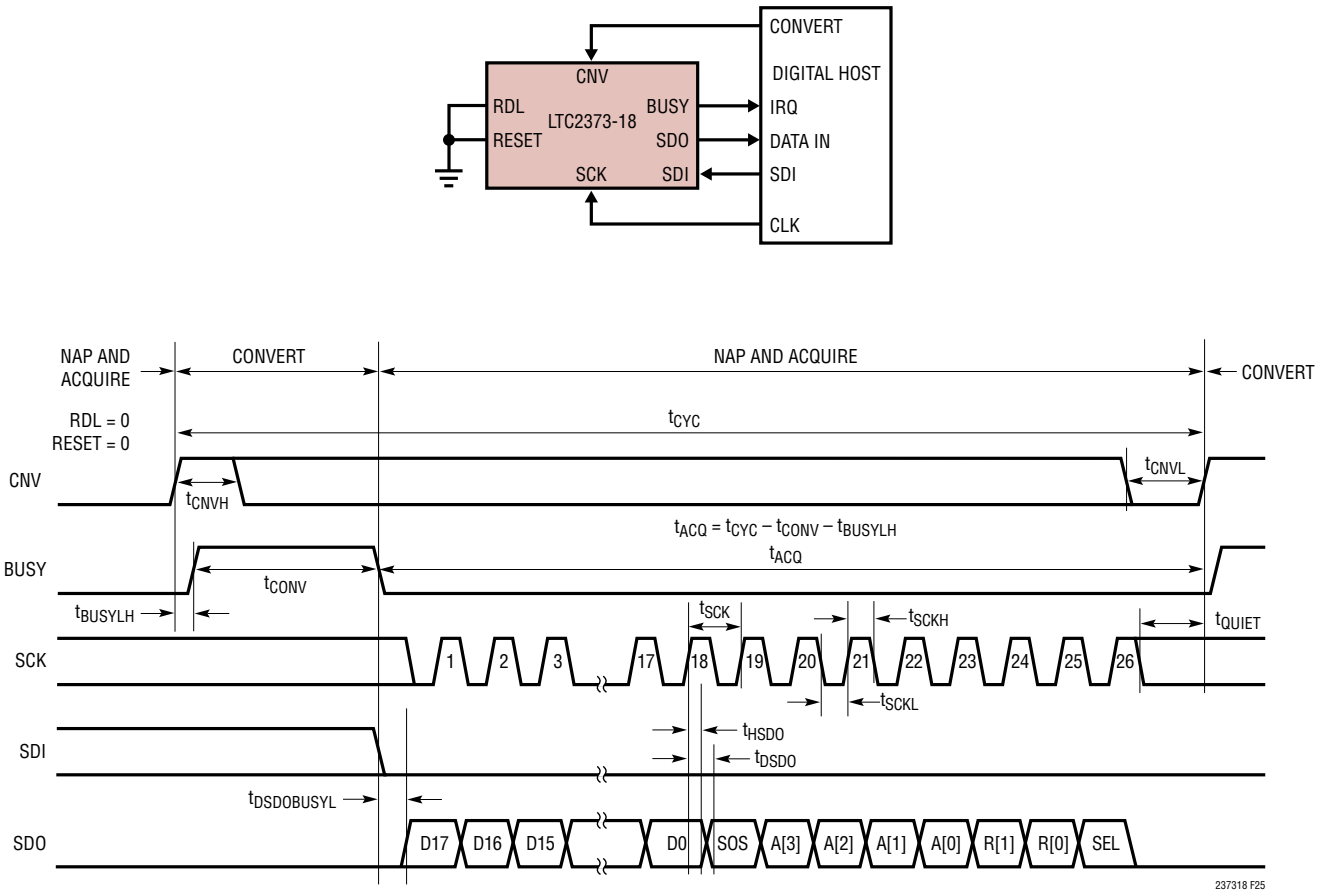


Figure 25. Using a Single LTC2373-18 without Programming the Sequencer

TIMING DIAGRAMS

Single Device, Sequencer Programmed

Figure 26 shows the timing for a single device being operated with RDL and RESET tied to ground. With RDL grounded, the serial data I/O bus is enabled and the MSB(D17) of the new conversion data is available at the falling edge of BUSY. The start-of-sequence (SOS) bit followed by the configuration used for the conversion just performed is shifted out after the new conversion data.

When SDI is high at the first rising edge of SCK after the falling edge of BUSY as shown, the sequencer programming window stays open, allowing the sequencer to be programmed. With the sequencer programming window open, a valid input configuration is detected on the 8th rising edge of SCK. At this point, the MUX turns OFF and resets and sequencer memory is reset and updated with the new configuration. The new channel configuration is applied when the MUX turns ON, marking the beginning of a new acquisition period.

'On the Fly' Device Programming

The sequencer may be programmed with one control word as shown in Figure 26 every conversion cycle to achieve complete flexibility in the multiplexer configuration, input range and digital gain compression setting on each conversion.

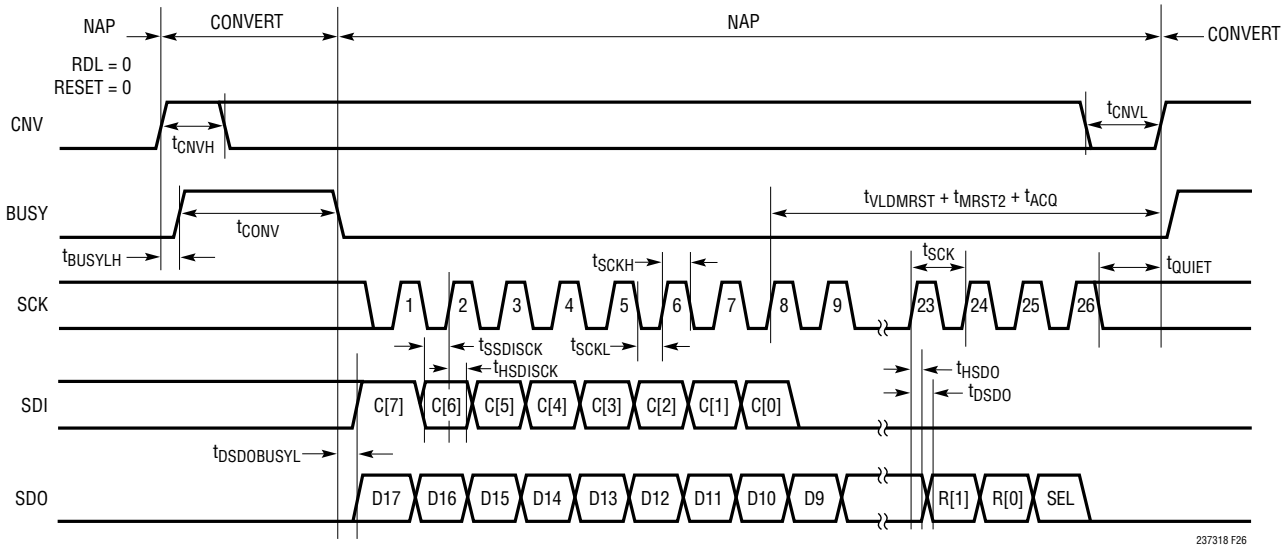


Figure 26. Using a Single LTC2373-18 Programming the Sequencer

TIMING DIAGRAMS

Multiple Devices

Figure 27 shows the multiple LTC2373-18 devices operating and sharing CNV, SDI, SCK and SDO. By sharing CNV, SDI, SCK and SDO, the number of signals required to operate multiple ADCs in parallel is reduced. Since SDO is shared, the RDL input of each ADC must be used to allow only one LTC2373-18 to drive SDO at a time in order to avoid bus conflicts. RDL must also be used to selectively program each ADC through the shared SDI input line. The RDL inputs idle high and are individually brought low to read data out of and selectively program each device between conversions. When RDL is brought low, the MSB(D17) of the selected device is output onto SDO.

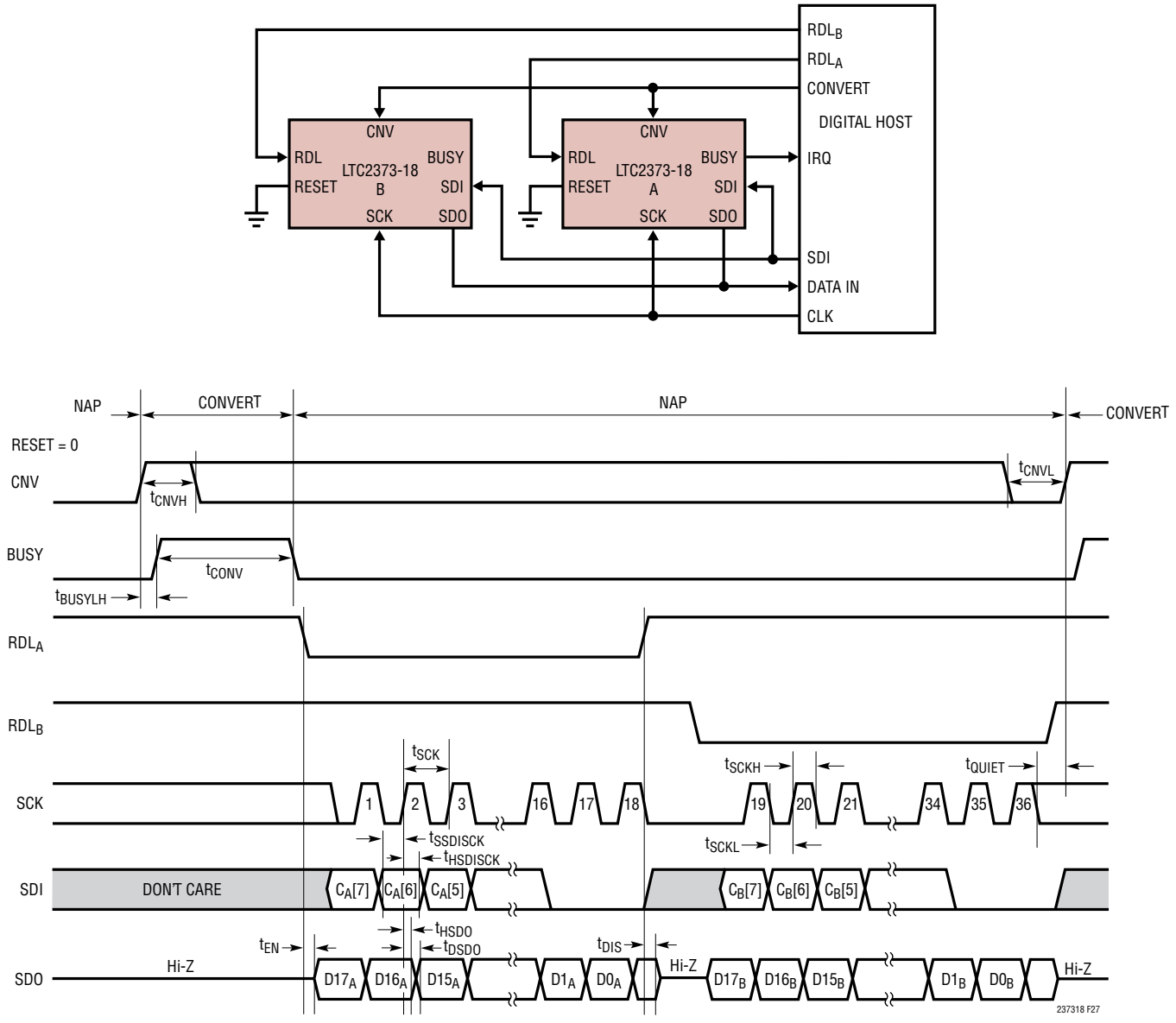


Figure 27. Multiple Devices Sharing CNV, SCK and SDO

TIMING DIAGRAMS

Sleep Mode

The LTC2373-18 automatically naps and starts acquiring the input once a conversion has completed. Only the ADC core powers down in nap mode. As a result, the auto nap feature provides limited power savings. To obtain greater power savings, the LTC2373-18 provides a sleep mode. During sleep mode, the entire part is powered down except for a small standby current resulting in a 300µW power dissipation. To enter sleep mode, toggle CNV twice with no intervening rising edge on SCK as shown in Figure 28. The part will enter sleep mode on the falling edge of BUSY from the last conversion initiated. Once in sleep mode, a rising edge on SCK will wake the part up. Upon emerging from sleep mode, wait t_{WAKE} ms before initiating a conversion to allow the reference and reference buffer to wake-up and charge the bypass capacitors at REFIN and REFBUF. The serial data I/O bus is enabled or disabled by RDL during sleep mode. Sleep mode does not affect the state of the sequencer memory or memory pointer.

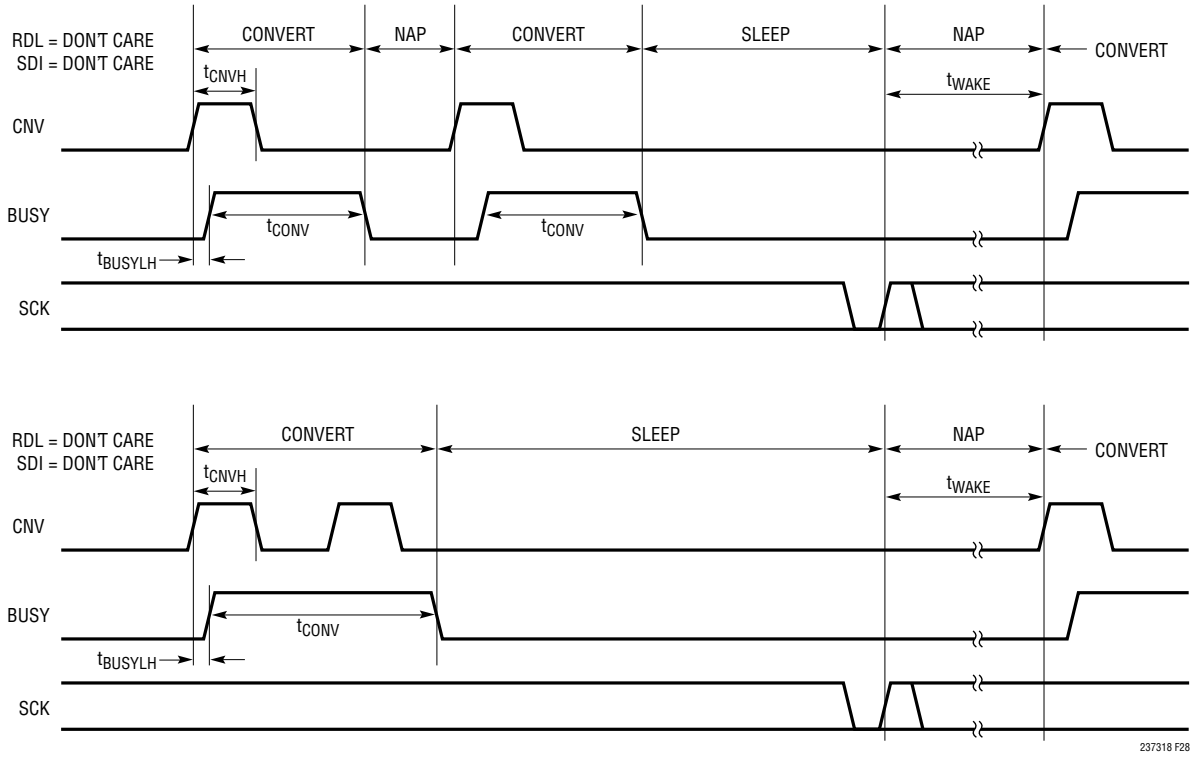


Figure 28. Sleep Mode Timing Diagram

TIMING DIAGRAMS

RESET Timing

When the RESET pin is high, the LTC2373-18 is reset and the serial I/O data bus is put into a high impedance mode, as shown in Figure 29. The serial data output register and sequencer memory are also cleared and set to their default states. If this occurs during a conversion, the conversion is immediately halted. During reset, requests for new conversions are ignored. Once RESET returns low, the LTC2373-18 is ready to start a new conversion after the acquisition time has been met.

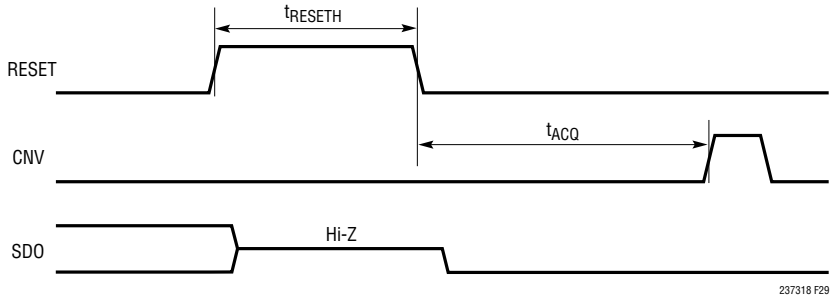


Figure 29. RESET Pin Timing

BOARD LAYOUT

To obtain the best performance from the LTC2373-18 a printed circuit board is recommended. Layout for the printed circuit board (PCB) should ensure the digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital clocks or signals alongside analog signals or underneath the ADC.

Recommended Layout

The following is an example of a recommended PCB layout. A single solid ground plane is used. Bypass capacitors to the supplies are placed as close as possible to the supply pins. Low impedance common returns for these bypass capacitors are essential to the low noise operation of the ADC. The analog input traces are screened by ground. For more details and information refer to DC2071, the evaluation kit for the LTC2373-18.

BOARD LAYOUT

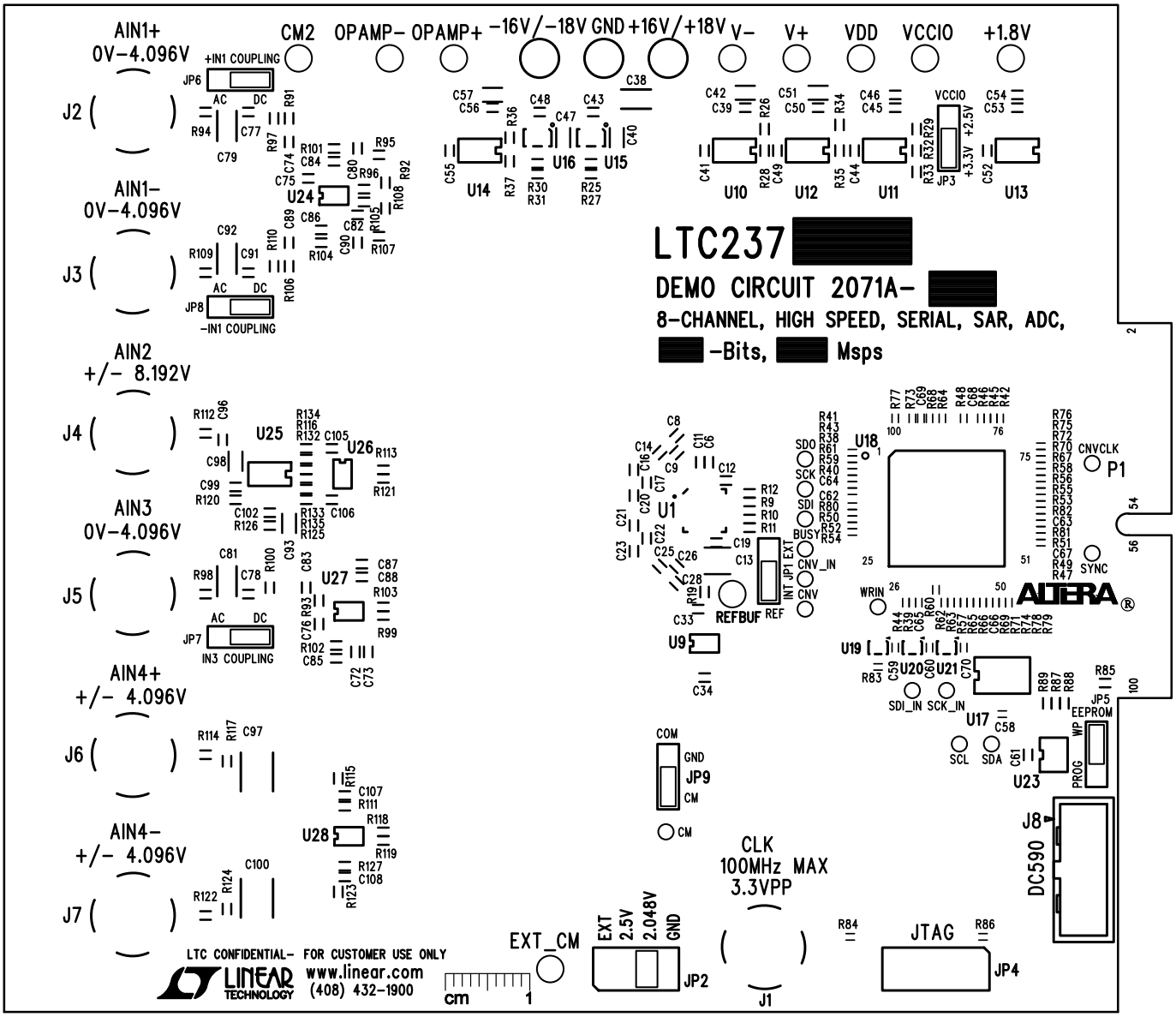


Figure 30. Top Silkscreen

BOARD LAYOUT

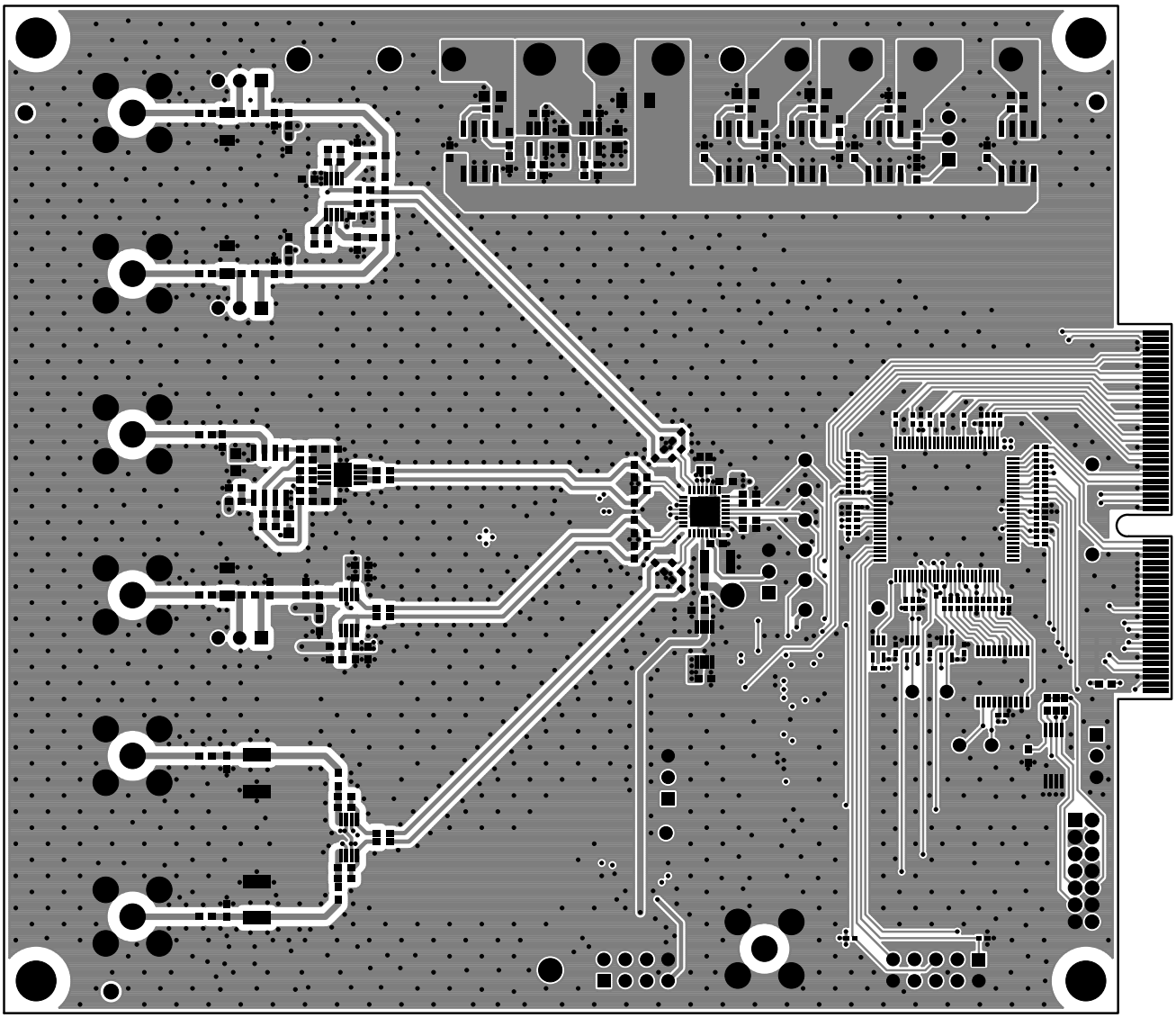


Figure 31. Layer 1 Component Side

BOARD LAYOUT

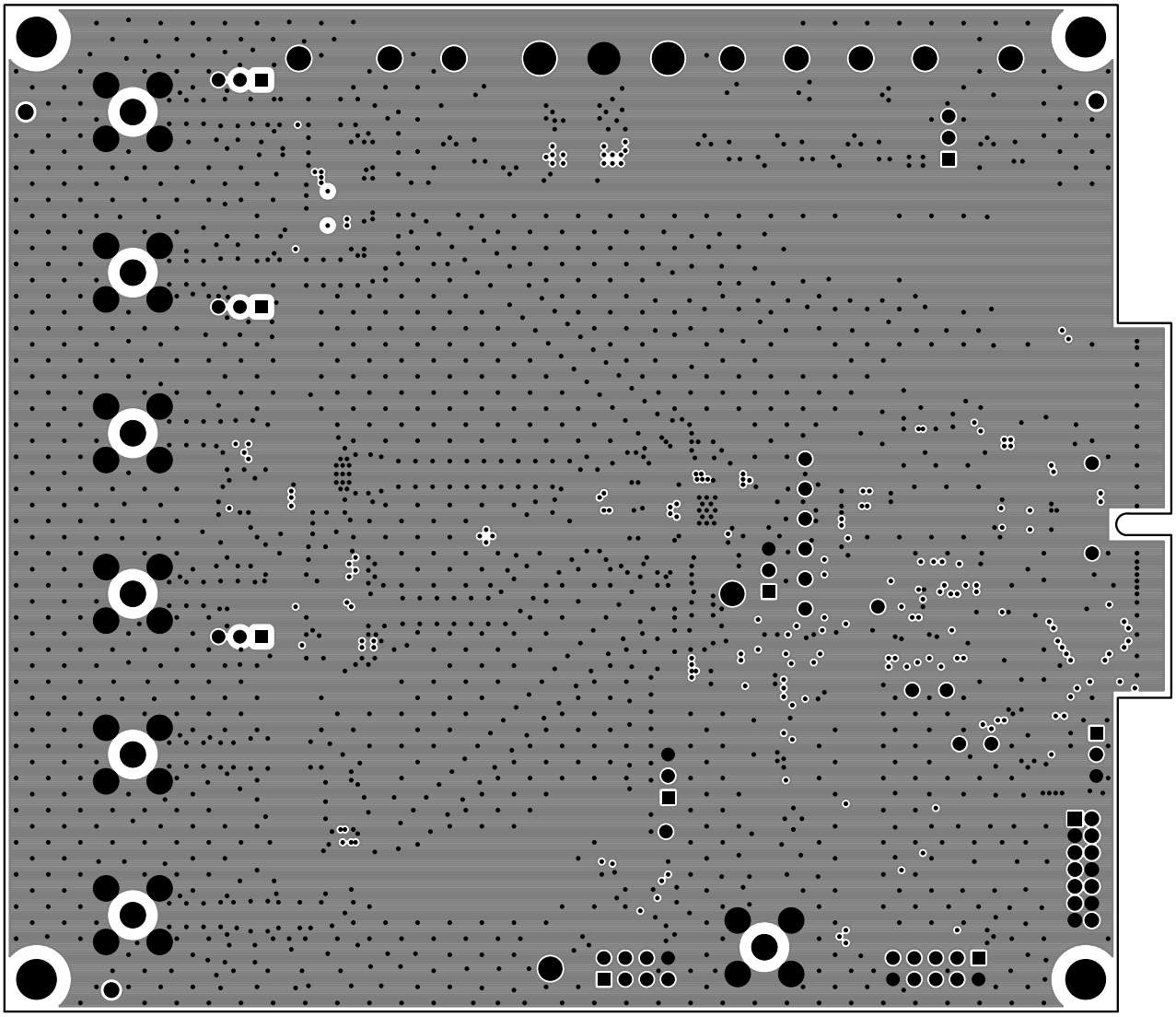


Figure 32. Layer 2 Ground Plane

BOARD LAYOUT

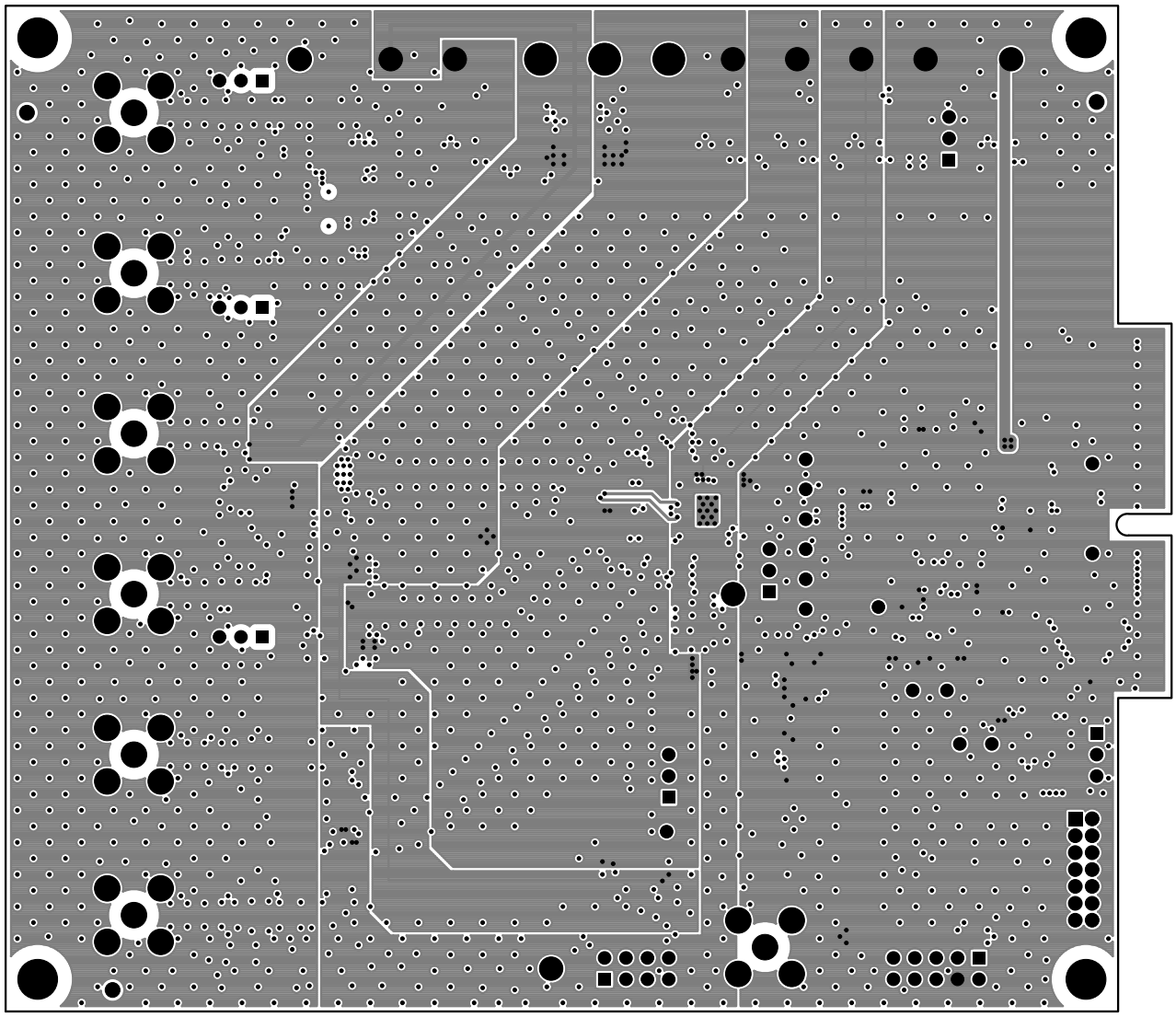


Figure 33. Layer 3 Power Plane

BOARD LAYOUT

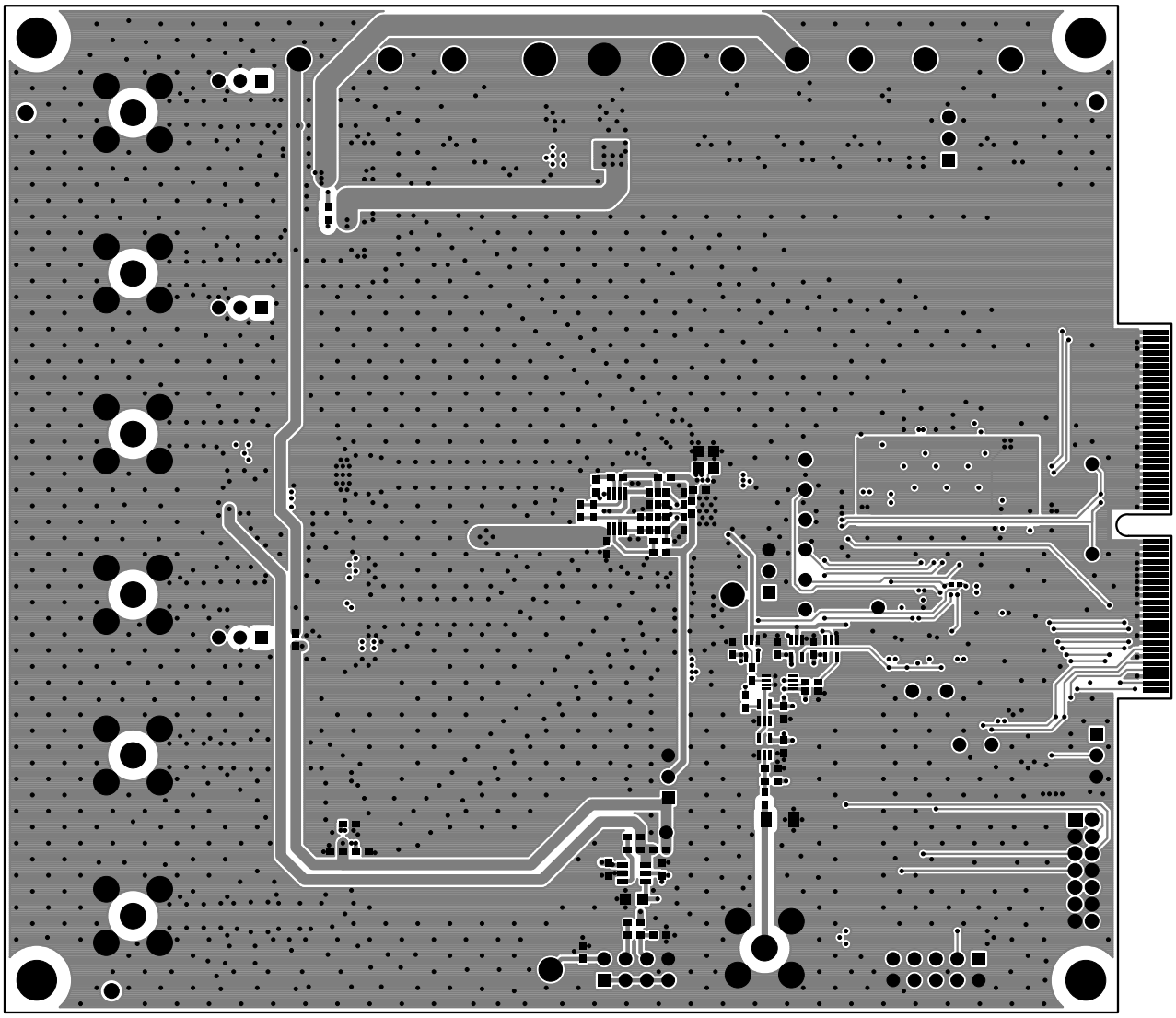
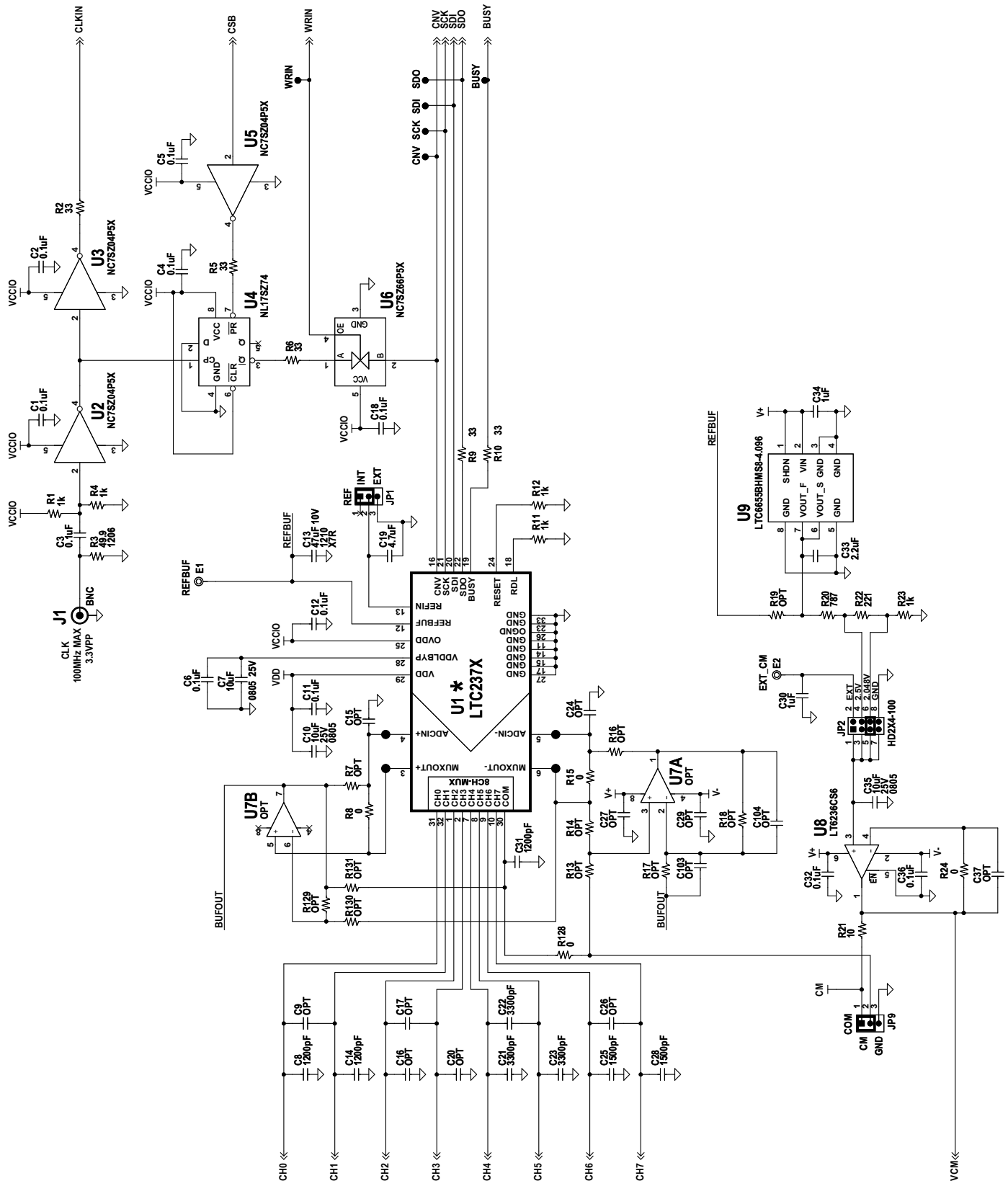
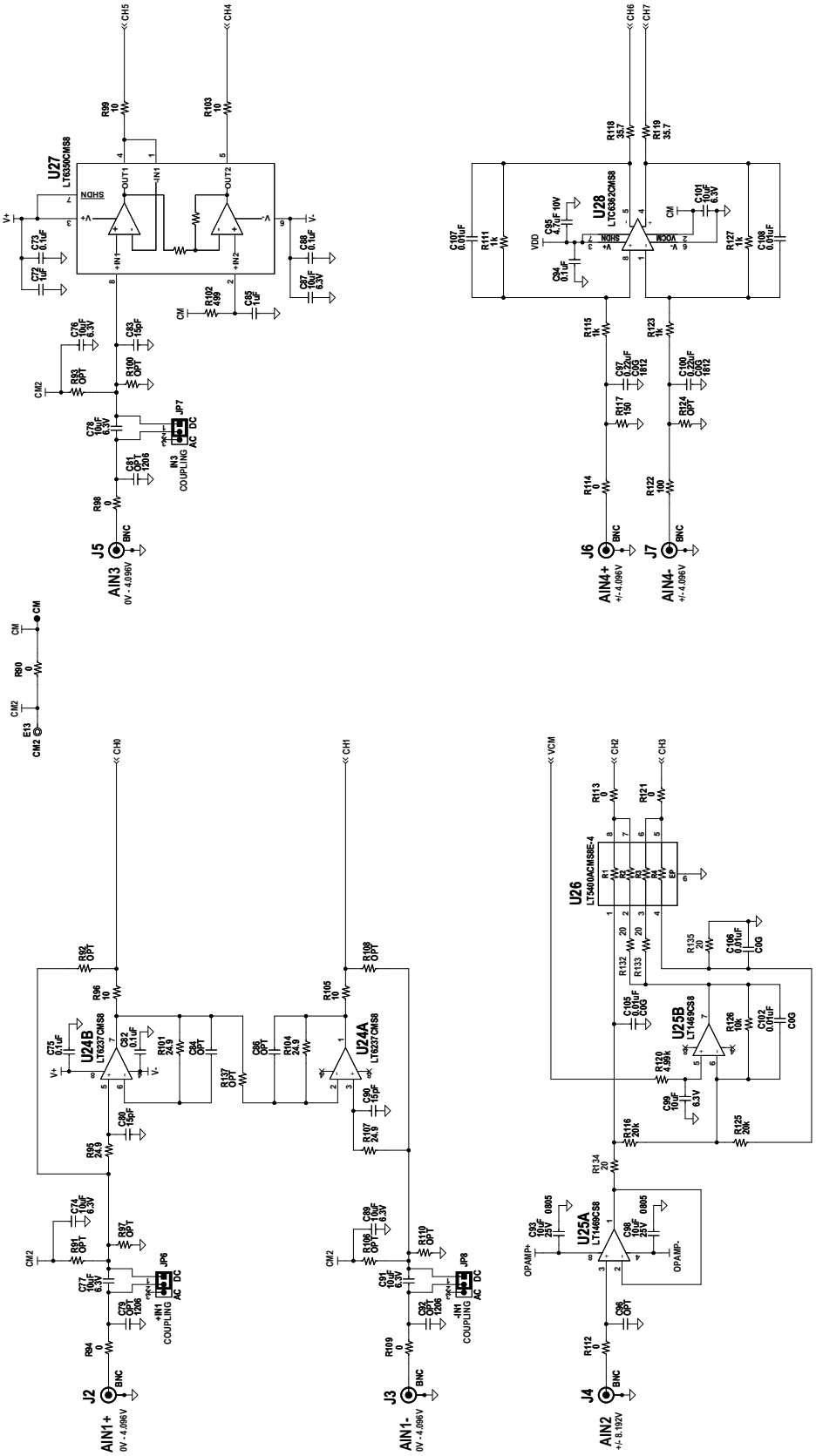


Figure 34. Layer 4 Bottom Layer

SCHEMATICS


U1 * LTC237X
U2 NC7SZ04P5X
U3 NC7SZ04P5X
U4 NL17SZ74
U5 NC7SZ04P5X
U6 NC7SZ66P5X
U7A OPT
U7B OPT
U8 LTC6236CS6
U9 LTC6655BHMS8-4.096
J1 BNC
JP1 INT EXT
JP2 HD2X4-100
JP9
CLKIN
CSB
WRIN
BUSY
CNV SCK SDI SDO
VCCIO
REFBUF
BUFOUT
EXT_CM
VCM
CM
CH0 CH1 CH2 CH3 CH4 CH5 CH6 CH7

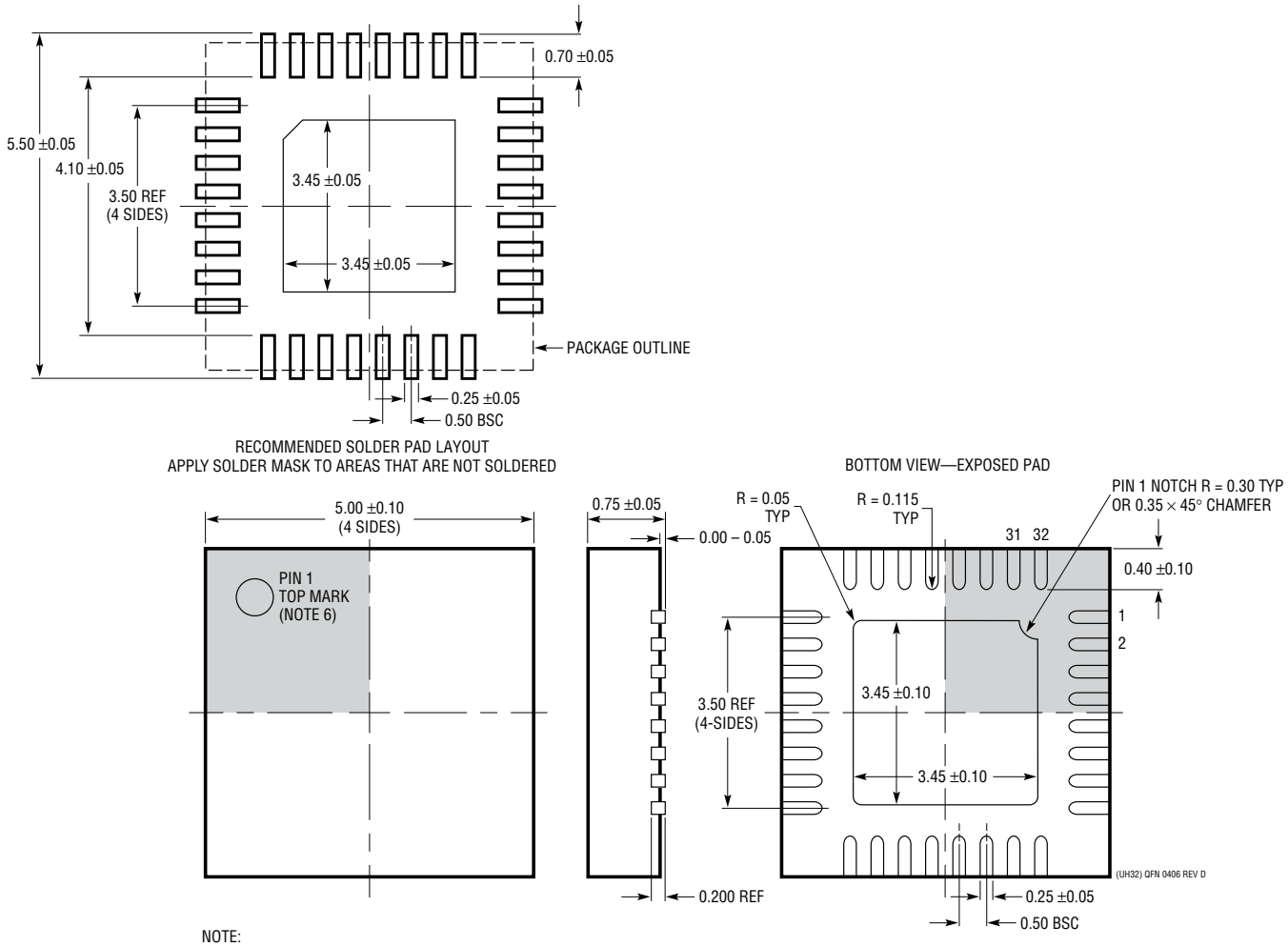
SCHEMATICS


U27
LT6350CMS8
U28
LTC6362CMS8
U26
LT5400ACMS8E-4
U25A
LT1469CS8
U25B
LT1469CS8
U24A
LT6237CMS8
U24B
LT6237CMS8
J2
AIN1+
0V - 4.096V
J3
AIN1-
0V - 4.096V
J4
AIN2
+/- 8.192V
J5
AIN3
0V - 4.096V
J6
AIN4+
+/- 4.096V
J7
AIN4-
+/- 4.096V
JP6
JP7
JP8
COUPLING
AC DC
CM
CM2
VCM
OPAMP+
OPAMP-

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693 Rev D)

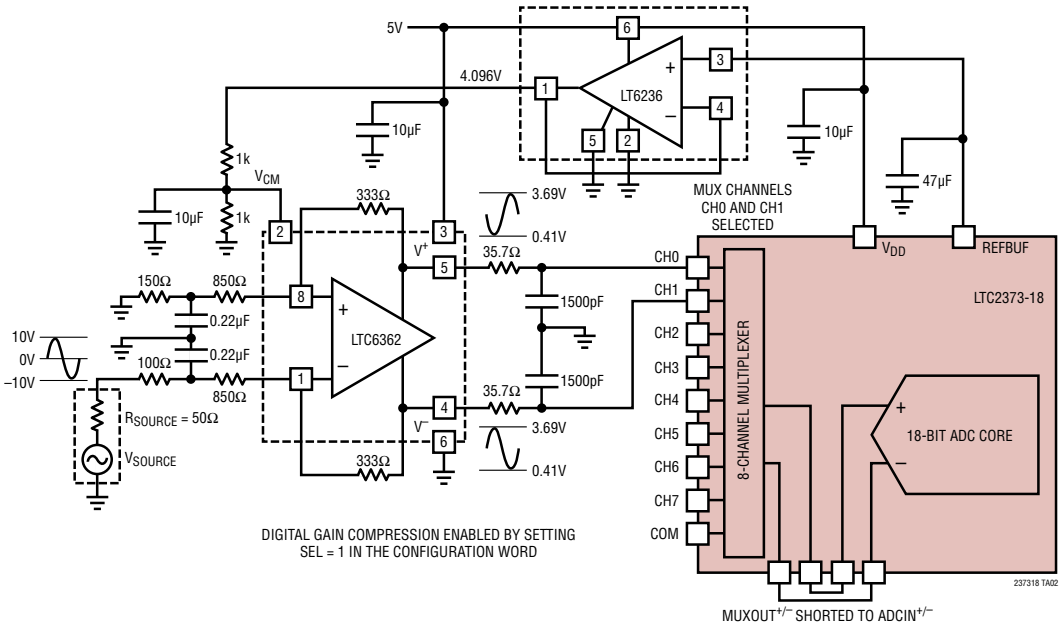


NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

LTC6362 Configured to Accept a ±10V Input Signal Using a Single 5V Supply with Digital Gain Compression Enabled on the LTC2373-18



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADCs		
LTC2378-20/LTC2377-20 LTC2376-20	20-Bit, 1Msps/500ksps/250ksps, ±0.5ppm INL Serial, Low Power ADC	2.5V Supply, ±5V Fully Differential Input, 104dB SNR, MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2379-18/LTC2378-18 LTC2377-18/LTC2376-18	18-Bit, 1.6Msps/1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Differential Input, 101.2dB SNR, ±5V Input Range, DGC, Pin-Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2380-16/LTC2378-16 LTC2377-16/LTC2376-16	16-Bit, 2Msps/1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Differential Input, 96.2dB SNR, ±5V Input Range, DGC, Pin-Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2369-18/LTC2368-18 LTC2367-18/LTC2364-18	18-Bit, 1.6Msps/1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Pseudo-Differential Unipolar Input, 96.5dB SNR, 0V to 5V Input Range, Pin-Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2370-16/LTC2368-16 LTC2367-16/LTC2364-16	16-Bit, 2Msps/1Msps/500ksps/250ksps Serial, Low Power ADC	2.5V Supply, Pseudo-Differential Unipolar Input, 94dB SNR, 0V to 5V Input Range, Pin-Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
DACs		
LTC2756	18-Bit, Serial I_{OUT} SoftSpan™ DAC	±1LSB INL/DNL, Software-Selectable Ranges, SSOP-28 Package
LTC2641	16-Bit/14-Bit/12-Bit Single Serial V_{OUT} DAC	±1LSB INL/DNL, MSOP-8 Package, 0V to 5V Output
LTC2630	12-Bit/10-Bit/8-Bit Single V_{OUT} DACs	SC70 6-Pin Package, Internal Reference, ±1LSB INL (12 Bits)
References		
LTC6655	Precision Low Drift Low Noise Buffered Reference	5V/2.5V/2.048V/1.2V, 5ppm/°C, 0.25ppm Peak-to-Peak Noise, MSOP-8 Package
LTC6652	Precision Low Drift Low Noise Buffered Reference	5V/2.5V/2.048V/1.2V, 5ppm/°C, 2.1ppm Peak-to-Peak Noise, MSOP-8 Package
Amplifiers		
LT6237/LT6236	Dual/Single Rail-to-Rail Output ADC Driver	215MHz GBW, 1.1nV/√Hz, 3.5mA Supply Current
LT6350	Low Noise Single-Ended-to-Differential ADC Driver	Rail-to-Rail Inputs and Outputs, 240ns, 0.01% Settling Time
LTC6362	Low Power, Fully Differential Input/Output Amplifier/Driver	Single 2.8V to 5.25V Supply, 1mA Supply Current, MSOP-8 and 3mm × 3mm DFN-8 Packages

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