32-Bit Oversampling ADC with Configurable Digital Filter

FEATURES

- **±0.5ppm INL (Typ)**
- **104dB SNR (Typ) at 1Msps**
- **148dB Dynamic Range (Typ) at 61sps**
- **Guaranteed 32-Bit No Missing Codes**
- **Configurable Digital Filter with Synchronization**
  - **Relaxed Anti-Aliasing Filter Requirements**
- **Dual Output 32-Bit SAR ADC**
  - **32-Bit Digitally Filtered Low Noise Output**
  - **24-Bit Differential + 7-Bit Common Mode 1Msps Output with Overrange Detection**
- **Wide Input Common Mode Range**
- Guaranteed Operation to 85°C
- 1.8V to 5V SPI-Compatible Serial I/O
- Low Power: 24mW at 1Msps
- 24-Lead 7mm × 4mm DFN Packages

APPLICATIONS

- Seismology
- Energy Exploration
- Automatic Test Equipment
- High Accuracy Instrumentation

DESCRIPTION

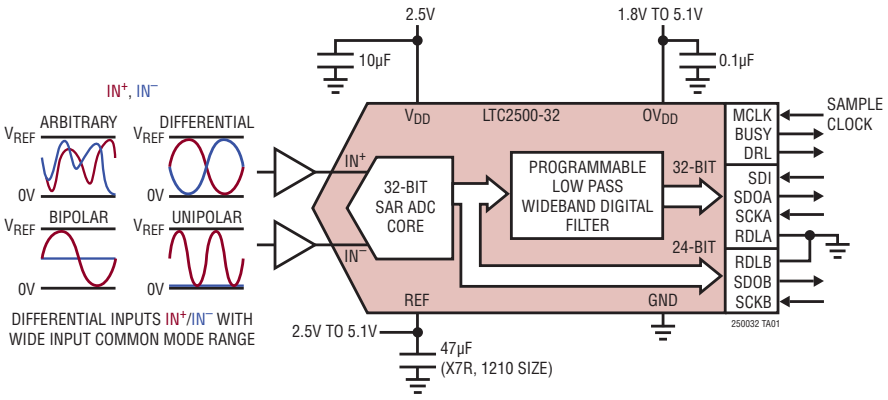
The LTC®2500-32 is a low noise, low power, high performance 32-bit ADC with an integrated configurable digital filter. Operating from a single 2.5V supply, the LTC2500-32 features a fully differential input range up to $\pm V_{REF}$, with V_{REF} ranging from 2.5V to 5.1V. The LTC2500-32 supports a wide common mode range from 0V to V_{REF} simplifying analog signal conditioning requirements.

The LTC2500-32 simultaneously provides two output codes: (1) a 32-bit digitally filtered high precision low noise code, and (2) a 32-bit no latency composite code. The configurable digital filter reduces measurement noise by lowpass filtering and downsampling the stream of data from the SAR ADC core, giving the 32-bit filtered output code. The 32-bit composite code consists of an overrange detection bit, a 24-bit code representing the differential input voltage and a 7-bit code representing the common mode input voltage. The 32-bit composite code is available each conversion cycle, with no cycle of latency.

The digital filter is highly configurable through the SPI-compatible interface and features many distinct filter types that suit a variety of applications. The digital lowpass filter relaxes the requirements for analog anti-aliasing. Multiple LTC2500-32 devices can be easily synchronized using the SYNC pin.

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TYPICAL APPLICATION



Integral Nonlinearity vs Output Code

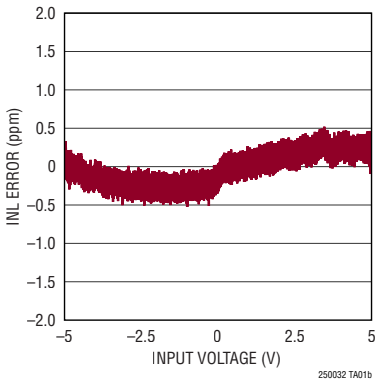


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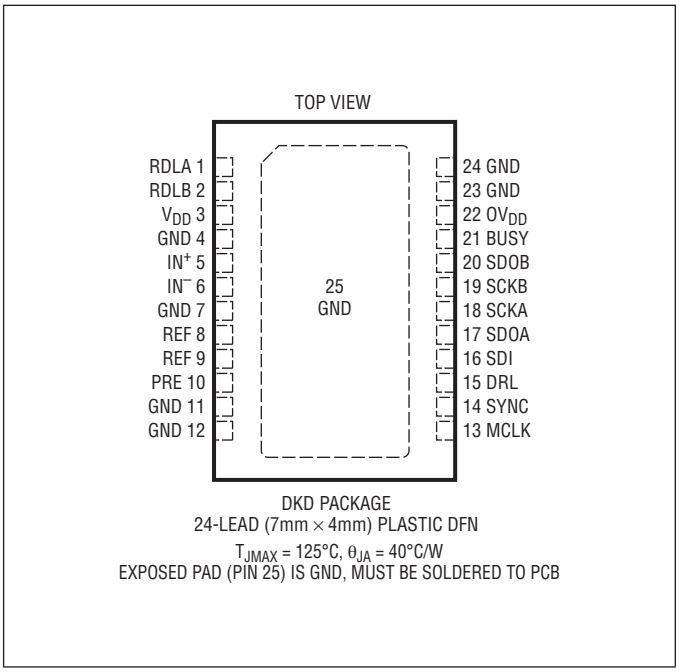
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ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD}) 2.8V
Supply Voltage (OV_{DD}) 6V
Reference Input (REF) 6V
Analog Input Voltage (Note 3)
  IN^+, IN^- ..... (GND – 0.3V) to (REF + 0.3V)
Digital Input Voltage
(Note 3) ..... (GND – 0.3V) to (OV_{DD} + 0.3V)
Digital Output Voltage
(Note 3) ..... (GND – 0.3V) to (OV_{DD} + 0.3V)
Power Dissipation 500mW
Operating Temperature Range
  LTC2500C-32 ..... 0°C to 70°C
  LTC2500I-32 ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DKD PACKAGE
24-LEAD (7mm × 4mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 40°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC2500-32#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2500CDKD-32#PBF	LTC2500CDKD-32#TRPBF	250032	24-Lead (7mm × 4mm) Plastic DFN	0°C to 70°C
LTC2500IDKD-32#PBF	LTC2500IDKD-32#TRPBF	250032	24-Lead (7mm × 4mm) Plastic DFN	–40°C to 85°C

Consult ADI Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}^+	Absolute Input Range (IN^+)	(Note 5)	●	0		V_{REF}	V
V_{IN}^-	Absolute Input Range (IN^-)	(Note 5)	●	0		V_{REF}	V
$V_{IN}^+ – V_{IN}^-$	Input Differential Voltage Range	$V_{IN} = V_{IN}^+ – V_{IN}^-$	●	$–V_{REF}$		V_{REF}	V
V_{CM}	Common Mode Input Range		●	0		V_{REF}	V
I_{IN}	Analog Input Leakage Current				10		nA
C_{IN}	Analog Input Capacitance	Sample Mode Hold Mode			45 5		pF pF
CMRR	Input Common Mode Rejection Ratio	No Latency Output $V_{IN}^+ = V_{IN}^- = 4.5V_{P-P}$, 2kHz Sine			128		dB

CONVERTER CHARACTERISTICS FOR FILTERED OUTPUT (SDOA)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Resolution		●	32			Bits
	No Missing Codes		●	32			Bits
	Transition Noise	(Note 6) See Table 2					
DF	Down-Sampling Factor			4		16384	
INL	Integral Linearity Error	(Notes 7, 8)	●	–2	±0.5	2	ppm
ZSE	Zero-Scale Error	(Notes 7, 9)	●	13	0	13	ppm
	Zero-Scale Error Drift	(Note 7)			±7		ppb/°C
FSE	Full-Scale Error	(Notes 7, 9)	●	–100	±10	100	ppm
	Full-Scale Error Drift	(Note 7)			±0.05		ppm/°C

DYNAMIC ACCURACY FOR FILTERED OUTPUT (SDOA)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and ssinc filter. (Notes 4, 9)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DR	Dynamic Range	DF = 4 $IN^+ = IN^- = V_{CM}$, V_{REF} = 5V, DF = 64 $IN^+ = IN^- = V_{CM}$, V_{REF} = 5V, DF = 1024	● ● ●	110 122 129.5	116 128 138		dB dB dB

CONVERTER CHARACTERISTICS FOR NO LATENCY OUTPUT (SDOB)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Resolution: Differential Common Mode		 ● ●	 24 7			 Bits Bits
	No Missing Codes: Differential Common Mode		 ● ●	 24 7			 Bits Bits
	Transition Noise: Differential Common Mode				 2.3 1		 ppm_{RMS} LSB_{RMS}

CONVERTER CHARACTERISTICS FOR NO LATENCY OUTPUT (SDOB)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
INL	Integral Linearity Error: Differential Common Mode	 7-Bit Output	●	–2	 ±0.5 ±0.1	2	 ppm LSB
ZSE	Zero-Scale Error: Differential Common Mode	 7-Bit Output	●	–13	 0 ±1	13	 ppm LSB
	Zero-Scale Error Drift: Differential				 ±7		 ppb/°C
FSE	Full-Scale Error: Differential Common Mode	 7-Bit Output	●	–100	 ±10 ±1	100	 ppm LSB
	Full-Scale Error Drift: Differential				 ±0.05		 ppm/°C

DYNAMIC ACCURACY FOR NO LATENCY OUTPUT (SDOB)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and A_{IN} = –1dBFS. The specifications are for the differential output (Notes 4, 10)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SINAD	Signal-to-(Noise + Distortion) Ratio	f_{IN} = 2kHz, V_{REF} = 5V	●	100	104		dB
SNR	Signal-to-Noise Ratio	f_{IN} = 2kHz, V_{REF} = 5V	●	100	104		dB
THD	Total Harmonic Distortion	f_{IN} = 2kHz, V_{REF} = 5V f_{IN} = 2kHz, V_{REF} = 2.5V	●		–120 –120	–114 –113	dB dB
SFDR	Spurious Free Dynamic Range	f_{IN} = 2kHz, V_{REF} = 5V	●	115	128		dB
	–3dB Input Linear Bandwidth				34		MHz
	Aperture Delay				500		ps
	Aperture Jitter				4		ps_{RMS}
	Transient Response	Full-Scale Step			125		ns

REFERENCE INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage	(Note 5)	●	2.5		5.1	V
I_{REF}	Reference Input Current	(Note 11)	●		0.9	1.4	mA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage		●	0.8 • OV_{DD}			V
V_{IL}	Low Level Input Voltage		●			0.2 • OV_{DD}	V
I_{IN}	Digital Input Current	V_{IN} = 0V to OV_{DD}	●	–10		10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	I_O = –500 µA	●	OV_{DD} – 0.2			V
V_{OL}	Low Level Output Voltage	I_O = 500 µA	●			0.2	V
I_{OZ}	Hi-Z Output Leakage Current	V_{OUT} = 0V to OV_{DD}	●	–10		10	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = OV_{DD}			10		mA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage		●	2.375	2.5	2.625	V
O_{VDD}	Supply Voltage		●	1.71		5.25	V
I_{VDD}	Supply Current	1Msps Sample Rate	●		9.5	14	mA
I_{OVDD}	Supply Current	1Msps Sample Rate (C_L = 20pF)			1		mA
I_{PD}	Power Down Mode	Conversion Done (I_{VDD} + I_{OVDD} + I_{REF})	●		6	350	µA
P_D	Power Dissipation	1Msps Sample Rate (I_{VDD})			24	35	mW
	Power Down Mode	Conversion Done (I_{VDD} + I_{OVDD} + I_{REF})			15	875	µW

ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SMPL}	Maximum Sampling Frequency		●			1	Msps
f_{DRA}	Output Data Rate at SDOA		●			250	ksps
f_{DRB}	Output Data Rate at SDOB		●			1	Msps
t_{CONV}	Conversion Time		●	600		660	ns
t_{ACQ}	Acquisition Time	t_{ACQ} = t_{CYC} – t_{CONV} – t_{BUSYLH} (Note 12)	●	327			ns
t_{CYC}	Time Between Conversions		●	1000			ns
t_{MCLKH}	Conversion High Time		●	20			ns
t_{MCLKL}	Minimum Low Time for MCLK	(Note 13)	●	20			ns
t_{BUSYLH}	MCLK↑ to BUSY↑ Delay	C_L = 20pF	●			13	ns
t_{QUIET}	SCKA, SCKB Quiet Time from MCLK↑	(Note 12)	●	10			ns
t_{SCKA}	SCKA Period	(Notes 13, 14)	●	10			ns
t_{SCKAH}	SCKA High Time		●	4			ns
t_{SCKAL}	SCKA Low Time		●	4			ns
$t_{SSDISCKA}$	SD1 Setup Time from SCKA↑	(Note 13)	●	4			ns
$t_{HSDISCKA}$	SD1 Hold Time from SCKA↑	(Note 13)	●	1			ns
t_{DSDOA}	SDOA Data Valid Delay from SCKA↑	C_L = 20pF, OV_{DD} = 5.25V	●			8.5	ns
		C_L = 20pF, OV_{DD} = 2.5V	●			8.5	ns
		C_L = 20pF, OV_{DD} = 1.71V	●			9.5	ns

ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{HSDOA}	SDOA Data Remains Valid Delay from SCKA↑	C_L = 20pF (Note 12)	●	1			ns
$t_{DSDOADRLL}$	SDOA Data Valid Delay from DRL↓	C_L = 20pF (Note 12)	●			5	ns
t_{ENA}	Bus Enable Time After RDLA↓	(Note 13)	●			16	ns
t_{DISA}	Bus Relinquish Time After RDLA↑	(Note 13)	●			13	ns
t_{SCKB}	SCKB Period	(Notes 13, 14)	●	10			ns
t_{SCKBH}	SCKB High Time		●	4			ns
t_{SCKBL}	SCKB Low Time		●	4			ns
t_{DSDOB}	SDOB Data Valid Delay from SCKB↑	C_L = 20pF, OV_{DD} = 5.25V C_L = 20pF, OV_{DD} = 2.5V C_L = 20pF, OV_{DD} = 1.71V	● ● ●			8.5 8.5 9.5	ns ns ns
t_{HSDOB}	SDOB Data Remains Valid Delay from SCKB↑	C_L = 20pF (Note 12)	●	1			ns
$t_{DSDOBBUSYL}$	SDOB Data Valid Delay from BUSY↓	C_L = 20pF (Note 12)	●			5	ns
t_{ENB}	Bus Enable Time After RDLB↓	(Note 13)	●			16	ns
t_{DISB}	Bus Relinquish Time After RDLB↑	(Note 13)	●			13	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground.

Note 3: When these pin voltages are taken below ground or above REF or O_{VDD}, they will be clamped by internal diodes. This product can handle input currents up to 100mA below ground or above REF or OV_{DD} without latchup.

Note 4: V_{DD} = 2.5V, OV_{DD} = 2.5V, REF = 5V, V_{CM} = 2.5V, f_{SMPL} = 1MHz.

Note 5: Recommended operating conditions.

Note 6: Transition noise is defined as the noise level of the ADC with IN^+ and IN^- shorted.

Note 7: The DC specifications at SDOA are measured and guaranteed at SDOB. The operation of the digital filters is tested separately to guarantee the same DC specifications at SDOA.

Note 8: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 9: Bipolar zero-scale error is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 0000 0000 0000 0000 0000 and 1111 1111 1111 1111 1111 1111 1111 1111. Full-scale bipolar error is the worst-case of –FS or +FS untrimmed deviation from ideal first and last code transitions and includes the effect of offset error.

Note 10: All specifications in dB are referred to a full-scale ±5V input with a 5V reference voltage.

Note 11: f_{SMPL} = 1MHz, I_{REF} varies proportionally with sample rate.

Note 12: Guaranteed by design, not subject to test.

Note 13: Parameter tested and guaranteed at OV_{DD} = 1.71V, OV_{DD} = 2.5V and OV_{DD} = 5.25V.

Note 14: t_{SCKA}, t_{SCKB} of 10ns maximum allows a shift clock frequency up to 100MHz for rising edge capture.

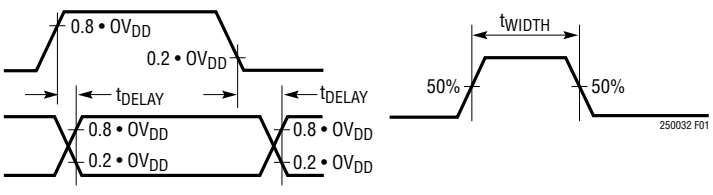
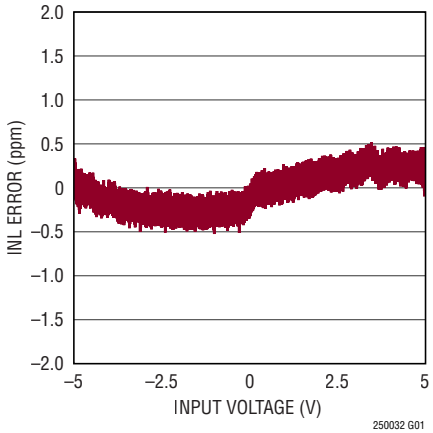


Figure 1. Voltage Levels for Timing Specifications

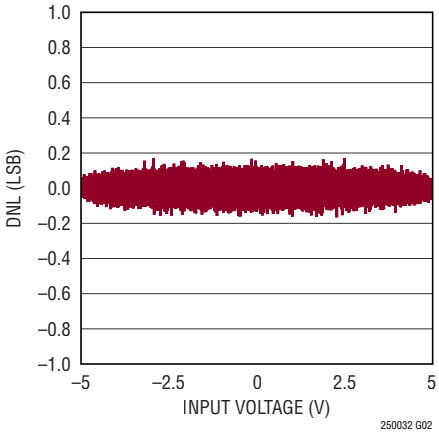
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 2.5V, OV_{DD} = 2.5V, V_{CM} = 2.5V, REF = 5V, f_{SMPL} = 1Msps, no latency output, unless otherwise noted.

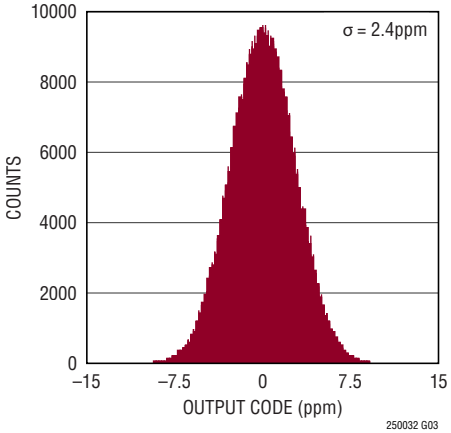
Integral Nonlinearity vs Input Voltage



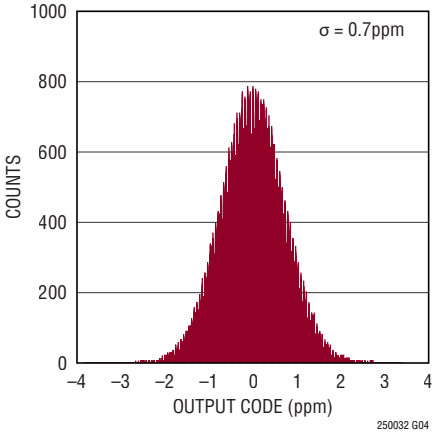
Differential Nonlinearity vs Input Voltage



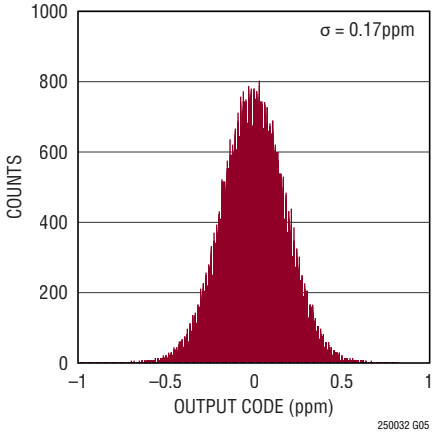
DC Histogram



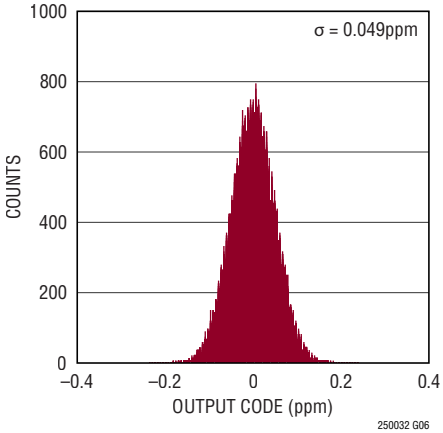
DC Histogram Filtered Output, DF = 4, SSINC Filter



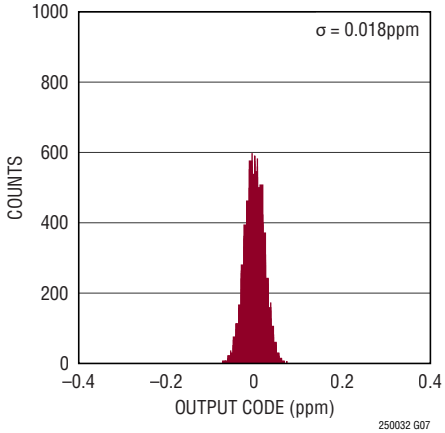
DC Histogram Filtered Output, DF = 64, SSINC Filter



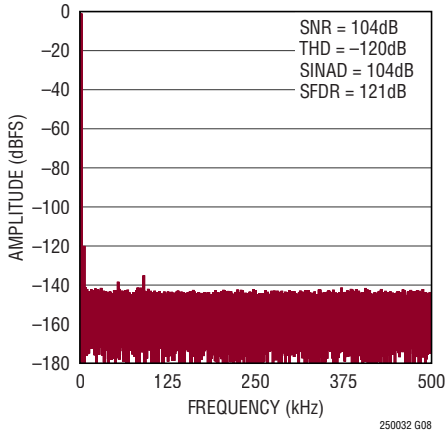
DC Histogram Filtered Output, DF = 1024, SSINC Filter



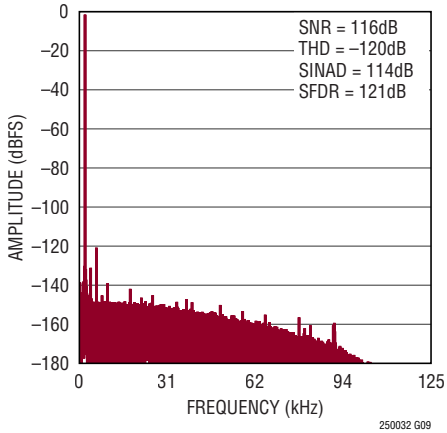
DC Histogram Filtered Output, DF = 16384, SSINC Filter



16k Point FFT f_{IN} = 2kHz



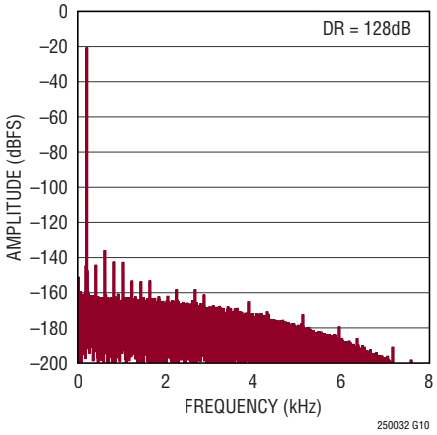
128k Point FFT Filtered Output, f_{IN} = 2kHz, DF = 4, SSINC Filter



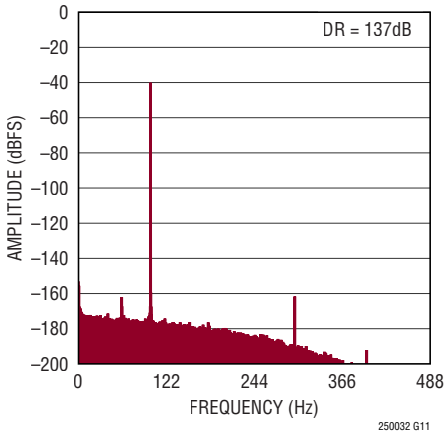
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 2.5V, OV_{DD} = 2.5V, V_{CM} = 2.5V, REF = 5V, f_{SMPL} = 1Msps, no latency output, unless otherwise noted.

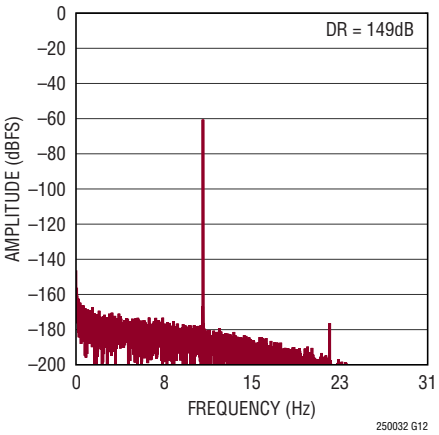
128k Point FFT Filtered Output, f_{IN} = 200Hz, DF = 64, SSINC Filter



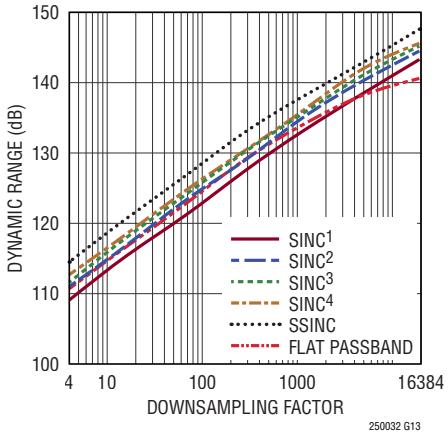
128k Point FFT Filtered Output, f_{IN} = 100Hz, DF = 1024, SSINC Filter



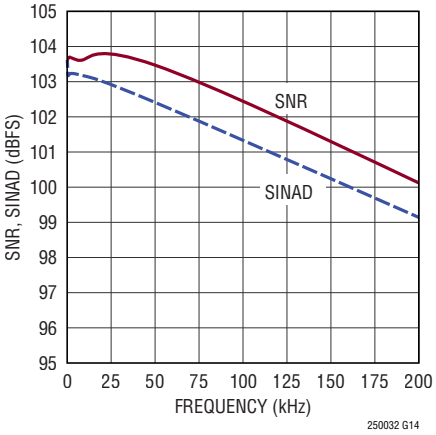
8k Point FFT Filtered Output, f_{IN} = 11Hz, DF = 16384, SSINC Filter



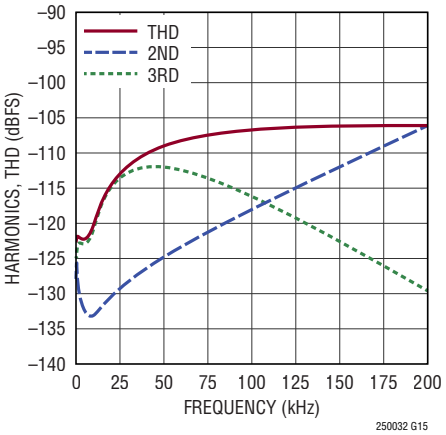
Filtered Output Dynamic Range vs DF



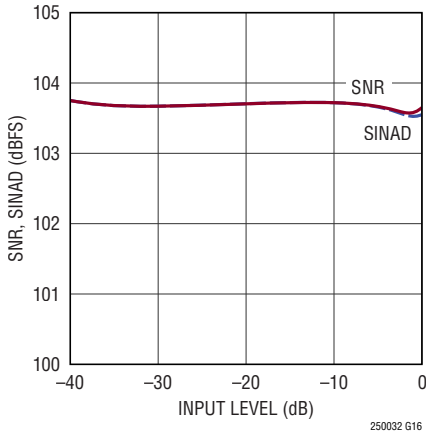
SNR, SINAD vs Input Frequency



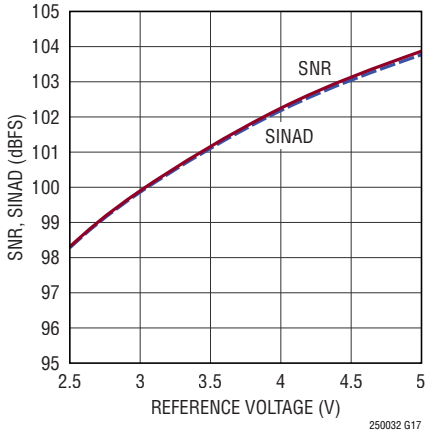
THD, Harmonics vs Input Frequency



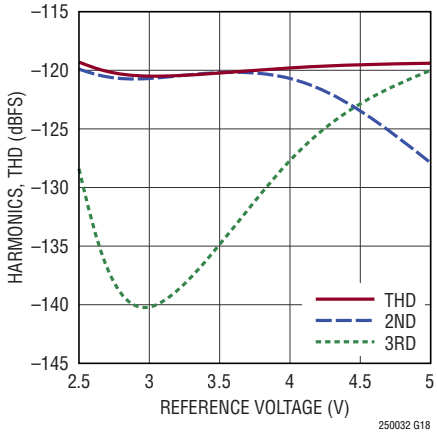
SNR, SINAD vs Input Level, f_{IN} = 2kHz



SNR, SINAD vs Reference Voltage, f_{IN} = 2kHz



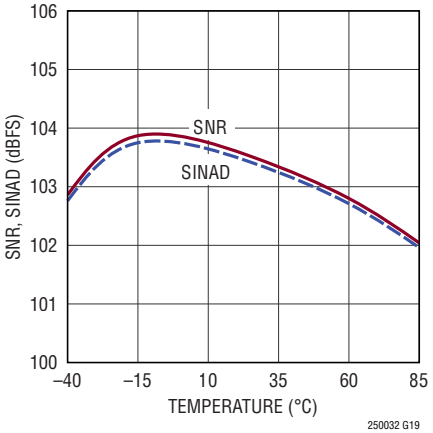
THD, Harmonics vs Reference Voltage, f_{IN} = 2kHz



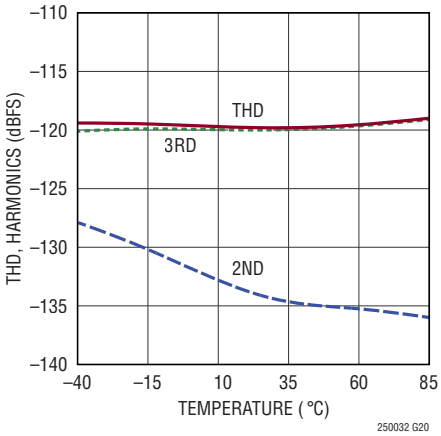
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 2.5V, OV_{DD} = 2.5V, V_{CM} = 2.5V, REF = 5V, f_{SMPL} = 1Msps, no latency output, unless otherwise noted.

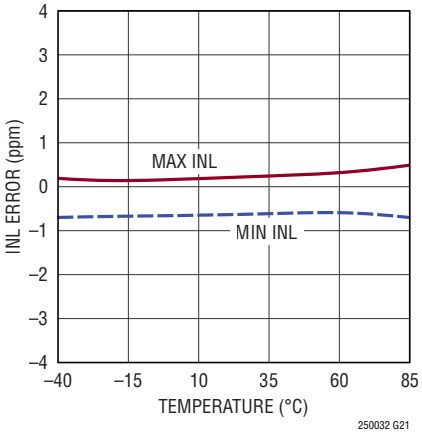
SNR, SINAD vs Temperature, f_{IN} = 2kHz



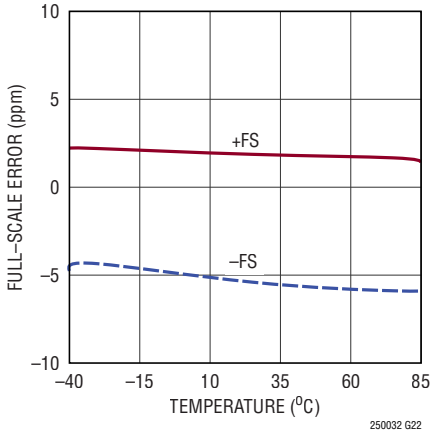
THD, Harmonics vs Temperature, f_{IN} = 100Hz



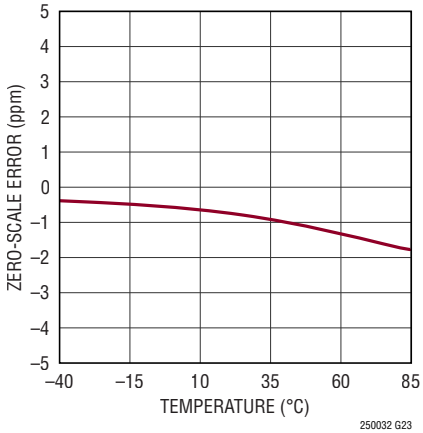
INL vs Temperature



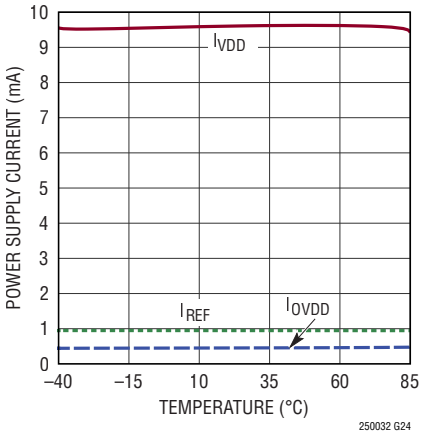
Full-Scale Error vs Temperature



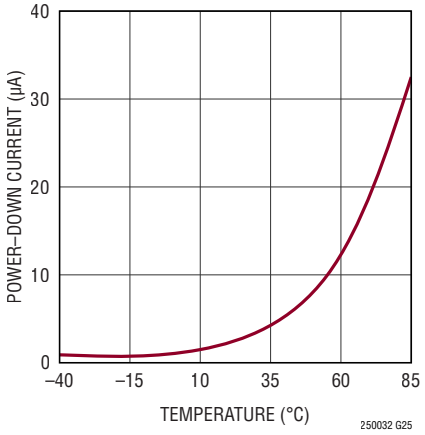
Offset Error vs Temperature



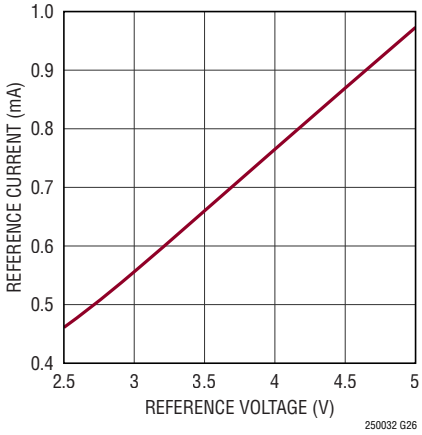
Supply Current vs Temperature



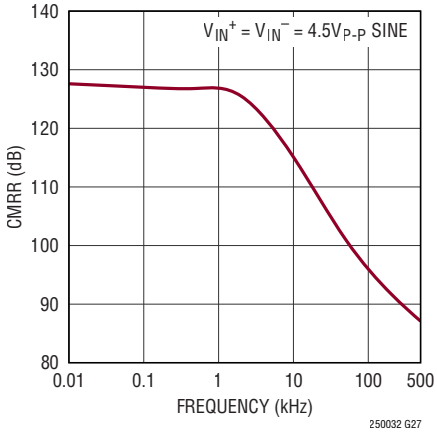
Shutdown Current vs Temperature



Reference Current vs Reference Voltage



CMRR vs Input Frequency



PIN FUNCTIONS

RDLA (Pin 1): Read Low Input A (Filtered Output). When RDLA is low, the serial data output A (SDOA) pin is enabled. When RDLA is high, SDOA pin is in a high impedance state. Logic levels are determined by OV_{DD}.

RDLB (Pin 2): Read Low Input B (No Latency Output). When RDLB is low, the serial data output B (SDOB) pin is enabled. When RDLB is high, SDOB pin is in a high impedance state. Logic levels are determined by OV_{DD}.

V_{DD} (Pin 3): 2.5V Power Supply. The range of V_{DD} is 2.375V to 2.625V. Bypass V_{DD} to GND with a 10µF ceramic capacitor.

GND (Pins 4, 7, 11, 12, 23, 24): Ground.

IN^+ (Pin 5): Positive Analog Input.

IN^- (Pin 6): Negative Analog Input.

REF (Pins 8, 9): Reference Input. The range of REF is 2.5V to 5.1V. This pin is referred to the GND pin and should be decoupled closely to the pin with a 47µF ceramic capacitor (X7R, 1210 size, 10V rating).

PRE (Pin 10): Preset Input. By setting PRE high, the SDI pin is used to select between two preset digital filter modes. Setting PRE low allows the digital filter to be configured by entering a configuration word at SDI. Logic levels are determined by REF, with range of REF being 2.5V to 5.1V.

MCLK (Pin 13): Master Clock Input. A rising edge on this input powers up the part and initiates a new conversion. Logic levels are determined by OV_{DD}.

SYNC (Pin 14): Synchronization Input. A pulse on this input is used to synchronize the phase of the digital filter. When applied across multiple devices, a SYNC pulse synchronizes all the devices to the same phase. Logic levels are determined by OV_{DD}.

DRL (Pin 15): Data Ready Low Output. A falling edge on this pin indicates that a new filtered output code is available in the output register of SDOA. Logic levels are determined by OV_{DD}.

SDI (Pin 16): Serial Data Input. Data provided on this line, in synchrony with SCKA, can be used to program the digital filter and DGC/DGE modes. Input data on SDI is latched on rising edges of SCKA. Logic levels are determined by OV_{DD}.

SDOA (Pin 17): Serial Data Output A (Filtered Output). The filtered output code appears on this pin (MSB first) on each rising edge of SCKA. The output data is in 2's complement format. Logic levels are determined by OV_{DD}.

SCKA (Pin 18): Serial Data Clock Input A (Filtered Output). When SDOA is enabled, the filtered output code is shifted out (MSB first) on the rising edges of this clock. Logic levels are determined by OV_{DD}.

SCKB (Pin 19): Serial Data Clock Input B (No Latency Output). When SDOB is enabled, the no latency output code is shifted out (MSB first) on the rising edges of this clock. Logic levels are determined by OV_{DD}.

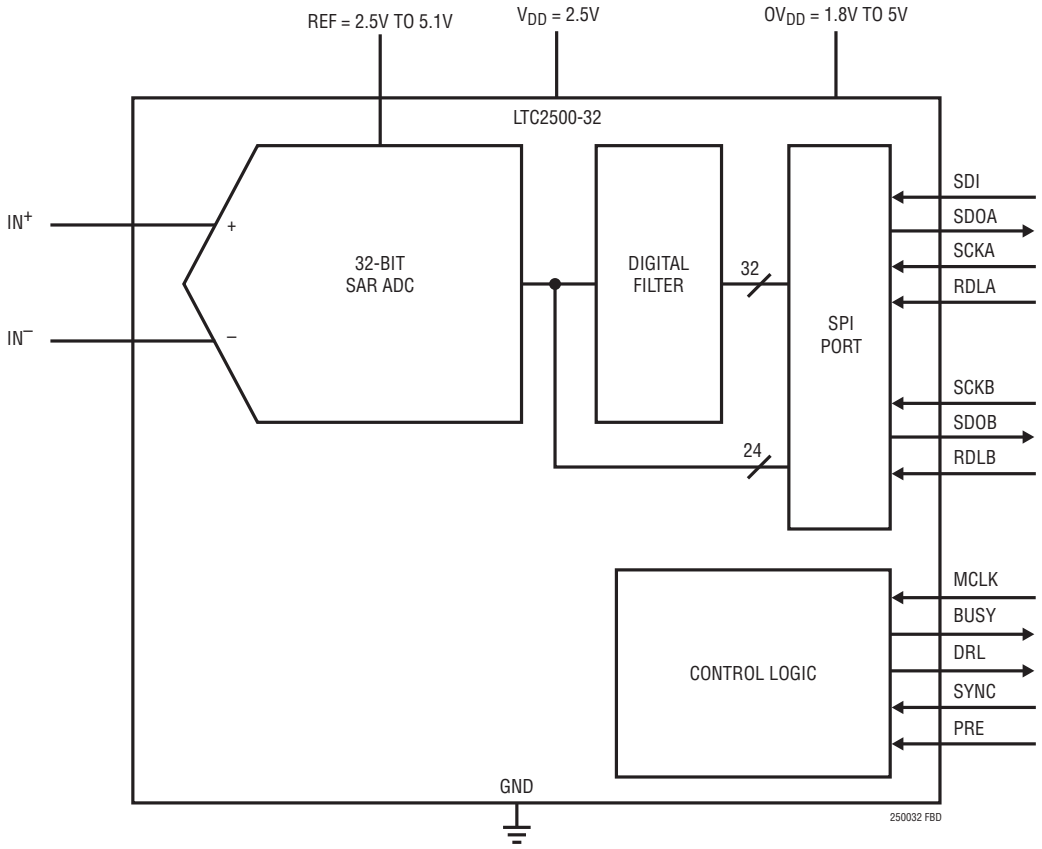
SDOB (Pin 20): Serial Data Output B (No Latency Output). The 32-bit no latency composite output code appears on this pin (MSB first) on each rising edge of SCKB. The output data is in 2's complement format. Logic levels are determined by OV_{DD}.

BUSY (Pin 21): BUSY Indicator. Goes high at the start of a new conversion and returns low when the conversion has finished. Logic levels are determined by OV_{DD}.

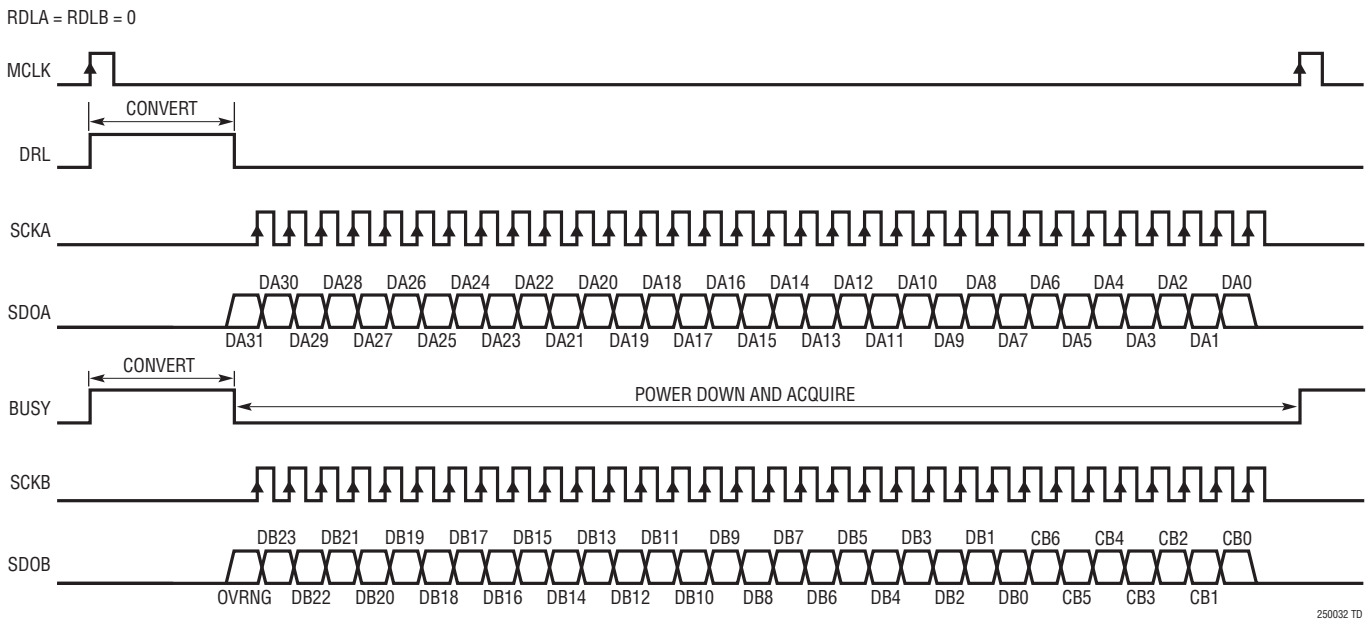
OV_{DD} (Pin 22): I/O Interface Digital Power. The range of OV_{DD} is 1.71V to 5.25V. This supply is nominally set to the same supply as the host interface (1.8V, 2.5V, 3.3V, or 5V). Bypass OV_{DD} to GND (Pin 23) with a 0.1µF capacitor.

GND (Exposed Pad Pin 25): Ground. Exposed pad must be soldered directly to the ground plane.

FUNCTIONAL BLOCK DIAGRAM



TIMING DIAGRAM



APPLICATIONS INFORMATION

OVERVIEW

The LTC2500-32 is a low noise, low power, high performance 32-bit ADC with an integrated configurable digital filter. Operating from a single 2.5V supply, the LTC2500-32 features a fully differential input range up to $\pm V_{REF}$, with V_{REF} ranging from 2.5V to 5.1V. The LTC2500-32 supports a wide common mode range from 0V to V_{REF} simplifying analog signal conditioning requirements.

The LTC2500-32 simultaneously provides two output codes: (1) a 32-bit digitally filtered high precision low noise code, and (2) a 32-bit no latency composite code. The configurable digital filter reduces measurement noise by lowpass filtering and down-sampling the stream of data from the SAR ADC core, giving the 32-bit filtered output code. The 32-bit composite code consists of an overrange detection bit, a 24-bit code representing the differential input voltage and a 7-bit code representing the common mode input voltage. The 32-bit composite code is available each conversion cycle, with no cycle of latency.

The digital filter is highly configurable through the SPI-compatible interface and features many distinct filter types that suit a variety of applications. The digital lowpass filter relaxes the requirements for analog anti-aliasing. Multiple LTC2500-32 devices can be easily synchronized using the SYNC pin.

CONVERTER OPERATION

The LTC2500-32 operates in two phases. During the acquisition phase, a 32-bit charge redistribution capacitor D/A converter (CDAC) is connected to the IN^+ and IN^- pins to sample the analog input voltages. A rising edge on the MCLK pin initiates a conversion. During the conversion phase, the 32-bit CDAC is sequenced through a successive approximation algorithm, effectively comparing the sampled inputs with binary-weighted fractions of the reference voltage (e.g. $V_{REF}/2$, $V_{REF}/4$ … $V_{REF}/4294967296$). At the end of conversion, the CDAC output approximates the sampled analog input. The ADC control logic then passes the 32-bit digital output code to the digital filter for further processing. The LTC2500-32 also has an overrange detector. The overrange detector bit is flagged as 1 if the differential input exceeds $\pm V_{REF}$, and is updated every conversion cycle. The 1-bit overrange detector bit, a 24-bit code representing the differential voltage and a 7-bit code representing the common mode voltage are combined to form a 32-bit composite code. The 32-bit composite code is available each conversion cycle, without any cycle of latency.

TRANSFER FUNCTION

The LTC2500-32 digitizes the full-scale differential voltage of $2 \times V_{REF}$ into 2^{32} levels, resulting in an LSB size of 2.3nV with a 5V reference. The ideal transfer function is shown in Figure 2. The output data is in 2's complement format.

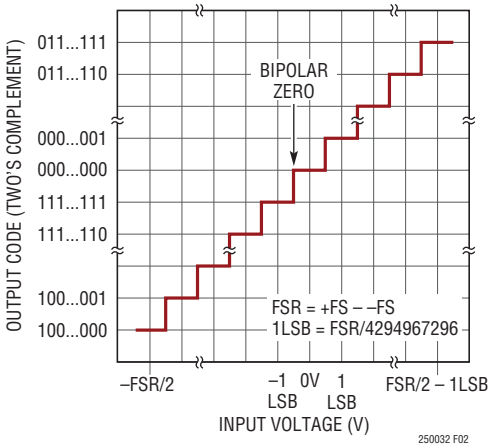


Figure 2. LTC2500-32 Transfer Function

ANALOG INPUT

The LTC2500-32 samples the voltage difference ($IN^+ – IN^-$) between its analog input pins over a wide common mode input range while attenuating unwanted signals common to both input pins by the common-mode rejection ratio (CMRR) of the ADC. Wide common mode input range coupled with high CMRR allows the IN^+/IN^- analog inputs to swing with an arbitrary relationship to each other, provided each pin remains between GND and V_{REF}. This unique feature of the LTC2500-32 enables it to accept a wide variety of signal swings, including traditional classes of analog input signals such as pseudo-differential unipolar, pseudo-differential bipolar, and fully differential, thereby simplifying signal chain design.

In the acquisition phase, each input sees approximately 45pF (C_{IN}) from the sampling circuit in series with 40Ω (R_{ON}) from the on-resistance of the sampling switch.

APPLICATIONS INFORMATION

The inputs draw a current spike while charging the C_{IN} capacitors during acquisition. During conversion, the analog inputs draw only a small leakage current.

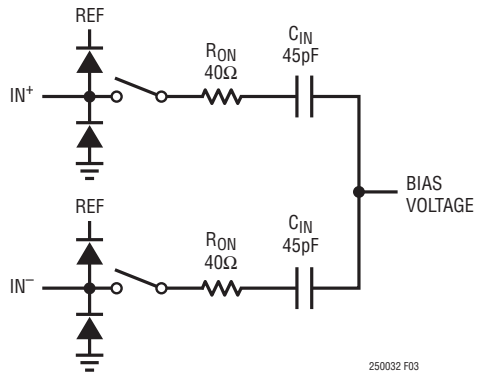


Figure 3. The Equivalent Circuit for the Differential Analog Input of the LTC2500-32

INPUT DRIVE CIRCUITS

A low impedance source can directly drive the high impedance inputs of the LTC2500-32 without gain error. A high impedance source should be buffered to minimize settling time during acquisition and to optimize ADC linearity. For best performance, a buffer amplifier should be used to drive the analog inputs of the LTC2500-32. The amplifier provides low output impedance, which produces fast settling of the analog signal during the acquisition phase. It also provides isolation between the signal source and the ADC inputs.

Noise and Distortion

The noise and distortion of the input buffer amplifier and other supporting circuitry must be considered since they add to the ADC noise and distortion. Noisy input signals should be filtered prior to the buffer amplifier with a low bandwidth filter to minimize noise. The simple one-pole RC lowpass filter (LPF1) shown in Figure 4 is sufficient for many applications.

A coupling filter network (LPF2) should be used between the buffer and ADC input to minimize disturbances reflected into the buffer from sampling transients. Long RC time constants at the analog inputs will slow down the settling of the analog inputs. Therefore, LPF2 typically requires a wider bandwidth than LPF1. This filter also helps minimize the noise contribution from the buffer. A buffer amplifier

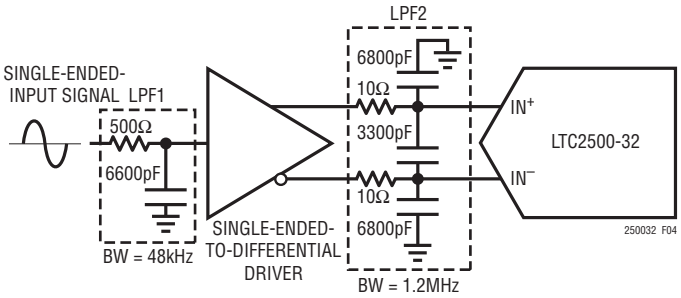


Figure 4. The Equivalent Input for the Differential Analog Input of the LTC2500-32

with a low noise density must be selected to minimize degradation of SNR.

High quality capacitors and resistors should be used in the RC filters since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self-heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

Input Currents

An important consideration when coupling an amplifier to the LTC2500-32 is in dealing with current spikes drawn by the ADC inputs at the start of each acquisition phase. The ADC inputs may be modeled as a switched capacitor load of the drive circuit. A drive circuit may rely partially on attenuating switched-capacitor current spikes with small filter capacitors C_{FILT} placed directly at the ADC inputs, and partially on the driver amplifier having sufficient bandwidth to recover from the residual disturbance. Amplifiers optimized for DC performance may not have sufficient bandwidth to fully recover at the ADC's maximum conversion rate, which can produce nonlinearity and other errors. Coupling filter circuits may be classified in three broad categories:

Fully Settled – This case is characterized by filter time constants and an overall settling time that is considerably shorter than the sample period. When acquisition begins, the coupling filter is disturbed. For a typical first order RC filter, the disturbance will look like an initial step with an exponential decay. The amplifier will have its own response to the disturbance, which may include ringing. If

APPLICATIONS INFORMATION

the input settles completely (to within the accuracy of the LTC2500-32), the disturbance will not contribute any error.

Partially Settled – In this case, the beginning of acquisition causes a disturbance of the coupling filter, which then begins to settle out towards the nominal input voltage. However, acquisition ends (and the conversion begins) before the input settles to its final value. This generally produces a gain error, but as long as the settling is linear, no distortion is produced. The coupling filter's response is affected by the amplifier's output impedance and other parameters. A linear settling response to fast switched-capacitor current spikes can NOT always be assumed for precision, low bandwidth amplifiers. The coupling filter serves to attenuate the current spikes' high frequency energy before it reaches the amplifier.

Fully Averaged – If the coupling filter capacitors (C_{FILT}) at the ADC inputs are much larger than the ADC's sample capacitors (45pF), then the sampling glitch is greatly attenuated. The driving amplifier effectively only sees the average sampling current, which is quite small. At 1Msps, the equivalent input resistance is approximately 22kΩ (as shown in Figure 5), a benign resistive load for most precision amplifiers. However, resistive voltage division will occur between the coupling filter's DC resistance and the ADC's equivalent (switched-capacitor) input resistance, thus producing a gain error.

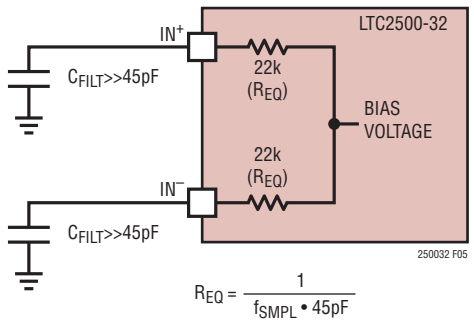


Figure 5. Equivalent Circuit for the Differential Analog Input of the LTC2500-32 at 1Msps

The input leakage currents of the LTC2500-32 should also be considered when designing the input drive circuit, because source impedances will convert input leakage currents to an added input voltage error. The input leakage currents, both common mode and differential, are typically

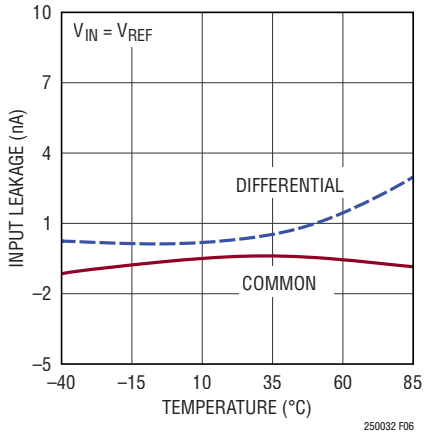


Figure 6. Common Mode and Differential Input Leakage Current Over Temperature

extremely small over the entire operating temperature range. Figure 6 shows the input leakage currents over temperature for a typical part.

Let R_{S1} and R_{S2} be the source impedances of the differential input drive circuit shown in Figure 7, and let I_{L1} and I_{L2} be the leakage currents flowing out of the ADC's analog inputs. The differential voltage error, V_E, due to the leakage currents can be expressed as:

$$V_E = \frac{R_{S1}+R_{S2}}{2} \bullet (I_{L1}-I_{L2}) + (R_{S1}-R_{S2}) \bullet \frac{I_{L1}+I_{L2}}{2}$$

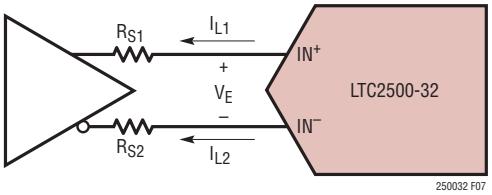


Figure 7. Source Impedances of a Driver and Input Leakage Currents of the LTC2500-32

The common mode input leakage current, $(I_{L1} + I_{L2})/2$, is typically extremely small (Figure 6) over the entire operating temperature range and common mode input voltage range. Thus, any reasonable mismatch (below 5%) of the source impedances R_{S1} and R_{S2} will cause only a negligible error. The differential leakage current is also typically very small, and its nonlinear component is even smaller. Only the nonlinear component will impact the ADC's linearity.

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For optimal performance, it is recommended that the source impedances, R_{S1} and R_{S2}, be between 5Ω and 50Ω and with 1% tolerance. For source impedances in this range, the voltage and temperature coefficients of R_{S1} and R_{S2} are usually not critical. The guaranteed AC and DC specifications are tested with 5Ω source impedances, and the specifications will gradually degrade with increased source impedances due to incomplete settling.

Arbitrary Analog Input Signals

The wide common mode input range and high CMRR of the LTC2500-32 allow analog inputs IN^+ and IN^- pins to swing with an arbitrary relationship to each other, provided that each pin remains between V_{REF} and GND. This unique feature of the LTC2500-32 enables it to accept a wide variety of signal swings, simplifying signal chain design.

Buffering AC Input Signals

It is recommended that the LTC2500-32 be driven using the LT6203 configured as two unity gain buffers when buffering high bandwidth input signals, as shown in Figure 8a. The LT6203 combines fast settling and good DC linearity with 1.9nV/RT(Hz) input-referred noise density, enabling it to achieve the full ADC data sheet SNR and THD specifications as shown in the FFT plot in Figure 8b.

Maximizing the SNR Using Fully Differential Input Drive

In order to maximize the SNR, the input signal swing must be maximized. A fully differential signal with a common-mode of $V_{REF}/2$ maximizes the input signal swing. The circuit in Figure 8a is capable of buffering such a signal.

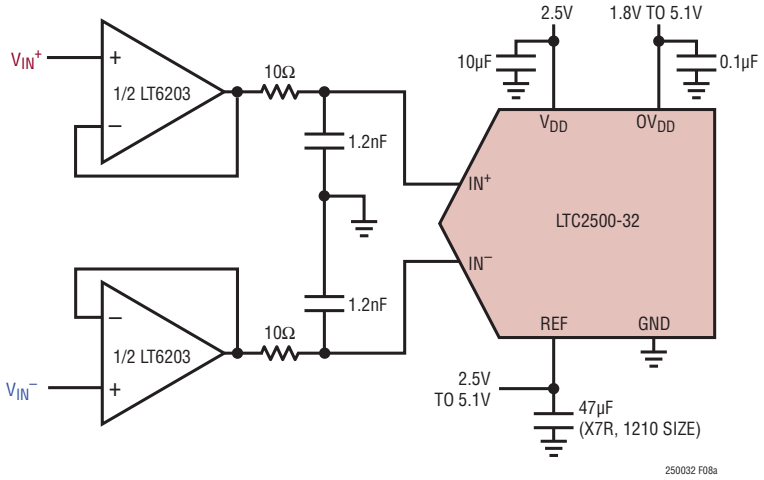


Figure 8a. Buffering Two Single-Ended Analog Input Signals

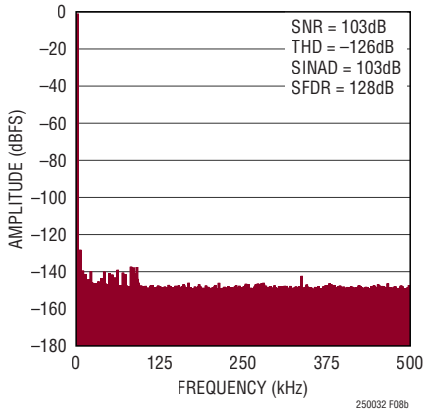


Figure 8b. 128k Point FFT Plot with F_{IN} = 2kHz for Circuit Shown in Figure 8a

APPLICATIONS INFORMATION

If the input signal does not have a common-mode of $V_{REF}/2$ or is single-ended, the LTC6363 differential amplifier may be used in conjunction with the LT5400-4 precision resistors to produce a fully differential signal with a common-mode of $V_{REF}/2$. Figure 9a shows the LTC6363 buffering, level-shifting and performing a single-ended to differential conversion on a ±5V single-ended true bipolar input signal. The FFT in Figure 9b shows that near data sheet performance is obtained with this driver solution. Though not shown here, the LTC6363 may also be configured to amplify or attenuate a signal to match the full scale input range of the LTC2500-32.

Buffering DC Input Signals

The LTC2500-32 has excellent INL specifications. This makes the LTC2500-32 ideal for applications which require high DC accuracy, including parameters such as offset and offset drift. To maintain high accuracy over the entire DC signal chain, amplifiers have to be selected very carefully. A large-signal open-loop gain of at least 126dB may be required to ensure 1ppm linearity for amplifiers configured for a gain of negative 1. However, less gain is sufficient if the amplifier's gain characteristic is known to be (mostly) linear. An amplifier's offset versus signal level must be considered for amplifiers configured as unity gain buffers. For example, 1ppm linearity may require that the offset is known to vary less than 5µV for a 5V swing. However, greater offset variations may be acceptable if the relationship is known to be (mostly) linear. Unity-gain buffer amplifiers typically require substantial headroom to the power supply rails for best performance. Inverting amplifier circuits configured to minimize swing at the amplifier input terminals may perform better with less headroom than unity-gain buffer amplifiers. The linearity and thermal properties of an inverting amplifier's feedback network should be considered carefully to ensure DC accuracy.

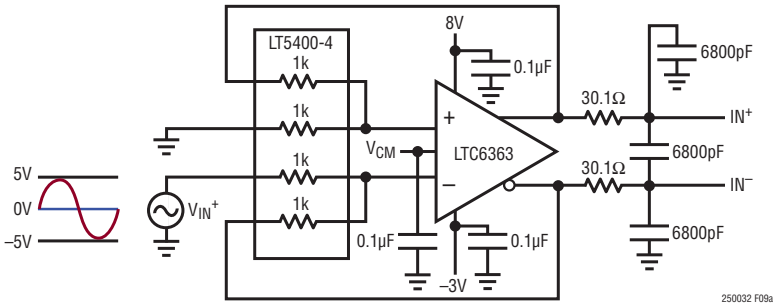


Figure 9a. Buffering and Converting a ±5V True Bipolar Input Signal to a Fully Differential Input

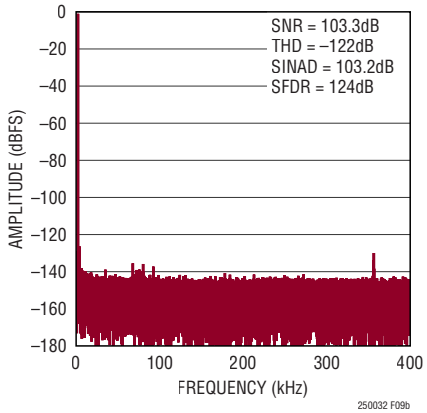


Figure 9b. 128k Point FFT Plot with F_{IN} = 2kHz f_{SMPL} = 800ksps for Circuit Shown in Figure 9a

APPLICATIONS INFORMATION

Figure 10 shows a typical application where two single ended analog input voltages are buffered using the LTC2057. The LTC2057 is a high precision zero drift amplifier which complements the low offset and offset drift of the LTC2500-32. The LTC2057 is shown in a non-inverting amplifier configuration. The LTC2500-32 has a guaranteed maximum offset error of 130µV (typical drift ±0.007ppm/°C), and a guaranteed maximum full-scale error of 150ppm (typical drift ±0.05ppm/°C). Low drift is important to maintain accuracy over a wide temperature range in a calibrated system.

Buffering Single-Ended Analog Input Signals

While the circuits shown in Figures 8a and 10 are capable of buffering single-ended input signals, the circuit shown in Figure 11 is preferable when the single-ended signal reference level is inherently low impedance and doesn't require buffering. This circuit eliminates one driver and lowpass filter, reducing part count, power dissipation, and SNR degradation due to driver noise.

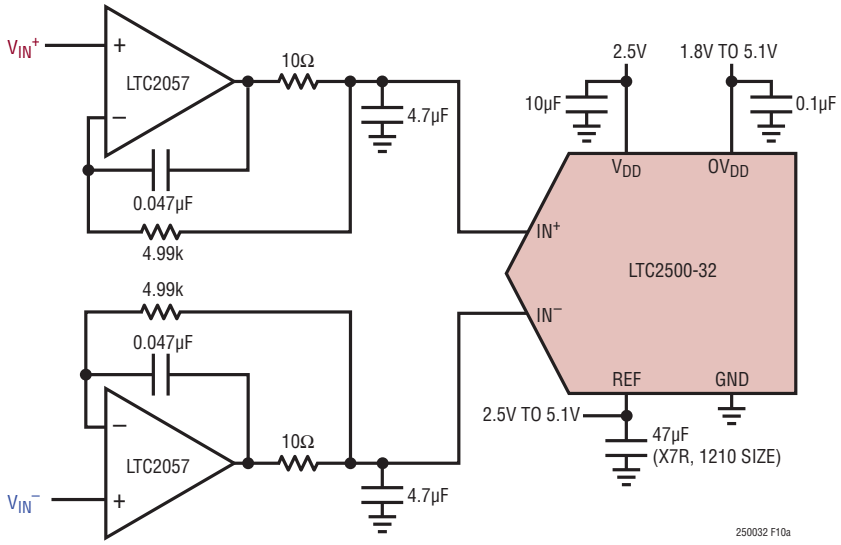


Figure 10. Buffering Two Single-Ended DC Analog Input Signals

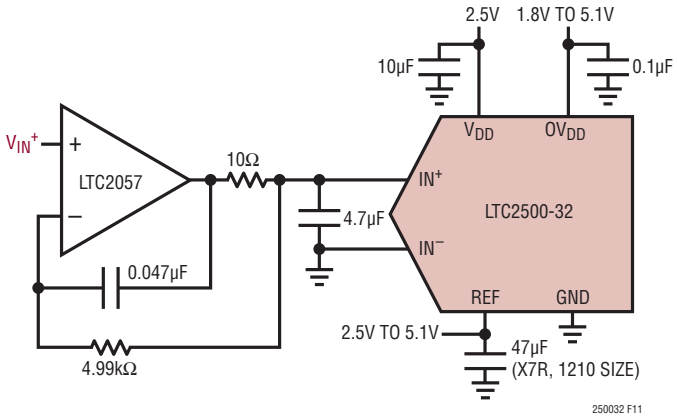


Figure 11. Buffering Single-Ended Signals

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Using Digital Gain Compression for Single Supply Operation

The LTC2500-32 offers a digital gain compression (DGC) feature which defines the full-scale input swing to be between 10% and 90% of the $\pm V_{REF}$ analog input range. This feature allows the SAR ADC driver to be powered off of a single positive supply since each input swings between 0.5V and 4.5V as shown in Figure 12, while maintaining full-scale output codes. Needing only one positive supply to power the SAR ADC driver results in additional power savings for the entire system versus conventional systems that have a negative supply for the ADC driver.

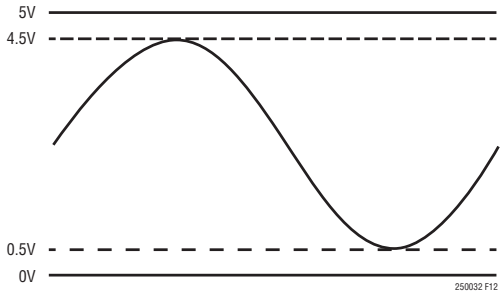


Figure 12. Input Swing of the LTC2500-32 with Gain Compression Enabled

With DGC enabled, the LTC2500-32 can be driven by the low power LTC6362 differential driver which is powered from a single 5V supply. Figure 13a shows how to configure the LTC6362 to accept a ±3.28V true bipolar single-ended input signal and level shift the signal to the reduced input range of the LTC2500-32 when digital gain compression is enabled. When paired with the LTC6655- 4.096 for the reference, the entire signal chain solution can be powered from a single 5V supply, minimizing power consumption and reducing complexity. As shown in the FFT of Figure 13b, the single 5V supply solution can achieve up to 100dB of SNR. To enable DGC, set DGC(C[9]) = 1 in the configuration word. The common-mode output is also subjected to DGC, thereby limiting the input common mode of the input to between 0.5V to 4.5V.

Using Digital Gain Expansion for System Calibration

The LTC2500-32 offers a digital gain expansion (DGE) feature, allowing the differential full-scale input swing to exceed the $\pm V_{REF}$ analog input range by 0.78% before the digital output code saturates. This is useful for system

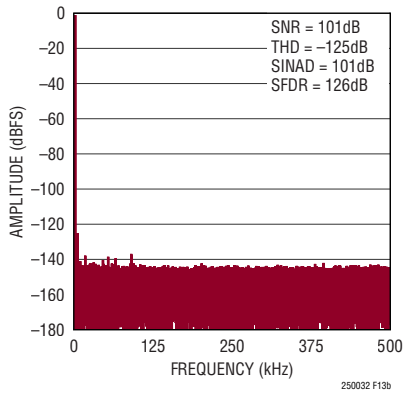


Figure 13b. 128k Point FFT Plot with f_{IN} = 2kHz for Circuit Shown in Figure 13a

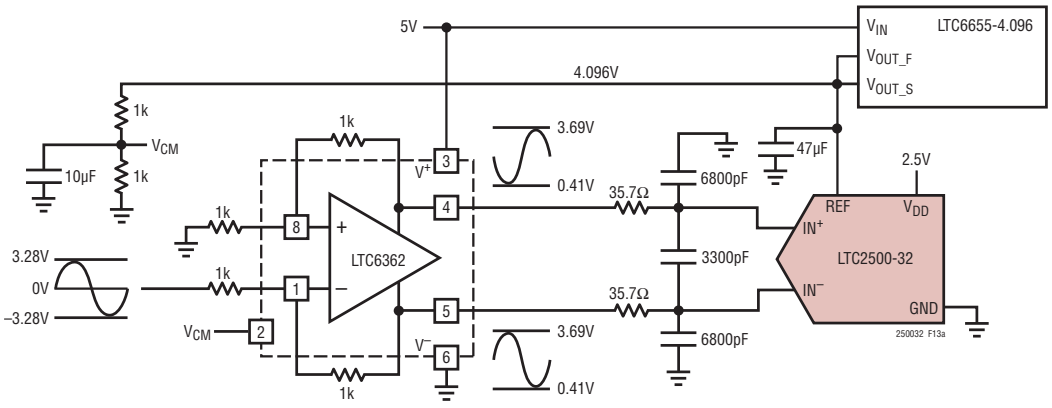


Figure 13a. LTC6362 Configured to Accept a ±3.28V Input Signal While Running from a Single 5V Supply When Digital Gain Compression Is Enabled in the LTC2500-32

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Table 1. Ideal Output Code vs Input Signal for Different DGC and DGE Conditions

DGC	DGE	ANALOG INPUT VOLTAGE ($V_{IN}^+ - V_{IN}^-$)	DOUTA (32-BIT)	DOUTB (24-BIT)
OFF	OFF	$\geq V_{REF}$	7FFFFFFFh	7FFFFFh
		$\leq -V_{REF}$	80000000h	800000h
	ON	$\geq 1.0078xV_{REF}$	407FFFFFh	407FFFh
		V_{REF}	3FFFFFFFh	3FFFFFh
		$-V_{REF}$	C0000000h	C00000h
		$\leq 1.0078xV_{REF}$	BF800000h	BF8000h
ON	OFF	$\geq 0.8V_{REF}$	7FFFFFFFh	7FFFFFh
		$\leq -0.8V_{REF}$	80000000h	800000h
	ON	$\geq 0.80624V_{REF}$	407FFFFFh	407FFFh
		$0.8V_{REF}$	3FFFFFFFh	3FFFFFh
		$-0.8V_{REF}$	C0000000h	C00000h
		$\leq 0.80624V_{REF}$	BF800000h	BF8000h

calibration where a full-scale input voltage may need to be measured, causing the digital output code to saturate. To enable DGE, set DGE(C[8]) = 1 in the configuration word.

Figure 14 shows the ADC transfer function with DGE=0 and DGE=1. The DGE=0 is the nominal transfer function of the ADC, with a $\pm V_{REF}$ full-scale analog input range. A $\pm V_{REF}$ full-scale analog input corresponds to digital output codes $\pm D_{FS}/2$ respectively, with D_{FS} being equal to 2^{32} or 2^{24} depending on whether the output code is read from the filtered output or the no latency output. When DGE=1, the full-scale analog input range increases to $\pm 1.0078xV_{REF}$. To accommodate the increased analog input range, the digital output is divided by a factor of 2. Therefore, a $\pm 1.0078xV_{REF}$ analog input corresponds to digital output codes of $\pm 1.0078xD_{FS}/4$. Table 1 summarizes the input voltages and their corresponding ideal digital output codes for different DGE conditions with DGC turned OFF. Note that the common-mode output does remains unaffected by DGE.

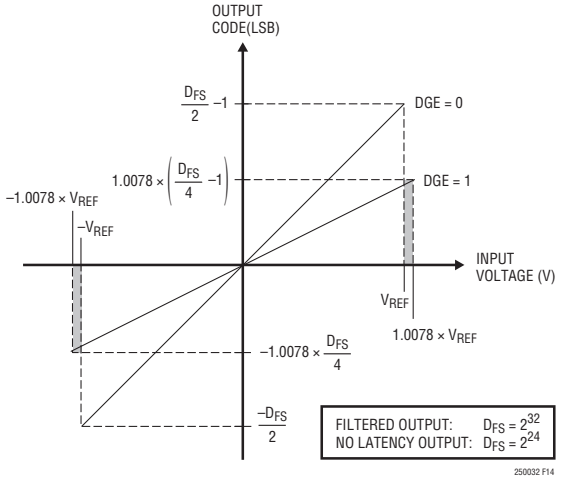


Figure 14. ADC Transfer Functions with DGE = 0 and DGE = 1

Figure 15 shows a use case of the DGE feature, where an ideal differential amplifier is driving the LTC2500-32. The feedback resistors have a ±0.1% tolerance and the reference driving the REF is a 5V reference with a ±0.025%

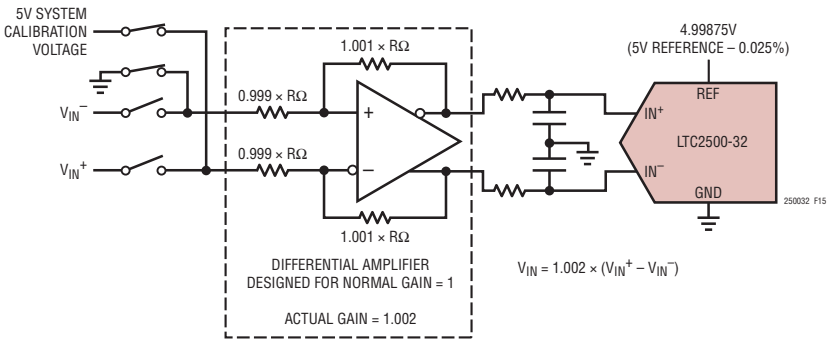


Figure 15. LTC2500-32 Driven By an Ideal Differential Amplifier with 0.1% Resistors

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tolerance. In a practical case where the resistors mismatch and the reference is at the low end of its specified range as shown, applying a 5V system calibration voltage results in an analog input voltage to the ADC is 0.225% greater than 5V, i.e. 5.01125V. With DGE=0, this input voltage would saturate the digital output code of the LTC2500-32. With DGE=1, however, the output code does not saturate and the gain error due to non-idealities can be measured and calibrated.

Using DGC and DGE Simultaneously

The LTC2500-32 allows for simultaneous operation of the DGC and DGE features. With DGC feature turned ON and DGE turned OFF, the input voltage range is limited to $\pm 0.8V_{REF}$. Turning DGE ON, along with DGC, increases this input voltage range by 0.78%, thereby resulting in an input voltage range equal to $\pm 0.8V_{REF} \times 1.0078$ (i.e. $\pm 0.80624V_{REF}$). Table 1 also summarizes the input voltages and their corresponding ideal digital output codes for this mode of operation.

ADC REFERENCE

An external reference defines the input range of the LTC2500-32. A low noise, low temperature drift reference is critical to achieving the full data sheet performance of the ADC. Linear Technology offers a portfolio of high performance references designed to meet the needs of many applications. With its small size, low power and high accuracy, the LTC6655-5 is particularly well suited for use with the LTC2500-32. The LTC6655-5 offers 0.025% (max) initial accuracy and 2ppm/°C (max) temperature coefficient for high precision applications.

When choosing a bypass capacitor for the LTC6655-5, the capacitor's voltage rating, temperature rating, and package size should be carefully considered. Physically larger capacitors with higher voltage and temperature ratings tend to provide a larger effective capacitance, better filtering the noise of the LTC6655-5, and consequently facilitating a higher SNR. Therefore, we recommend bypassing the LTC6655-5 with a 47µF ceramic capacitor (X7R, 1210 size, 10V rating) close to the REF pin.

The REF pin of the LTC2500-32 draws charge (Q_{CONV}) from the 47µF bypass capacitor during each conversion cycle. The reference replenishes this charge with an average current, $I_{REF} = Q_{CONV}/t_{CYC}$. The current drawn from the REF pin, I_{REF}, depends on the sampling rate and output code. If the LTC2500-32 continuously samples a signal at a constant rate, the LTC6655-5 will keep the deviation of the reference voltage over the entire code span to less than 0.5ppm.

When idling, the REF pin on the LTC2500-32 draws only a small leakage current (< 1µA). In applications where a burst of samples is taken after idling for long periods as shown in Figure 16, I_{REF} quickly goes from approximately 0µA to a maximum of 1mA at 1Msps. This step in average current drawn causes a transient response in the reference that must be considered, since any deviation in the reference output voltage will affect the accuracy of the output code. In applications where the transient response of the reference is important, the fast settling LTC6655-5 reference is also recommended.

Reference Noise

The dynamic range of the ADC will increase approximately 6dB for every 4× increase in the down-sampling factor (DF). The SNR should also improve as a function of DF in the same manner. For large input signals near full-scale, however, any reference noise will limit the improvement of the SNR as DF increases, because any noise on the REF pin will modulate around the fundamental frequency of the input signal. Therefore, it is critical to use a low noise reference, especially if the input signal amplitude

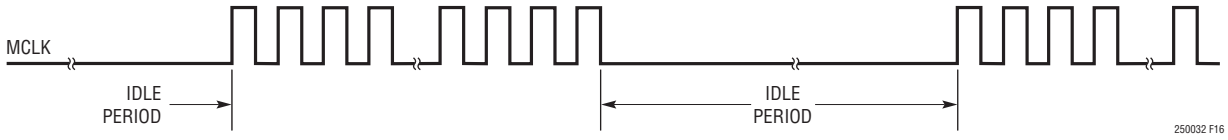


Figure 16. MCLK Waveform Showing Burst Sampling

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approaches full-scale. For small input signals, the dynamic range will improve as described earlier in this section.

DYNAMIC PERFORMANCE

Fast fourier transform (FFT) techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. The LTC2500-32 provides guaranteed tested limits for both AC distortion and noise measurements.

Dynamic Range

The dynamic range is the ratio of the RMS value of a full scale input to the total RMS noise measured with the inputs shorted to $V_{REF}/2$. The dynamic range of the LTC2500-32's 32-bit ADC core is 104dB. The dynamic range of the filtered output improves by 6dB for every 4× increase in the down-sampling factor.

Signal-to-Noise and Distortion Ratio (SINAD)

The signal-to-noise and distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the ADC output. The output is band-limited to frequencies from above DC and below half the sampling frequency. Figure 17 shows that the 32-bit ADC core of the LTC2500-32 achieves a typical SINAD of 104dB at a 1MHz sampling rate with a 2kHz input.

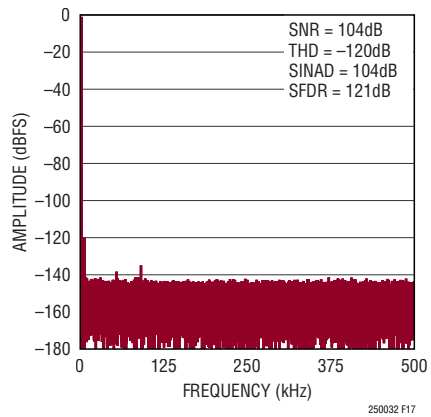


Figure 17. 128k Point FFT Plot of the LTC2500-32 with, f_{IN} = 2kHz and f_{SMPL} = 1MHz

Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC. Figure 17 shows that the 32-bit ADC core of the LTC2500-32 achieves an SNR of 104dB when sampling a 2kHz input at a 1MHz sampling rate.

Total Harmonic Distortion (THD)

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency ($f_{SMPL}/2$). THD is expressed as:

$$THD = 20\log\frac{\sqrt{V2^2+V3^2+V4^2+...+VN^2}}{V1}$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through VN are the amplitudes of the second through Nth harmonics.

POWER CONSIDERATIONS

The LTC2500-32 has two power supply pins: the 2.5V power supply (V_{DD}), and the digital input/output interface power supply (OV_{DD}). The flexible OV_{DD} supply allows the LTC2500-32 to communicate with any digital logic operating between 1.8V and 5V, including 2.5V and 3.3V systems.

Power Supply Sequencing

The LTC2500-32 does not have any specific power supply sequencing requirements. Care should be taken to adhere to the maximum voltage relationships described in the Absolute Maximum Ratings section. The LTC2500-32 has a power-on-reset (POR) circuit that will reset the LTC2500-32 at initial power-up or whenever the power supply voltage drops below 1V. Once the supply voltage reenters the nominal supply voltage range, the POR will reinitialize the ADC. No conversions should be initiated

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until 200µs after a POR event to ensure the reinitialization period has ended. Any conversions initiated before this time will produce invalid results.

TIMING AND CONTROL

MCLK Timing

A rising edge on MCLK will power up the LTC2500-32 and start a conversion. Once a conversion has been started, further transitions on MCLK are ignored until the conversion is complete. For best results, the falling edge of MCLK should occur within 40ns from the start of the conversion, or after the conversion has been completed. For optimum performance, MCLK should be driven by a clean low jitter signal. Converter status is indicated by the BUSY output which remains high while the conversion is in progress. Once the conversion has completed, the LTC2500-32 powers down and begins acquiring the input signal.

Internal Conversion Clock

The LTC2500-32 has internal timing circuity that is trimmed to achieve a maximum conversion time of 660ns. With a maximum sample rate of 1Msps, a minimum acquisition time of 327ns is guaranteed without any external adjustments.

Auto Power Down

The LTC2500-32 automatically powers down after a conversion has been completed and powers up once a new conversion is initiated on the rising edge of MCLK. During power-down, data from the last conversion can be clocked out. To minimize power dissipation during power-down, disable SDOA, SDOB and turn off SCKA, SCKB. The auto power-down feature will reduce the power dissipation of the LTC2500-32 as the sampling rate is reduced. Since power is consumed only during a conversion, the LTC2500-32 remains powered down for a larger fraction of the conversion cycle (t_{CYC}) at lower sample rates, thereby reducing the average power dissipation which scales with the sampling rate as shown Figure 18.

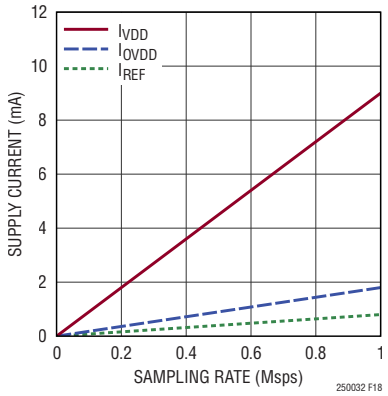


Figure 18. Power Supply Current of the LTC2500-32 vs Sampling Rate

DECIMATION FILTERS

Many ADC applications use digital filtering techniques to reduce noise. An FPGA or DSP is typically needed to implement a digital filter. The LTC2500-32 features a highly configurable integrated decimation filter that provides a variety of filtering functions without any external hardware, thus simplifying the application solution. Figure 19 shows the LTC2500-32 digitally filtered output signal path, wherein the output $D_{ADC}(n)$ of the 32-bit SAR ADC core is passed on to the integrated decimation filter.

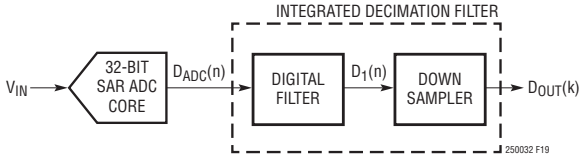


Figure 19. LTC2500-32 Digitally Filtered Output Signal Path

Digital Filtering

The input to the LTC2500-32 is sampled at a rate f_{SMPL}, and digital words $D_{ADC}(n)$ are transmitted to the digital filter at that rate. Noise from the 32-bit SAR ADC core is distributed uniformly in frequency from DC to $f_{SMPL}/2$ Figure 20 shows the frequency spectrum of $D_{ADC}(n)$ at the



Figure 20. Frequency Spectrum of SAR ADC Core Output

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output of the SAR ADC core. In this example, the bandwidth of interest f_B is a small fraction of $f_{SMPL}/2$.

The digital filter integrated in the LTC2500-32 suppresses out-of-band noise power, thereby lowering overall noise and increasing the dynamic range (DR). The lower the filter bandwidth, the lower the noise, and the higher the DR. Figure 21 shows the corresponding frequency spectrum of D1(n) at the output of the digital filter, where noise beyond the cutoff frequency is suppressed by the digital filter.

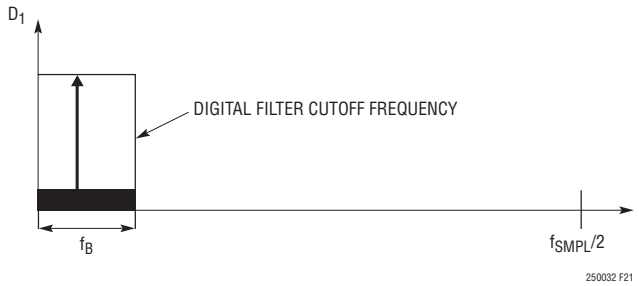


Figure 21. Frequency Spectrum of Digital Filter Core Output

Down-Sampling

The output data rate of the digital filter is reduced by a down-sampler without causing spectral interference in the bandwidth of interest.

The down-sampler reduces the data rate by passing every DF^{th} sample to the output, while discarding all other samples. The sampling frequency f_O at the output of the down sampler is the ratio of f_{SMPL} and DF, i.e., $f_O = f_{SMPL}/DF$. DF is adjustable through the digital interface, allowing the filter bandwidth to be tailored to the application.

Aliasing

The maximum bandwidth that a signal being sampled can have and be accurately represented by its samples is the Nyquist bandwidth. The Nyquist bandwidth ranges from DC to half the sampling frequency (a.k.a. the Nyquist frequency). An input signal whose bandwidth exceeds the Nyquist frequency, when sampled, will experience distortion due to an effect called aliasing.

When aliasing, frequency components greater than the Nyquist frequency undergo a frequency shift and appear within the Nyquist bandwidth. Figure 22 illustrates aliasing in the time domain. The solid line shows a sinusoidal input signal of a frequency greater than the Nyquist frequency ($f_O/2$). The circles show the signal sampled at f_O. Note that the sampled signal is identical to that of sampling another sinusoidal input signal of a lower frequency shown with the dashed line. To avoid aliasing, it is necessary to band limit an input signal to the Nyquist bandwidth before sampling. A filter that suppresses spectral components outside the Nyquist bandwidth is called an anti-aliasing filter (AAF).

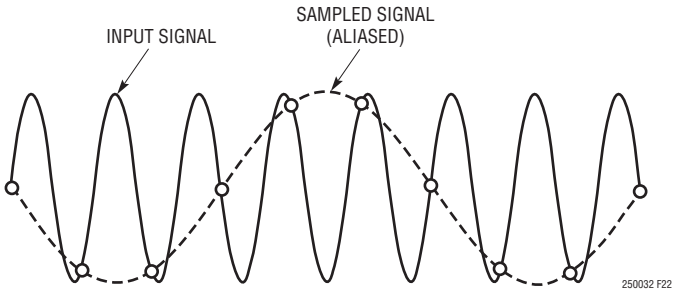


Figure 22. Time Domain View of Aliasing

Anti-Aliasing Filters

Figure 23 shows a typical signal chain including a lowpass AAF and an ADC sampling at a rate of f_O. The AAF rejects input signal components exceeding $f_O/2$, thus avoiding aliasing. If the bandwidth of interest is close to $f_O/2$, then the AAF must have a very steep roll-off. The complexity of the analog AAF increases with the steepness of the roll-off, and it may be prohibitive if a very steep filter is required.

Alternatively, a simple low order analog filter in combination with a digital filter can be used to create a mixed-mode equivalent AAF with a very steep roll-off. A mixed-mode filter implementation is shown in Figure 24 where an analog filter with a gradual roll-off is followed by the LTC2500-32 sampling at a rate of $f_{SMPL} = DF \bullet f_O$. The LTC2500-32 has an integrated digital filter at the output of the ADC core. The equivalent AAF, $H_{EQ}(f)$, is the product of the frequency responses of the analog filter $H_1(f)$ and digital filter $H_2(f)$, as shown in Figure 25. The digital filter provides a steep roll-off, allowing the analog filter to have a relatively gradual roll-off.

The digital filter in the LTC2500-32 operates at the ADC sampling rate f_{SMPL} and suppresses signals at frequencies exceeding $f_O/2$. The frequency response of the digital filter $H_2(f)$ repeats at multiples of f_{SMPL}, resulting in unwanted passbands at each multiple of f_{SMPL}. The analog filter

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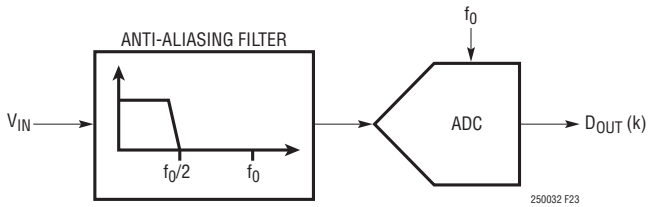


Figure 23. ADC Signal Chain with AAF

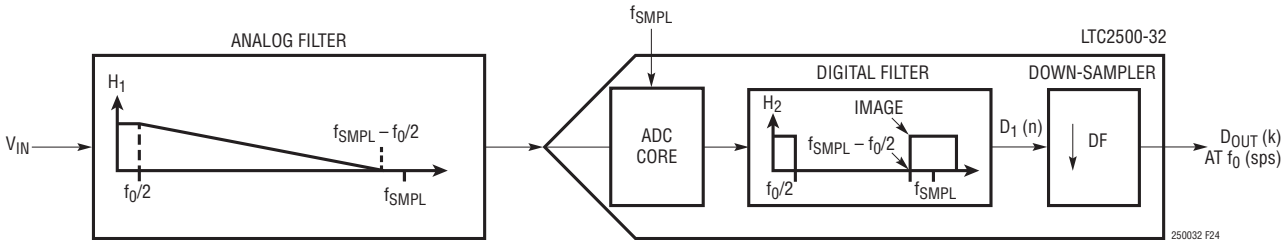


Figure 24. Mixed Mode Filter Signal Chain

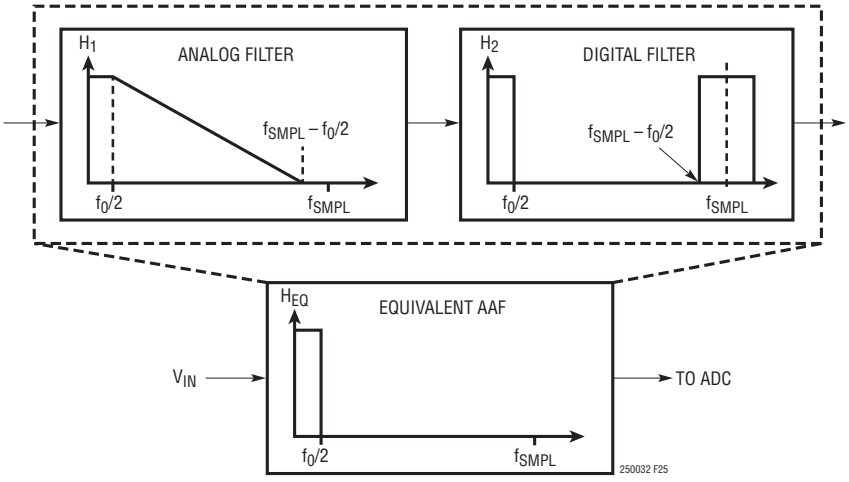


Figure 25. Mixed-Mode Anti-Aliasing Filter (AAF)

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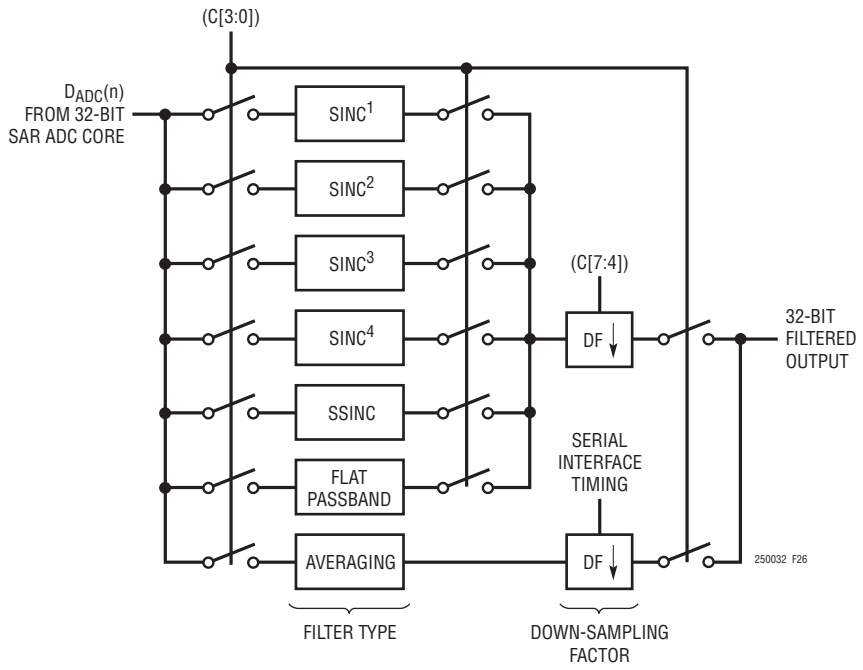


Figure 26. Digital Filter Block Diagram

should be designed to provide adequate suppression of the unwanted passbands, such that $H_{EQ}(f)$ has only one passband corresponding to the frequency range of interest. Larger DF settings correspond to less bandwidth of the digital filter, allowing for the analog filter to have a more gradual roll-off. A simple first- or second-order analog filter will provide adequate suppression for most systems.

DIGITAL FILTER TYPES

The LTC2500-32 offers seven digital filter types that are selected and configured through the digital interface with the C[3:0] bits in the configuration word. The filter types are: $sinc^1$, $sinc^2$, $sinc^3$, $sinc^4$, spread-sinc (ssinc), flat passband and averaging as shown in Figure 26. The output of the selected digital filter type is multiplexed into a down-sampler with a programmable down-sampling factor (DF). DF is set through the digital interface with the C[7:4] bits in the configuration word for all of the filter types except the averaging filter. The averaging filter determines DF by how data is read from the device through the serial interface. The configurability of the digital filter type and down-sampling rates offered in the LTC2500-32 allows the frequency response, filter settling time and output data rate to be tailored to the application.

Frequency Response of the Digital Filters

All of the filter types available on the LTC2500-32 are finite impulse response (FIR) filters with lowpass amplitude response and linear phase responses. The FIR filter coefficients for each filter are available at www.linear.com/docs/55712. The sections below describe the amplitude response of each filter in more detail.

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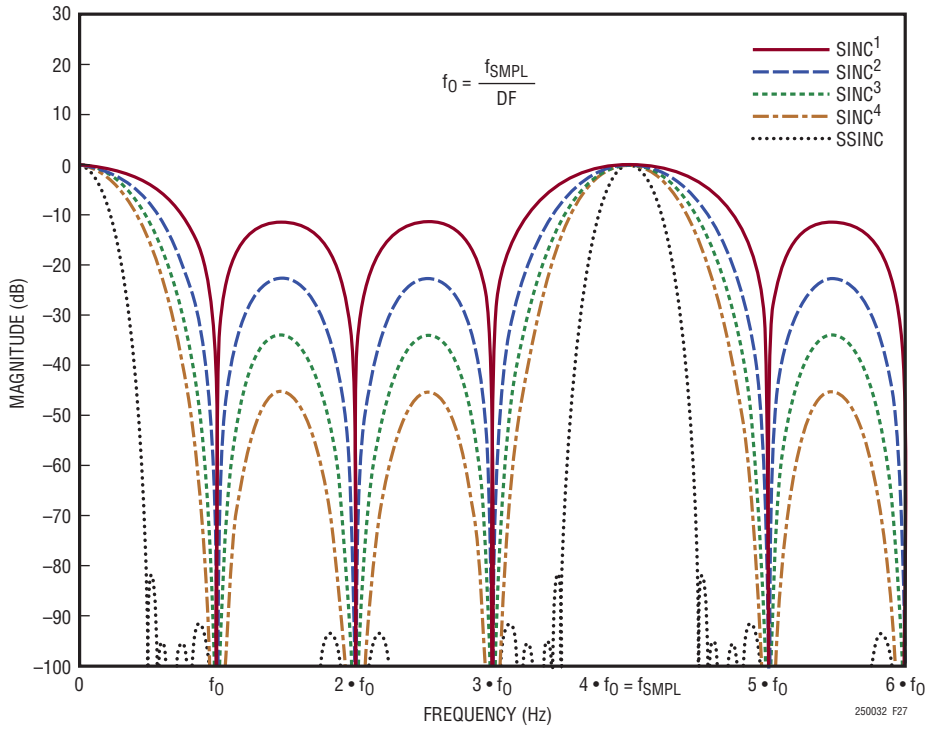


Figure 27. Magnitude of Frequency Response Overlay of Sinc Type Digital Filters with DF = 4

Sinc Filters

There are five types of sinc filters available on the LTC2500-32: $sinc^1$, $sinc^2$, $sinc^3$, $sinc^4$ and spread-sinc (ssinc). Figure 27 shows an overlay of the five sinc filter amplitude responses with DF = 4 at a sampling rate of f_{SMPL}. In this case, f_O is $f_{SMPL}/4$. Note that nulls occur in the amplitude responses of the $sinc^1$, $sinc^2$, $sinc^3$ and $sinc^4$ filters at multiples of f_O, except at multiples of f_{SAMP} where replicas of the passband reside. There is a large suppression of frequencies at the nulls, making it possible to reject specific frequencies by properly choosing f_O. The peaks in the amplitude response between nulls are often referred to as side-lobes. The magnitude of the side-lobes decreases with increasing filter order and provides at most 45dB of attenuation with the $sinc^4$ filter. This may be an unacceptable level of attenuation if the analog input contains unwanted signals in the side-lobe regions.

The spread-sinc (ssinc) filter is a composite sinc filter with the nulls distributed or spread in such a way as to minimize the magnitude of the side-lobes to at most 80dB, providing substantially more attenuation of unwanted signals outside of the passband.

Sinc filters are often used in data acquisition applications where DC or low frequency signals are being digitized. Sinc filters are also very often the first stage in multistage digital decimation filters.

Averaging Filter

The frequency response of the averaging filter on the LTC2500-32 is the same as that of a $sinc^1$ filter. The DF of the averaging filter ranges from 1 to 16384 and is adjustable on the fly, providing more flexibility than the $sinc^1$ filter.

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Flat Passband Filter

Figure 28a shows the amplitude response of the flat passband filter with DF = 4 at a sampling rate of f_{SMPL}. As in the previous section, $f_0 = f_{SAMPL}/4$. Note that a replica of the passband occurs at f_{SMPL} and multiples thereof.

Figure 28b shows the amplitude response in the frequency range from DC to f_0. Labels are shown for four distinct regions: a low ripple passband, a 3dB passband, a transition band and a stopband. The low ripple passband ranges from DC to $f_0/4$ and provides a constant amplitude (±0.001dB) as shown in Figure 28c. The 3dB passband ranges from DC to $f_0/3$ where the amplitude response has dropped by 3dB. The transition band is defined from $f_0/3$ to $f_0/2$ and is where the magnitude of the amplitude response undergoes a sharp decrease. At $f_0/2$, the stopband begins. There is a minimum of 65dB attenuation over the entire stopband region for frequencies in the range of $f_0/2$ to $f_{SMPL} - f_0/2$. The minimum attenuation in the stopband improves to 80dB over the frequency range of $2f_0/3$ to $f_{SMPL} - 2f_0/3$.

The flatness of the flat passband filter lends itself to signal processing applications where large bandwidth signals are digitized.

Settling Time and Group Delay

The length of each digital filter's impulse response determines it's settling time. Linear phase filters exhibit constant delay time versus input frequency (that is, constant group delay). Group delay of the digital filter is defined to be the delay to the center of the impulse response.

The ssinc and flat passband filters unique to the LTC2500-32 are optimized for low latency and provide fast settling. Figure 29 shows the output settling behavior of the sinc type filters after a step change on the analog inputs of the LTC2500-32. Figure 30 shows the output settling behavior of the flat passband filter after a step change on the analog inputs of the LTC2500-32. The X axis in both figures is given in units of output sample number.

Digital Filter Summary

Table 2 summarizes various parameters of each digital filter type across all down-sampling factors. When operating at 1.024Msps, the acquisition time (t_{ACQ}) of the LTC2500-32 is reduced to 303.6ns and the output data rate correspondingly increases. Note that the dynamic range and noise values are not affected by sampling rate.

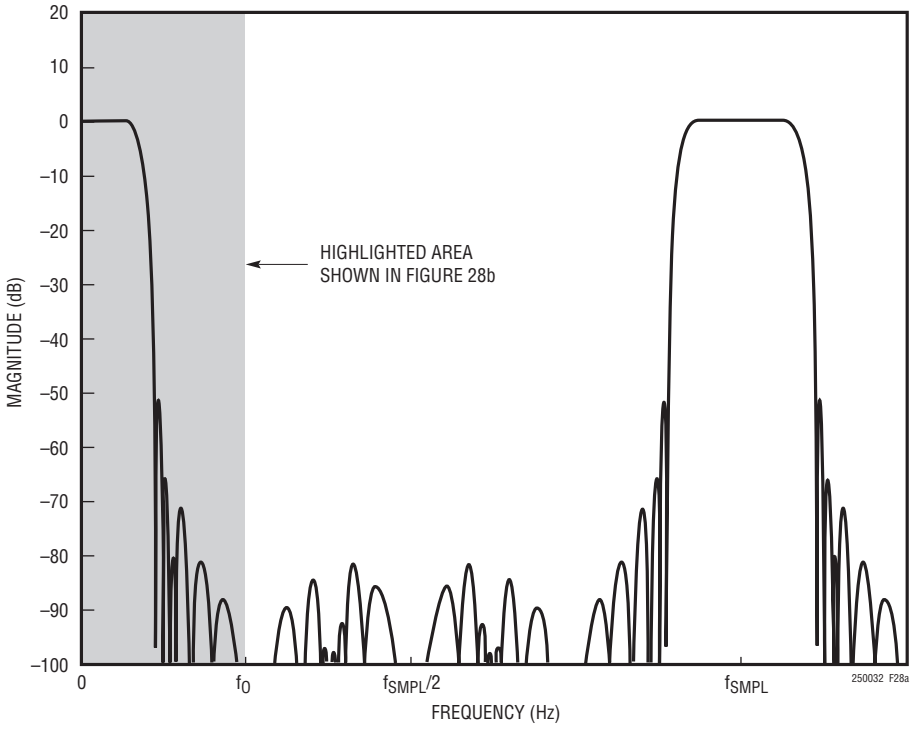


Figure 28a. Magnitude of Frequency Response of Flat Passband Filter with DF = 4

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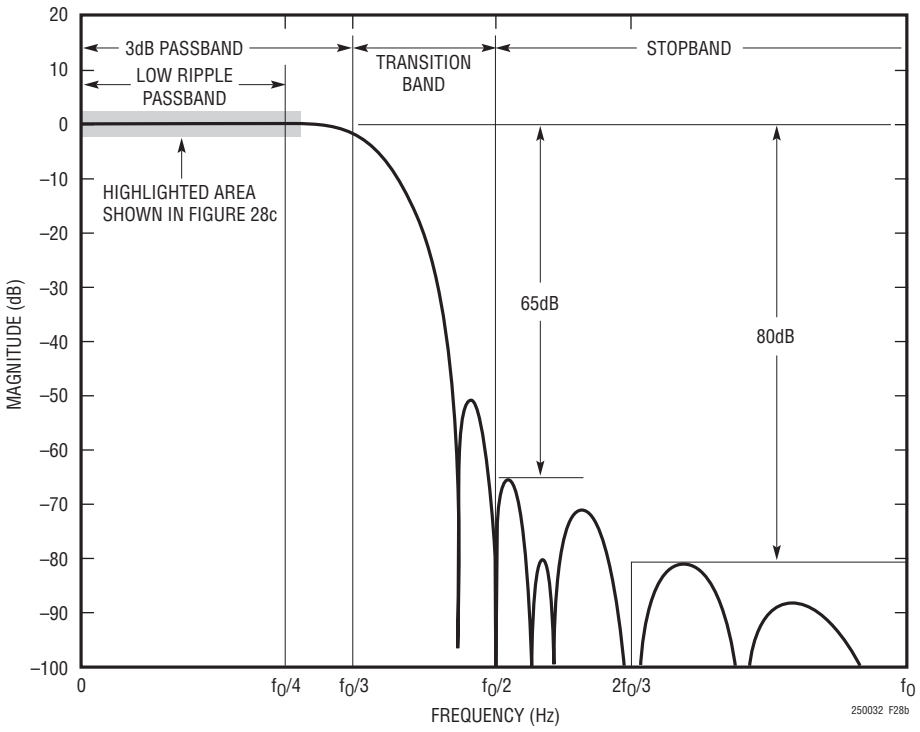


Figure 28b. Highlighted Portion of Frequency Response from Figure 28a

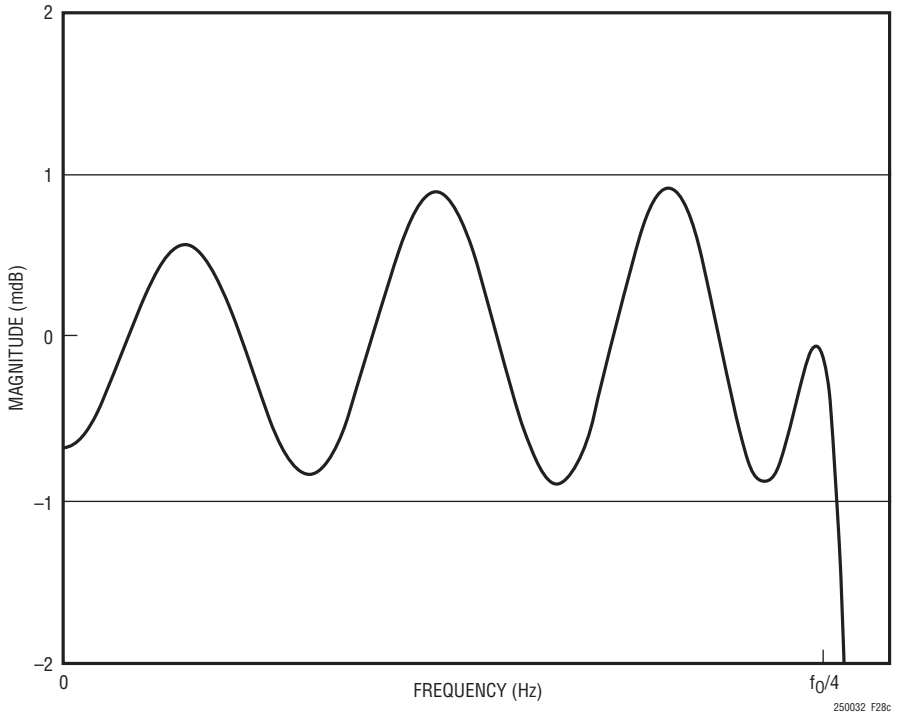


Figure 28c. Low Ripple Passband Portion of Frequency Response from Figure 28b

APPLICATIONS INFORMATION

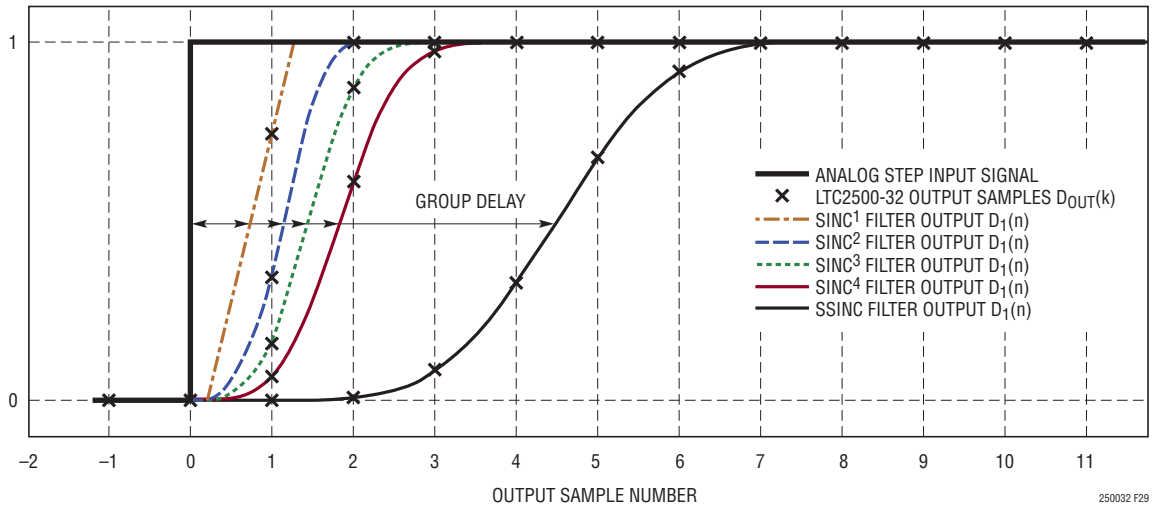


Figure 29. Overlaid Step Responses of Sinc Type Filters

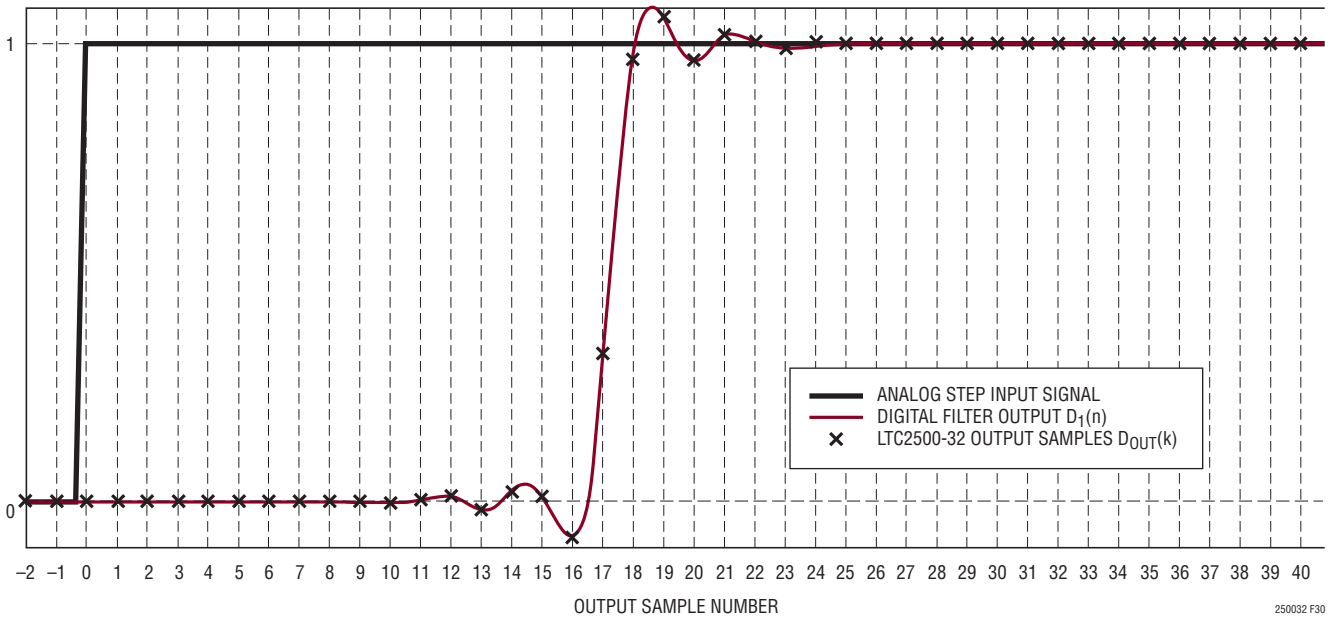


Figure 30. Step Response of Flat Passband Filter

APPLICATIONS INFORMATION

Table 2. Digital Filter Parameters for Different Filter Types and Down-Sampling Factors

FILTER TYPE	DOWN-SAMPLING FACTOR (DF)	OUTPUT DATA RATE		–3dB BANDWIDTH		FILTER LENGTH	GROUP DELAY (f_{SMPL} = 1Msps)	DYNAMIC RANGE (dB)	NOISE (µV RMS)
		f_{SMPL} = 1Msps	f_{SMPL} = 1.024Msps	f_{SMPL} = 1Msps	f_{SMPL} = 1.024Msps				
	4	250ksps	256ksps	113.85kHz	116.58kHz	6	3µs	109.1	12.87
	8	125ksps	128ksps	55.75kHz	57.08kHz	10	5µs	112.2	9.09
	16	62.5ksps	64ksps	27.73kHz	28.40kHz	18	9µs	115.5	6.19
	32	31.25ksps	32ksps	13.85kHz	14.18kHz	34	17µs	118.4	4.42
	64	15.63ksps	16ksps	6.92kHz	7.09kHz	66	33µs	121.2	3.21
	128	7.81ksps	8ksps	3.46kHz	3.54kHz	130	65µs	124	2.31
SINC[1]	256	3.91ksps	4ksps	1.73kHz	1.77kHz	258	129µs	127.4	1.56
	512	1.95ksps	2ksps	865.13Hz	885.89Hz	514	257µs	130.4	1.1
	1024	977sps	1ksps	432.57Hz	442.95Hz	1026	513µs	133.1	0.81
	2048	488sps	500sps	216.28Hz	221.47Hz	2050	1025µs	136	0.58
	4096	244sps	250sps	108.14Hz	110.74Hz	4098	2049µs	138.3	0.44
	8192	122sps	125sps	54.07Hz	55.37Hz	8194	4097µs	141.4	0.31
	16384	61sps	62.5sps	27.04Hz	27.68Hz	16386	8195µs	143.3	0.25
	4	250ksps	256ksps	82.16kHz	84.13kHz	9	4.5µs	111	10.37
	8	125ksps	128ksps	40.16kHz	41.12kHz	17	8.5µs	114.3	7.14
	16	62.5ksps	64ksps	19.97kHz	20.45kHz	33	16.5µs	117	5.21
	32	31.25ksps	32ksps	9.97kHz	10.21kHz	65	32.5µs	120.2	3.59
	64	15.6ksps	16ksps	4.98kHz	5.10kHz	129	64.5µs	123.3	2.51
	128	7.8ksps	8ksps	2.49kHz	2.55kHz	257	128.5µs	125.9	1.86
SINC[2]	256	3.9ksps	4ksps	1.25kHz	1.28kHz	513	256.5µs	128.9	1.31
	512	1.95ksps	2ksps	622.89Hz	637.84Hz	1024	512.5µs	131.9	0.94
	1024	977sps	1ksps	311.44Hz	318.92Hz	2049	1024.5µs	135	0.65
	2048	488sps	500sps	155.72Hz	159.46Hz	4097	2048.5µs	137.6	0.48
	4096	244sps	250sps	77.86Hz	79.73Hz	8193	4096.5µs	140.1	0.36
	8192	122sps	125sps	38.93Hz	39.86Hz	16385	8192.5µs	142.5	0.27
	16384	61sps	62.5sps	19.47Hz	19.93Hz	32769	16384.5µs	144.5	0.21
	4	250ksps	256ksps	67.53kHz	69.15kHz	12	6µs	111.6	9.67
	8	125ksps	128ksps	32.99kHz	33.78kHz	24	12µs	114.9	6.59
	16	62.5ksps	64ksps	16.40kHz	16.80kHz	48	24µs	118.1	4.58
	32	31.25ksps	32ksps	8.19kHz	8.39kHz	96	48µs	121.1	3.26
	64	15.6ksps	16ksps	4.09kHz	4.19kHz	192	96µs	124.1	2.3
	128	7.8ksps	8ksps	2.05kHz	2.10kHz	384	192µs	126.7	1.69
SINC[3]	256	3.9ksps	4ksps	1.02kHz	1.05kHz	768	384µs	130.1	1.15
	512	1.95ksps	2ksps	511.60Hz	523.88Hz	1536	768µs	132.9	0.82
	1024	977sps	1ksps	255.80Hz	261.94Hz	3072	1536µs	135.6	0.61
	2048	488sps	500sps	127.90Hz	130.97Hz	6144	3072µs	138.6	0.43
	4096	244sps	250sps	63.95Hz	65.48Hz	12288	6144µs	140.9	0.33
	8192	122sps	125sps	31.97Hz	32.74Hz	24576	12288µs	143	0.26
	16384	61sps	62.5sps	15.99Hz	16.37Hz	49152	24576µs	145.2	0.2

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Table 2. Digital Filter Parameters for Different Filter Types and Down-Sampling Factors

FILTER TYPE	DOWN-SAMPLING FACTOR (DF)	OUTPUT DATA RATE		–3dB BANDWIDTH		FILTER LENGTH	GROUP DELAY (f_{SMPL} = 1Msps)	DYNAMIC RANGE (dB)	NOISE (µV RMS)
		f_{SMPL} = 1Msps	f_{SMPL} = 1.024Msps	f_{SMPL} = 1Msps	f_{SMPL} = 1.024Msps				
SINC4	4	250ksps	256ksps	58.68kHz	60.08kHz	15	7.5µs	112.7	8.56
	8	125ksps	128ksps	28.66kHz	29.34kHz	31	15.5µs	115.8	5.97
	16	62.5ksps	64ksps	14.25kHz	14.59kHz	63	31.5µs	118.6	4.34
	32	31.25ksps	32ksps	7.11kHz	7.28kHz	127	63.5µs	121.8	2.98
	64	15.6ksps	16ksps	3.56kHz	3.64kHz	255	127.5µs	124.7	2.15
	128	7.8ksps	8ksps	1.78kHz	1.82kHz	511	255.5µs	127.4	1.56
	256	3.9ksps	4ksps	888.72Hz	910.05Hz	1023	511.5µs	130.3	1.12
	512	1.95ksps	2ksps	444.36Hz	455.02Hz	2047	1023.5µs	133.6	0.76
	1024	977sps	1ksps	222.18Hz	227.51Hz	4095	2047.5µs	136	0.58
	2048	488sps	500sps	111.09Hz	113.76Hz	8191	4095.5µs	139	0.41
	4096	244sps	250sps	55.54Hz	56.88Hz	16383	8191.5µs	141.8	0.3
	8192	122sps	125sps	27.77Hz	28.44Hz	32767	16383.5µs	143.3	0.25
	16384	61sps	62.5sps	13.89Hz	14.22Hz	65535	32767.5µs	145.6	0.19
SSINC	4	250ksps	256ksps	30.93kHz	31.67kHz	36	18µs	114.5	6.97
	8	125ksps	128ksps	15.44kHz	15.81kHz	72	36µs	117.7	4.8
	16	62.5ksps	64ksps	7.72kHz	7.90kHz	144	72µs	120.8	3.36
	32	31.25ksps	32ksps	3.86kHz	3.95kHz	288	144µs	123.7	2.39
	64	15.6ksps	16ksps	1.93kHz	1.98kHz	576	288µs	126.8	1.68
	128	7.8ksps	8ksps	964.45Hz	987.59Hz	1152	576µs	129.7	1.2
	256	3.9ksps	4ksps	482.21Hz	493.78Hz	2304	1152µs	132.9	0.83
	512	1.95ksps	2ksps	241.10Hz	246.89Hz	4608	2304µs	135.9	0.59
	1024	977sps	1ksps	120.55Hz	123.45Hz	9216	4608µs	138	0.46
	2048	488sps	500sps	60.28Hz	61.72Hz	18432	9216µs	141.1	0.32
	4096	244sps	250sps	30.14Hz	30.86Hz	36864	18432µs	142.7	0.27
	8192	122sps	125sps	15.07Hz	15.43Hz	73728	36864µs	145.3	0.2
	16384	61sps	62.5sps	7.53Hz	7.72Hz	147456	73728µs	147.6	0.15
Flat Passband	4	250ksps	256ksps	85.74kHz	87.80kHz	140	70µs	110.7	10.69
	8	125ksps	128ksps	42.92kHz	43.95kHz	280	140µs	114	7.34
	16	62.5ksps	64ksps	21.47kHz	21.98kHz	560	280µs	116.8	5.33
	32	31.25ksps	32ksps	10.73kHz	10.99kHz	1120	560µs	120	3.68
	64	15.6ksps	16ksps	5.37kHz	5.50kHz	2240	1120µs	122.8	2.66
	128	7.8ksps	8ksps	2.68kHz	2.75kHz	4480	2240µs	126.1	1.83
	256	3.9ksps	4ksps	1.34kHz	1.37kHz	8960	4480µs	129	1.31
	512	1.95ksps	2ksps	670.85Hz	686.95Hz	17920	8960µs	131.4	0.98
	1024	977sps	1ksps	335.42Hz	343.47Hz	35840	17920µs	134	0.73
	2048	488sps	500sps	167.71Hz	171.74Hz	71680	35840µs	136.8	0.53
	4096	244sps	250sps	83.85Hz	85.87Hz	143360	71680µs	138.1	0.45
	8192	122sps	125sps	41.93Hz	42.93Hz	286720	143360µs	139.8	0.37
	16384	61sps	62.5sps	20.96Hz	21.47Hz	573440	286720µs	140.6	0.34

APPLICATIONS INFORMATION

Table 2. Digital Filter Parameters for Different Filter Types and Down-Sampling Factors

FILTER TYPE	DOWN-SAMPLING FACTOR (DF)	OUTPUT DATA RATE		–3dB BANDWIDTH		FILTER LENGTH	GROUP DELAY (f_{SMPL} = 1Msps)	DYNAMIC RANGE (dB)	NOISE (µV RMS)
		f_{SMPL} = 1Msps	f_{SMPL} = 1.024Msps	f_{SMPL} = 1Msps	f_{SMPL} = 1.024Msps				
Averaging	2	500ksps	512ksps	227.34kHz	232.8	2	1µs	106.4	17.57
	4	250ksps	256ksps	113.85kHz	116.58kHz	4	2µs	109.1	12.87
	8	125ksps	128ksps	55.75kHz	57.08kHz	8	4µs	112.2	9.09
	16	62.5ksps	64ksps	27.73kHz	28.40kHz	16	8µs	115.5	6.19
	32	31.25ksps	32ksps	13.85kHz	14.18kHz	32	16µs	118.4	4.42
	64	15.6ksps	16ksps	6.92kHz	7.09kHz	64	32µs	121.2	3.21
	128	7.8ksps	8ksps	3.46kHz	3.54kHz	128	64µs	124	2.31
	256	3.9ksps	4ksps	1.73kHz	1.77kHz	256	128µs	127.4	1.56
	512	1.95ksps	2ksps	865.13Hz	885.89Hz	512	256µs	130.4	1.1
	1024	977sps	1ksps	432.57Hz	442.95Hz	1024	512µs	133.1	0.81
	2048	488sps	500sps	216.28Hz	221.47Hz	2048	1024µs	136	0.58
	4096	244sps	250sps	108.14Hz	110.74Hz	4096	2048µs	138.3	0.44
	8192	122sps	125sps	54.07Hz	55.37Hz	8192	4096µs	141.4	0.31
	16384	61sps	62.5sps	27.04Hz	27.68Hz	16384	8192µs	143.3	0.25

DIGITAL INTERFACE

The LTC2500-32 features two digital serial interfaces. Serial interface A is used to read the filtered output data. Serial interface B is used to read the no latency output data. Both interfaces support a flexible OV_{DD} supply, allowing the LTC2500-32 to communicate with any digital logic operating between 1.8V and 5V, including 2.5V and 3.3V systems.

Serial interface A is enabled when RDLA is low and serial interface B is enabled when RDLB is low. Serial data is clocked out on the SDOA pin and serial configuration data is clocked in at the SDI pin when an external clock is applied to the SCKA pin if serial interface A is enabled. Serial data is clocked out on the SDOB pin when an external clock is applied to the SCKB pin if serial interface B is enabled. Output data from serial interface A transitions on rising edges of SCKA and output data from serial interface B transitions on rising edges of SCKB. Serial input data at SDI is latched on rising edges of SCKA.

The configuration of the LTC2500-32 is programmed through serial interface A with a configuration word that is input at SDI. The following sections describe the various ways the LTC2500-32 can be configured and general use of the LTC2500-32.

LTC2500-32 Control Word

The various modes of operation of the LTC2500-32 are programmed by 10 bits of a 12-bit control word, C[11:0]. The control word is shifted in at SDI on the rising edges of SCKA, MSB first. The control word is defined and shown in Figure 31.

C[11]	C[10]	C[9]	C[8]	C[7]	C[6]	C[5]	C[4]	C[3]	C[2]	C[1]	C[0]
X	X	DGC	DCE	DOWN-SAMPLING FACTOR(DF)				FILTER TYPE			

250032 F31

Figure 31. Control Word

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C[11] and C[10] are used during the programming of the LTC2500-32 and do not control the configuration of the digital filter or ADC. Bits C[3:0] select the filter type. Bits C[7:4] select the down-sampling factor (DF). C[8] enables/disables digital gain expansion (DGE) and C[9] enables/disables digital gain compression (DGC). Table 3 summarizes the configuration options.

Table 3. Configuration Option Summary

BITS	VALUE	SETTING
C[3:0] = FILTER TYPE	0001	$SINC^1$
	0010	$SINC^2$
	0011	$SINC^3$
	0100	$SINC^4$
	0101	SSINC
	0110	FLAT PASSBAND
	0111	AVERAGING
	OTHER CODES	INVALID CODE
C[7:4] = DF	0010	4
	0011	8
	0100	16
	0101	32
	0110	64
	0111	128
	1000	256
	1001	512
	1010	1024
	1011	2048
	1100	4096
	1101	8192
	1110	16384
	OTHER CODES	INVALID CODE
C[8] = DGE	0	DGE OFF
	1	DGE ON
C[9] = DGC	0	DGC OFF
	1	DGC ON

Programming the Configuration

A transaction window opens at power-up, at the falling edge of DRL, at the falling edge of a RDLA pulse, or when the filter configuration is reset using a SYNC pulse. A transaction window opening allows the filter configuration of the LTC2500-32 to be programmed. Once the transaction window opens, the state machine controlling the programming of the configuration is in a reset state, waiting for a control word to be shifted in at SDI on the first 12 SCKA clock pulses. The transaction window closes at the start of the next conversion when DRL transitions from low to high as shown in Figure 32, or at the end of the 12th SCKA pulse since the transition window opened. Serial input data at SDI should be avoided when BUSY is high.

Input Control Word

The input control word is used to determine whether or not the configuration is programmed. In many cases, the user will simply need to configure the converter once for their specific application after power-up and then drive the SDI pin to GND. This will force the control word bits to all zeros and the LTC2500-32 will operate with the programmed configuration.

The control word is a 12-bit word as described in the LTC2500-32 control word section. A valid input control word is one where C[11:10] = 10 and the remaining lower

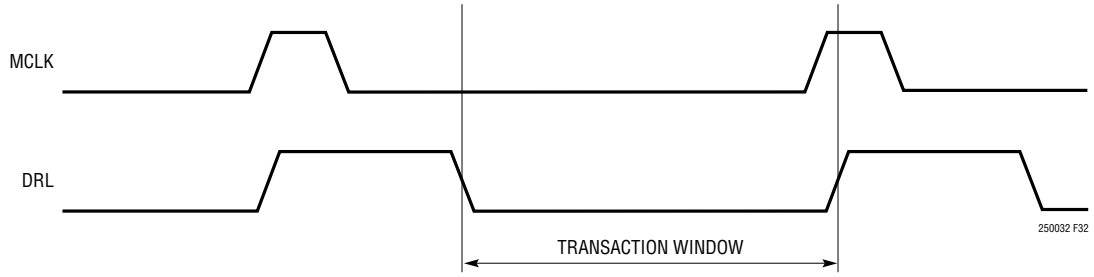


Figure 32. Sequencer Programming Transaction Window

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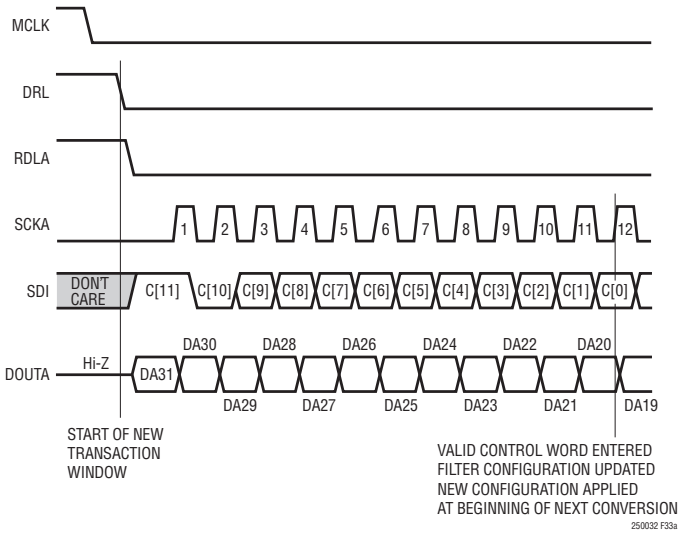


Figure 33a. Valid Control Word Successfully Programmed, C[11:10] = 2`b10

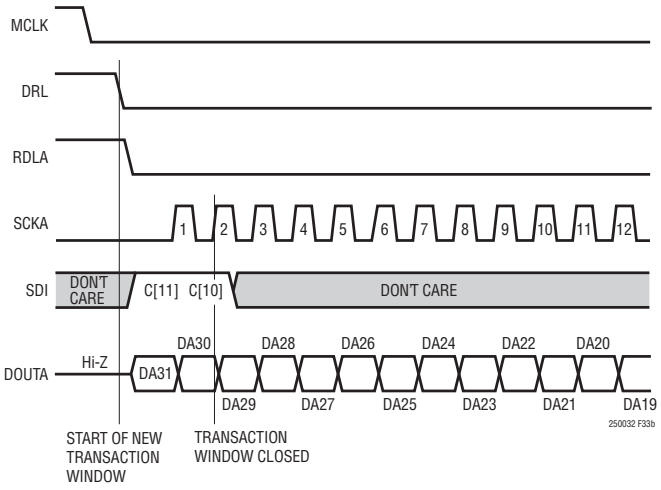


Figure 33b. Invalid Control Word Entered, C[11:10] = 2`b11

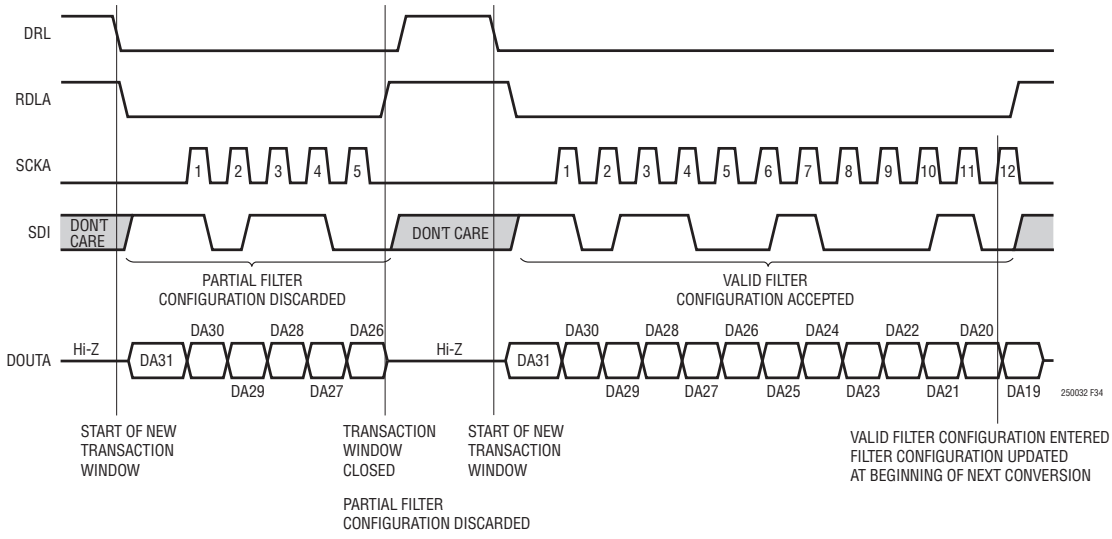


Figure 34. Truncated Programming Transaction Followed by the Successful Programming of One Configuration

10 bits, C[9:0], have been shifted in before the transaction window closes as shown in Figure 33a. When a valid control word is successfully entered on the 12th rising edge of SCKA, the digital filter is reset if the configuration changes and is configured to operate as programmed starting with the next conversion. The configuration of the LTC2500-32 is only programmed by valid input control words and discards control words that are partially written or have C[11:10] ≠ 10. If C[11:10] ≠ 10, the LTC2500-32 closes the input transaction window until the next transaction window as shown in Figure 33b. Figure 34 shows a truncated programming transaction where a partial input control word is discarded and a second complete valid input control word is successfully programmed.

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PRESET FILTER MODES

The LTC2500-32 offers a preset mode that allows the user to select one of two preset digital filter configurations using the logic level of the SDI pin. The preset mode is entered by tying the PRE pin to REF, thereby avoiding the need for SPI programming. Once in preset mode, tying the SDI high configures the digital filter to be an averaging filter with DGC and DGE off. Tying SDI low configures the digital filter to be an ssinc filter with a DF = 64 and both DGC and DGE off. Table 4 lists the preset configurations and the function of the SDI pin when PRE pin is tied high or low.

FILTERED OUTPUT DATA

Figure 35 shows a typical operation for reading the filtered output data for all filter modes with the exception of the averaging filter. The filtered output register contains filtered output codes $D_{OUT}(k)$ provided by the decimation filter. $D_{OUT}(k)$ is updated once in every DF number of conversion cycles. A timing signal DRL indicates when $D_{OUT}(k)$ is updated. DRL goes high at the beginning of every DF^{th} conversion, and it goes low when the conversion completes. The 32-bits of $D_{OUT}(k)$ can be read out before the beginning of the next A/D conversion.

Table 4. Filter Configurations for Different PRE Pin and SDI Pin Configurations

PRE PIN	SDI	DIGITAL FILTER CONFIGURATION
0	Used to Configure the Digital Filter	Based on the SDI Configuration
1	1	Averaging Filter, with DGC and DGE Off
1	0	ssinc with DF = 64, with DGC and DGE Off

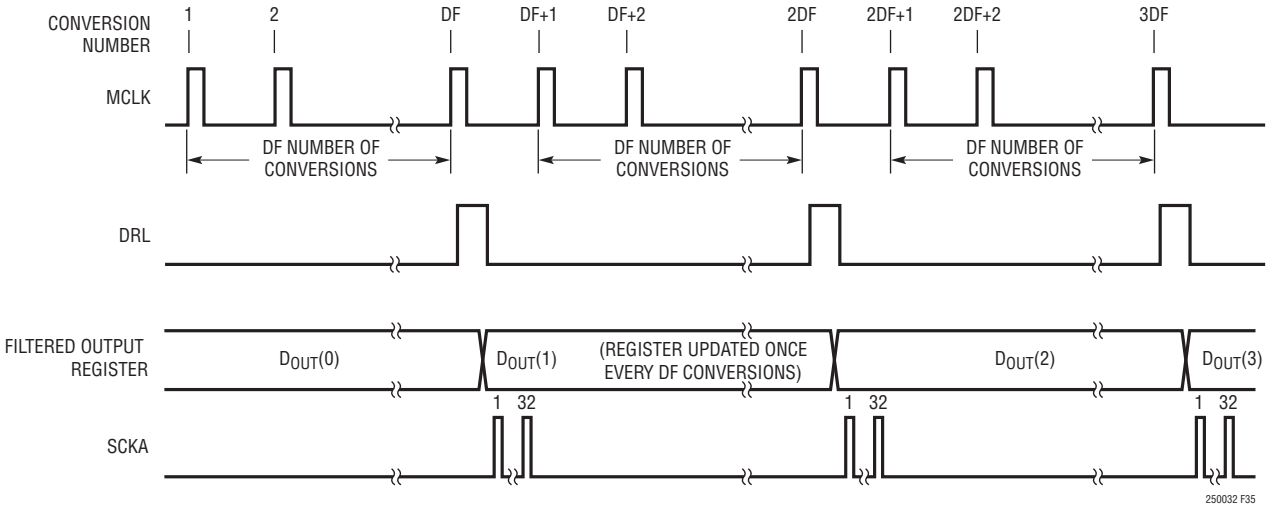


Figure 35. Typical Filtered Output Data Operation Timing

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Distributed Read

LTC2500-32 enables the user to read out the contents of the filtered output register over multiple conversions. Figure 36 shows a case where one bit of $D_{OUT}(k)$ is read for each of 32 consecutive A/D conversions, enabling use of a much slower serial clock (SCKA). Transitions on the digital interface should be avoided during A/D conversion operations (when BUSY is high).

Synchronization

The output of the digital filter $D_1(n)$ is updated every conversion, whereas the down-sampler output $D_{OUT}(k)$ is updated only once every DF number of conversions. Synchronization is the process of selecting when the output $D_{OUT}(k)$ is updated.

This is done by applying a pulse on the SYNC pin of the LTC2500-32. The filtered output register for $D_{OUT}(k)$ is updated at each multiple of DF number of conversions after a SYNC pulse is provided, as shown in Figure 37. A timing signal DRL indicates when $D_{OUT}(k)$ is updated.

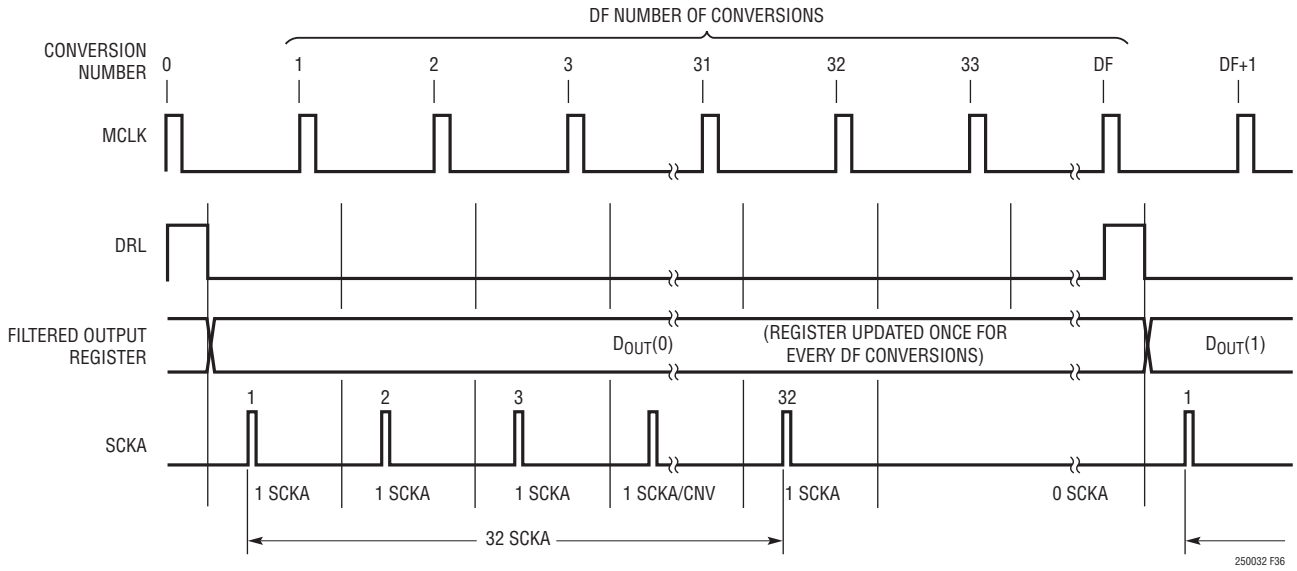


Figure 36. Reading Out Filtered Output Data with Distributed Read

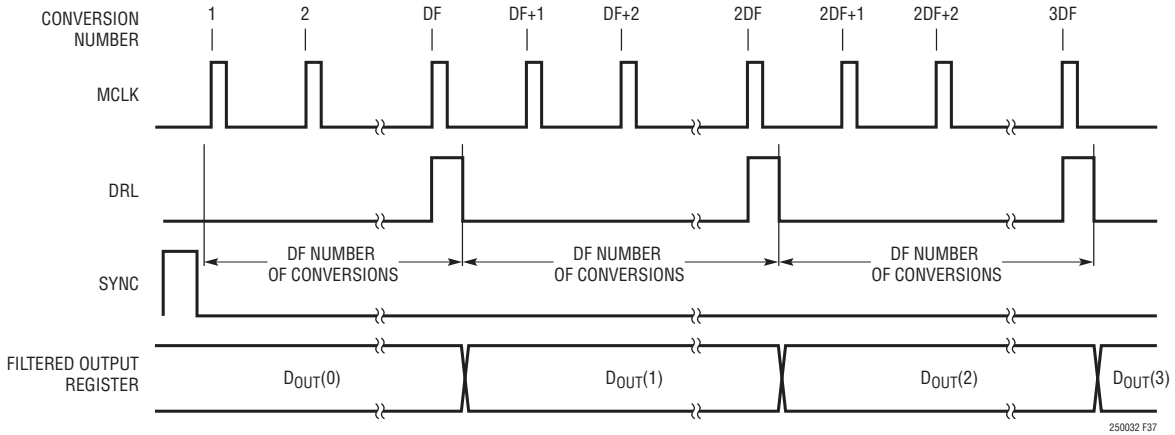


Figure 37. Synchronization Using a Single SYNC Pulse

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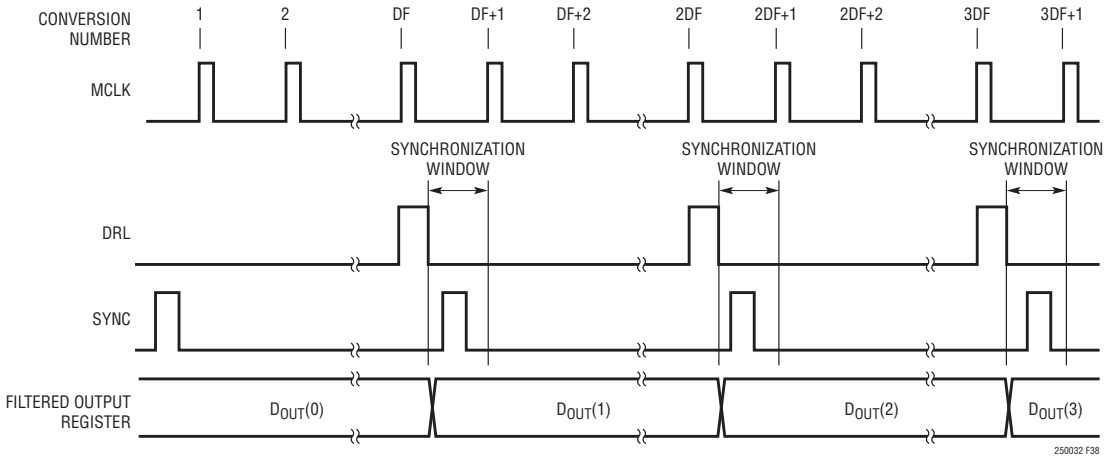


Figure 38. Synchronization Using a Periodic SYNC Pulse

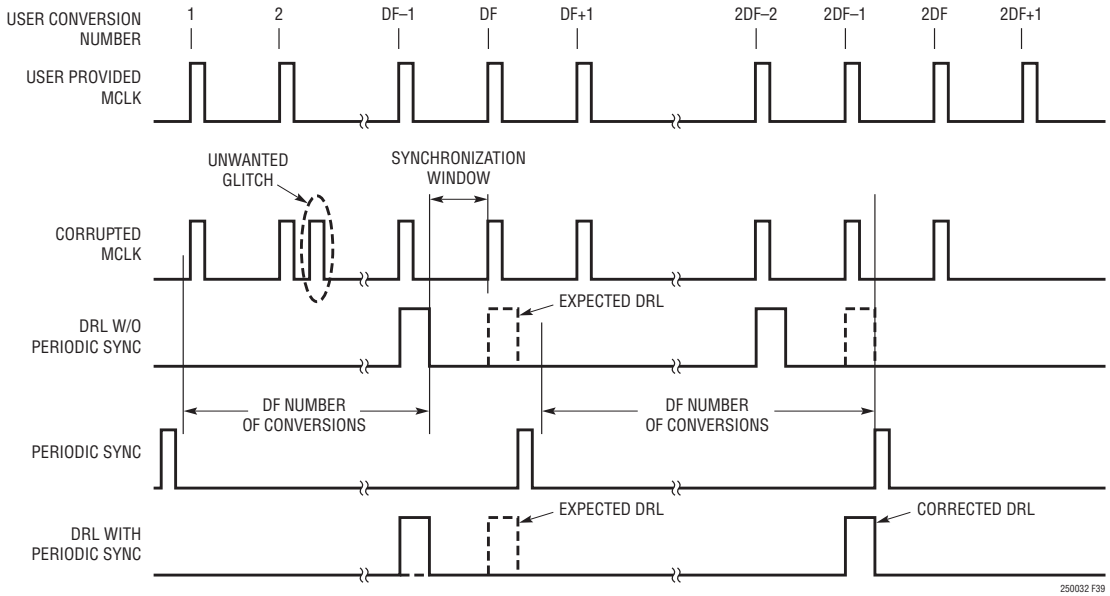


Figure 39. Receiving Synchronization from Unexpected Glitch

The SYNC function allows multiple LTC2500 devices, operated from the same master clock using a common SYNC signal, to be synchronized with each other. This allows each LTC2500 device to update its output register at the same time. Note that all devices being synchronized must operate with the same DF.

Periodic Synchronization

SYNC pulses that reinforce an existing synchronization do not interfere with normal operation. Figure 38 shows a case where a SYNC pulse is applied for each DF number of conversions to continually reinforce a synchronization. Figure 38 indicates synchronization windows when a SYNC pulse may be applied to reinforce the synchronized operation.

Self-Correcting Synchronization

Figure 39 shows a case where an unexpected glitch on MCLK causes an extra A/D conversion to occur. This extra conversion alters the update instants for $D_{OUT}(k)$. The applied periodic SYNC pulse reestablishes the desired synchronization and self corrects within one conversion

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cycle. Note that the digital filter is reset when the synchronization is changed (reestablished).

Configuration Word

An 8-bit configuration word, WA[7:0], is appended to the 32-bit output code on SDOA to produce a total output word of 40 bits as shown in Figure 40. The configuration word designates the downsampling factor (DF) and filter type the digital filter is configured to operate with. Clocking out the configuration word is optional. Table 3 lists the configuration summary for different filter types and downsampling factors.

Averaging Filter (SINC^1 Decimation Filter)

The averaging filter in the LTC2500-32 can be used to average blocks of as few as N = 1 or as many as N = 16384 conversion results. The digital averaging filter described in this section is also known as a SINC^1 digital decimation filter. A SINC^1 digital decimation filter is an FIR filter with N equal valued taps.

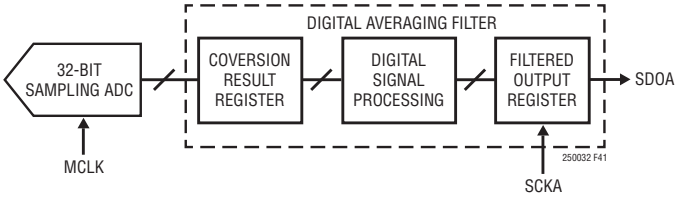


Figure 41. Block Diagram with Digital Averaging Filter

Block Diagram

Figure 41 illustrates a block diagram of the digital averaging filter, including a conversion result register, the digital signal processing (DSP) block, and a filtered output register.

The conversion result register holds the 32-bit conversion result from the most recent sample taken at the rising edge of MCLK. The DSP block provides an averaging operation, loading average values of conversion results into the filtered output register for the user to read through the serial interface.

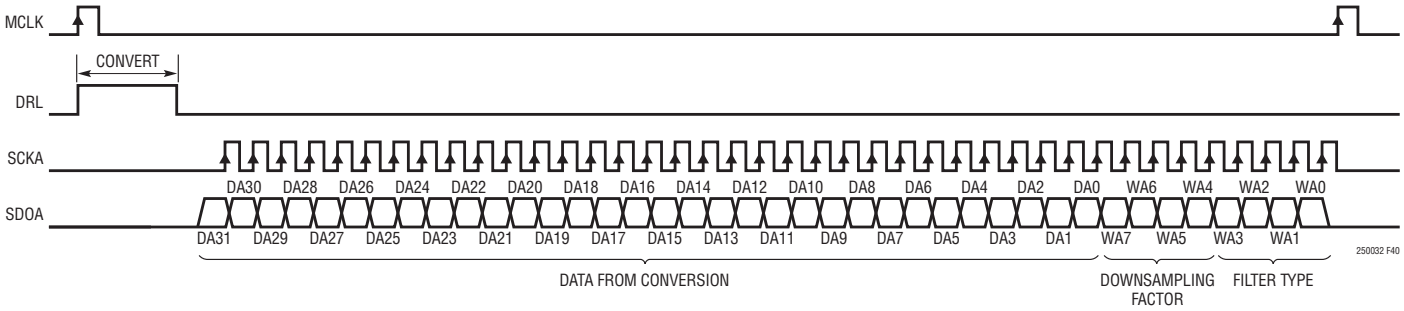


Figure 40. Filtered Output Data Formatting

APPLICATIONS INFORMATION

Conventional SAR Operation (N = 1)

The digital filter of the LTC2500-32 may be operated like a conventional no latency SAR as shown in Figure 42. Each conversion result is read out via the serial interface before the next conversion is initiated. Note how the contents of the filtered output register track the contents of the conversion result register and that both registers contain a result corresponding to a single conversion. The digital averaging filter is transparent to the user when the LTC2500-32 is operated in this way. No programming is required. Simply read out each conversion result in each cycle. Ri represents the 32-bit conversion result corresponding to conversion number i. As few as 20 SCKs may be given in each conversion cycle (instead of the 32 shown in Figure 42) to obtain a 20-bit accurate result. When the LTC2500-32 is configured to operate in the averaging filter mode, DRL indicates when the conversion result register Ri is updated, and is identical to BUSY.

Averaging Four Conversion Results

Digital averaging techniques are often employed to reduce the uncertainty of measurements due to noise. Figure 43 shows a case where a filter output result is read out once for every four conversions initiated. As shown, the output result read out from the filtered output register is the average of the four previous conversion results. The digital averaging filter will automatically average conversion results until a filtered output result is read out. When a filtered output result is read out, the digital averaging filter is reset and a new averaging operation starts with the next conversion result.

In this example, filtered output results are read out after conversion numbers 0, 4 and 8. The digital averaging filter is reset after conversion number 0 and starts a new averaging operation beginning with conversion number 1. The filtered output result (R1 + R2 + R3 + R4)/4 is read out after conversion number 4, which resets the digital averaging filter again. Since the digital averaging filter automatically averages conversion results for each new conversion performed, an arbitrary number of conversion results, up to the upper limit of 16384, may be averaged with no programming required.

Averaging Three Conversion Results

The filtered output result, when averaging N conversion results for values of N that are not a power of two, will be scaled by N/M, where M is a weighting factor that is the next power of two greater than N (described later in the weighting factor section). Figure 44 shows an example where only three conversion results are averaged. The filtered output result read out is scaled by N/M = 3/4.

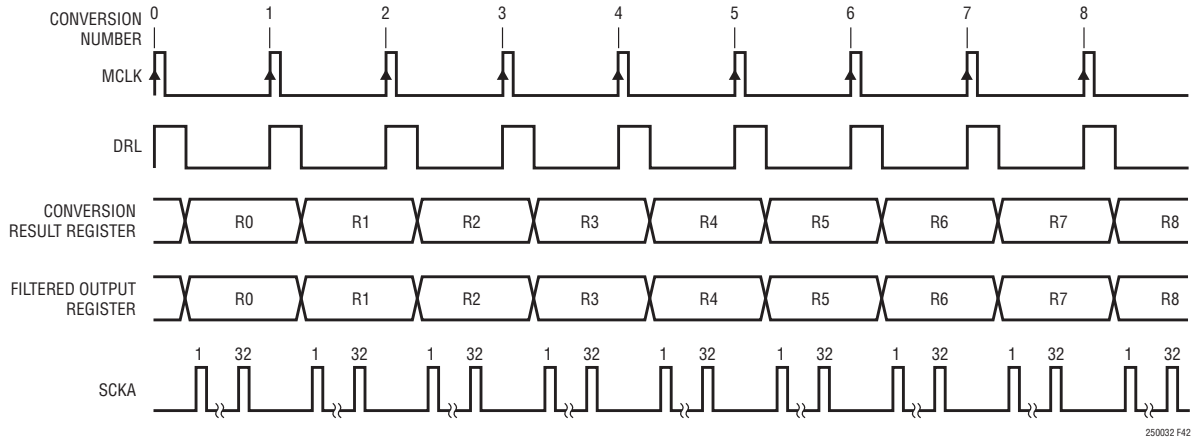


Figure 42. Conventional SAR Operation Timing

APPLICATIONS INFORMATION

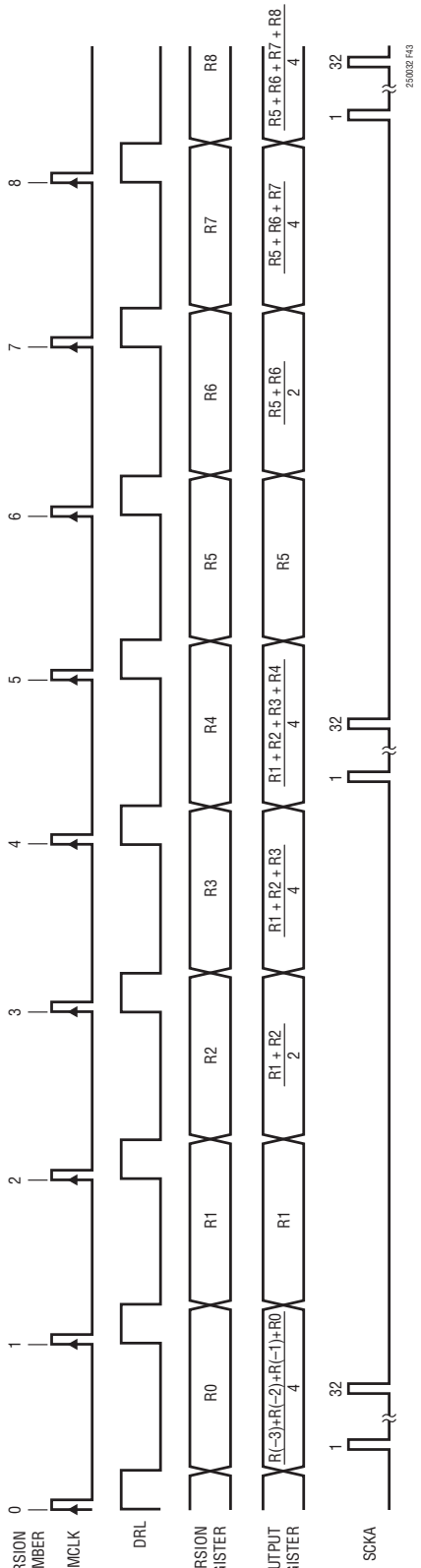


Figure 43. Averaging Four Conversion Results

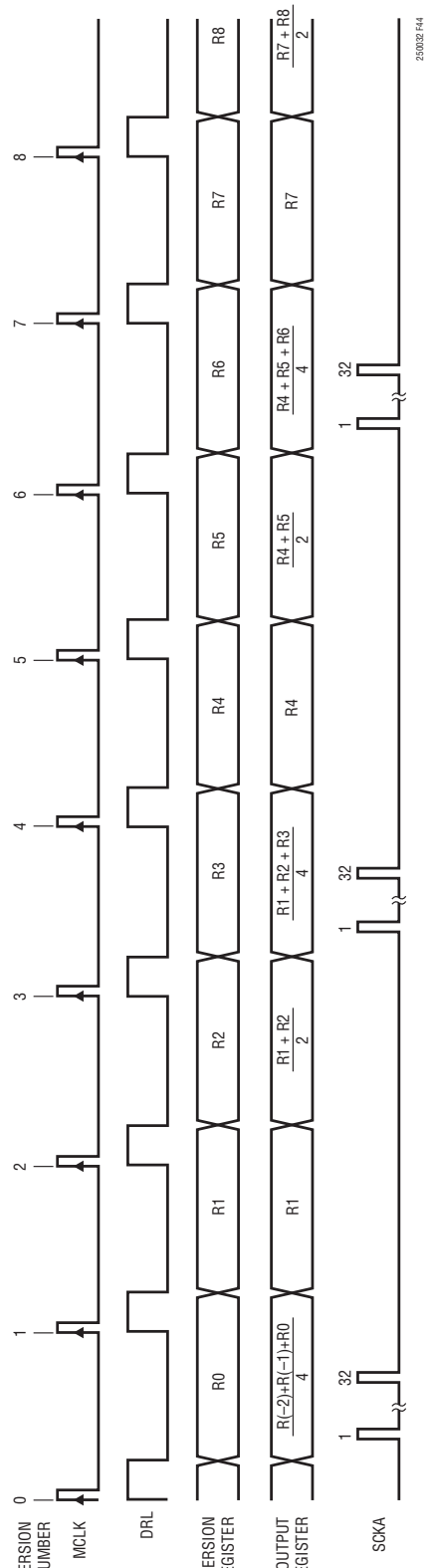


Figure 44. Averaging Three Conversion Results

APPLICATIONS INFORMATION

Using the Digital Averaging Filter with Reduced Data Rate

The examples given in Figures 42, 43 and 44 illustrate some of the most common ways to use the digital averaging filter in LTC2500-32. Simply read each individual conversion result, or read an average of N conversion results. In each case, the result is read out between two consecutive A/D conversion (DRL) periods, thereby requiring a fast SCKA signal to read out all the 32-bits.

Distributed Read with Averaging Filter

Distributed read allows for the use of a slower SCKA signal, while reading out all the 32-bits. Distributed reads require that multiple conversion results be averaged. If at least 1 but less than 20 SCKA pulses(0 < SCKAs < 20) are given in a conversion cycle between 2 DRL falling edges (see Figure 45), the filtered output register is not updated with the output of the digital averaging filter, preserving its contents. This allows a filtered output result to be read from the filtered output register over multiple conversion cycles, easing the speed requirements of the serial interface.

A read is initiated by a rising edge of a first SCKA pulse and it must be terminated before a next read can be initiated. The digital averaging filter is reset upon the initiation of a read wherein a new averaging operation begins. Conversions completed after the digital averaging filter is reset will automatically be averaged until a new read is initiated. Thus, the digital averaging filter will calculate averages of conversion results from conversions completed between a time when one read is initiated to when a next read is initiated.

A read is terminated by providing either 0 or greater than 19 SCKA pulses (rising edges) in a conversion cycle between 2 DRL falling edges, allowing the filtered output register to be updated with new averages from the output of the digital averaging filter.

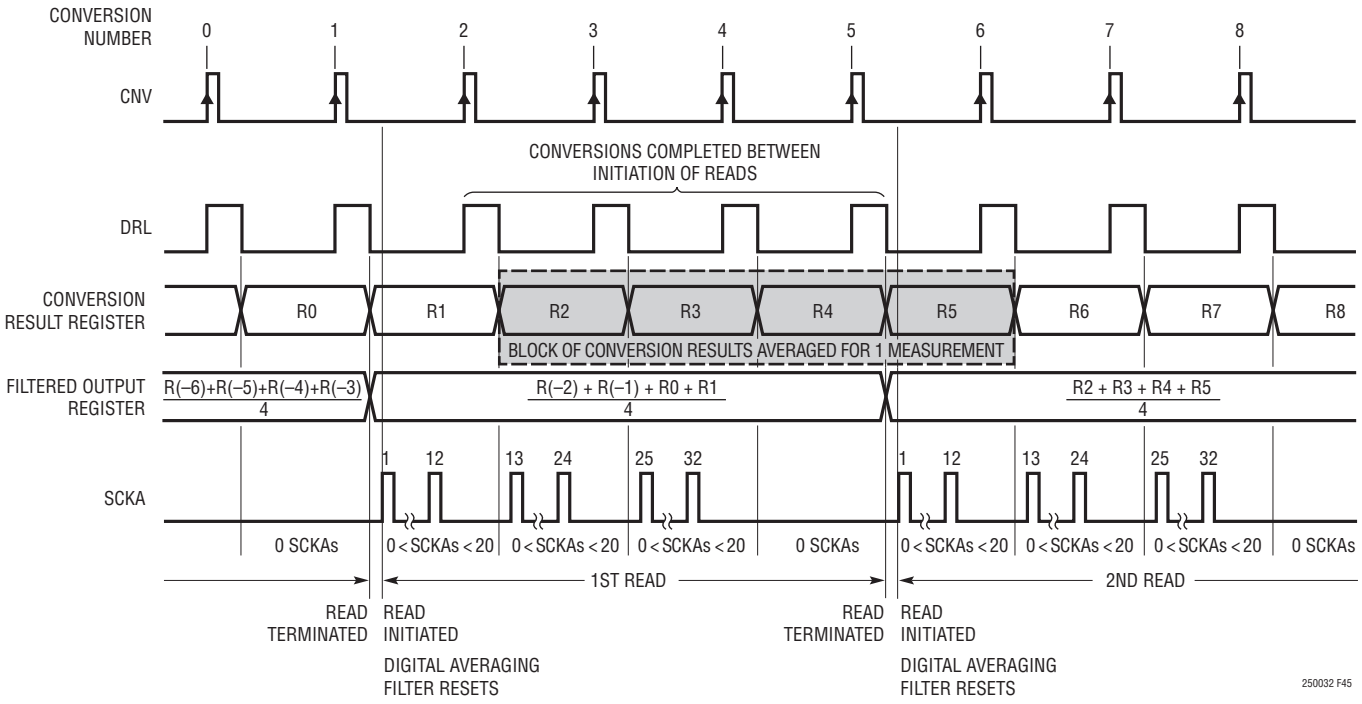


Figure 45. Averaging Four Conversion Results and Reading Out Data with a Distributed Read

APPLICATIONS INFORMATION

Averaging Four Conversions Using a Distributed Read

Figure 45 shows an example where reads are initiated every four conversion cycles, and the filtered output register is read over three conversion cycles. This allows the serial interface to run at 1/3 of the speed that it would otherwise have to run. The first rising SCKA edge initiates a 1st read, and three groups of 12, 12, 8-bits are read out over three conversion cycles. No SCKA pulses are provided between the DRL falling edges of conversion numbers 4 and 5, whereby the read is terminated at the completion of conversion number 5. A second read is initiated after conversion number 5, which results in (R2 + R3 + R4 + R5)/4 being read out from the filtered output register since conversion numbers 2, 3, 4 and 5 completed between the initiation of the two reads shown.

Averaging 33 Conversions Using a Distributed Read

Figure 46 shows an example where a read is initiated every 33 conversion cycles, using a single SCKA pulse per conversion cycle to read the output result from the filtered output register. The first rising SCKA edge initiates a read where a single bit is then read out over the next 31 conversion cycles. No SCKA pulses are provided between the DRL falling edges of conversion numbers 33 and 34, whereby the read is terminated at the completion of conversion number 34. A 2nd read is initiated after conversion number 34, resulting in (R2 + R3 +…+ R25 + R34)/64 being read out from the filtered output register. Since 0 < SCKAs < 20 pulses are given each conversion period during the read, the contents of the filtered output register are not updated, allowing the distributed read to occur without interruption.

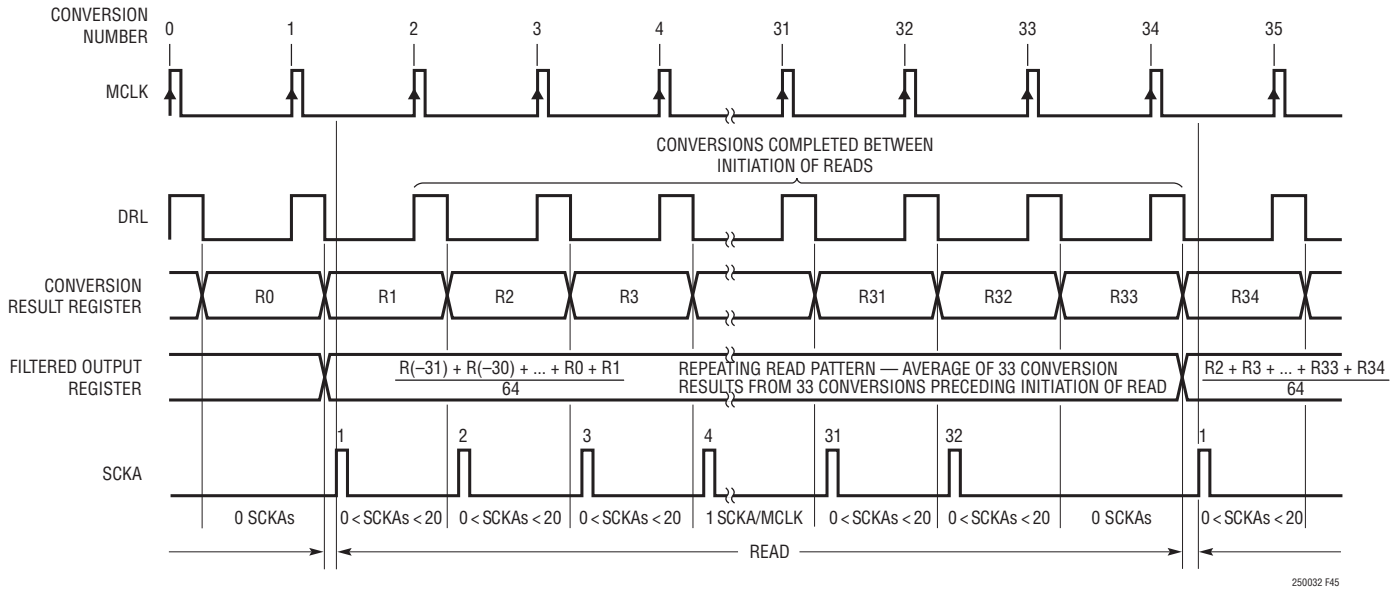


Figure 46. Averaging 33 Conversion Results and Reading Out Data with a Distributed Read

APPLICATIONS INFORMATION

Minimum Shift Clock Frequency with Averaging Filter

Requiring at least 1 SCKA pulse per conversion cycle while performing a read sets a lower limit on the SCKA frequency that can be used which is: $f_{SCKA} = f_{SMPL}$, the maximum sampling frequency $f_{SMPL(MAX)}$ = 1Msps.

Weighting Factor

When conversion results are averaged, the resulting output code represents an equally weighted average of the previous N samples if N is a power of 2. If N is not a power of 2, a weighting factor, M, is chosen according to Table 1. Specifically, if Ri represents the 32-bit conversion result of the i^{th} analog sample, then the output code, D, representing N averaged conversion results is defined as:

$$D = \sum_{i=1}^{N} \frac{R_i}{M}$$

Table 5 illustrates weighting factors for any number of averages, N, between 1 and 16384 and the resulting data throughputs. Note that M reaches a maximum value of 16384 when N = 16384. For N > 16384, the digital averaging filter will continue to accumulate conversion results such that N/M > 1. In such a case, if the ADC core produces conversion results that have a non-zero mean, the output result will eventually saturate at positive or negative full-scale.

Table 5. Weighing Factors and Throughput Rates for Various Values of N

N	M	OUTPUT DATA RATE (f_{SMPL} = 1Msps)
1	1	1Msps
2	2	500ksps
3 to 4	4	333ksps to 250ksps
5 to 8	8	200ksps to 125ksps
9 to 16	16	111ksps to 62.5ksps
17 to 32	32	58.8ksps to 31.25ksps
33 to 64	64	30.3ksps to 15.6ksps
65 to 128	128	15.4ksps to 7.8ksps
129 to 256	256	7.8ksps to 3.9ksps
257 to 512	512	3.9ksps to 2ksps
513 to 1024	1024	2ksps to 1ksps
1025 to 2048	2048	976sps to 488sps
2049 to 4096	4096	488sps to 244sps
4097 to 8192	8192	244sps to 122sps
8193 to 16384	16384	122sps to 61sps

Count

As with other filter configurations, an 8-bit configuration word, WA[7:0], is appended to the 32-bit output code on SDOA. The digital averaging filter also outputs an additional 14-bit word, CO[13:0], that is appended to the configuration word to produce a total output word of 54 bits, as shown in Figure 47. CO[13:0] is the straight binary representation (MSB first) of the number of samples averaged to produce

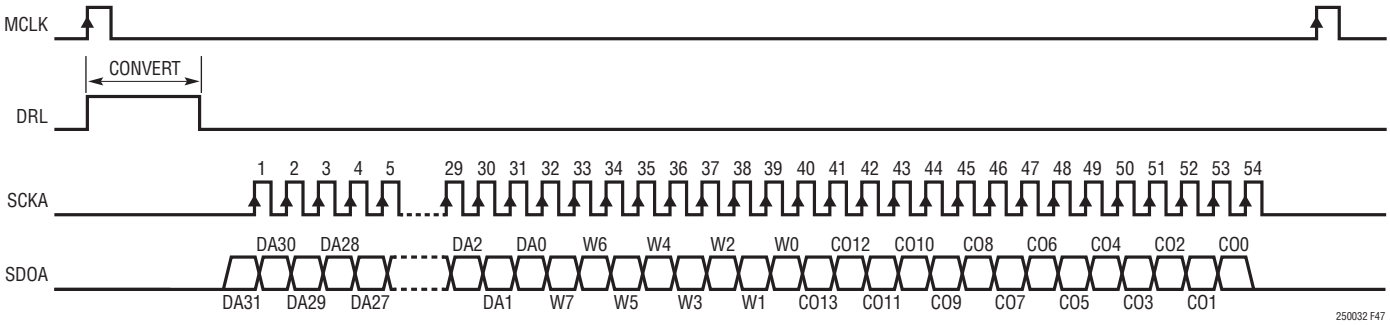


Figure 47. Serial Output Code Formatting for Digital Averaging Filter

APPLICATIONS INFORMATION

the output result minus one. For instance, if N samples are averaged to produce the output result, CO[13:0] will equal N – 1. Thus, if N is 1 which is the case with no averaging, CO[13:0] will always be 0. If N is 8192, then CO[13:0] will equal 8191, and so on. If more than 16384 samples are averaged, then CO[13:0] saturates at 16383.

NO LATENCY OUTPUT DATA

Figure 48 shows a typical operation for reading the no latency output data. The no latency I/O register holds a 32-bit composite code R(n) from the most recent conversion result. The first bit represents the overrange bit. The overrange bit is equal to 1 if the differential input to the LTC2500-32 is greater than the digital saturation limit, as described in Table 1. The following 24 bits of R(n) represent the input voltage difference ($IN^+ – IN^–$), MSB first. The last 7 bits represent the common mode input voltage ($(IN^+ + IN^–)/2$, MSB first. Table 6 shows the output bit format for the 32-bit no latency output data.

Table 6. Output Bit Format for the 32-Bit No Latency Output Data

DB[31]	DB[30:7]	DB[6:0]
Overrange Detection Bit	24-Bit Differential Output	7-Bit Common Mode Output

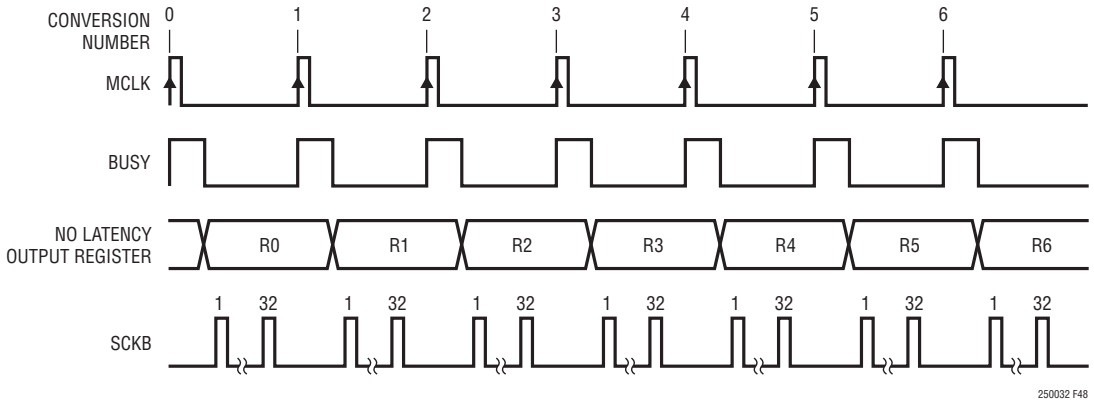


Figure 48. Typical Nyquist Output Data Operation Timing

APPLICATIONS INFORMATION

Filtered Output Data, Single Device

Figure 49 shows an LTC2500-32 configured to operate to read out the filtered output. With RDLA grounded, SDOA is enabled and the MSB (DA31) of the output result is available $t_{DSDOBUSYL}$ after the falling edge of DRL.

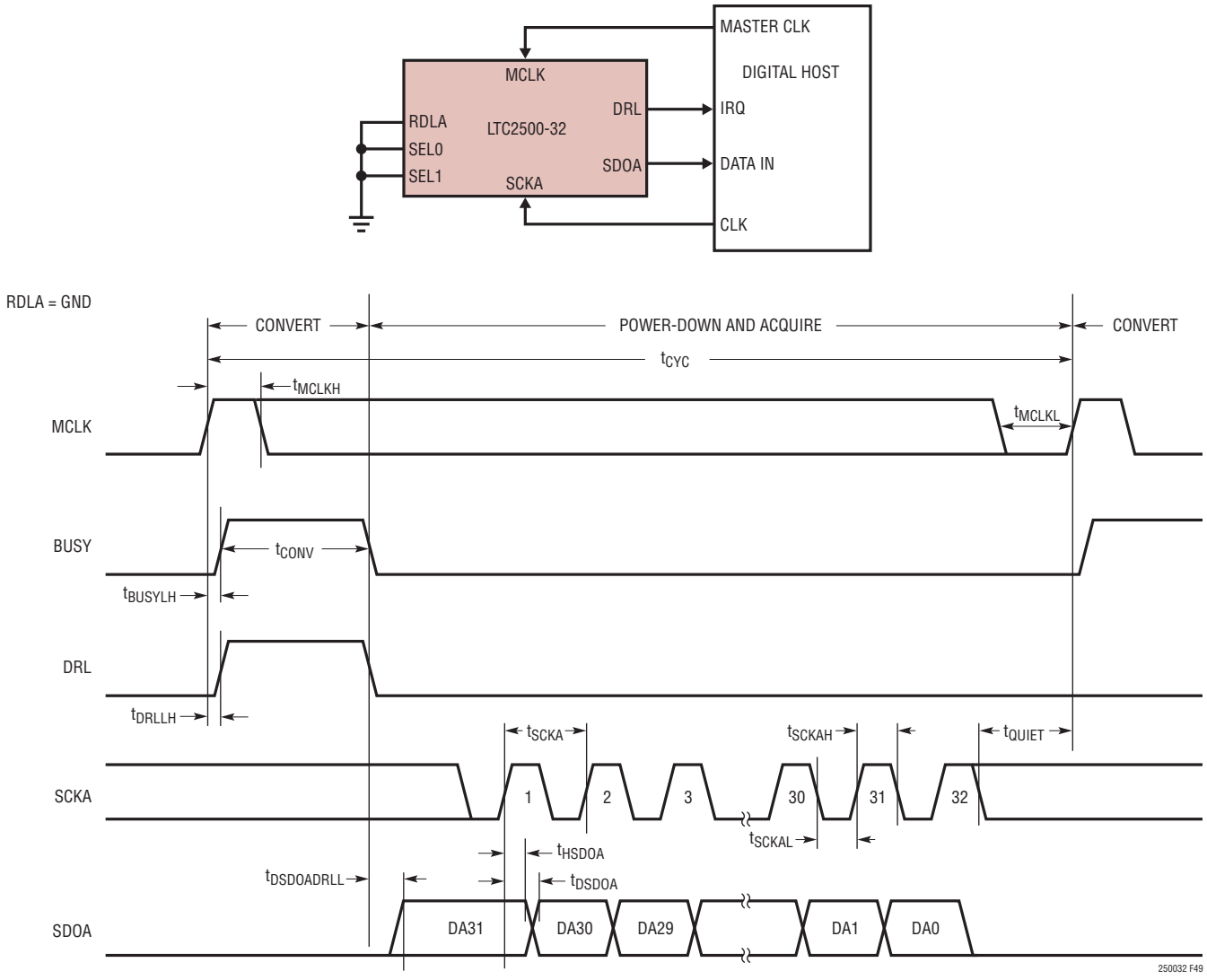


Figure 49. Using a Single LTC2500-32 to Read Filtered Output

APPLICATIONS INFORMATION

Filtered Output Data, Multiple Devices

Figure 50 shows two LTC2500-32 devices configured to operate read out the filtered output, while sharing MCLK, SYNC, SCKA and SDOA. By sharing MCLK, SYNC, SCKA and SDOA, the number of required signals to operate multiple ADCs in parallel is reduced. Since SDOA is shared, the RDLA input of each ADC must be used to allow only one LTC2500-32 to drive SDOA at a time in order to avoid bus conflicts. As shown in Figure 50, the RDLA inputs idle high and are individually brought low to read data out of each device between conversions. When RDLA is brought low, the MSB of the selected device is output on SDOA.

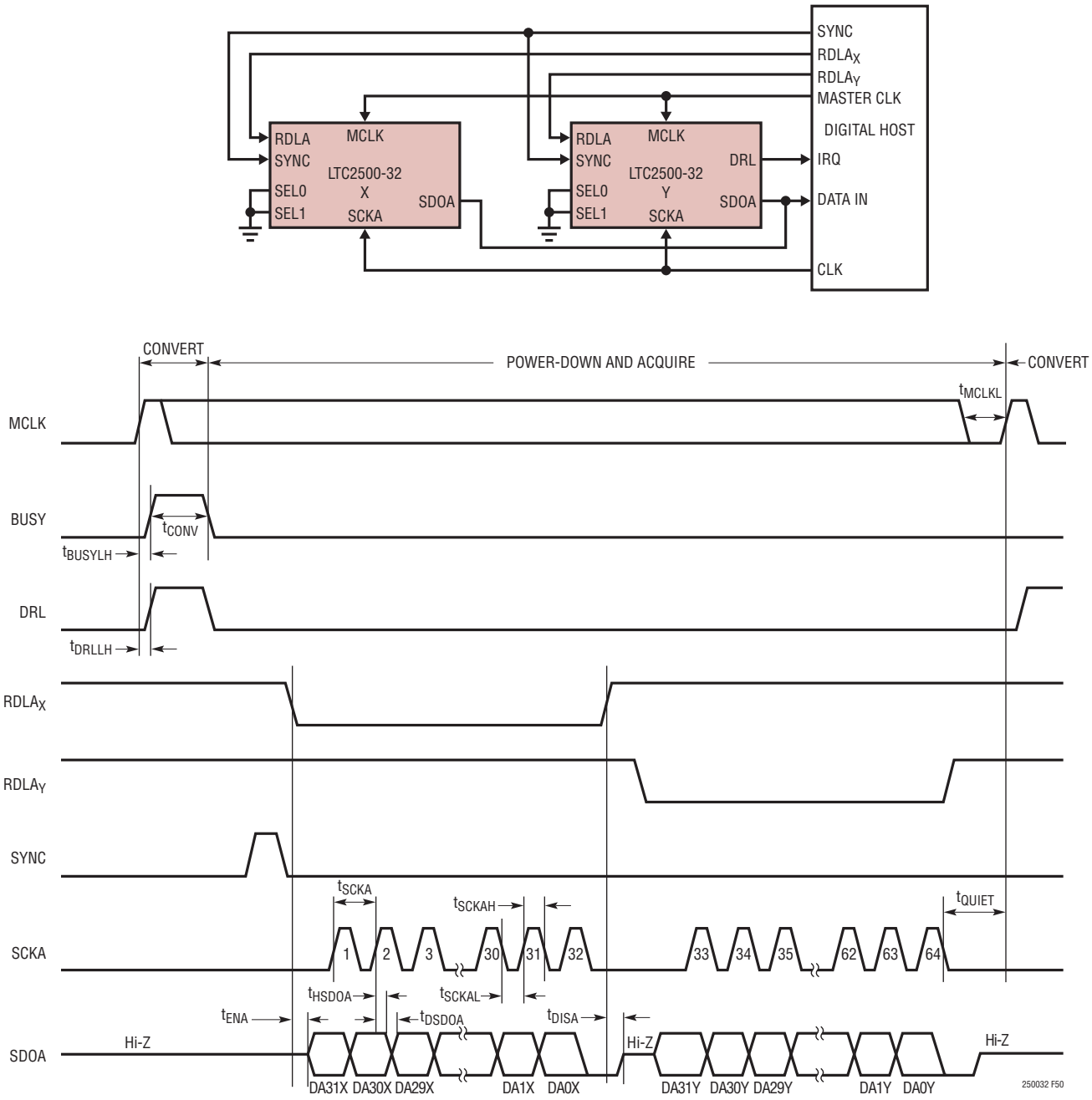


Figure 50. Reading Filtered Output with Multiple LTC2500-32 Devices Sharing MCLK, SCKA and SDOA

APPLICATIONS INFORMATION

No Latency Output Data, Single Device

Figure 51 shows a single LTC2500-32 configured to read the no latency data out. With RDLB grounded, SDOB is enabled the overrange bit (OVRNG) of the output result is available $t_{DSDOBUSYL}$ after the falling edge of BUSY.

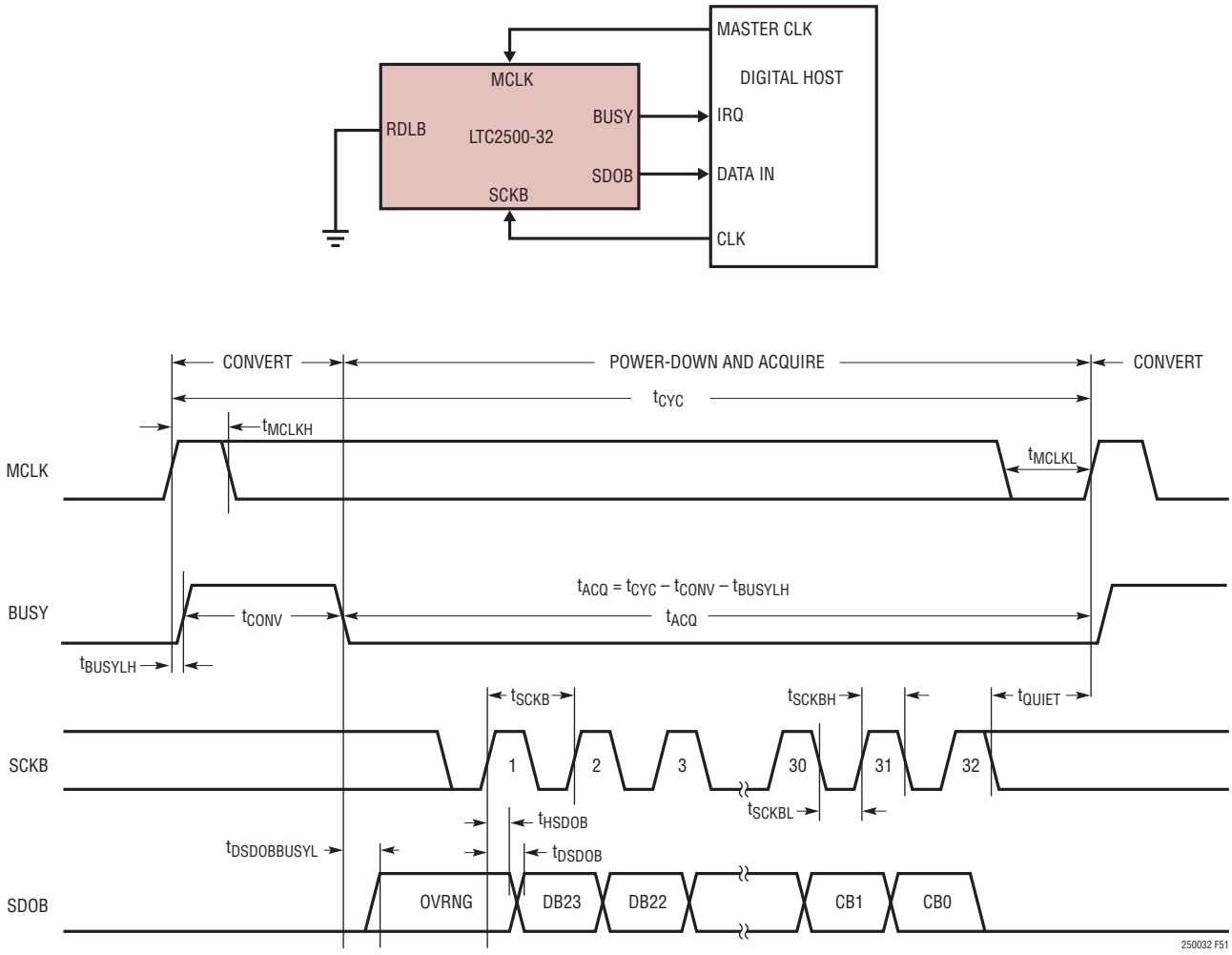


Figure 51. Using a Simple LTC2500-32 to Read No Latency Output

APPLICATIONS INFORMATION

No Latency Output Data, Multiple Devices

Figure 52 shows multiple LTC2500-32 devices configured to read no latency data out, while sharing MCLK, SCKB and SDOB. By sharing MCLK, SCKB and SDOB, the number of required signals to operate multiple ADCs in parallel is reduced. Since SDOB is shared, the RDLB input of each ADC must be used to allow only one LTC2500-32 to drive SDOB at a time in order to avoid bus conflicts. As shown in Figure 52, the RDLB inputs idle high and are individually brought low to read data out of each device between conversions. When RDLB is brought low, the overrange bit of the selected device is output on SDOB.

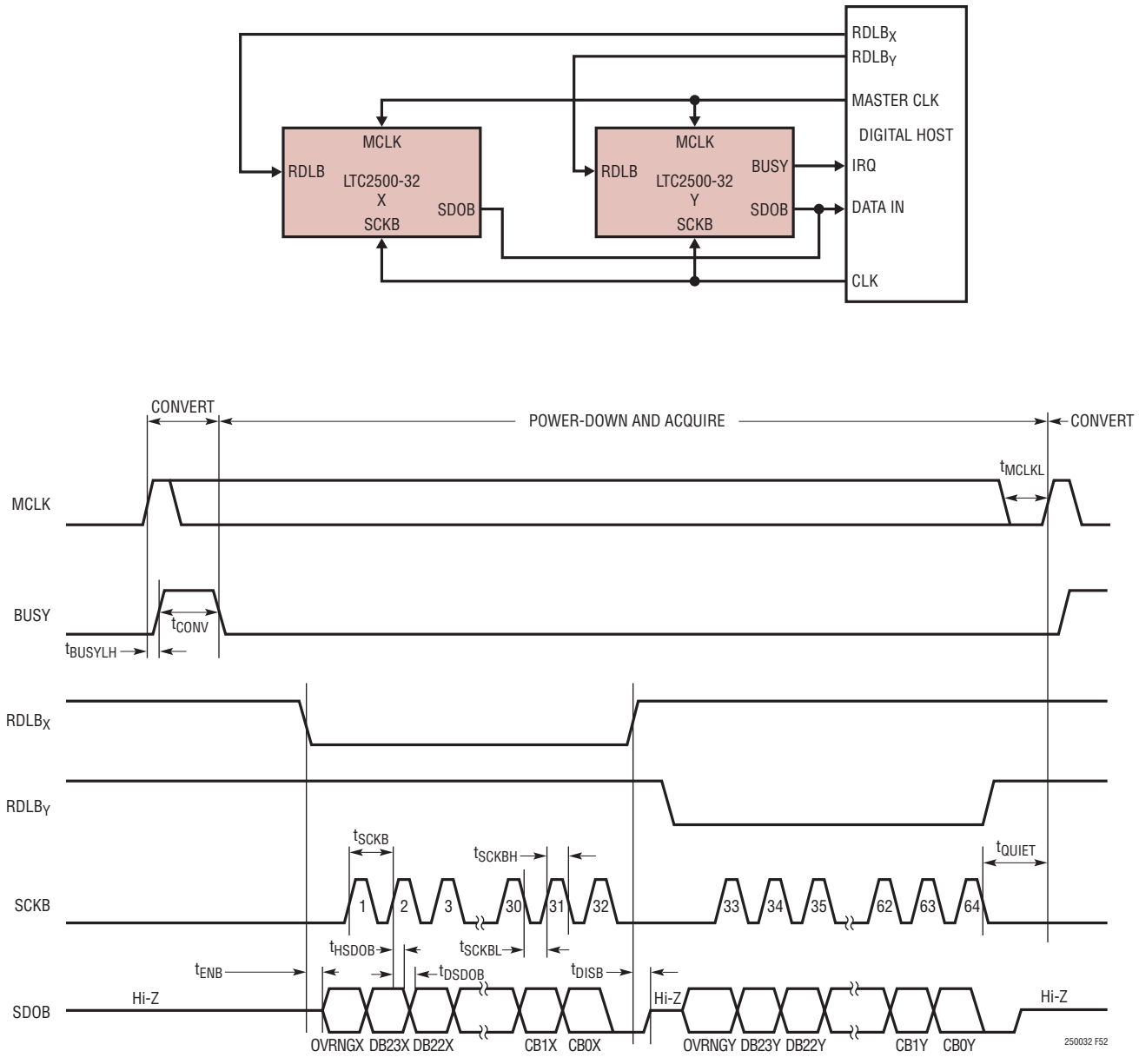


Figure 52. Reading Filtered Output with Multiple LTC2500-32 Devices Sharing MCLK, SCKB and SDOB

APPLICATIONS INFORMATION

Filtered Output Data, No Latency Data, Single Device

Figure 53 shows a single LTC2500-32 device configured to read filtered output data and no latency output data, while sharing SDOA with SDOB and SCLKA with SCKB. Sharing signals reduces the total number of required signals to read both the filtered and no latency data from the ADC. Since SDOA and SDOB are shared, the RDLA and RDLB inputs of the ADC must be used to allow only one output to drive the shared SDO bus at a time in order to avoid bus conflicts. As shown in Figure 53, the RDLA and RDLB inputs idle high and are individually brought low to read data from each serial output when data is available. When RDLA is brought low, the MSB of the filtered output data from SDOA is output on the shared SDO bus. When RDLB is brought low, the overrange (OVRNG) bit of the no latency data output from SDOB is output on the shared SDO bus.

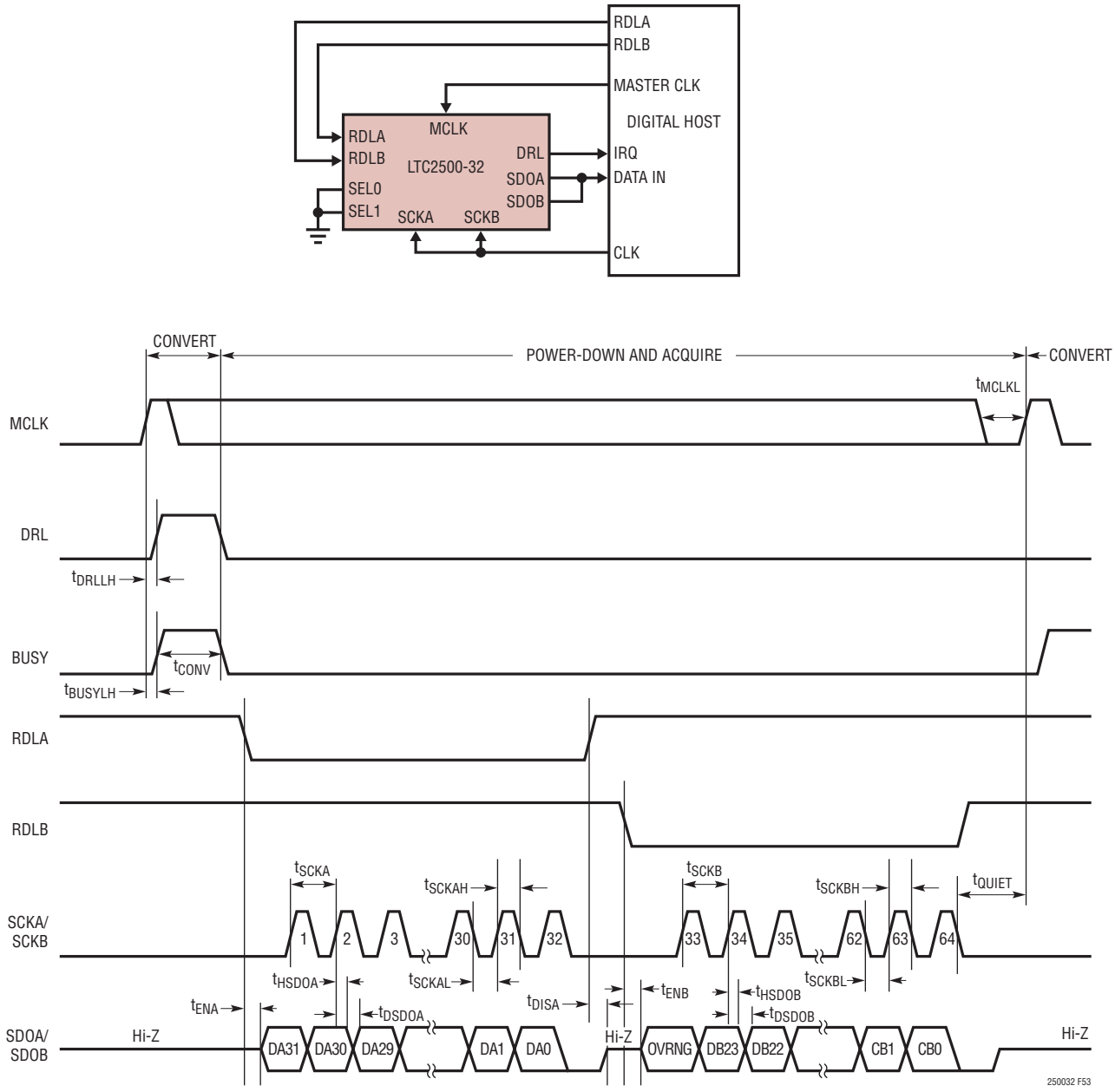


Figure 53. Reading Filtered Output and No Latency Output by Sharing SCK and SDO

BOARD LAYOUT

To obtain the best performance from the LTC2500-32, a four-layer printed circuit board (PCB) is recommended. Layout for the PCB should ensure the digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital clocks or signals alongside analog signals or underneath the ADC.

Supply bypass capacitors should be placed as close as possible to the supply pins. Low impedance common returns for these bypass capacitors are essential to the low noise operation of the ADC. A single solid ground plane is recommended for this purpose. When possible, screen the analog input traces using ground.

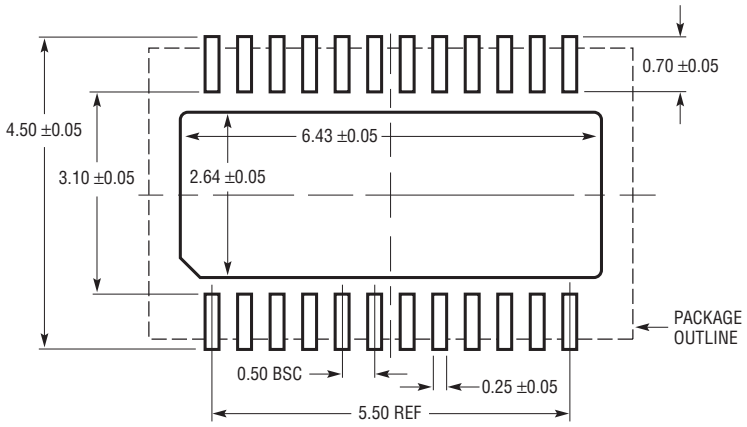
Reference Design

For a detailed look at the reference design for this converter, including schematics and PCB layout, please refer to DC2222, the evaluation kit for the LTC2500-32.

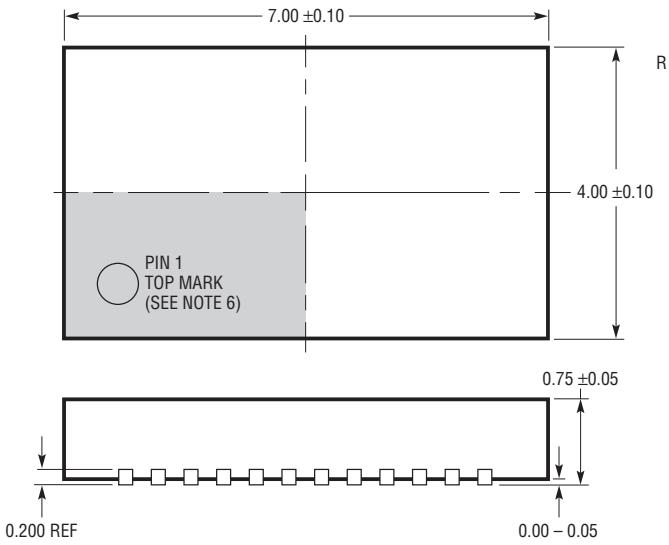
PACKAGE DESCRIPTION

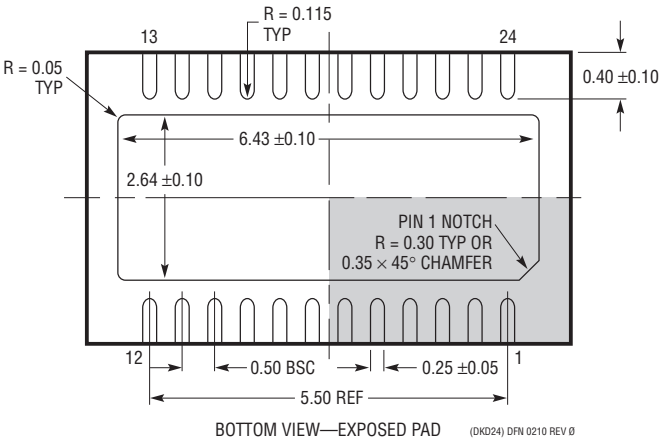
Please refer to http://www.linear.com/product/LTC2500-32#packaging for the most recent package drawings.

DKD Package
24-Lead Plastic DFN (7mm × 4mm)
(Reference LTC DWG # 05-08-1864 Rev Ø)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





BOTTOM VIEW—EXPOSED PAD (DKD24) DFN 0210 REV Ø

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WXXX) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

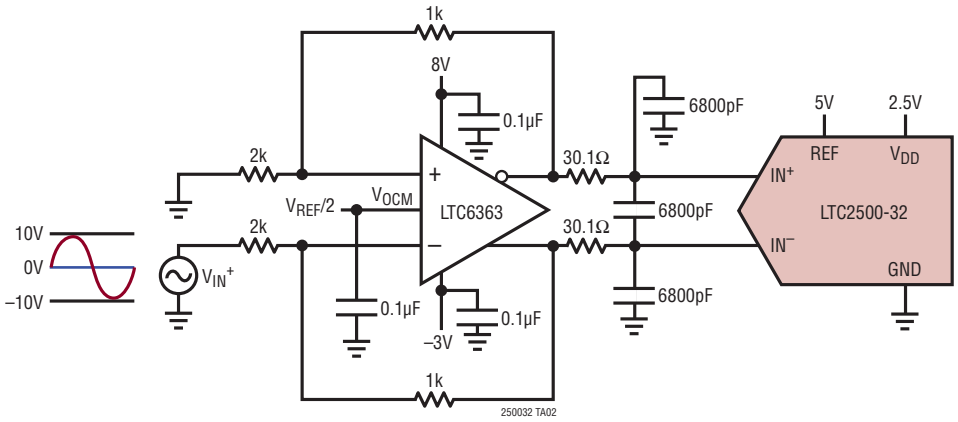
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	6/17	Updated zero scale error drift	4, 5
		Corrected σ value on DC Histogram	8
		Included filter values of 1.024Msps operation	28, 31-33
B	01/18	Corrected preset filter mode SDI logic	36

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TYPICAL APPLICATION

Buffering and Converting a ±10V True Bipolar Input Signal to a Fully Differential ADC Input



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADCs		
LTC2380-24	24-Bit, 1.5/2Msps, ±0.5ppm INL Serial, Low Power ADC	2.5V Supply, ±5V Fully Differential Input, 100dB SNR, MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2368-24	24-Bit, 1Msps, ±0.5ppm INL Serial, Low Power ADC with Unipolar Input Range	2.5V Supply, 0V to 5V Fully Unipolar Input, 98dB SNR, MSOP-16 and 4mm × 3mm DFN-16 Packages
DACs		
LTC2757	18-Bit, Single Parallel I_{OUT} SoftSpan™ DAC	±1LSB INL/DNL, Software-Selectable Ranges, 7mm × 7mm LQFP-48 Package
LTC2641	16-Bit/14-Bit/12-Bit Single Serial V_{OUT} DAC	±1LSB INL /DNL, MSOP-8 Package, 0V to 5V Output
LTC2630	12-Bit/10-Bit/8-Bit Single V_{OUT} DACs	SC70 6-Pin Package, Internal Reference, ±1LSB INL (12 Bits)
References		
LTC6655	Precision Low Drift Low Noise Buffered Reference	5V/4.906V/3.3V/3V/2.5V/2.048V/1.25V, 5ppm/°C, 0.25ppm Peak-to-Peak Noise, MSOP-8 Package
LTC6652	Precision Low Drift Low Noise Buffered Reference	5V/4.906V/3.3V/3V/2.5V/2.048V/1.25V, 5ppm/°C, 2.1ppm Peak-to-Peak Noise, MSOP-8 Package
Amplifiers		
LTC2057	Low Noise Zero-Drift Operational Amplifier	4µV Offset Voltage, 0.015µV/°C Offset Voltage Drift
LTC6363	Low Power, Fully Differential Output Amplifier/Driver	Single 2.8V to 11V Supply, 1.9mA Supply Current, MSOP-8 and 2mm × 3mm DFN-8 Packages
LTC2508-32	32-Bit Oversampling ADC with Configurable Digital Filter	3.5ppm INL, Up to 145dB Dynamic Range, 7mm × 4mm DFN-24 Package
LTC2512-24	24-Bit Oversampling ADC with Configurable Flat Passband Digital Filter	3.5ppm INL, Up to 117dB Dynamic Range, 7mm × 4mm DFN-24 Package
LT6203	Dual 100MHz Rail-to-Rail Input/Output Low Noise Power Amplifier	1.9nV/√Hz, 3mA Maximum Supply Current 100MHz Gain Bandwidth
LTC2378-20/ LTC2377-20/ LTC2376-20	20-Bit, 1Msps/500ksps/250ksps, ±0.5ppm INL Serial, Low Power ADC	2.5V Supply, ±5V Fully Differential Input, 104dB SNR, MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC6362	Low Power, Fully Differential Input/Output Amplifier/Driver	Single 2.8V to 5.25V Supply, 1mA Supply Current, MSOP-8 and 3mm × 3mm DFN-8 Packages

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