Complete Isolated RS485/RS422 µModule Transceiver + Power

FEATURES

- **RS485/RS422 Transceiver: 2500V_{RMS} for 1 Minute**
- **UL-CSA Recognized File #E151738**
- **CSA Component Acceptance Notice 5A**
- **Isolated DC Power: 5V at Up to 200mA**
- **No External Components Required**
- **20Mbps or Low EMI 250kbps Data Rate**
- **High ESD: ±15kV HBM on Transceiver Interface**
- **High Common Mode Transient Immunity: 30kV/µs**
- **Integrated Selectable 120Ω Termination**
- 3.3V (LTM2881-3) or 5.0V (LTM2881-5) Operation
- 1.62V to 5.5V Logic Supply Pin for Flexible Digital Interface
- Maximum Continuous Working Voltage: 560V_{PEAK}
- High Input Impedance Failsafe RS485 Receiver
- Current Limited Drivers and Thermal Shutdown
- Compatible with TIA/EIA-485-A and PROFIBUS
- High Impedance Output During Internal Fault Condition
- Low Current Shutdown Mode (< 10µA)
- General Purpose CMOS Isolated Channel
- 15mm × 11.25mm BGA and LGA Packages

APPLICATIONS

- Isolated RS485/RS422 Interface
- Industrial Networks
- Breaking RS485 Ground Loops
- Isolated PROFIBUS-DP Networks

DESCRIPTION

The LTM®2881 is a complete galvanically isolated full-duplex RS485/RS422 µModule® (micromodule) transceiver. No external components are required. A single supply powers both sides of the interface through an integrated, isolated, low noise, efficient 5V output DC/DC converter.

Coupled inductors and an isolation power transformer provide 2500V_{RMS} of isolation between the line transceiver and the logic interface. This device is ideal for systems where the ground loop is broken allowing for large common mode voltage variation. Uninterrupted communication is guaranteed for common mode transients greater than 30kV/µs.

Maximum data rates are 20Mbps or 250kbps in slew limited mode. Transmit data, DI and receive data, RO, are implemented with event driven low jitter processing. The receiver has a one-eighth unit load supporting up to 256 nodes per bus. A logic supply pin allows easy interfacing with different logic levels from 1.62V to 5.5V, independent of the main supply.

Enhanced ESD protection allows this part to withstand up to ±15kV (human body model) on the transceiver interface pins to isolated supplies and ±10kV through the isolation barrier to logic supplies without latch-up or damage.

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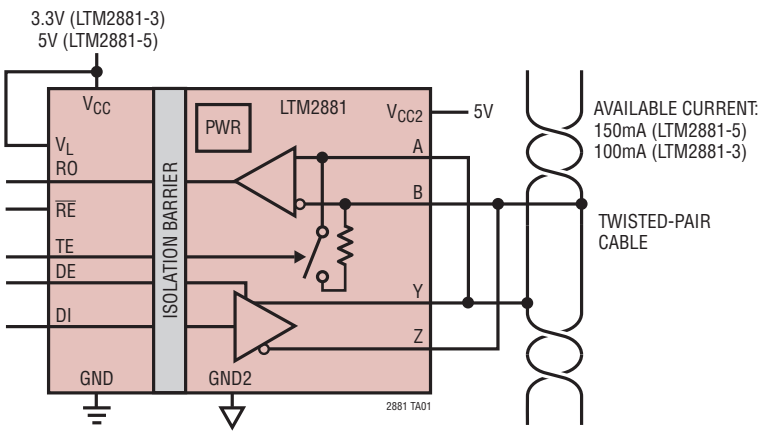
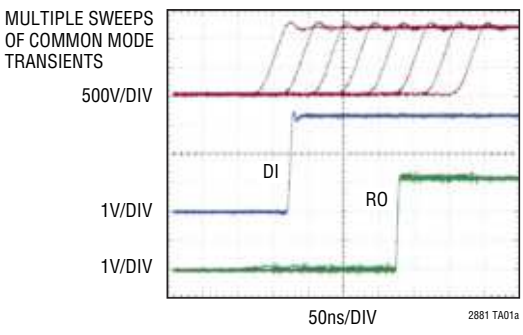
TYPICAL APPLICATION

Isolated Half-Duplex RS485 µModule Transceiver



LTM2881 Operating Through 35kV/µs CM Transients

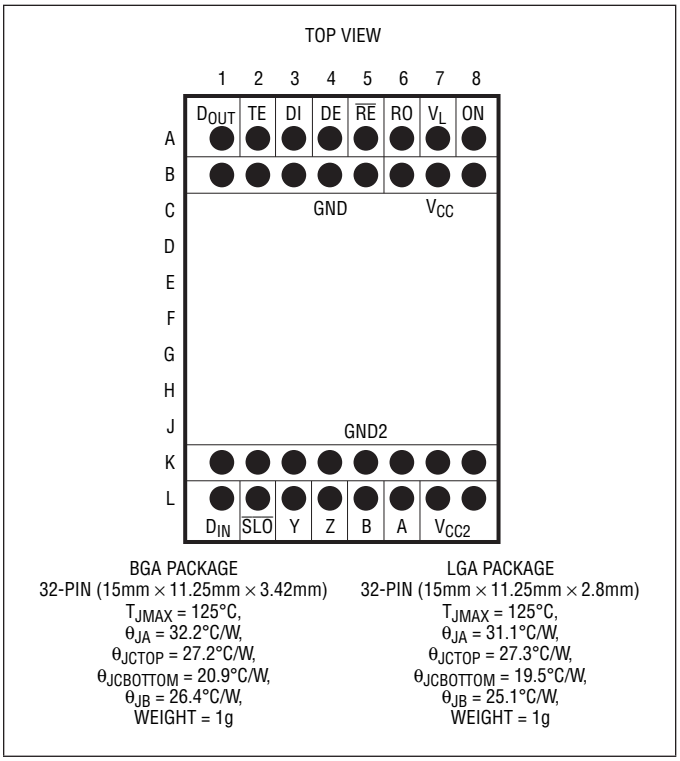


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} to GND ..... –0.3V to 6V
V_{CC2} to GND2..... –0.3V to 6V
V_L to GND ..... –0.3V to 6V
Interface Voltages
(A, B, Y, Z) to GND2..... V_{CC2} –15V to 15V
(A-B) with Terminator Enabled.....±6V
Signal Voltages ON, RO, DI, DE,
$\overline{RE}$, TE, D_{OUT} to GND..... –0.3V to V_L +0.3V
Signal Voltages $\overline{SLO}$,
D_{IN} to GND2.....–0.3V to V_{CC2} +0.3V
Operating Temperature Range
LTM2881C ..... 0°C to 70°C
LTM2881I.....–40°C to 85°C
LTM2881H ..... –40°C to 105°C
LTM2881MP ..... –55°C to 105°C
Maximum Internal Operating Temperature ..... 125°C
Storage Temperature Range .....–55°C to 150°C
Peak Package Body Reflow Temperature ..... 245°C

PIN CONFIGURATION



BGA PACKAGE
32-PIN (15mm × 11.25mm × 3.42mm)
T_{JMAX} = 125°C,
θ_{JA} = 32.2°C/W,
θ_{JCTOP} = 27.2°C/W,
$\theta_{JCBOTTOM}$ = 20.9°C/W,
θ_{JB} = 26.4°C/W,
WEIGHT = 1g

LGA PACKAGE
32-PIN (15mm × 11.25mm × 2.8mm)
T_{JMAX} = 125°C,
θ_{JA} = 31.1°C/W,
θ_{JCTOP} = 27.3°C/W,
$\theta_{JCBOTTOM}$ = 19.5°C/W,
θ_{JB} = 25.1°C/W,
WEIGHT = 1g

ORDER INFORMATION

http://www.linear.com/product/LTM2881#orderinfo

PART NUMBER	INPUT VOLTAGE	PAD OR BALL FINISH	PART MARKING		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE
			DEVICE	FINISH CODE			
LTM2881CY-3#PBF	3V to 3.6V	SAC305 (RoHS)	LTM2881Y-3	e1	BGA	3	0°C to 70°C
LTM2881IY-3#PBF							–40°C to 85°C
LTM2881HY-3#PBF							–40°C to 105°C
LTM2881HY-3		SnPb (63/37)		e0			–40°C to 105°C
LTM2881MPY-3#PBF		SAC305 (RoHS)		e1			–55°C to 105°C
LTM2881MPY-3		SnPb (63/37)		e0			–55°C to 105°C
LTM2881CY-5#PBF	4.5V to 5.5V	SAC305 (RoHS)	LTM2881Y-5	e1			0°C to 70°C
LTM2881IY-5#PBF							–40°C to 85°C
LTM2881HY-5#PBF							–40°C to 105°C
LTM2881HY-5		SnPb (63/37)		e0			–40°C to 105°C
LTM2881MPY-5#PBF		SAC305 (RoHS)		e1			–55°C to 105°C
LTM2881MPY-5		SnPb (63/37)		e0			–55°C to 105°C
LTM2881CV-3#PBF	3V to 3.6V	Au (RoHS)	LTM2881V-3	e4	LGA		0°C to 70°C
LTM2881IV-3#PBF							–40°C to 85°C
LTM2881HV-3#PBF							–40°C to 105°C
LTM2881CV-5#PBF	4.5V to 5.5V		LTM2881V-5				0°C to 70°C
LTM2881IV-5#PBF							–40°C to 85°C
LTM2881HV-5#PBF							–40°C to 105°C

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Terminal Finish Part Marking: www.linear.com/leadfree
- This product is not recommended for second side reflow. For more information, go to: www.linear.com/BGA-assy
- Recommended BGA and LGA PCB Assembly and Manufacturing Procedures: www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings: www.linear.com/packaging
- This product is moisture sensitive. For more information, go to: www.linear.com/umodule/pcbassembly

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. LTM2881-3 V_{CC} = 3.3V, LTM2881-5 V_{CC} = 5.0V, V_L = 3.3V, GND = GND2 = 0V, ON = V_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{CC}	V_{CC} Supply Voltage	LTM2881-3 LTM2881-5	● ●	3.0 4.5	3.3 5.0	3.6 5.5	V V
V_L	V_L Supply Voltage		●	1.62		5.5	V
I_{CCPOFF}	V_{CC} Supply Current in Off Mode	ON = 0V	●		0	10	µA
I_{CCS}	V_{CC} Supply Current in On Mode	LTM2881-3 DE = 0V, $\overline{RE}$ = V_L, No Load LTM2881-5 DE = 0V, $\overline{RE}$ = V_L, No Load	● ●		20 15	30 25	mA mA
V_{CC2}	Regulated V_{CC2} Output Voltage, Loaded	LTM2881-3 DE = 0V, $\overline{RE}$ = V_L, I_{LOAD} = 100mA LTM2881-5 DE = 0V, $\overline{RE}$ = V_L, I_{LOAD} = 150mA LTM2881-3, H/MP-Grade, I_{LOAD} = 90mA	● ● ●	4.75 4.75 4.75	5.0 5.0		V V V
$V_{CC2NOLOAD}$	Regulated V_{CC2} Output Voltage, No Load	DE = 0V, $\overline{RE}$ = V_L, No Load		4.8	5.0	5.35	V
	Efficiency	I_{CC2} = 100mA, LTM2881-5 (Note 2)			62		%
I_{CC2S}	V_{CC2} Short-Circuit Current	DE = 0V, $\overline{RE}$ = V_L, V_{CC2} = 0V			200		mA
Driver							
$\|V_{OD}\|$	Differential Driver Output Voltage	R = ∞ (Figure 1) R = 27Ω (RS485) (Figure 1) R = 50Ω (RS422) (Figure 1)	● ● ●	 2.1 2.1		V_{CC2} V_{CC2} V_{CC2}	V V V
$\Delta\|V_{OD}\|$	Difference in Magnitude of Driver Differential Output Voltage for Complementary Output States	R = 27Ω or R = 50Ω (Figure 1)	●			0.2	V
V_{OC}	Driver Common Mode Output Voltage	R = 27Ω or R = 50Ω (Figure 1)	●			3	V
$\Delta\|V_{OC}\|$	Difference in Magnitude of Driver Common Mode Output Voltage for Complementary Output States	R = 27Ω or R = 50Ω (Figure 1)	●			0.2	V
I_{OZD}	Driver Three-State (High Impedance) Output Current on Y and Z	DE = 0V, (Y or Z) = –7V, +12V DE = 0V, (Y or Z) = –7V, +12V, H/MP-Grade	● ●			±10 ±50	µA µA
I_{OSD}	Maximum Driver Short-Circuit Current	–7V ≤ (Y or Z) ≤ 12V (Figure 2)	●	–250		250	mA
Receiver							
R_{IN}	Receiver Input Resistance	$\overline{RE}$ = 0V or V_L, V_{IN} = –7V, –3V, 3V, 7V, 12V (Figure 3) $\overline{RE}$ = 0V or V_L, V_{IN} = –7V, –3V, 3V, 7V, 12V (Figure 3), H/MP-Grade	● ●	96 48	125 125		kΩ kΩ
R_{TE}	Receiver Termination Resistance Enabled	TE = V_L, V_{AB} = 2V, V_B = –7V, 0V, 10V (Figure 8)	●	108	120	156	Ω
I_{IN}	Receiver Input Current (A, B)	ON = 0V V_{CC2} = 0V or 5V, V_{IN} = 12V (Figure 3) ON = 0V V_{CC2} = 0V or 5V, V_{IN} = 12V (Figure 3), H/MP-Grade	● ●			125 250	µA
		ON = 0V V_{CC2} = 0V or 5V, V_{IN} = –7V (Figure 3) ON = 0V V_{CC2} = 0V or 5V, V_{IN} = –7V (Figure 3), H/MP-Grade	● ●	–100 –145			µA
V_{TH}	Receiver Differential Input Threshold Voltage (A-B)	–7V ≤ B ≤ 12V	●	–0.2		0.2	V
ΔV_{TH}	Receiver Input Failsafe Hysteresis	B = 0V			25		mV
	Receiver Input Failsafe Threshold	B = 0V		–0.2	–0.05	0	V

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logic							
V_{IL}	Logic Input Low Voltage	1.62V ≤ V_L ≤ 5.5V	●			0.4	V
V_{IH}	Logic Input High Voltage	D_{IN}	●	0.67•V_{CC2}			V
		$\overline{SLO}$	●	2			V
		DI, TE, DE, ON, $\overline{RE}$:					
		V_L ≥ 2.35V	●	0.67•V_L			V
		1.62V ≤ V_L < 2.35V	●	0.75•V_L			V
I_{INL}	Logic Input Current		●		0	±1	µA
V_{HYS}	Logic Input Hysteresis	(Note 2)			150		mV
V_{OH}	Output High Voltage	Output High, I_{LOAD} = –4mA (Sourcing), 5.5V ≥ V_L ≥ 3V	●	V_L –0.4			V
		Output High, I_{LOAD} = –1mA (Sourcing), 1.62V ≤ V_L < 3V	●	V_L –0.4			V
V_{OL}	Output Low Voltage	Output Low, I_{LOAD} = 4mA (Sinking), 5.5V ≥ V_L ≥ 3V	●			0.4	V
		Output High, I_{LOAD} = 1mA (Sinking), 1.62V ≤ V_L < 3V	●			0.4	V
I_{OZR}	Three-State (High Impedance) Output Current on RO	$\overline{RE}$ = V_L, 0V ≤ RO ≤ V_L	●			±1	µA
I_{OSR}	Short-Circuit Current	0V ≤ (RO or D_{OUT}) ≤ V_L	●			±85	mA

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. LTM2881-3 V_{CC} = 3.3V, LTM2881-5 V_{CC} = 5.0V, V_L = 3.3V, GND = GND2 = 0V, ON = V_L unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Driver $\overline{SLO}$ = V_{CC2}							
f_{MAX}	Maximum Data Rate	(Note 3)		20			Mbps
t_{PLHD} t_{PHLD}	Driver Input to Output	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)	●		60	85	ns
Δt_{PD}	Driver Input to Output Difference $\lvert t_{PLHD} - t_{PHLD} \rvert$	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)	●		1	8	ns
t_{SKEWD}	Driver Output Y to Output Z	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)	●		1	±8	ns
t_{RD} t_{FD}	Driver Rise or Fall Time	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)	●		4	12.5	ns
t_{ZLD}, t_{ZHD}, t_{LZD}, t_{HZD}	Driver Output Enable or Disable Time	R_L = 500Ω, C_L = 50pF (Figure 5)	●			170	ns
Driver $\overline{SLO}$ = GND2							
f_{MAX}	Maximum Data Rate	(Note 3)		250			kbps
t_{PLHD} t_{PHLD}	Driver Input to Output	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)			1	1.55	µs
Δt_{PD}	Driver Input to Output Difference $\lvert t_{PLHD} - t_{PHLD} \rvert$	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)			50	500	ns
t_{SKEWD}	Driver Output Y to Output Z	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)			±200	±500	ns
t_{RD} t_{FD}	Driver Rise or Fall Time	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)	●		0.9	1.5	µs

SWITCHING CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{ZLD}, t_{ZHD}, t_{LZD}, t_{HZD}	Driver Output Enable or Disable Time	R_L = 500Ω, C_L = 50pF (Figure 5)	●			400	ns
Receiver							
t_{PLHR} t_{PHLR}	Receiver Input to Output	C_L = 15pF, V_{CM} = 2.5V, $\|V_{AB}\|$ = 1.4V, t_R and t_F < 4ns, (Figure 6)	●		100	140	ns
t_{SKEWR}	Differential Receiver Skew $\|t_{PLHR} - t_{PHLR}\|$	C_L = 15pF (Figure 6)	●		1	8	ns
t_{RR} t_{FR}	Receiver Output Rise or Fall Time	C_L = 15pF (Figure 6)	●		3	12.5	ns
t_{ZLR}, t_{ZHR}, t_{LZR}, t_{HZR}	Receiver Output Enable Time	R_L =1kΩ, C_L = 15pF (Figure 7)	●			50	ns
t_{RTEN}, t_{RTZ}	Termination Enable or Disable Time	$\overline{RE}$ = 0V, DE = 0V, V_{AB} = 2V, V_B = 0V (Figure 8)	●			100	µs
Generic Logic Input							
t_{PLHL1} t_{PHLL1}	D_{IN} to D_{OUT} Input to Output	C_L = 15pF, t_R and t_F < 4ns	●		60	100	ns
Power Supply Generator							
	V_{CC2}–GND2 Supply Start-Up Time (0V to 4.5V)	ON ⊥↑ V_L, No Load	●		325	800	µs

ISOLATION CHARACTERISTICS

T_A = 25°C, LTM2881-3 V_{CC} = 3.3V, LTM2881-5 V_{CC} = 5.0V, V_L = 3.3V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{ISO}	Rated Dielectric Insulation Voltage	1 Minute (Derived from 1 Second Test)	2500			V_{RMS}
		1 Second (Notes 5, 6)	±4400			V_{DC}
	Common Mode Transient Immunity	LTM2881-3 V_{CC} = 3.3V, LTM2881-5 V_{CC} = 5V, V_L = ON = 3.3V, V_{CM} = 1kV, Δt = 33ns (Note 2)	±30			kV/µs
V_{IORM}	Maximum Working Insulation Voltage	(Notes 2, 5)	560 400			V_{PEAK} V_{RMS}
	Partial Discharge	V_{PR} = 1050 V_{PEAK} (Note 2)			5	pC
CTI	Comparative Tracking Index	IEC 60112 (Note 2)	600			V_{RMS}
	Depth of Erosion	IEC 60112 (Note 2)		0.017		mm
DTI	Distance Through Insulation	(Note 2)		0.06		mm
	Input to Output Resistance	(Notes 2, 5)	10^9			Ω
	Input to Output Capacitance	(Notes 2, 5)		6		pF
	Creepage Distance	(Notes 2, 5)		9.48		mm

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Guaranteed by design and not subject to production test.

Note 3: Maximum Data rate is guaranteed by other measured parameters and is not tested directly.

Note 4: This µModule transceiver includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above specified maximum operating junction temperature may result in device degradation or failure.

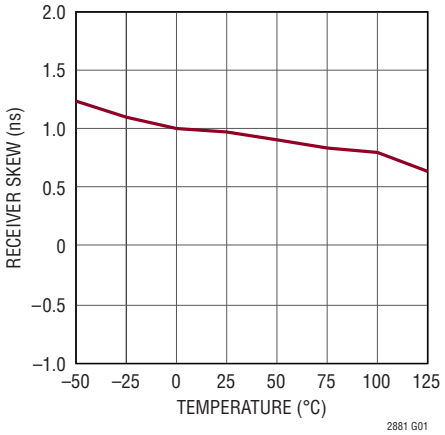
Note 5: Device considered a 2-terminal device. Pin group A1 through B8 shorted together and pin group K1 through L8 shorted together.

Note 6: The rated dielectric insulation voltage should not be interpreted as a continuous voltage rating.

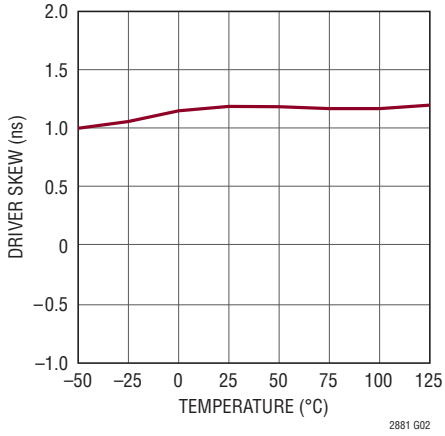
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, LTM2881-3 V_{CC} = 3.3V, LTM2881-5 V_{CC} = 5.0V, V_L = 3.3V unless otherwise noted.

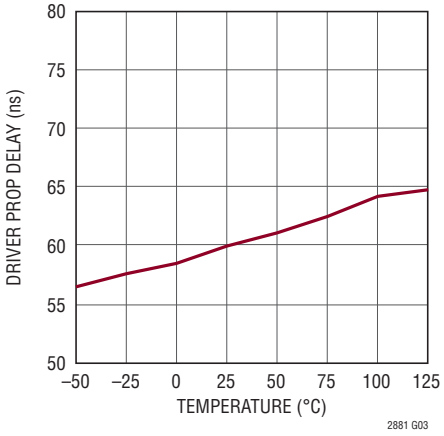
Receiver Skew vs Temperature



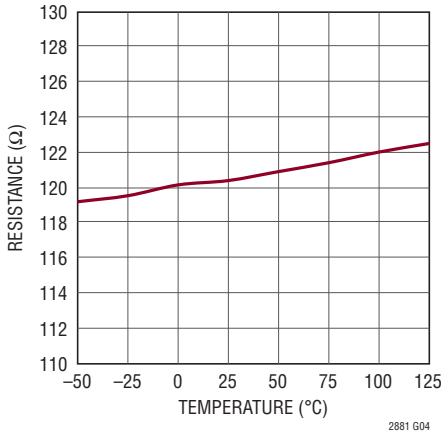
Driver Skew vs Temperature



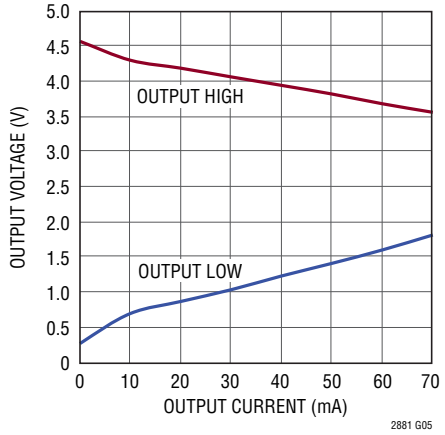
Driver Propagation Delay vs Temperature



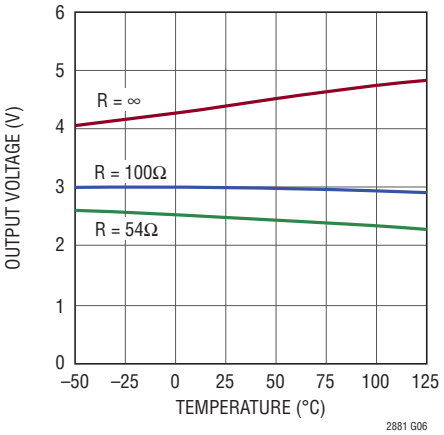
R_{TERM} vs Temperature



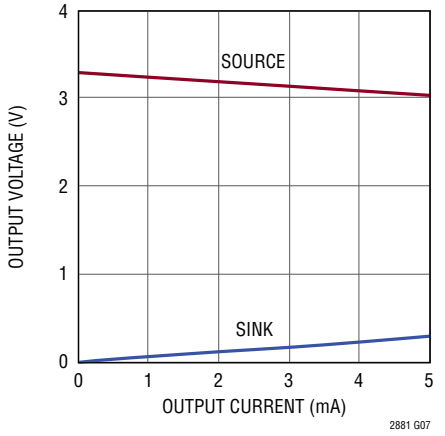
Driver Output Low/High Voltage vs Output Current



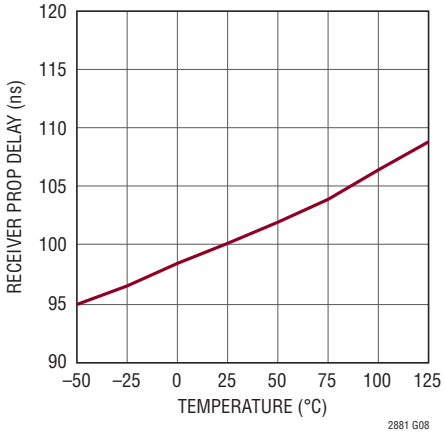
Driver Differential Output Voltage vs Temperature



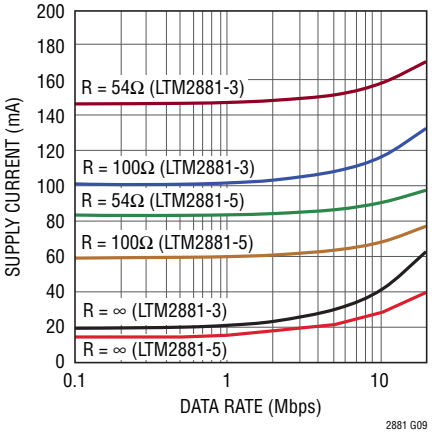
Receiver Output Voltage vs Output Current (Source and Sink)



Receiver Propagation Delay vs Temperature



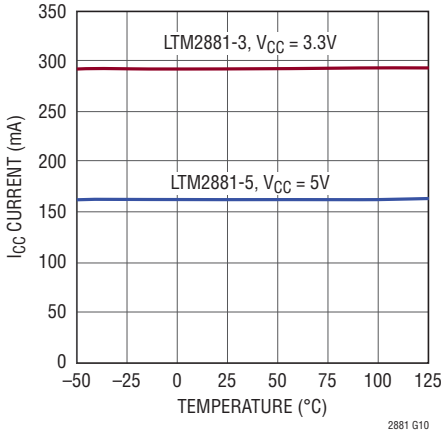
Supply Current vs Data Rate



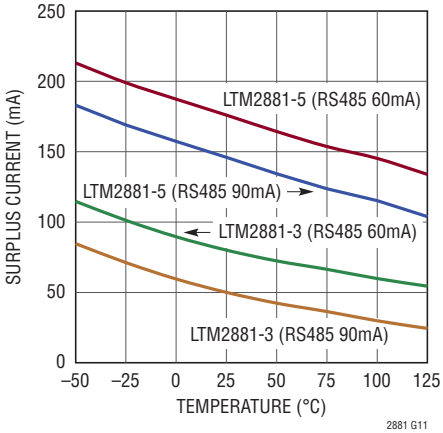
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, LTM2881-3 V_{CC} = 3.3V, LTM2881-5 V_{CC} = 5.0V, V_L = 3.3V unless otherwise noted.

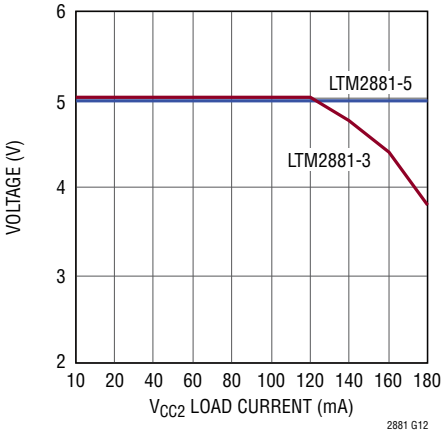
V_{CC} Supply Current vs Temperature at I_{LOAD} = 100mA on V_{CC2}



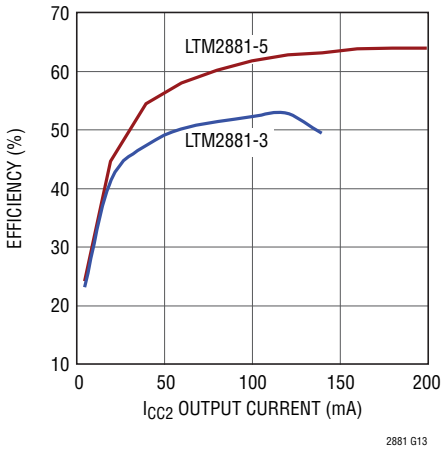
V_{CC2} Surplus Current vs Temperature



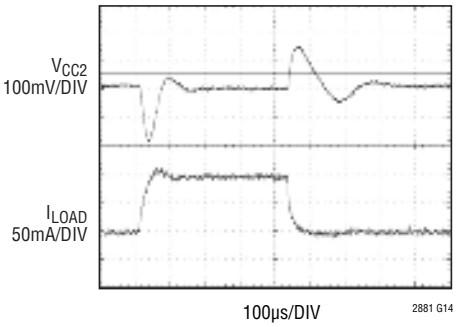
V_{CC2} vs Load Current



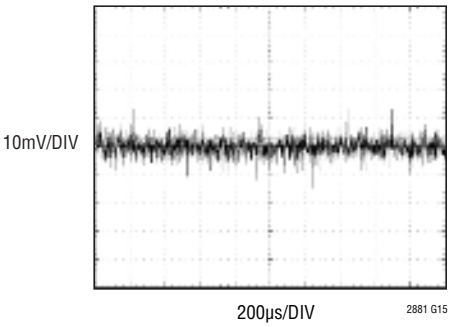
V_{CC2} Power Efficiency



V_{CC2} Load Step (100mA)



V_{CC2} Noise



PIN FUNCTIONS

LOGIC SIDE (V_{CC}, V_L, GND)

D_{OUT} (Pin A1): General Purpose Logic Output. Logic output connected through isolation path to D_{IN}. Under the condition of an isolation communication failure D_{OUT} is in a high impedance state.

TE (Pin A2): Terminator Enable. A logic high enables a termination resistor (typically 120Ω) between pins A and B.

DI (Pin A3): Driver Input. If the driver outputs are enabled (DE high), then a low on DI forces the driver noninverting output (Y) low and the inverting output (Z) high. A high on DI, with the driver outputs enabled, forces the driver noninverting output (Y) high and inverting output (Z) low.

DE (Pin A4): Driver Enable. A logic low disables the driver leaving the outputs Y and Z in a high impedance state. A logic high enables the driver.

$\overline{RE}$ (Pin A5): Receiver Enable. A logic low enables the receiver output. A logic high disables RO to a high impedance state.

RO (Pin A6): Receiver Output. If the receiver output is enabled ($\overline{RE}$ low) and if A – B is > 200mV, RO is a logic high, if A – B is < –200mV RO is a logic low. If the receiver inputs are open, shorted, or terminated without a valid signal, RO will be high. Under the condition of an isolation communication failure RO is in a high impedance state.

V_L (Pin A7): Logic Supply. Interface supply voltage for pins RO, $\overline{RE}$, TE, DI, DE, D_{OUT}, and ON. Recommended operating voltage is 1.62V to 5.5V. Internally bypassed to GND with 2.2µF.

ON (Pin A8): Enable. Enables power and data communication through the isolation barrier. If ON is high the part is enabled and power and communications are functional to the isolated side. If ON is low the logic side is held in reset and the isolated side is unpowered.

GND (Pins B1-B5): Circuit Ground.

V_{CC} (Pins B6-B8): Supply Voltage. Recommended operating voltage is 3V to 3.6V for LTM2881-3 and 4.5V to 5.5V for LTM2881-5. Internally bypassed to GND with 2.2µF.

ISOLATED SIDE (V_{CC2}, GND2)

D_{IN} (Pin L1): General Purpose Isolated Logic Input. Logic input on the isolated side relative to V_{CC2} and GND2. A logic high on D_{IN} will generate a logic high on D_{OUT}. A logic low on D_{IN} will generate a logic low on D_{OUT}.

$\overline{SLO}$ (Pin L2): Driver Slew Rate Control. A low input, relative to GND2, will force the driver into a reduced slew rate mode for reduced EMI. A high input, relative to GND2, puts the driver into full speed mode to support maximum data rates.

Y (Pin L3): Non Inverting Driver Output. High impedance when the driver is disabled.

Z (Pin L4): Inverting Driver Output. High impedance when the driver is disabled.

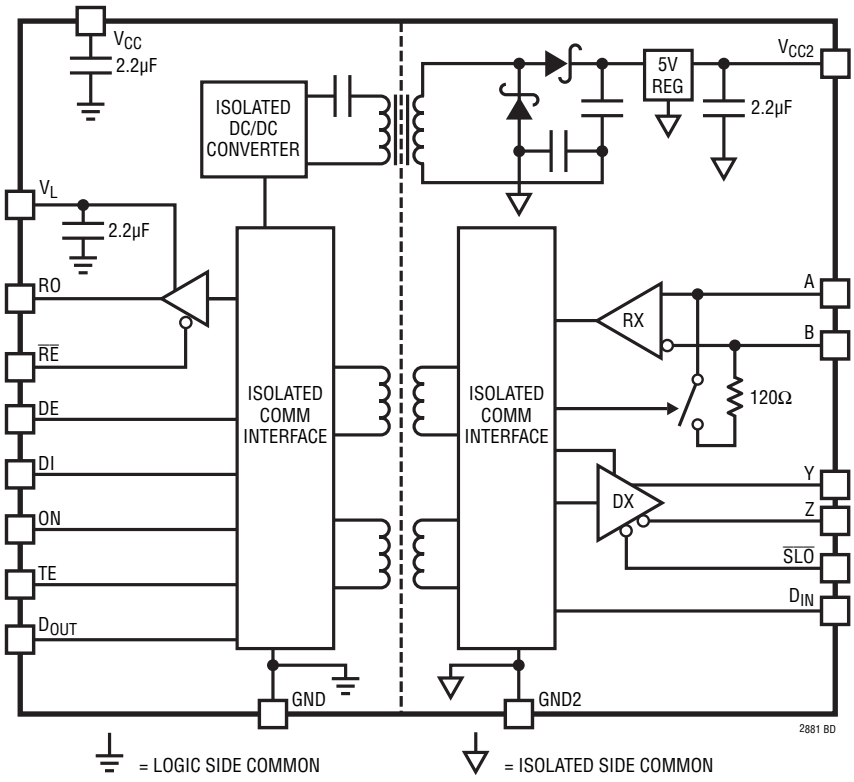
B (Pin L5): Inverting Receiver Input. Impedance is > 96kΩ in receive mode with TE low or unpowered.

A (Pin L6): Non Inverting Receiver Input. Impedance is > 96kΩ in receive mode with TE low or unpowered.

V_{CC2} (Pins L7-L8): Isolated Supply Voltage. Internally generated from V_{CC} by an isolated DC/DC converter and regulated to 5V. Internally bypassed to GND2 with 2.2µF.

GND2 (Pins K1-K8): Isolated Side Circuit Ground. The pads should be connected to the isolated ground and/or cable shield.

BLOCK DIAGRAM



TEST CIRCUITS

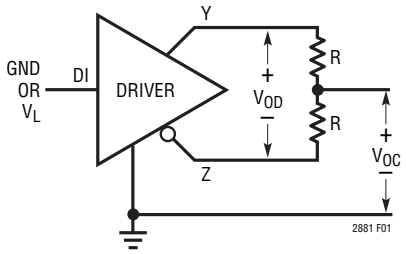


Figure 1. Driver DC Characteristics

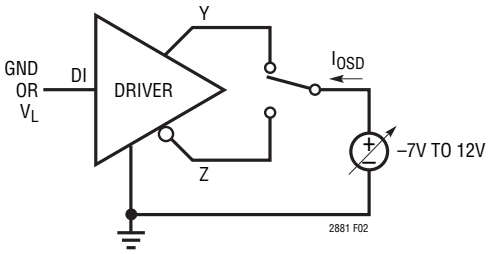


Figure 2. Driver Output Short-Circuit Current

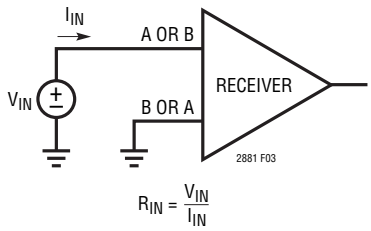


Figure 3. Receiver Input Current and Input Resistance

TEST CIRCUITS

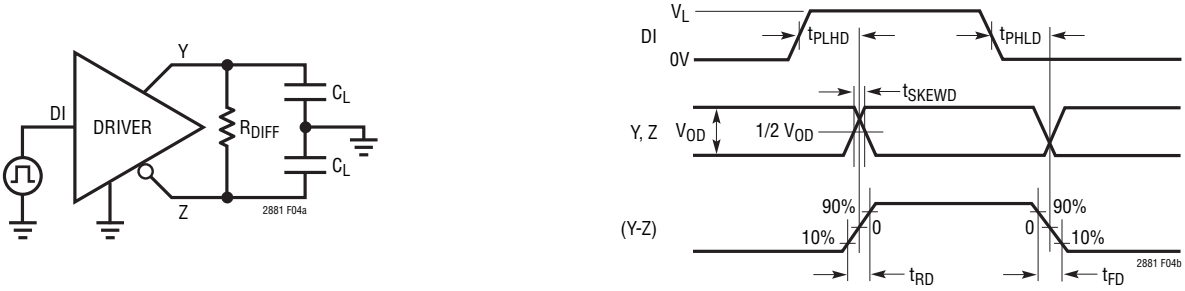


Figure 4. Driver Timing Measurement

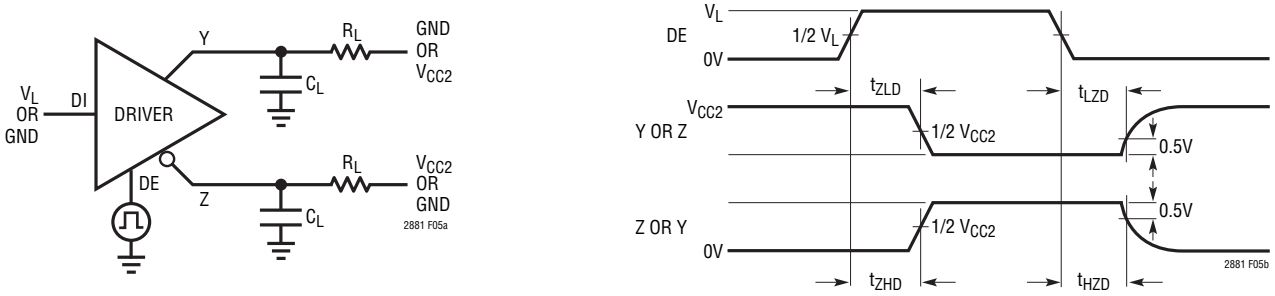


Figure 5. Driver Enable and Disable Timing Measurements

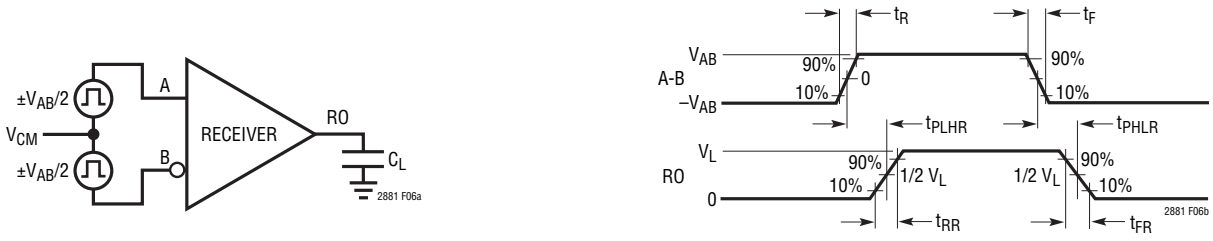


Figure 6. Receiver Propagation Delay Measurements

TEST CIRCUITS

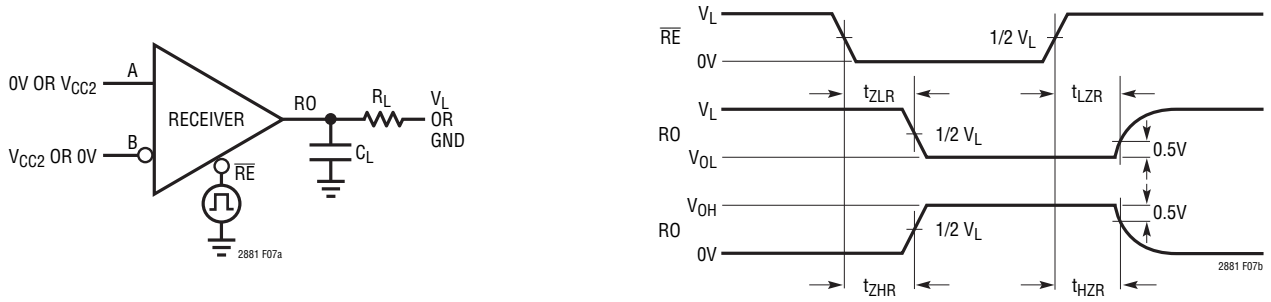


Figure 7. Receiver Enable/Disable Time Measurements

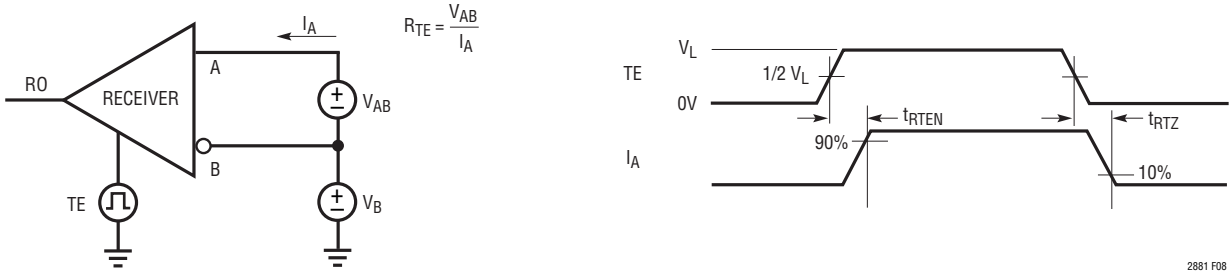


Figure 8. Termination Resistance and Timing Measurements

FUNCTIONAL TABLE

LOGIC INPUTS				MODE	A, B	Y, Z	RO	DC/DC CONVERTER	TERMINATOR
ON	$\overline{RE}$	TE	DE						
1	0	0	0	Receive	R_{IN}	Hi-Z	Enabled	On	Off
1	0	0	1	Transceiver	R_{IN}	Driven	Enabled	On	Off
1	1	0	1	Transmit	R_{IN}	Driven	Hi-Z	On	Off
1	0	1	0	Receive + Term On	R_{TE}	Hi-Z	Enabled	On	On
0	X	X	X	Off	R_{IN}	Hi-Z	Hi-Z	Off	Off

APPLICATIONS INFORMATION

Overview

The LTM2881 µModule transceiver provides a galvanically-isolated robust RS485/RS422 interface, powered by an integrated, regulated DC/DC converter, complete with decoupling capacitors. A switchable termination resistor is integrated at the receiver input to provide proper termination to the RS485 bus. The LTM2881 is ideal for use in networks where grounds can take on different voltages. Isolation in the LTM2881 blocks high voltage differences and eliminates ground loops and is extremely tolerant of common mode transients between ground potentials. Error free operation is maintained through common mode events greater than 30kV/µs providing excellent noise isolation.

µModule Technology

The LTM2881 utilizes isolator µModule technology to translate signals and power across an isolation barrier. Signals on either side of the barrier are encoded into pulses and translated across the isolation boundary using coreless transformers formed in the µModule substrate. This system, complete with data refresh, error checking, safe shutdown on fail, and extremely high common mode immunity, provides a robust solution for bidirectional signal isolation. The µModule technology provides the means to combine the isolated signaling with our RS485 transceiver and powerful isolated DC/DC converter in one small package.

DC/DC Converter

The LTM2881 contains a fully integrated isolated DC/DC converter, including the transformer, so that no external components are necessary. The logic side contains a full-bridge driver, running about 2MHz, and is AC-coupled to a single transformer primary. A series DC blocking capacitor prevents transformer saturation due to driver duty cycle imbalance. The transformer scales the primary voltage, and is rectified by a full-wave voltage doubler. This topology eliminates transformer saturation caused by secondary imbalances.

The DC/DC converter is connected to a low dropout regulator (LDO) to provide a regulated low noise 5V output.

The internal power solution is sufficient to support the transceiver interface at its maximum specified load and data rate, and external pins are supplied for extra decoupling (optional) and heat dissipation. The logic supplies, V_{CC} and V_L have a 2.2µF decoupling capacitance to GND and the isolated supply V_{CC2} has a 2.2µF decoupling capacitance to GND2 within the µModule package.

V_{CC2} Output

The on-board DC/DC converter provides isolated 5V power to output V_{CC2}. V_{CC2} is capable of suppling up to 1W of power at 5V in the LTM2881-5 option and up to 600mW of power in the LTM2881-3 option. This surplus current is available to external applications. The amount of surplus current is dependent upon the implementation and current delivered to the RS485 driver and line load. An example of available surplus current is shown in the Typical Performance Characteristics graph, V_{CC2} Surplus Current vs Temperature. Figure 19 demonstrates a method of using the V_{CC2} output directly and with a switched power path that is controlled with the isolated RS485 data channel.

Driver

The driver provides full RS485 and RS422 compatibility. When enabled, if DI is high, Y–Z is positive. When the driver is disabled, both outputs are high impedance with less than 10µA of leakage current over the entire common mode range of –7V to 12V, with respect to GND2.

Driver Overvoltage and Overcurrent Protection

The driver outputs are protected from short circuits to any voltage within the absolute maximum range of (V_{CC2} –15V) to (GND2 +15V) levels. The maximum V_{CC2} current in this condition is 250mA. If the pin voltage exceeds about ±10V, current limit folds back to about half of the peak value to reduce overall power dissipation and avoid damaging the part.

The device also features thermal shutdown protection that disables the driver and receiver output in case of excessive power dissipation (See Note 4 in the Electrical Characteristics section).

$\overline{SLO}$ Mode

The LTM2881 features a logic-selectable reduced slew rate mode ($\overline{SLO}$ mode) that softens the driver output edges to

APPLICATIONS INFORMATION

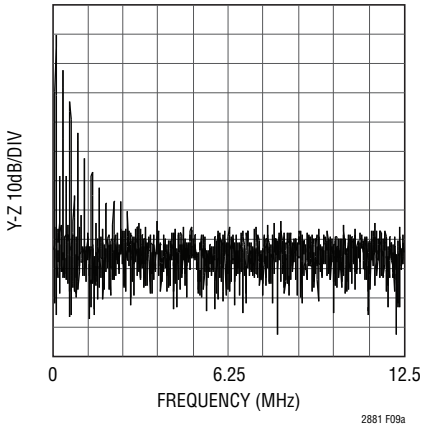


Figure 9a. Frequency Spectrum $\overline{SLO}$ Mode 125kHz Input

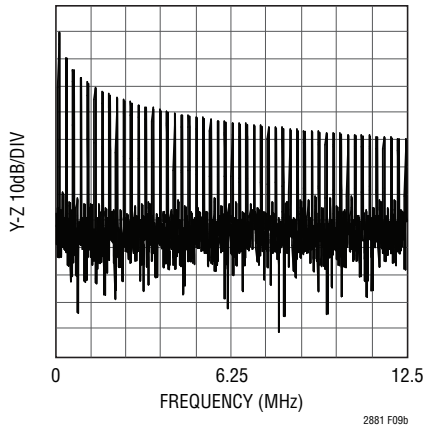


Figure 9b. Normal Mode Frequency Spectrum 125kHz Input

reduce EMI emissions from equipment and data cables. The reduced slew rate mode is entered by taking the $\overline{SLO}$ pin low to GND2, where the data rate is limited to about 250kbps. Slew limiting also mitigates the adverse effects of imperfect transmission line termination caused by stubs or mismatched cables.

Figures 9a and 9b show the frequency spectrums of the LTM2881 driver outputs in normal and $\overline{SLO}$ mode operating at 250kbps. $\overline{SLO}$ mode significantly reduces the high frequency harmonics.

Receiver and Failsafe

With the receiver enabled, when the absolute value of the differential voltage between the A and B pins is greater than 200mV, the state of RO will reflect the polarity of (A-B). During data communication the receiver detects the state of the input with symmetric thresholds around 0V. The symmetric thresholds preserve duty cycle for attenuated signals with slow transition rates on high capacitive busses, or long cable lengths. The receiver incorporates a failsafe feature that guarantees the receiver output to be a logic-high during an idle bus, when the inputs are shorted, left open or terminated, but not driven. The failsafe feature eliminates the need for system level integration of network pre-biasing by guaranteeing a logic-high on RO under the conditions of an idle bus. Further network biasing constructed to condition transient noise during an idle state is unnecessary due to the common mode transient rejection of the LTM2881. The failsafe detector monitors A and B in parallel with the receiver and detects the state of the bus when A-B is above the input failsafe threshold for longer than about 3µs with a hysteresis of 25mV. This failsafe feature is guaranteed to work for inputs spanning the entire common mode range of –7V to 12V.

The receiver output is internally driven high (to V_L) or low (to GND) with no external pull-up needed. When the receiver is disabled the RO pin becomes Hi-Z with leakage of less than ±1µA for voltages within the supply range.

Receiver Input Resistance

The receiver input resistance from A or B to GND2 is greater than 96k permitting up to a total of 256 receivers per system without exceeding the RS485 receiver loading specification. High temperature H-/MP-Grade operation reduces the input resistance to 48k permitting 128 receivers on the bus. The input resistance of the receiver is unaffected by enabling/disabling the receiver or by powering/unpowering the part. The equivalent input resistance looking into A and B is shown in Figure 10.

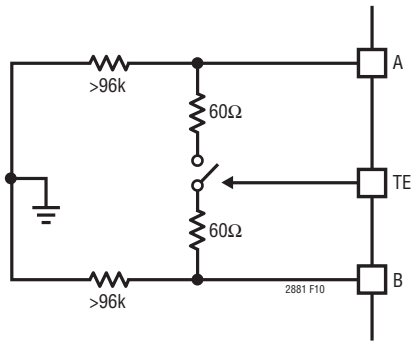


Figure 10. Equivalent Input Resistance into A and B

APPLICATIONS INFORMATION

Switchable Termination

Proper cable termination is very important for signal fidelity. If the cable is not terminated with its characteristic impedance, reflections will distort the signal waveforms.

The integrated switchable termination resistor provides logic control of the line termination for optimal performance when configuring transceiver networks.

When the TE pin is high, the termination resistor is enabled and the differential resistance from A to B is 120Ω. Figure 11 shows the I/V characteristics between pins A and B with the termination resistor enabled and disabled. The resistance is maintained over the entire RS485 common mode range of –7V to 12V as shown in Figure 12. The integrated termination resistor has a high frequency response which does not limit performance at the maximum specified data rate. Figure 13 shows the magnitude and phase of the termination impedance versus frequency. The termination resistor cannot be enabled by TE if the device is unpowered, ON is low or the LTM2881 is in thermal shutdown.

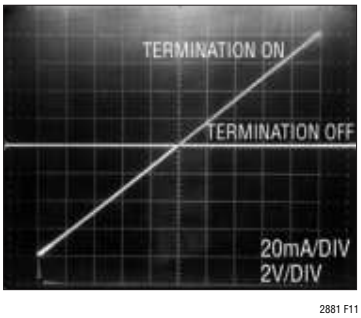


Figure 11. Curve Trace Between A and B with Termination Enabled and Disabled

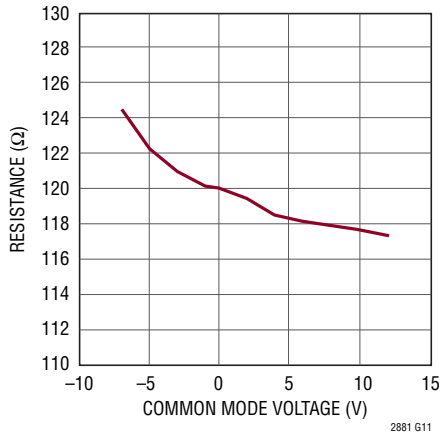


Figure 12. Termination Resistance vs Common Mode Voltage

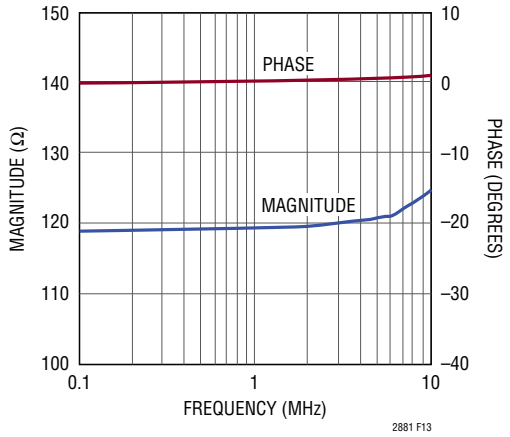


Figure 13. Termination Magnitude and Phase vs Frequency

Supply Current

The static supply current is dominated by power delivered to the termination resistance. Power supply current increases with data rate due to capacitive loading. Figure 14 shows supply current versus data rate for three different loads for the circuit configuration of Figure 4. Supply current increases with additional external applications drawing current from V_{CC2}.

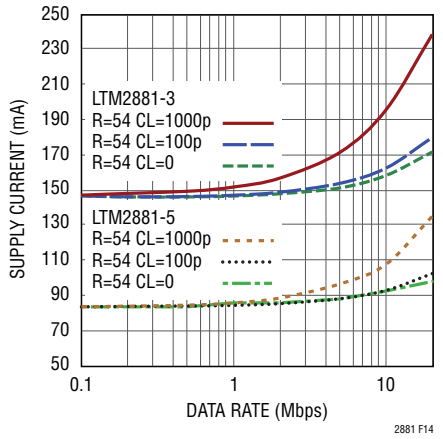


Figure 14. Supply Current vs Data Rate

APPLICATIONS INFORMATION

PROFIBUS Applications

The LTM2881 can be used in PROFIBUS-DP networks where isolation is required. The standard PROFIBUS termination differs from RS485 termination and is shown in Figure 15. If used in this way, the internal termination should remain disabled (TE low). The 390Ω resistors in Figure 15 pre-bias the bus so that when the line is not driven, the receiver delivers a high output. Since the LTM2881 uses a fail-safe receiver, the pre-biasing resistors are not necessary and standard RS485 termination can be used with control from TE.

V_{CC2}, provides an isolated source for the external termination resistor as shown in the Figure 15. When using the LTM2881 in PROFIBUS applications, it is recommended that no additional loads are connected to V_{CC2} in order to maintain the specified driver output swing.

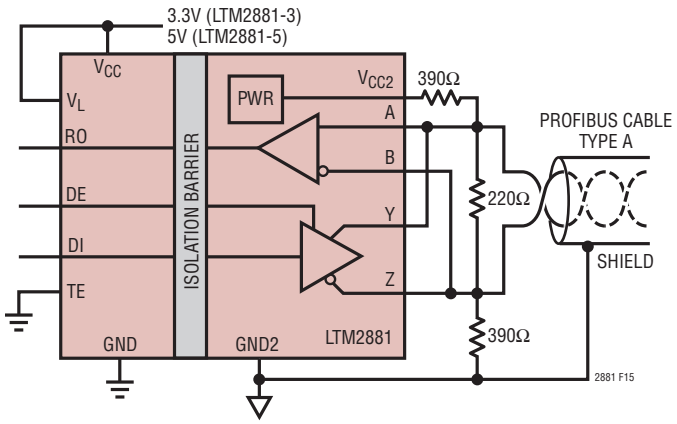


Figure 15. PROFIBUS-DP Connections with Termination

PCB Layout Considerations

The high integration of the LTM2881 makes PCB layout very simple. However, to optimize its electrical isolation characteristics, EMI, and thermal performance, some layout considerations are necessary.

- Under heavily loaded conditions V_{CC} and GND current can exceed 300mA. Sufficient copper must be used on the PCB to insure resistive losses do not cause the supply voltage to drop below the minimum allowed level. Similarly, the V_{CC2} and GND2 conductors must be sized to support any external load current. These heavy copper traces will also help to reduce thermal stress and improve the thermal conductivity.
- Input and Output decoupling is not required, since these components are integrated within the package. An additional bulk capacitor with a value of 6.8µF to 22µF is recommended. The high ESR of this capacitor reduces board resonances and minimizes voltage spikes caused by hot plugging of the supply voltage. For EMI sensitive applications, an additional low ESL ceramic capacitor of 1µF to 4.7µF, placed as close to the power and ground terminals as possible, is recommended. Alternatively, a number of smaller value parallel capacitors may be used to reduce ESL and achieve the same net capacitance.
- Do not place copper on the PCB between the inner columns of pads. This area must remain open to withstand the rated isolation voltage.
- The use of solid ground planes for GND and GND2 is recommended for non-EMI critical applications to optimize signal fidelity, thermal performance, and to minimize RF emissions due to uncoupled PCB trace conduction. The drawback of using ground planes, where EMI is of concern, is the creation of a dipole antenna structure which can radiate differential voltages formed between GND and GND2. If ground planes are used it is recommended to minimize their area, and use contiguous planes as any openings or splits can exacerbate RF emissions.
- For large ground planes a small capacitance (≤ 330pF) from GND to GND2, either discrete or embedded within the substrate, provides a low impedance current return path for the module parasitic capacitance, minimizing any high frequency differential voltages and substantially reducing radiated emissions. Discrete capacitance will not be as effective due to parasitic ESL. In addition, voltage rating, leakage, and clearance must be considered for component selection. Embedding the capacitance within the PCB substrate provides a near ideal capacitor and eliminates component selection issues; however, the PCB must be 4 layers. Care must be exercised in applying either technique to insure the voltage rating of the barrier is not compromised.

APPLICATIONS INFORMATION

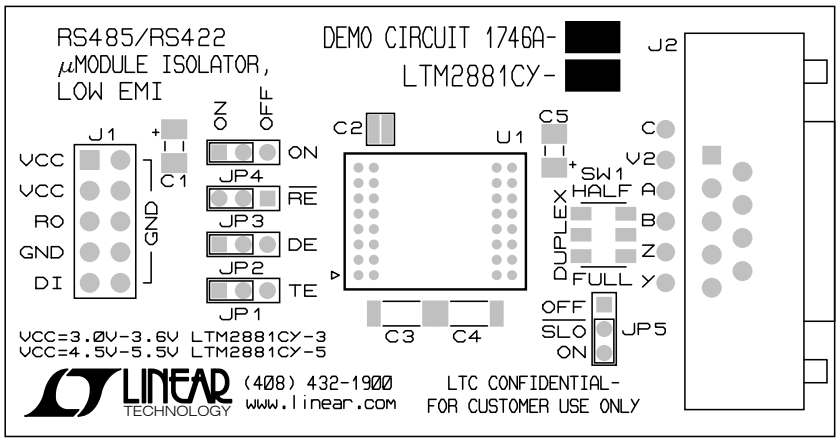


Figure 16a. Low EMI Demo Board Layout

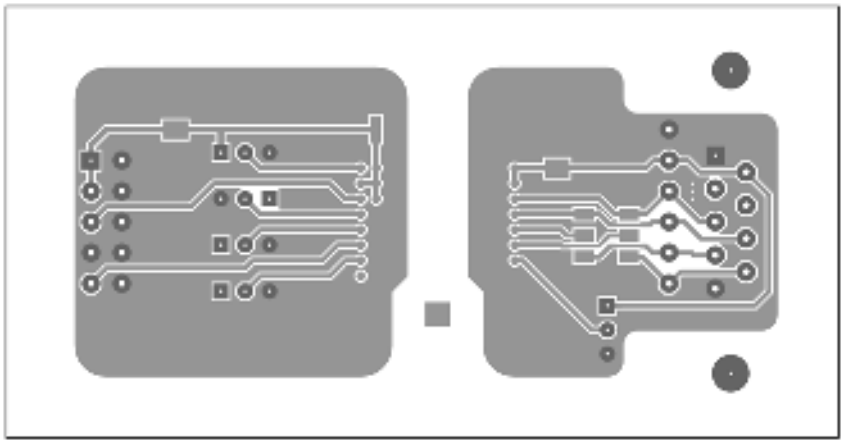


Figure 16b. Low EMI Demo Board Layout (DC1746A), Top Layer

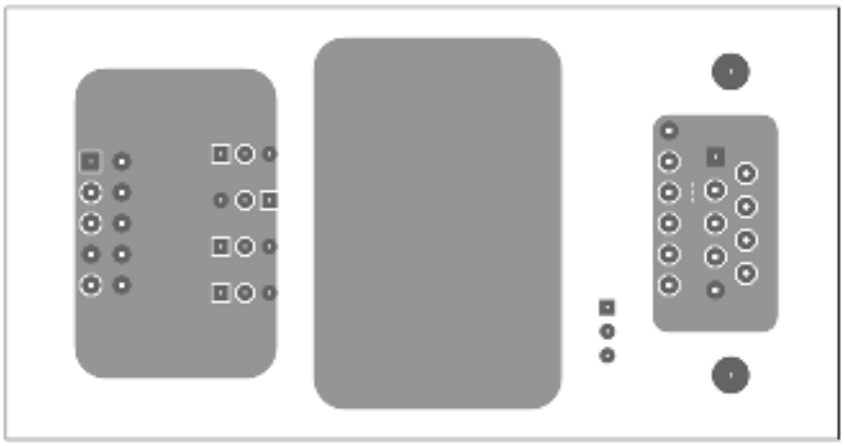


Figure 16c. Low EMI Demo Board Layout (DC1746A), Inner Layer 1

APPLICATIONS INFORMATION



Figure 16d. Low EMI Demo Board Layout (DC1746A), Inner Layer 2



Figure 16e. Low EMI Demo Board Layout (DC1746A), Bottom Layer

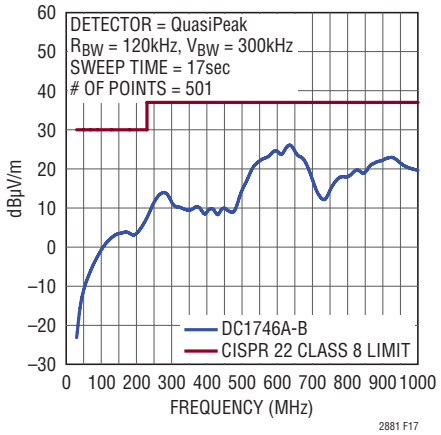


Figure 17. Low EMI Demo Board Emissions

APPLICATIONS INFORMATION

The PCB layout in Figures 16a to 16e show the low EMI demo board for the LTM2881. The demo board uses a combination of EMI mitigation techniques, including both embedded PCB bridge capacitance and discrete GND to GND2 capacitors. Two safety rated type Y2 capacitors are used in series, manufactured by Murata, part number GA342QR7GF471KW01L. The embedded capacitor effectively suppresses emissions above 400MHz, whereas the discrete capacitors are more effective below 400MHz.

EMI performance is shown in Figure 17, measured using a Gigahertz Transverse Electromagnetic (GTEM) cell and method detailed in IEC 61000-4-20, "Testing and Measurement Techniques – Emission and Immunity Testing in Transverse Electromagnetic Waveguides."

Cable Length versus Data Rate

For a given data rate, the maximum transmission distance is bounded by the cable properties. A typical curve of cable length versus data rate compliant with the RS485 standard is shown in Figure 18. Three regions of this curve reflect different performance limiting factors in data transmission. In the flat region of the curve, maximum distance is determined by resistive loss in the cable. The downward sloping region represents limits in distance and rate due to the AC losses in the cable. The solid vertical line represents the specified maximum data rate in the RS485 standard. The dashed line at 250kbps shows the maximum data rate when $\overline{SLO}$ is low. The dashed line at 20Mbps shows the maximum data rate when $\overline{SLO}$ is high.

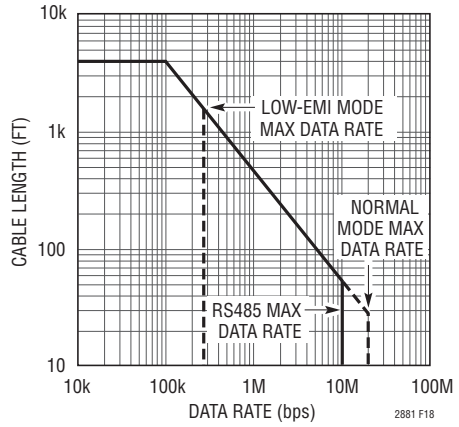


Figure 18. Cable Length vs Data Rate

RF, Magnetic Field Immunity

The LTM2881 has been independently evaluated and has successfully passed the RF and magnetic field immunity testing requirements per European Standard EN 55024, in accordance with the following test standards:

EN 61000-4-3 Radiated, Radio-Frequency, Electromagnetic Field Immunity

EN 61000-4-8 Power Frequency Magnetic Field Immunity

EN 61000-4-9 Pulsed Magnetic Field Immunity

Tests were performed using an unshielded test card designed per the data sheet PCB layout recommendations. Specific limits per test are detailed in Table 1.

Table 1

TEST	FREQUENCY	FIELD STRENGTH
EN 61000-4-3, Annex D	80MHz to 1GHz	10V/m
	1.4MHz to 2GHz	3V/m
	2GHz to 2.7GHz	1V/m
EN 61000-4-8, Level 4	50Hz and 60Hz	30A/m
EN 61000-4-8, Level 5	60Hz	100A/m*
EN 61000-4-9, Level 5	Pulse	1000A/m

*Non IEC Method

TYPICAL APPLICATIONS

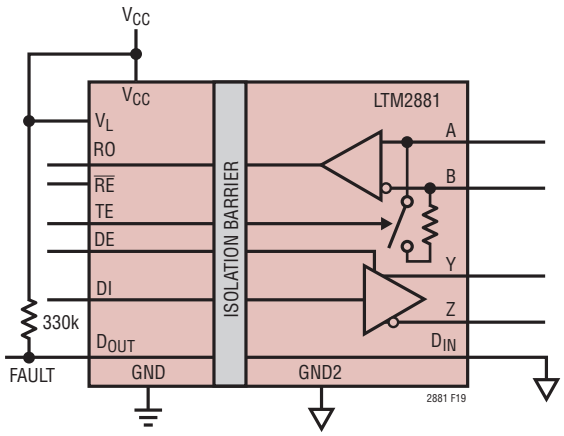


Figure 19. Isolated System Fault Detection

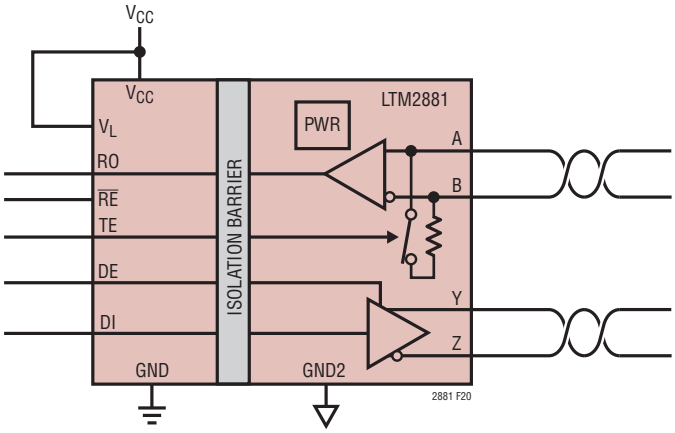


Figure 20. Full-Duplex RS485 Connection

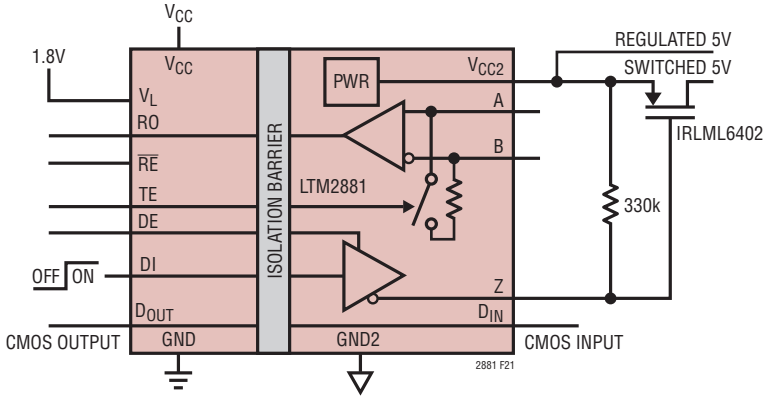


Figure 21. Switched 5V Power with Isolated CMOS Logic Connection with Low Voltage Interface

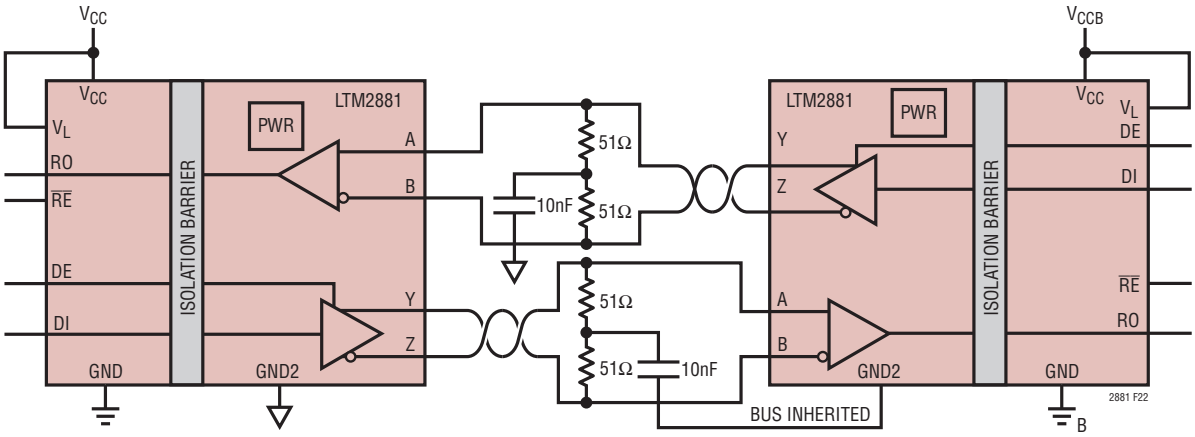
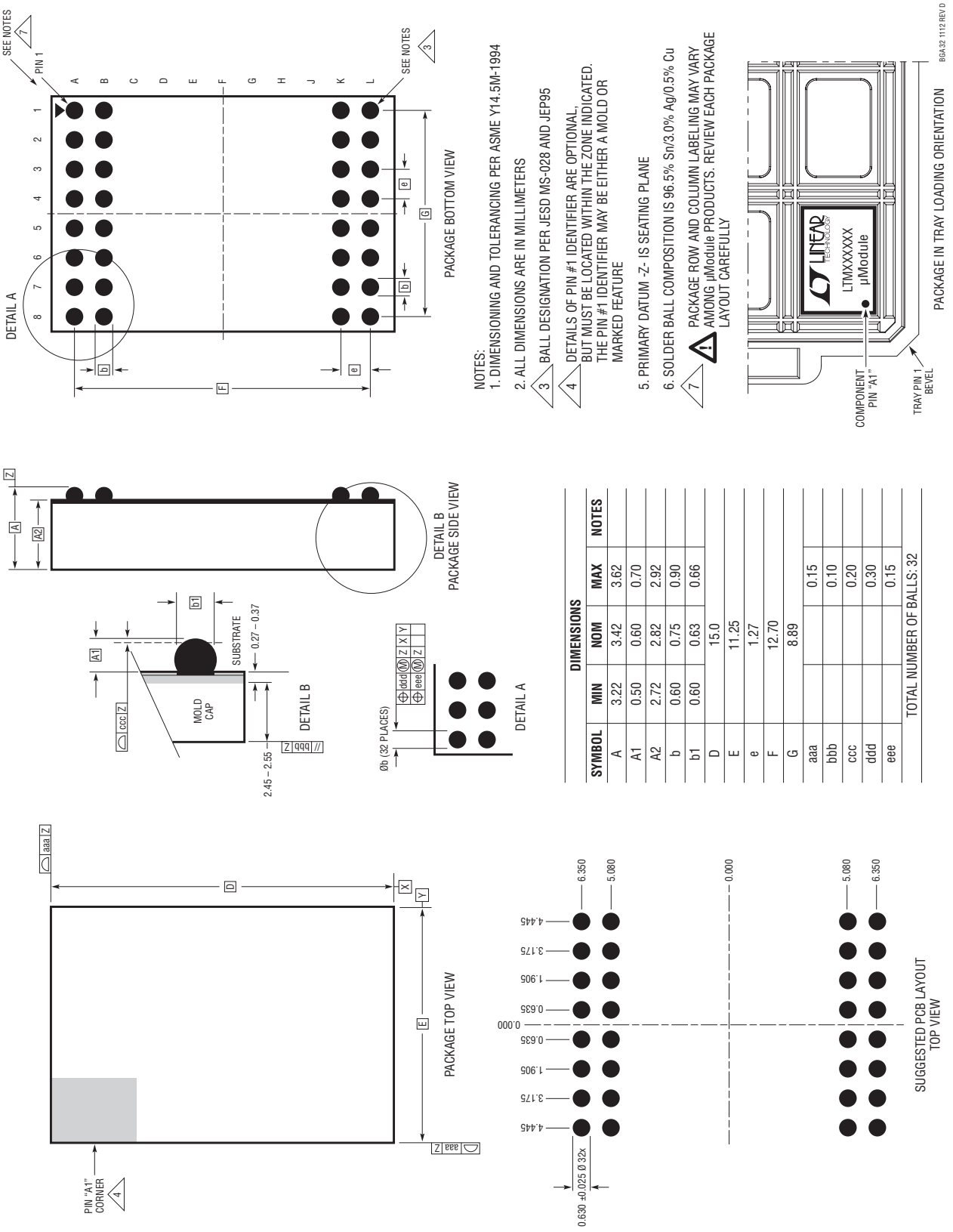


Figure 22. 4-Wire Full Duplex Self Biasing for Unshielded CAT5 Connection

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTM2881#packaging for the most recent package drawings.

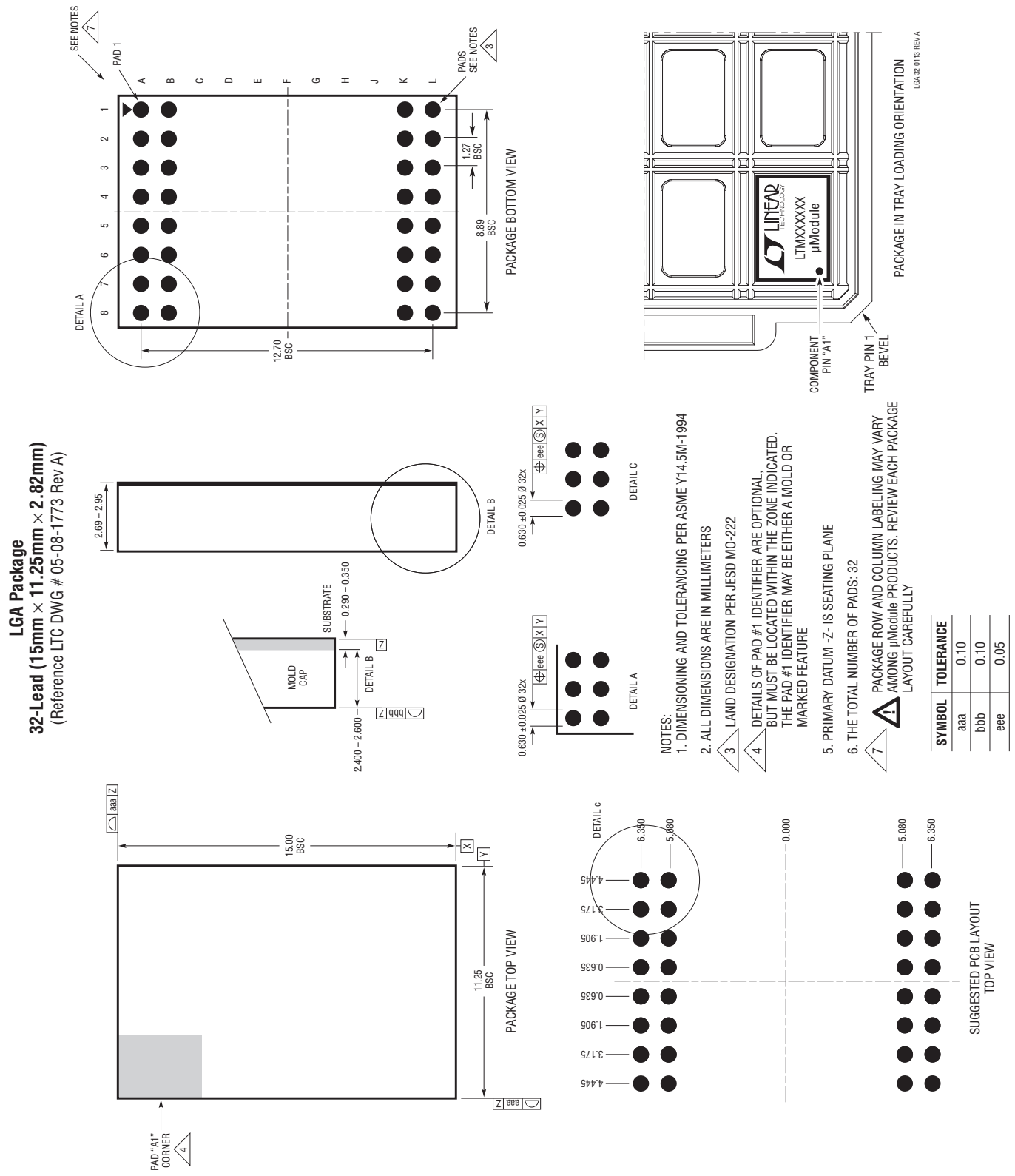
BGA Package
32-Lead (15mm × 11.25mm × 3.42mm)
(Reference LTC DWG # 05-08-1851 Rev D)



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	3.22	3.42	3.62	
A1	0.50	0.60	0.70	
A2	2.72	2.82	2.92	
b	0.60	0.75	0.90	
b1	0.60	0.63	0.66	
D		15.0		
E		11.25		
e		1.27		
F		12.70		
G		8.89		
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 32				

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTM2881#packaging for the most recent package drawings.



REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	3/10	Changes to Features, Description and Typical Application	1
		Add BGA Package to Pin Configuration, Order Information and Package Description Sections	2, 19
		Changes to LGA Package in Pin Configuration Section	2
		Changes to Electrical Characteristics Section	3
		Changes to Graphs G09, G13, G14	6, 7
		Update to Pin Functions	8
		Update to Applications Information	12
		Change to X-Axis on Figures 9a and 9b	13
		Update to Supply Current Section	14
		“PCB Layout Isolation Considerations” Section Replaced	15
		RF, Magnetic Field Immunity Section Added	16
		Changes to Related Parts	22
B	8/10	H-Grade parts added. Reflected throughout the data sheet.	1-22
C	5/11	HV-Grade parts removed. Reflected throughout the data sheet.	1-24
		Updated the PCB Layout section.	15, 16, 17
		Updated the Related Parts.	24
D	1/12	HV and MPY parts added. Reflected throughout the data sheet.	1-24
E	4/12	Added H/MP-Grade condition for I_{OZD}	3
		Corrected Figure 15	15
F	2/13	Storage Temperature Range corrected	2
G	4/14	Added lead finish part numbers	3
		Added CTI and DTI parameters	6
H	8/14	I_{CC2S}, V_{CC2} Short-Circuit Current: Deleted max spec. Added typical spec. Removed temp dot.	4
I	4/16	Added CSA information	1
		Changed I_{CCS} limits	4
J	11/16	Corrected LGA Part Marking	3

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

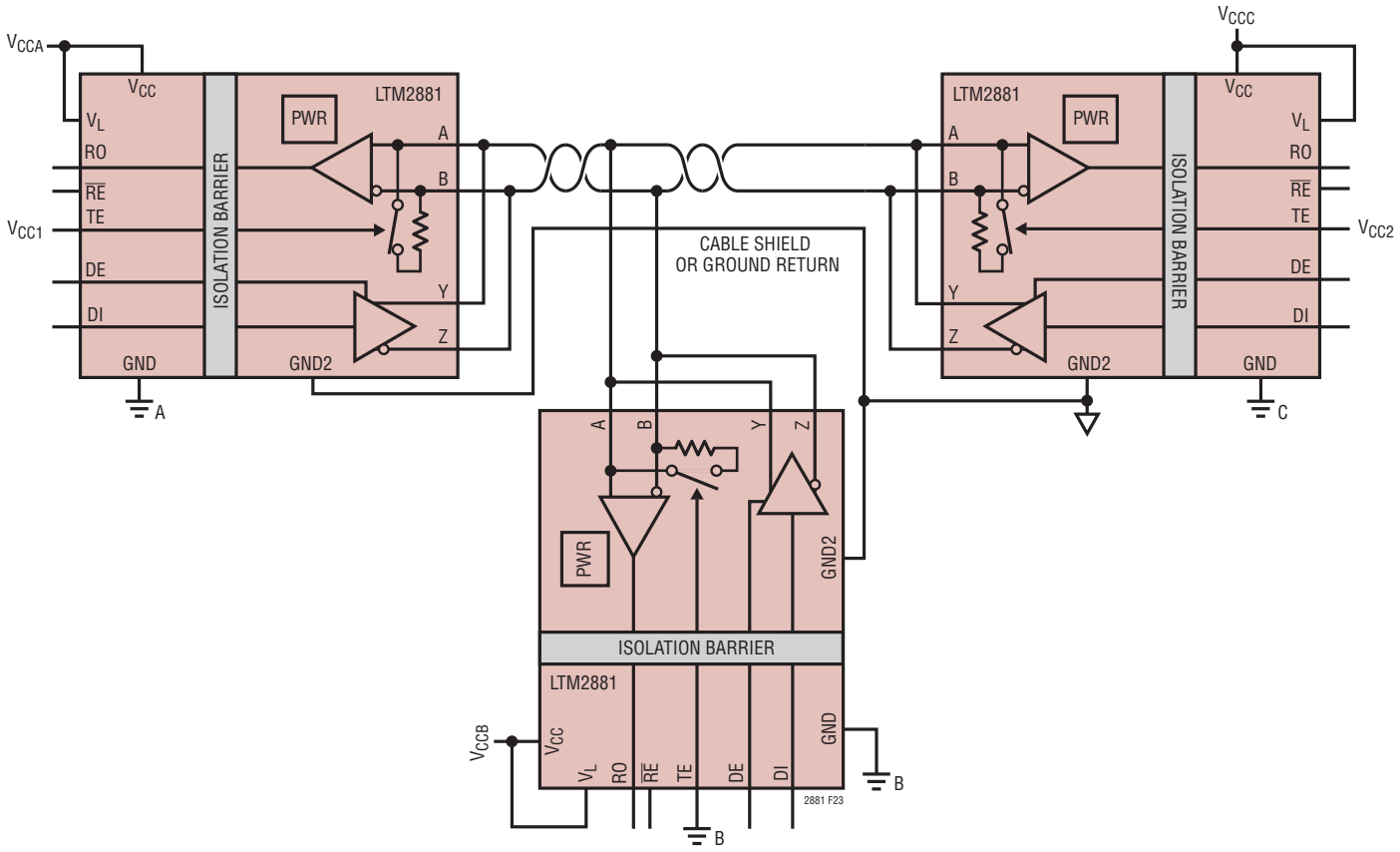


Figure 23. Multi-Node Network with End Termination and Single Ground Connection on Isolation Bus

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM2882	Dual Isolated RS232 µModule Transceiver + Power	1Mbps, ±10kV HBM ESD, 2500V_{RMS}
LTC1535	Isolated RS485 Transceiver	2500V_{RMS} Isolation in Surface Mount Package
LT1785	±60V Fault-Protected Transceiver	Half Duplex
LT1791	±60V Fault-Protected Transceiver	Full Duplex
LTC2861	20Mbps RS485 Transceivers with Integrated Switchable Termination	Full Duplex 15kV ESD
LTC2870/LTC2871	RS232/RS485 Multiprotocol Transceivers with Integrated Termination	20Mbps RS485 and 500kbps RS232, ±26kV ESD, 3V to 5V Operation
LTC2862/LTC2863/ LTC2864/LTC2865	±60V Fault Protected 3V to 5.5V RS485/RS422 Transceivers	20Mbps or 250kbps, ±15kV HBM ESD, ±25V Common Mode Range
LTM2883	SPI/Digital or I^2C Isolated µModule with Adjustable 5V and ±12V Rails	2500V_{RMS} Isolation with Power in BGA Package
LTM2892	SPI/Digital or I^2C Isolated µModule	3500V_{RMS} Isolation, 6 Channels

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