



IS29GL064

IS29GL032

64Mb/32Mb

3.0V PAGE MODE PARALLEL FLASH MEMORY

DATA SHEET

IS29GL064/032

64/32 Megabit Flash Memory

Page mode Flash Memory, CMOS 3.0 Volt-only

FEATURES

- Supply operation
 - $V_{CC} = 2.7 \sim 3.6V$
 - $V_{CCQ} = 1.65 \sim 3.6V$ (I/O buffers)
 - $V_{HH} = 9.5 \sim 10.5V$ (WP#/ACC)
- Asynchronous random or page read
 - Page size: 8 words or 16 bytes
 - Page access: 25ns
 - Random access ($V_{CCQ} = 2.7 \sim 3.6V$): 70ns
- Buffer program: 256-word MAX program buffer
- Program time
 - 0.56us per byte (1.8MB/s TYP when using 256-word buffer size in buffer program without V_{HH})
 - 0.31us per byte (3.2MB/s TYP when using 256-word buffer size in buffer program with V_{HH})
- Memory Organization
 - 32Mb: 64x 64KB (Uniform), or 8x 8KB (Top or Bottom Boot)+63x64KB
 - 64Mb: 128x 64KB (Uniform), or 8x 8KB (Top or Bottom Boot)+127x64KB
- Program/erase suspend and resume capability
 - Program suspend: Read from another sector
 - Erase suspend: Read or Program from another sector
- BLANK CHECK operation to verify an erased sector
- Unlock bypass, sector erase, chip erase, and buffer program capability
 - Fast buffered/batch programming
 - Fast sector and chip erase
- WP#/ACC pin protection
 - V_{HH} voltage on WP#/ACC to accelerate programming performance
 - Protects highest/lowest sector (H/L uniform) or top/bottom two sectors (T/B boot)
- Software Protection
 - Advanced Sector Protection (ASP)
- Support CFI (Common Flash Interface)
- Extended Memory Sector
 - 128-word (256-byte) sector for permanent secure identification
 - Program or lock implemented at the factory or by customer
- Low Power consumption: Standby mode
- Data retention: 20 years (TYP)
- 100K minimum ERASE cycles per sector
- Package Options
 - 48-pin TSOP
 - 56-pin TSOP
 - 64-ball 9mm x 9mm BGA (Call Factory)
 - 64-ball 11mm x 13mm BGA
 - 48-ball 6mm x 8mm BGA
- Temperature Range
 - Extended Grade: $-40^{\circ}C$ to $+105^{\circ}C$
 - Automotive A3 Grade: $-40^{\circ}C$ to $+125^{\circ}C$

GENERAL DESCRIPTION

The IS29GL064/032 offer fast page access time of 25ns with a corresponding random access time as fast as 70ns. It features a Write Buffer that allows a maximum of 256 words/512 bytes to be programmed in one operation, resulting in faster effective programming time than standard programming algorithms. This makes the device ideal for today's embedded applications that require higher density, better performance and lower power consumption.

PRODUCT SELECTOR GUIDE

- Speed bin depends on V_{CCQ} voltage.

Supply Voltage for Input/Output & Package	IS29GL064/032	
	Temperature	
	-40°C to +105°C	-40°C to +125°C
$V_{CCQ} = 2.7 - 3.6V$	70ns	70ns
$V_{CCQ} < 2.7V$	75ns	75ns

Note:

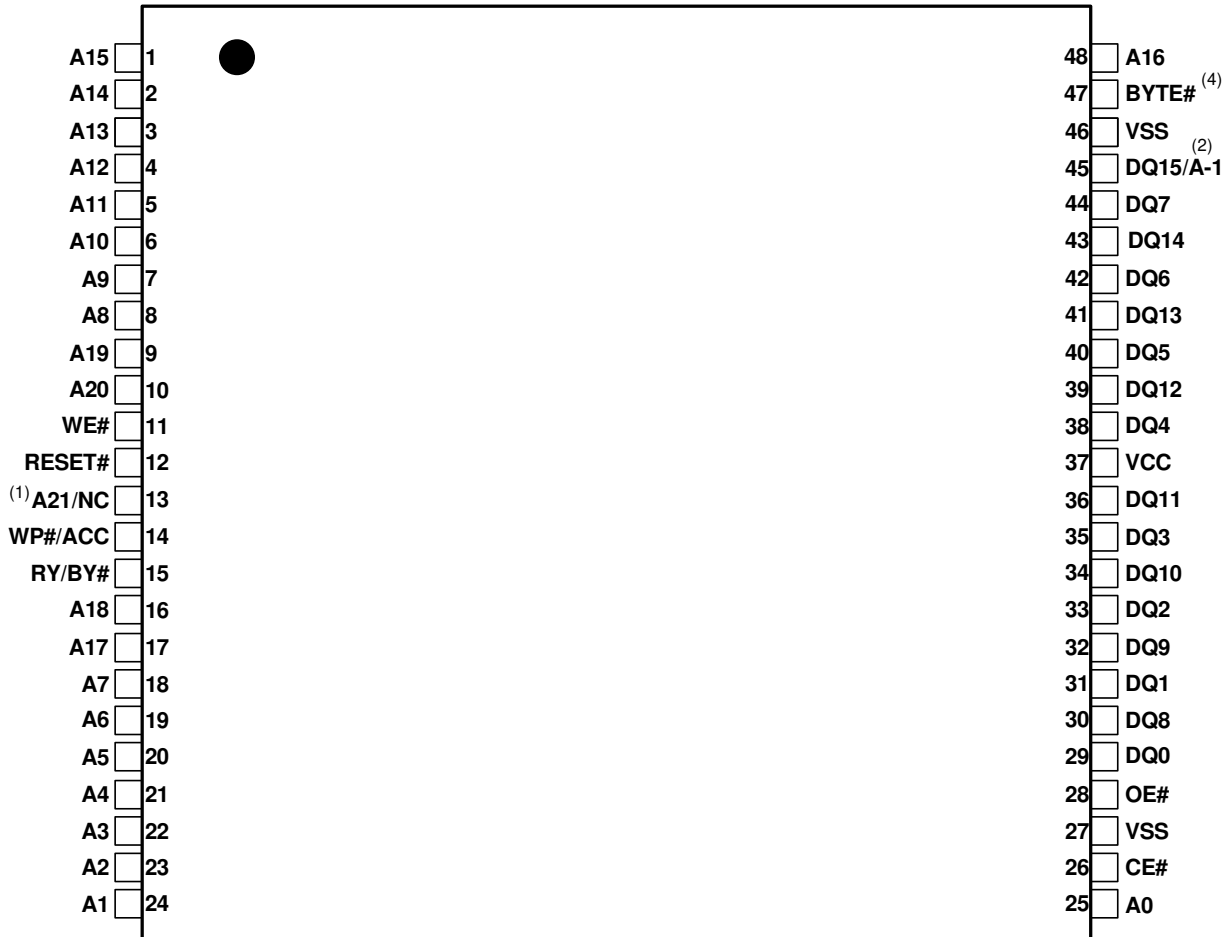
1. No V_{CCQ} pin for 48-pin TSOP and 48-ball BGA.

TABLE OF CONTENTS

GENERAL DESCRIPTION	3
PRODUCT SELECTOR GUIDE	3
TABLE OF CONTENTS	4
1. PIN CONFIGURATION	5
2. PIN DESCRIPTIONS	9
3. LOGIC DIAGRAM AND BLOCK DIAGRAM	10
4. MEMORY CONFIGURATION	12
5. BUS OPERATIONS	16
6. COMMAND OPERATIONS	17
7. STATUS REGISTER	32
8. PROTECTION	37
8.1 Device Protection Methods	37
8.2 Sector Protection Methods	37
8.3 Dynamic Protection Bits	40
8.4 Persistent Protection Bits	40
8.5 Lock Register	41
8.6 PPB Lock Bit	42
8.8 Password Lock mode	42
8.9 Sector Protection Command Definitions	45
9. Secured Silicon Region Command Sequence	49
10. COMMON FLASH INTERFACE (CFI)	50
11. POWER-UP AND RESET CHARACTERISTICS	54
12. ELECTRICAL CHARACTERISTICS	56
12.1 ABSOLUTE MAXIMUM RATINGS	56
12.2 OPERATING RANGE	56
12.3 DC CHARACTERISTICS	57
12.4 AC MEASUREMENT CONDITIONS	58
12.5 AC CHARACTERISTICS	59
13. PACKAGE INFORMATION	70
14. ORDERING INFORMATION	75

1. PIN CONFIGURATION

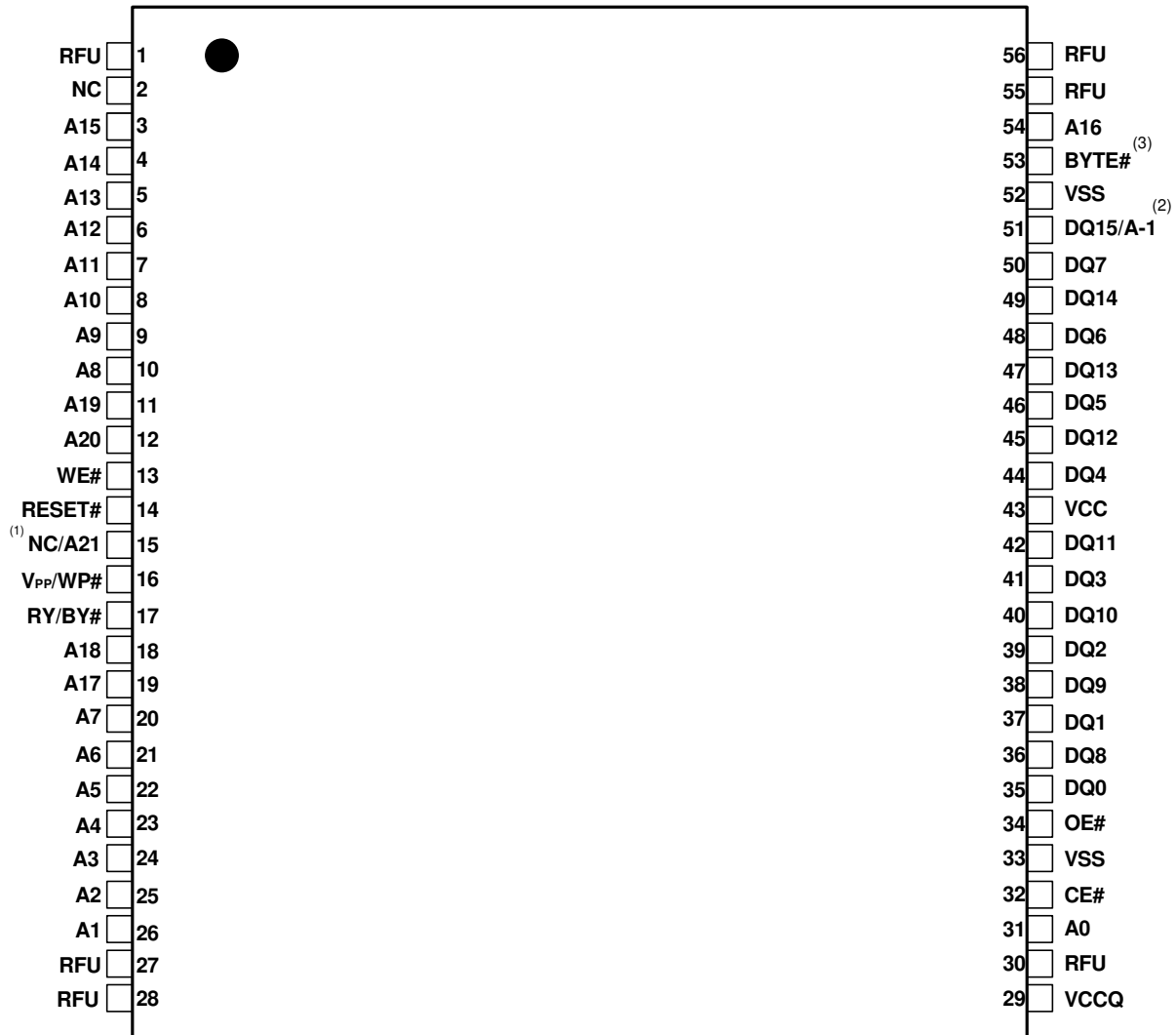
Figure 1.1 48-pin TSOP (Top View), (PKG Code: T)



Notes:

1. A21 is valid for 64Mb, and it is NC in 32Mb
2. A-1 is the least significant address in x8 mode
3. For 48-pin, there is no V_{CCQ} pin. V_{cc} also supply IO, it can only be 2.7~3.6V
4. Word mode (x16) only supported. Please contact Factory for Byte mode and Word mode.

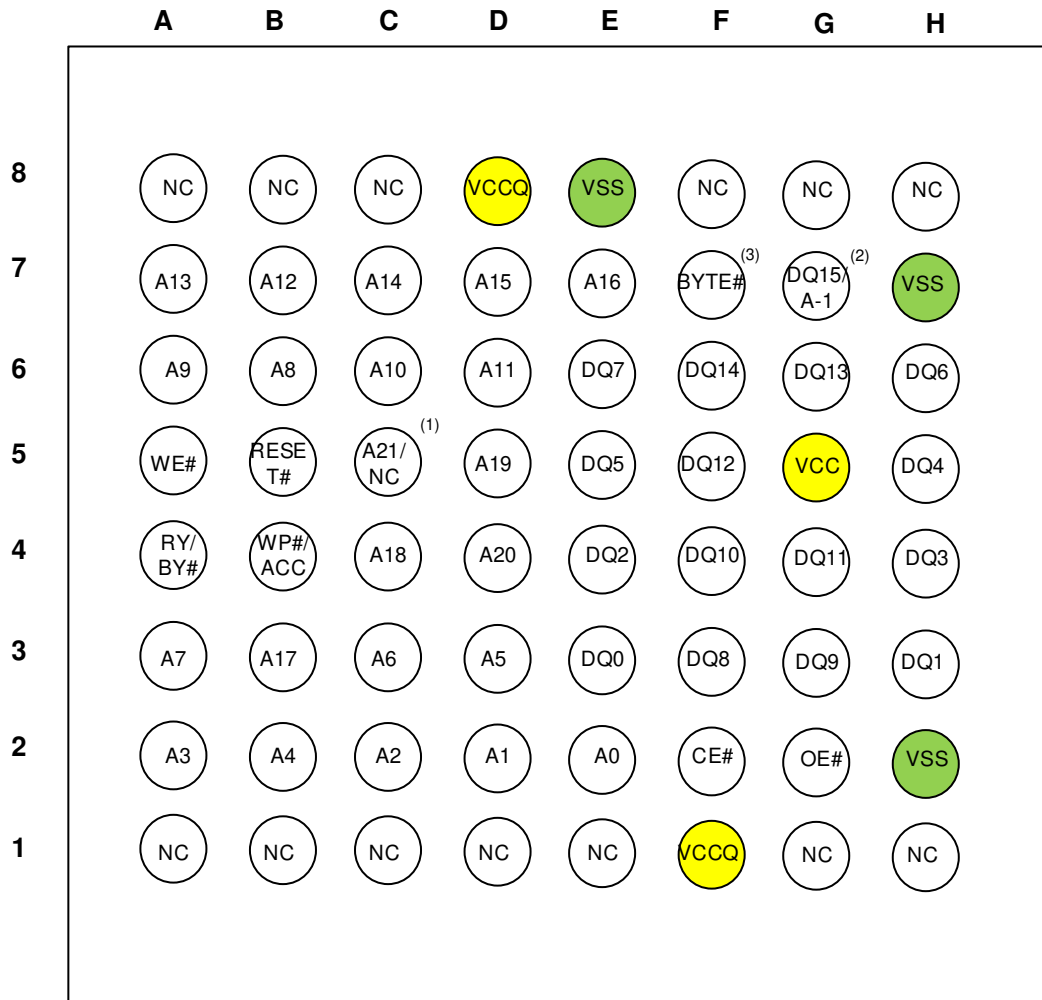
Figure 1.2. 56-pin TSOP (Top View), (PKG Code: S)



Notes:

1. A21 is valid for 64Mb, and it is NC in 32Mb
2. A-1 is the least significant address in x8 mode
3. Word mode (x16) only supported. Please contact Factory for Byte mode and Word mode.

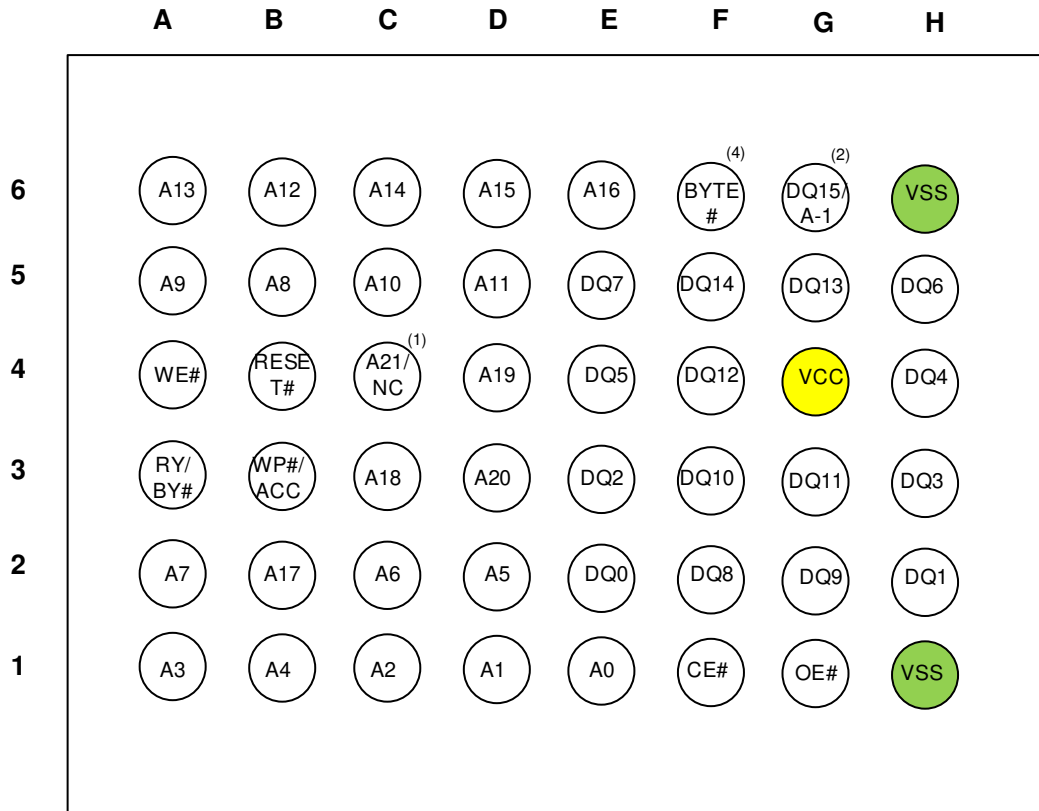
Figure 1.3. 64-ball Ball Grid Array (Top View, Balls Facing Down), (PKG Code: F)



Notes:

1. A21 is valid for 64Mb, and it is NC in 32Mb
2. A-1 is the least significant address in x8 mode
3. Word mode (x16) only supported. Please contact Factory for Byte mode and Word mode.

Figure 1.4. 48-ball Ball Grid Array (Top View, Balls Facing Down)



Notes:

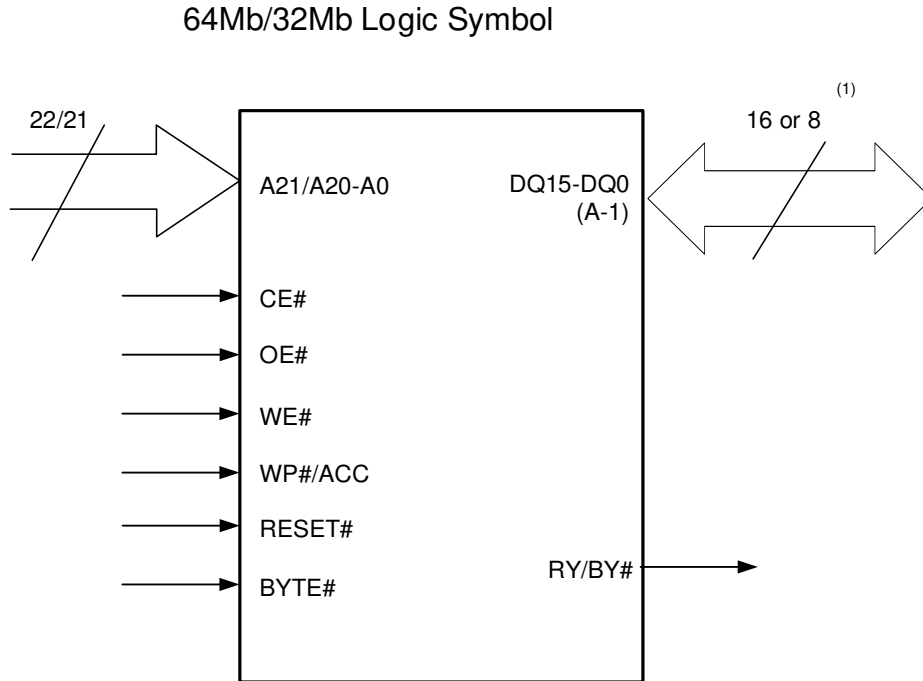
1. A21 is valid for 64Mb, and it is NC in 32Mb
2. A-1 is the least significant address in x8 mode
3. For 48-ball, there is no V_{CCQ} pin. V_{CC} also supply IO, it can only be 2.7~3.6V
4. Word mode (x16) only supported. Please contact Factory for Byte mode and Word mode.

2. PIN DESCRIPTIONS

Pin Name	Function
A21(A20)–A0	Address
DQ0-DQ14	Data input/output.
DQ15 / A-1	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
CE#	Chip Enable
OE#	Output Enable
RESET#	Hardware Reset Pin
RY/BY#	Ready/Busy Output
WE#	Write Enable
Vcc	Supply Voltage
Vccq	Supply Voltage for Input/Output.
Vss	Ground
BYTE#	Word mode only supported. Please contact Factory for Byte mode and Word mode
WP#/ACC	Write Protect / Acceleration Pin (WP# has an internal pull-up; when unconnected, WP# is at V _{IH} .)
NC	No Connect

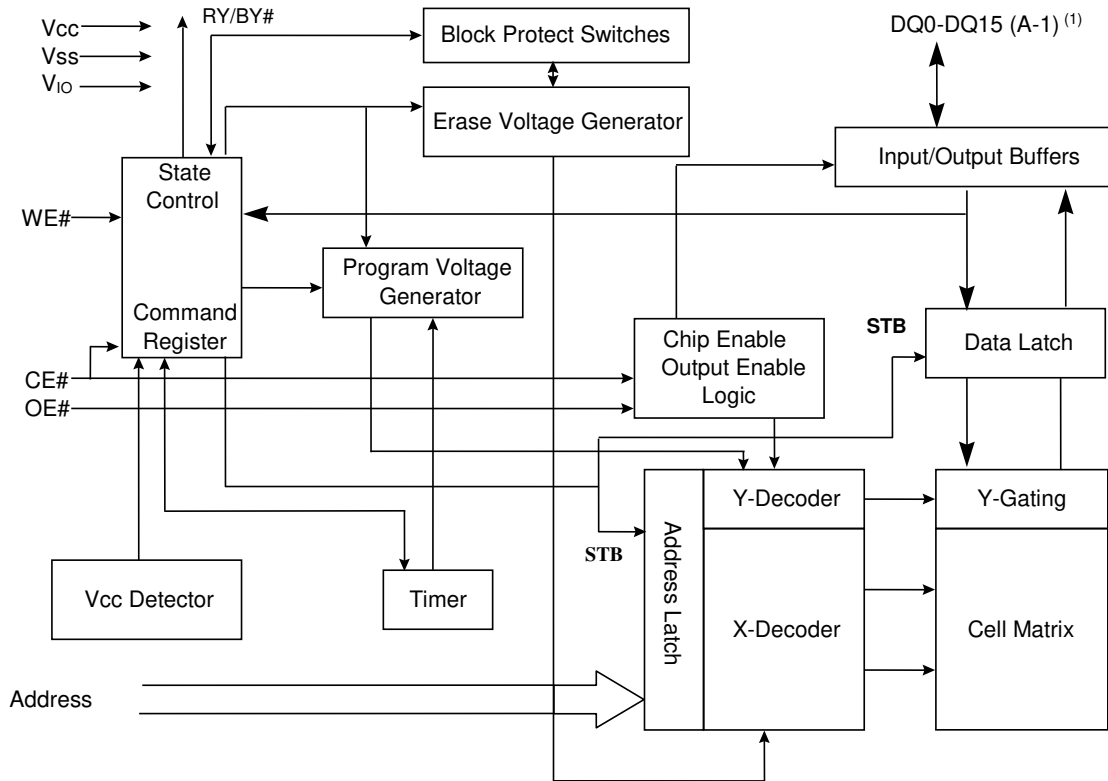
3. LOGIC DIAGRAM AND BLOCK DIAGRAM

FIGURE 3.1. LOGIC DIAGRAM



Note:

1. Word mode (x16) only supported. Please contact Factory for Byte mode and Word mode.

FIGURE 3.2 BLOCK DIAGRAM


Note:

1. Word mode (x16) only supported. Please contact Factory for Byte mode and Word mode.

4. MEMORY CONFIGURATION

- The 64Mb device (x8/x16) can be divided into 127 main sectors (64KB each) and 8 top or bottom boot sectors (8KB each).
It is also divided into 128 main uniform sectors (64KB each)
- The 32Mb device (x8/x16) can be divided into 63 main sectors (64KB each) and 8 top or bottom boot sectors (8KB each).
It is also divided into 64 main uniform sectors (64KB each)

Table 4.1. 64Mb Memory Map – x8 Top and Bottom Boot [134:0]

Sector	Sector Size	Address Range (x8 Top Boot)		Sector	Sector Size	Address Range (x8 Bottom Boot)	
		Start	End			Start	End
134	8KB	007F E000	007F FFFF	134	64KB	007F 0000	007F FFFF
133		007F C000	007F DFFF	133		007E 0000	007E FFFF
132		007F A000	007F BFFF	132		007D 0000	007D FFFF
131		007F 8000	007F 9FFF	:	:	:	:
130		007F 6000	007F 7FFF	8	64KB	0001 0000	0001 FFFF
129		007F 4000	007F 5FFF	7	8KB	0000 E000	0000 FFFF
128		007F 2000	007F 3FFF	6		0000 C000	0000 DFFF
127		007F 0000	007F 1FFF	5		0000 A000	0000 BFFF
126	64KB	007E 0000	007E FFFF	4		0000 8000	0000 9FFF
:	:	:	:	3		0000 6000	0000 7FFF
2	64KB	0002 0000	0002 FFFF	2		0000 4000	0000 5FFF
1		0001 0000	0001 FFFF	1		0000 2000	0000 3FFF
0		0000 0000	0000 FFFF	0		0000 0000	0000 1FFF

Table 4.2. 64Mb Memory Map – x16 Top and Bottom Boot [134:0]

Sector	Sector Size	Address Range (x16 Top Boot)		Sector	Sector Size	Address Range (x16 Bottom Boot)	
		Start	End			Start	End
134	4KW	003F F000	003F FFFF	134	32KW	003F 8000	003F FFFF
133		003F E000	003F EFFF	133		003F 0000	003F 7FFF
132		003F D000	003F DFFF	132		003E 8000	003E FFFF
131		003F C000	003F CFFF	:	:	:	:
130		003F B000	003F BFFF	8	32KW	0000 8000	0000 FFFF
129		003F A000	003F AFFF	7	4KW	0000 7000	0000 7FFF
128		003F 9000	003F 9FFF	6		0000 6000	0000 6FFF
127		003F 8000	003F 8FFF	5		0000 5000	0000 5FFF
126	32KW	003F 7000	003F 7FFF	4		0000 4000	0000 4FFF
:	:	:	:	3		0000 3000	0000 3FFF
2	32KW	0001 0000	0001 7FFF	2		0000 2000	0000 2FFF
1		0000 8000	0000 FFFF	1		0000 1000	0000 1FFF
0		0000 0000	0000 7FFF	0		0000 0000	0000 0FFF

Table 4.3. 64Mb Memory Map – x8/x16 Uniform Sectors [127:0]

Sector	Sector Size	Address Range (x8)		Sector	Sector Size	Address Range (x16)	
		Start	End			Start	End
127	64KB	07F 0000h	07F FFFFh	127	32KW	03F 8000h	03F FFFFh
:		:	:	:		:	:
63		03F 0000h	03F FFFFh	63		01F 8000h	01F FFFFh
:		:	:	:		:	:
0		000 0000h	000 FFFFh	0		000 0000h	0000 7FFFh

Table 4.4. 32Mb Memory Map – x8 Top and Bottom Boot [70:0]

Sector	Sector Size	Address Range (x8 Top Boot)		Sector	Sector Size	Address Range (x8 Bottom Boot)	
		Start	End			Start	End
70	8KB	003F E000	003F FFFF	70	64KB	003F 0000	003F FFFF
69		003F C000	003F DFFF	69		003E 0000	003E FFFF
68		003F A000	003F BFFF	68		003D 0000	003D FFFF
67		003F 8000	003F 9FFF	:	:	:	:
66		003F 6000	003F 7FFF	8	64KB	0001 0000	0001 FFFF
65	8KB	003F 4000	003F 5FFF	7	8KB	0000 E000	0000 FFFF
64		003F 2000	003F 3FFF	6		0000 C000	0000 DFFF
63		003F 0000	003F 1FFF	5		0000 A000	0000 BFFF
62	64KB	003E 0000	003E 1FFF	4		0000 8000	0000 9FFF
:	:	:	:	3		0000 6000	0000 7FFF
2	64KB	0002 0000	0002 FFFF	2		0000 4000	0000 5FFF
1		0001 0000	0001 FFFF	1		0000 2000	0000 3FFF
0		0000 0000	0000 FFFF	0		0000 0000	0000 1FFF

Table 4.5. 32Mb Memory Map – x16 Top and Bottom Boot [70:0]

Sector	Sector Size	Address Range (x16 Top Boot)		Sector	Sector Size	Address Range (x16 Bottom Boot)	
		Start	End			Start	End
70	4KW	001F F000	001F FFFF	70	32KW	001F 8000	001F FFFF
69		001F E000	001F EFFF	69		001F 0000	001F 7FFF
68		001F D000	001F DFFF	68		001E 8000	001E FFFF
67		001F C000	001F CFFF	:	:	:	:
66		001F B000	001F BFFF	8	32KW	0000 8000	0000 FFFF
65		001F A000	001F AFFF	7	4KW	0000 7000	0000 7FFF
64		001F 9000	001F 9FFF	6		0000 6000	0000 6FFF
63	32KW	001F 8000	001F 8FFF	5		0000 5000	0000 5FFF
62		001F 7000	001F 7FFF	4		0000 4000	0000 4FFF
:	:	:	:	3		0000 3000	0000 3FFF
2	32KW	0001 0000	0001 7FFF	2		0000 2000	0000 2FFF
1		0000 8000	0000 FFFF	1		0000 1000	0000 1FFF
0		0000 0000	0000 7FFF	0		0000 0000	0000 0FFF

Table 4.6. 32Mb Memory Map – x8/x16 Uniform Sectors [63:0]

Sector	Sector Size	Address Range (x8)		Sector	Sector Size	Address Range (x16)	
		Start	End			Start	End
63		03F 0000h	03F FFFFh	63		01F 8000h	01F FFFFh
:		:	:	:		:	:
0		000 0000h	000 FFFFh	0		000 0000h	0000 7FFFh

5. BUS OPERATIONS

Table 5.1. Device OPERATING MODES

Operation	CE#	OE#	WE#	RESET#	WP#/ACC	Byte Mode (x8) ⁽⁵⁾			Word Mode (x16) ⁽⁵⁾	
						A[MAX:0], DQ15/A-1	DQ[14:8]	DQ[7:0]	A[MAX:0]	DQ15/A-1, DQ[14:0]
READ	L	L	H	H	X	Byte address	High-Z	Data output	Word address	Data output
WRITE	L	H	L	H	H ⁽³⁾	Command address	High-Z	Data input ⁽⁴⁾	Command address	Data input ⁽⁴⁾
STANDBY	H	X	X	H	H	X	High-Z	High-Z	X	High-Z
OUTPUT DISABLE	L	H	H	H	X	X	High-Z	High-Z	X	High-Z
RESET	X	X	X	L	X	X	High-Z	High-Z	X	High-Z

Notes:

1. Typical glitch of less than 3ns on CE#, and WE# are ignored by the device and do not affect bus operation.
2. H = Logic level HIGH (V_{IH}); L = Logic Level LOW (V_{IL}); X = HIGH or LOW
3. If WP# is LOW, then the highest or lowest sector remains protected, or the top two sectors or the bottom two sectors, depending on the item.
4. Data input is required when issuing a command sequence or when performing data polling or sector protection.
5. BYTE# = H for Word mode, L for Byte mode.

6. COMMAND OPERATIONS

Table 6.1. Standard Command Definitions

Command	Bus Size	Address and Data Cycles												Notes
		1st		2nd		3rd		4th		5th		6th		
		A	D	A	D	A	D	A	D	A	D	A	D	
READ and AUTO SELECT Operations														
READ/RESET (F0h)	X8	X	F0											
		AAA	AA	555	55	X	F0							
	X16	X	F0											
		555	AA	2AA	55	X	F0							
READ CFI (98h)	X8	AA	98											
	X16	55												
AUTO SELECT (90h)	X8	AAA	AA	555	55	AAA	90	Note 2	Note 2					2,3,4
	X16	555		2AA		555								
BYPASS Operations														
UNLOCK BYPASS (20h)	X8	AAA	AA	555	55	AAA	20							
	X16	555		2AA		555								
UNLOCK BYPASS RESET (90h/00h)	X8	X	90	X	00									
	X16													
PROGRAM Operations														
PROGRAM (A0h)	X8	AAA	AA	555	55	AAA	A0	PA	PD					
	X16	555		2AA		555								
UNLOCK BYPASS PROGRAM (A0h)	X8	X	A0	PA	PD									5
	X16													
DOUBLE BYTE/WORD PROGRAM (50h)	X8	AAA	50	PA2	PD									
	X16	555												
QUADRUPLE BYTE/WORD PROGRAM (56h)	X8	AAA	56	PA4	PD									
	X16	555												
OCTUPLE BYTE PROGRAM (8Bh)	X8	AAA	8B	PA8	PD									6

Table 6.1. Standard Command Definitions (Continued)

Command	Bus Size	Address and Data Cycles												Notes
		1st		2nd		3rd		4th		5th		6th		
		A	D	A	D	A	D	A	D	A	D	A	D	
WRITE BUFFER LOAD (25h)	X8	AAA	AA	555	55	BSAd	25	BSAd	N	WBP A	PD			7, 8
	X16	555		2AA										
UNLOCK BYPASS WRITE BUFFER LOAD (25h)	X8	BSAd	25	BSAd	N	WBP A	PD							5, 7, 8
	X16													
PROGRAM BUFFER TO FLASH CONFIRM (29h)	X8	BSAd	29											
	X16													
BUFFERED PROGRAM ABORT and RESET (F0h)	X8	AAA	AA	555	55	AAA	F0							
	X16	555		2AA		555								
PROGRAM SUSPEND (B0h)	X8	X	B0											
	X16													
PROGRAM RESUME (30h)	X8	X	30											
	X16													
ERASE Operations														
CHIP ERASE (80/10h)	X8	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10	
	X16	555		2AA		555		555		2AA		555		
UNLOCK BYPASS CHIP ERASE (80/10h)	X8	X	80	X	10									5
	X16													
SECTOR ERASE (80/30h)	X8	AAA	AA	555	55	AAA	80	AAA	AA	555	55	BAd	30	9
	X16	555		2AA		555		555		2AA				
UNLOCK BYPASS SECTOR ERASE (80/30h)	X8	X	80	BAd	30									5
	X16													
ERASE SUSPEND (B0h)	X8	X	B0											
	X16													
ERASE RESUME (30h)	X8	X	30											
	X16													

Table 6.1. Standard Command Definitions (Continued)

Command	Bus Size	Address and Data Cycles												Notes
		1st		2nd		3rd		4th		5th		6th		
		A	D	A	D	A	D	A	D	A	D	A	D	
BLANK CHECK Operations														
BLANK CHECK SETUP (EB/76h)	X8	AAA	AA	555	55	BAd	EB	BAd	76	BAd	00	BAd	00	
	X16	555		2AA										
BLANK CHECK CONFIRM and READ (29h)	X8	BAd	29	BAd	Note 2									2
	X16													

Notes:

1. A = Address; D = Data; X = Don't Care, BAd = Any address in the sector; BSAd = Any address in the sector with constant A[Max:12]; WBPA = write buffer program address with A[Max:12] = BSAd, N = Number of bytes to be programmed; PA = program address; PA2 = Program address with constant A[Max:0] for x8 or A[Max:1] for x16, which should be used two times to select adjacent two bytes/words; PA4 = Program address with constant A[Max:1] for x8 or A[Max:2] for x16, which should be used four times to select four bytes/words; PA8 = Program address with constant A[Max:2] for x8, which should be used eight times to select adjacent eight bytes; PD = Program data; Gray shading = Not applicable. All values in the table are hexadecimal. Some commands require both a command code and subcode.
2. These cells represent READ cycles (versus WRITE cycles for others).
3. AUTO SELECT enables the device to read the manufacturer code, device code, sector protection status, and Secured Silicon Region protection indicator.
4. AUTO SELECT addresses and data are specified in the Electronic Signature table and the Secured Silicon Region table.
5. For any UNLOCK BYPASS ERASE/PROGRAM command, the first two UNLOCK cycles are unnecessary.
6. This command is only for x8 devices.
7. WRITE BUFFER LOAD operation: maximum cycles = 261 (x8) and 261 (x16).
UNLOCK BYPASS WRITE BUFFER LOAD operation: maximum cycles = 259 (x8), 259 (x16).
WRITE BUFFER LOAD operation: N + 1 = bytes to be programmed;
Maximum buffer size = 256 bytes (x8) and 512 bytes (x16)
8. For x8, A [Max: 7] address pins for WBPA should remain unchanged while A [6:0] and A-1 pins for WBPA are used to select a byte within the N+1 byte page. For x16, A [Max: 8] address pins for WBPA should remain unchanged while A [7:0] pins for WBPA are used to select a word within the N+1 word page.
9. BLOCK ERASE address cycles can extend beyond six address data cycles, depending on the number of sectors to erase.

6.1 Read Operation

Bus READ operations read from the memory cells, or CFI space. To accelerate the READ operation, the memory array can be read in page mode where data is internally read and stored in a page buffer.

Page size is 8 words (16 bytes) and is addressed by address inputs A [2:0] in x16 bus mode and A[2:0] plus DQ15/A-1 in x8 bus mode. The Secured Silicon Region and CFI area do not support page mode.

A valid bus READ operations involves setting the desired address on the address inputs, taking CE# and OE# LOW, and holding WE# HIGH. The data I/Os will output the value.

6.2 Page Read Operation

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. The page size of the device is 8 words/16 bytes. The appropriate page is selected by the higher address bits Amax-A3. Address bits A2-A0 in word mode (A2 to A-1 in byte mode) determine the specific word within a page. The microprocessor supplies the specific word location.

The random or initial page access is equal to tACC or tCE and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to tPACC. When CE# is deasserted and reasserted for a subsequent access, the access time is tACC or tCE. Fast page mode accesses are obtained by keeping the “read-page addresses” constant and changing the “intra-read page” addresses.

6.3 Autoselect Operation

The Autoselect mode provides manufacturer ID, Device identification, sector protection status and Secured Silicon Region protection indicator with executing a READ operation with control signals and addresses set. In addition, this device information can be read or set by issuing an AUTO SELECT command.

The device only support to use Autoselect command to access Autoselect codes.

It does not support the mode of applying V_{HH} on address pin A9.

- The Autoselect command sequence may be written to an address within a sector that is either in the read or erase-suspend-read mode.
- The Autoselect command may not be written while the device is actively programming or erasing.
- The system must write the reset command to return to the read mode (or erase-suspend-read mode if the sector was previously in Erase Suspend).

Table 6.2. Manufacturer ID and Device ID

Read Cycle		CE#	OE#	WE#	Address Input						Data Input/Output			
					X8/x16						x8 only	X8 only		x16 only
					A[Max:11]	A[10:4]	A3	A2	A1	A0	A-1	DQ[14:8]	DQ[7:0]	DQ[15:0]
Manufacturer code		L	L	H	X	L	L	L	L	L	X	X	9Dh	009Dh
Device ID 1		L	L	H	X	L	L	L	L	H	X	X	7Eh	227Eh
Device ID 2	64Mb boot	L	L	H	X	L	H	H	H	L	X	X	10h	2210h
	64Mb uniform												0Ch	220Ch
	32Mb boot												1Ah	221Ah
	32Mb uniform												1Dh	221Dh
Device ID 3	64/32Mb High protection	L	L	H	X	L	H	H	H	H	X	X	01h	2201h
	64/32Mb Top boot													
	64/32Mb Low protection												00h	2200h
	64/32Mb Bottom boot													

Note:

1. H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); X = HIGH or LOW.

Table 6.3. Sector Protection

Read Cycle		CE#	OE#	WE#	Address Input						Data Input/Output		
					X8/x16					x8 only	X8 only		x16 only
	Opti on ⁽⁶⁾				A[Max:15]	A[14:11]	A[10:2]	A1	A0	A-1	DQ[14:8]	DQ[7:0]	DQ[15:0]
Secured Silicon Region protection indicator (DQ7)	L	L	L	H	X	X	L	H	H	X	X	8Ah ⁽²⁾	008Ah ⁽²⁾
												0Ah ⁽³⁾	000Ah ⁽³⁾
	H	L	L	H	X	X	L	H	H	X	X	9Ah ⁽²⁾	009Ah ⁽²⁾
												1Ah ⁽³⁾	001Ah ⁽³⁾
	B	L	L	H	X	X	L	H	H	X	X	8Ah ⁽²⁾	008Ah ⁽²⁾
												0Ah ⁽³⁾	000Ah ⁽³⁾
	T	L	L	H	X	X	L	H	H	X	X	9Ah ⁽²⁾	009Ah ⁽²⁾
												1Ah ⁽³⁾	001Ah ⁽³⁾
Sector Protection status		L	L	H	Sector base address	L	L	H	L	X	X	01h ⁽⁴⁾	0001h ⁽⁴⁾
												00h ⁽⁵⁾	0000h ⁽⁵⁾

Notes:

- H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); X = HIGH or LOW.
- ISSI – prelocked (permanent).
- Customer lockable.
- Protected: DQ [7:0] = 01h. This protection status includes PPB and DYB but does not include WP#/ACC=L effect
- Unprotected: DQ [7:0] = 00h.
- Sector Protection Option:
 - H = Highest sector protected by WP#/ACC; uniform sector
 - L = Lowest sector protected by WP#/ACC; uniform sector
 - T = Top boot; top two sectors protected by WP#/ACC
 - B = Bottom boot; bottom two sectors protected by WP#/ACC

6.4 UNLOCK BYPASS Operation

The UNLOCK BYPASS (20h) command is also used to place the device in unlock bypass mode. Three bus WRITE operations are required to issue the UNLOCK BYPASS command.

When the device enters unlock bypass mode, the two initial UNLOCK cycles required for a standard PROGRAM or ERASE operation are not needed, thus enabling faster total program or erase time.

During the unlock bypass mode, below UNLOCK BYPASS COMMANDs are available.

UNLOCK BYPASS PROGRAM
 UNLOCK BYPASS WRITE BUFFER LOAD
 UNLOCK BYPASS CHIP ERASE
 UNLOCK BYPASS SECTOR ERASE
 UNLOCK BYPASS RESET

The UNLOCK BYPASS RESET (90/00h) command is used to return to read/reset mode from unlock bypass mode. Two bus WRITE operations are required to issue the UNLOCK BYPASS RESET command. The READ/RESET command does not exit from unlock bypass mode.

Also the device automatically enters UNLOCK BYPASS mode when WP# /ACC is raised to V_{HH} .

Note: It is recommended that entering and exiting unlock bypass mode using the ENTER UNLOCK BYPASS and UNLOCK BYPASS RESET commands rather than raising WP#/ACC to V_{HH} .

WP#/ACC should never be raised to V_{HH} from any mode except read mode; otherwise, the device may be left in an indeterminate state.

6.5 Program Operations

The PROGRAM (A0h) command is used to program a value to address in the memory array.

The command requires 4 bus WRITE operations, and the final WRITE operation latches the address and data in the internal state machine and starts the program/erase controller. After programming has started, bus READ operations output the status register content.

Programming can be suspended and then resumed by issuing a PROGRAM SUSPEND command and a PROGRAM RESEUM command, respectively.

If programming address is within a protected sector, the PROGRAM command is ignored, and the data remains unchanged. The status register is not read, and no error condition is given.

After the PROGRAM operation has completed, the device returns to read mode, unless an error has occurred.

When an error occurs, bus READ operations to the device continue to output the status register. A READ/RESET command must be issued to reset the error condition and return the device to read mode.

The PROGRAM command cannot change a bit set to 0 back to 1, and an attempt to do so is masked during a PROGRAM operation. Instead, an ERASE command must be used to set all bits in one memory sector or in the entire memory from 0 to 1.

The PROGRAM operation is aborted by performing a hardware reset or by powering-down the device. In this case, data integrity cannot be ensured, and it is recommended that the words or bytes that were aborted be reprogrammed.

6.6 ACCELERATED PROGRAM

Accelerated single word programming and write buffer programming operations are enabled through the WP#/ACC pin. This method is faster than the standard program command sequences.

If the system asserts V_{HH} on this input, the device automatically enters the Accelerated Program mode and uses the higher voltage and current provided by WP#/ACC pin to reduce the time required for program operations. Also the device automatically enters UNLOCK BYPASS mode when WP# /ACC is raised to V_{HH} .

The system can then use the Write Buffer Load command sequence provided by the Accelerated Program mode. When WP#/ACC returns to V_{IH} or V_{IL} , upon completion of the embedded program operation, returns the device to normal operation.

- Sectors must be unprotected prior to raising WP#/ACC to V_{HH} .
- The WP#/ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result.
- It is recommended that WP#/ACC apply V_{HH} after power-up sequence is completed. In addition, it is recommended that WP#/ACC apply from V_{HH} to V_{IH}/V_{IL} before powering down V_{CC}/V_{CCQ} .

6.7 DOUBLE BYTE/WORD PROGRAM

The DOUBLE BYTE/WORD PROGRAM (50h) command is used to write a page of two adjacent bytes/words in parallel. The two bytes/words must differ only for the address A-1 or A0, respectively.

Three bus write cycles are necessary to issue the command:

- The first bus cycle sets up the command.
- The second bus cycle latches the address and data of the first byte/word to be programmed.
- The third bus cycle latches the address and data of the second byte/word to be programmed and starts the program/erase controller.

6.8 QUADRUPLE BYTE/WORD PROGRAM

The QUADRUPLE BYTE/WORD PROGRAM (56h) command is used to write a page of four adjacent bytes/words in parallel. The four bytes/words must differ only for the address A0, DQ15/A-1 in x8 mode or for addresses A1, A0 in x16 mode.

Five bus write cycles are necessary to issue the command:

- The first bus cycle sets up the command.
- The second bus cycle latches the address and data of the first byte/word to be programmed.
- The third bus cycle latches the address and data of the second byte/word to be programmed.
- The fourth bus cycle latches the address and data of the third byte/word to be programmed.
- The fifth bus cycle latches the address and data of the fourth byte/word to be programmed and starts the program/erase controller.

Note: The DOUBLE/QUADRUPLE PROGRAM commands are available in the 32Mb and 64Mb device; also only V_{PPL} is to be applied to the WP#/ACC pin.

6.9 OCTUPLE BYTE PROGRAM

The OCTUPLE BYTE PROGRAM (8Bh) command is used to write a page of eight adjacent bytes in parallel. The eight bytes must differ only for the address A1, A0, DQ15/A-1 in x8 mode only.

Nine bus write cycles are necessary to issue the command:

The first bus cycle sets up the command.

The second bus cycle latches the address and data of the first byte to be programmed.

The third bus cycle latches the address and data of the second byte to be programmed.

The fourth bus cycle latches the address and data of the third byte to be programmed.

The fifth bus cycle latches the address and data of the fourth byte to be programmed.

The sixth bus cycle latches the address and data of the fifth byte to be programmed.

The seventh bus cycle latches the address and data of the sixth byte to be programmed.

The eighth bus cycle latches the address and data of the seventh byte to be programmed.

The ninth bus cycle latches the address and data of the eighth byte to be programmed and starts the program/erase controller.

Note: The OCTUPLE BYTE PROGRAM command is available only in the 32Mb and 64Mb X8 devices; also only V_{PPL} is to be applied to the WP#/ACC pin.

6.10 WRITE BUFFER PROGRAM Operation

Write Buffer Programming allows the system to write a maximum of 256 words in one programming operation. This results in a faster effective word programming time than the standard “word/byte” programming algorithms. When issuing a WRITE BUFFER LOAD command, WP#/ACC can be held HIGH or raised to V_{HH} . Also, it can be held LOW if the sector is not the lowest or highest sector or the top/bottom two sectors, depending on the part number. When V_{HH} is applied to the WP#/ACC pin during execution of the command, programming speed increases.

The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the **WRITE BUFFER LOAD** command written at the Boot Sector Address (BSAd; A[Max:12]) in which programming occurs.

At this point, the system writes the number of words/bytes to be programmed. Value n is written to the same Boot Sector address (BSAd), where $n+1$ is the number of words/bytes to be programmed. Value $n+1$ must not exceed the size of the program buffer, or the operation will abort. For example, if the system programs 6 address locations, then 05h should be written to the device.

The fifth cycle loads the starting address/data combination. This starting address is the first address/data pair to be programmed, and selects the “write-buffer-page” address. All subsequent address/data pairs must fall within the selected-write-buffer-page.

After writing the Starting Address/Data pair, the system then writes the remaining address/data pairs into the write buffer. Addresses must be within the range from the **start address+1** to the **start address + (n-1)**. For x8 device, maximum buffer size is 256 bytes; for x16 device, maximum buffer size is 512 bytes.

The “write-buffer-page” is selected by using A[Max:8] within Write Buffer Program Address (WBPA, where A[Max:12] of WBPA = BSAd). A[Max:8] must be the same for all address/data pairs loaded into the write buffer. This means Write Buffer Programming cannot be performed across multiple “write-buffer-pages.” This also means that Write Buffer Programming cannot be performed across multiple sectors.

Note that if a Write Buffer address location is loaded multiple times, the “address/data pair” counter is decremented for every data load operation. Also, the last data loaded at a location before the “**Program Buffer to Flash**” confirm command is the data programmed into the device. It is the software’s responsibility to comprehend ramifications of loading a write-buffer location more than once. The counter decrements for each data load operation, NOT for each unique write-buffer-address location. Once the specified number of write buffer locations have been loaded, the system must then write the “Program Buffer to Flash” command at the Sector Address. Any other address/data write combinations abort the Write Buffer Programming operation. The Write Operation Status bits should be used while monitoring the last address location loaded into the write buffer. This eliminates the need to store an address in memory because the system can load the last address location, issue the program confirm command at the last loaded address location, and then check the write operation status at that same address. The status register bits DQ1, DQ5, DQ6, DQ7 can be used to monitor the device status during Write Buffer Programming.

The write-buffer “embedded” programming operation can be suspended or resumed using the standard suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device returns to READ mode.

The Write Buffer Programming Sequence is ABORTED under any of the following conditions:

- Load a value that is greater than the page buffer size during the “Number of Locations to Program” step.
- Write to a different BSAd, A[Max:12], different than the one specified during the Write-Buffer-Load command.
- Write an Address/Data pair to a different write-buffer-page than the one selected by the “Starting Address” during the “write buffer data loading” stage of the operation.
- Writing anything other than the Program to Buffer Flash Command after the specified number of “data load” cycles.

BUFFERED PROGRAM ABORT AND RESET (F0h) command must be issued to reset the device to read mode when the BUFFER PROGRAM operation is aborted. The buffer programming sequence can be aborted in the following ways.

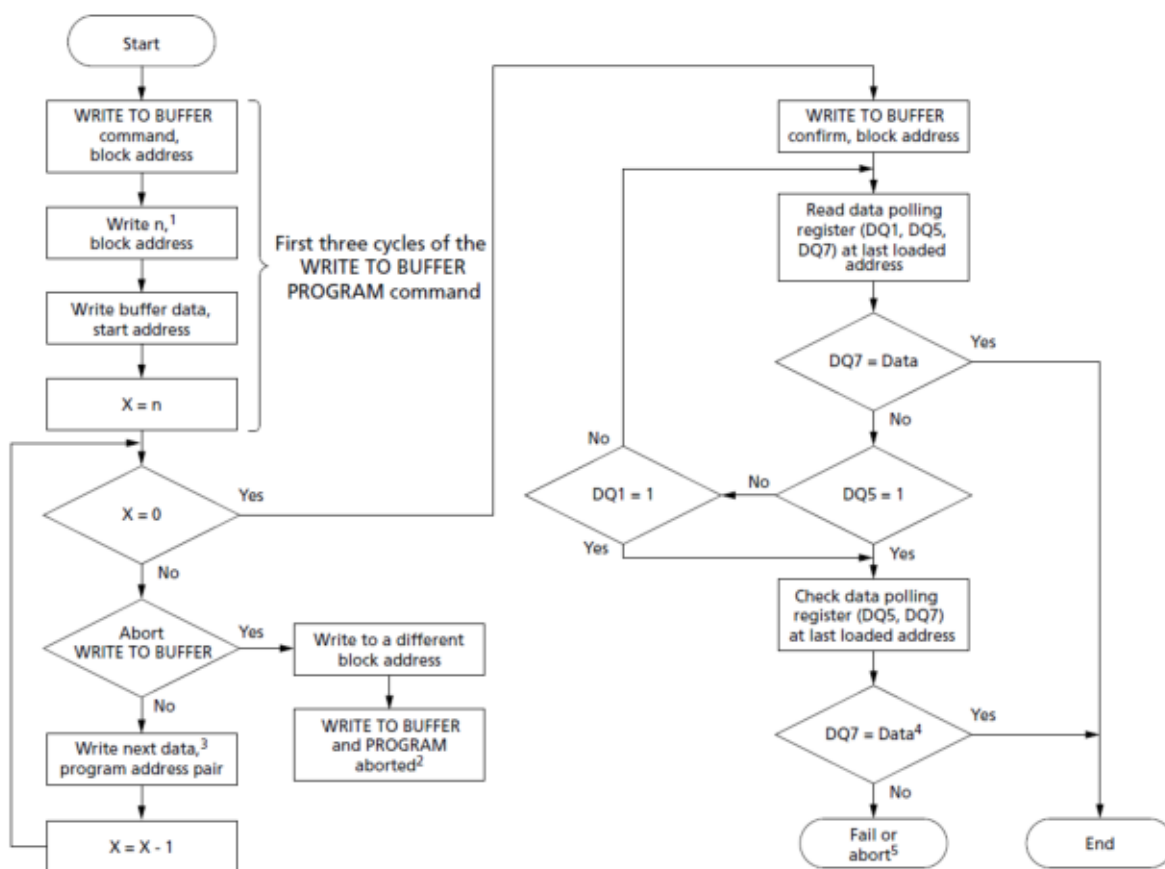
The abort condition is indicated by DQ1 = 1, DQ7 = DQ7# (for the last address location loaded), DQ6 = toggle, DQ5 = 0 (all of which are status register bits).

Note: The full three-cycle BUFFERED PROGRAM ABORT and RESET command sequence is required when using buffer programming features in unlock bypass mode.

6.11 PROGRAM BUFFER TO FLASH OPERATION

The PROGRAM BUFFER TO FLASH (29h) command is used to confirm a WRITE BUFFER LOAD command to program the n+1 words/bytes loaded in the program buffer.

Figure 6.1. BUFFER PROGRAM Flowchart



6.12 PROGRAM SUSPEND OPERATION

The PROGRAM SUSPEND (B0h) command allows the system to interrupt a PROGRAM operation or a "Buffer Program" operation so that data can be read from any non-suspended sector. When the PROGRAM SUSPEND command is issued during a programming process, the device suspends the programming operation within the program suspend latency time (**15 μ s maximum, 5 μ s typical**) and updates the status register bits. Addresses are "don't-cares" when writing the Program Suspend command.

After the PROGRAM operation has been suspended, data can be read array data from any non-suspended sector.

The PROGRAM SUSPEND command may also be issued during a PROGRAM operation while an erase is suspended. In this case, data may be read from any addresses not within a sector in ERASE SUSPEND or PROGRAM SUSPEND.

If a read is needed from the Secured Silicon Region area (one-time programmable area), the ENTER/EXIT Secured Silicon Region command sequence must be issued.

The system may also issue the AUTO SELECT command sequence and CFI query command when the device is in program suspend mode. The system can read as many auto select codes as required.

When the device exits the auto select mode, the device reverts to Program Suspend mode, and is ready for another valid operation.

The PROGRAM SUSPEND operation is aborted by performing a device reset or power down. In this case, data integrity cannot be ensured, and it is recommended that the words or bytes that were aborted be reprogrammed.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the write operation status bits, just as in the standard program operation.

6.13 PROGRAM RESUME command

The PROGRAM RESUME (30h) command must be issued to exit a program suspend mode and resume a PROGRAM operation. The host can use DQ7 or DQ6 status bits to determine the status of the PROGRAM operation. After a PROGRAM RESUME command is issued, subsequent PROGRAM RESUME commands are ignored. Another PROGRAM SUSPEND command can be issued after the device has resumed programming.

6.14 CHIP ERASE OPERATION

Chip Erase (80/10h) is a six-bus cycle operation. These commands invoke the Embedded Erase algorithm, which does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory to an all zero data pattern prior to electrical erase. After a successful chip erase, all locations of the chip contain FFFFh, except for any protected sectors. The system is not required to provide any controls or timings during these operations.

Protected sectors are not erased. If all sectors are protected, the data remains unchanged. No error is reported when protected sectors are not erased.

When the Embedded Erase algorithm is complete, that sector returns to the read mode and addresses are no longer latched.

Any commands including suspend command written during the chip erase operation are ignored.

However, note that a hardware reset or powering down the device immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that sector has returned to reading array data, to ensure the entire array is properly erased.

6.15 SECTOR ERASE OPERATION

Sector Erase (80/30h) is a six bus cycle operation. The sector erase command sequence is initiated by writing two un-lock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, with the sector erase command. The Command Definitions table shows the address and data requirements for the sector erase command sequence.

During the period specified by the sector erase timeout parameter, additional sector addresses and SECTOR ERASE commands can be written. Any command except SECTOR ERASE or SECTOR SUSPEND during this timeout period resets the device to the read mode. The system can monitor DQ3 to determine if the sector erase timer has timed out.

After the program/erase controller has started, it is not possible to select any more sectors. Each additional sector must therefore be selected within the timeout period of the last sector. The timeout timer restarts when an additional sector is selected.

After the sixth bus WRITE operation, a bus READ operation outputs the data polling register. If an error occurs, READ/RESET command must be issued to reset the error condition and return to read mode.

When the Embedded Erase algorithm is completed, the device returns to reading array data and addresses are no longer latched.

6.16 SECTOR ERASE SUSPEND OPERATION

The SECTOR ERASE SUSPEND (B0h) command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erase. One bus WRITE operation is required to issue the command. The sector address is "Don't Care." The Suspend command is ignored if written during the chip erase operation.

When the SECTOR ERASE SUSPEND command is written during the sector erase operation, the device requires erase suspend latency time of the ERASE SUSPEND command being issued to suspend the erase operation.

However, when the ERASE SUSPEND command is written during the sector erase timeout, the device immediately terminates the timeout period and suspends the ERASE operation.

If the ERASE SUSPEND operation is aborted by performing a device hardware reset or power-down, data integrity cannot be ensured, and it is recommended that the suspended sectors be erased again.

After the program/erase controller has stopped, the device enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure.

During erase-suspend-read mode, it is possible to execute below operations:

- READ (main memory array)
- PROGRAM
- WRITE BUFFER LOAD
- AUTO SELECT
- READ CFI
- UNLOCK BYPASS
- Secured Silicon Region commands
- READ/RESET

Reading from a suspended sector will output the data polling register. If an attempt is made to program in a protected or suspended sector, the PROGRAM command is ignored and the data remains unchanged; also, the data polling register is not read and no error condition is given.

Before the RESUME command is initiated, the READ/RESET command must be issued to exit AUTO SELECT and READ CFI operations. In addition, the EXIT UNLOCK BYPASS and EXIT Secured Silicon Region commands must be issued to exit unlock bypass mode and the Secured Silicon Region mode.

6.17 SECTOR ERASE RESUME OPERATION

To resume the sector erase operation from erase-suspend-read mode, the system must write SECTOR ERASE RESUME (30h).

The device must be in read mode before the RESUME command will be accepted.

An erase can be suspended and resumed more than once.

6.18 BLANK CHECK OPERATION

The BLANK CHECK operation will confirm if a selected sector is currently erased.

Two commands are required to execute a BLANK CHECK operation: BLANK CHECK SETUP (EBh/76h) and BLANK CHECK CONFIRM AND READ (29h).

It can also be used to determine whether a previous ERASE operation was successful, including ERASE operations that might have been interrupted by power loss.

If it finds any bit not erased, the device will halt the operation and report the results. A READ/RESET command must be issued to reset the error condition and return the device to read mode.

If it returns a passing status, the sector is guaranteed blank (all 1s) and is ready to program.

After the BLANK CHECK operation has completed, the device returns to read mode unless an error has occurred.

Before executing, the ERASE operation initiates an embedded BLANK CHECK operation, and if the target sector is blank, the ERASE operation is skipped, benefitting overall cycle performance; otherwise, the ERASE operation continues.

The BLANK CHECK operation can occur in only one sector at a time, and during its execution, reading the data polling register is the only other operation allowed. Reading from any address in the device enables reading the data polling register to monitor blank check progress or errors. Operations such as READ (array data), PROGRAM, ERASE, and any suspended operation are not allowed.

7. STATUS REGISTER

Table 7.1. Status Register Bit Definitions

Bit	Name	Setting	Description	Notes
DQ15:DQ8	EIP	All 0 = Erase in Progress, All 1 = No Erase in Progress	Indicates Erase in progress for x16 device.	8
DQ7	Data polling bit	0 or 1, depending on operations	Monitors whether the program/erase controller has successfully completed its operation, or has responded to an ERASE SUSPEND operation.	2, 3, 4
DQ6	Toggle bit	Toggles: 0 to 1; 1 to 0; and so on	Monitors whether the program/erase controller has successfully completed its operations, or has responded to an ERASE SUSPEND operation. During a PROGRAM/ERASE operation, DQ6 toggles from 0 to 1, 1 to 0, and so on, with each successive READ operation from any address.	3, 4, 5
DQ5	Error bit	0 = Success 1 = Failure	Identifies errors detected by the program/erase controller. DQ5 is set to 1 when a PROGRAM, SECTOR ERASE, or CHIP ERASE operation fails to write the correct data to the memory, or when a BLANK CHECK operation fails.	4, 6
DQ3	Erase timer bit	0 = Erase not in progress 1 = Erase in progress	Identifies the start of program/erase controller operation during a SECTOR ERASE command. Before the program/erase controller starts, this bit set to 0, and additional sectors to be erased can be written to the command interface.	4
DQ2	Alternative toggle bit	Toggles: 0 to 1; 1 to 0; and so on	Monitors the program/erase controller during ERASE operations. During CHIP ERASE, SECTOR ERASE, and ERASE SUSPEND operations, DQ2 toggles from 0 to 1, 1 to 0, and so on, with each successive READ operation from addresses within the sectors being erased.	3, 4, 7
DQ1	Buffered program abort bit	1 = Abort	Indicates a BUFFER PROGRAM operation abort. The BUFFERED PROGRAM ABORT and RESET command must be issued to return the device to read mode.	

Notes:

1. The status register can be read during PROGRAM, ERASE, or ERASE SUSPEND operations; the READ operation outputs data on DQ [7:0].
2. For a PROGRAM operation in progress, DQ7 outputs the complement of the bit being programmed. For a READ operation from the address previously programmed successfully, DQ7 outputs existing DQ7 data. For a READ operation from addresses with sectors to be erased while an SECTOR ERASE SUSPEND operation, DQ7 outputs 1. For an ERASE or BLANK CHECK operation in progress, DQ7 outputs 0; upon either operation's successful completion, DQ7 outputs 1.
3. After successful completion of a PROGRAM, ERASE, or BLANK CHECK operation, the device returns to read mode.
4. During SECTOR ERASE SUSPEND mode, READ operations to address within sectors not being erased output memory array data as if in read mode. A protected sector is treated the same as a sector not being erased.
5. During SECTOR ERASE SUSPEND, DQ6 toggles when addressing a cell within a sector being erased. The toggling stops when the program/erase controller has suspended the SECTOR ERASE operation.
6. When DQ5 is set to 1, a READ/RESET command must be issued before any subsequent command.
7. DQ2 toggles for an actively erasing sector during SECTOR ERASE operation.
8. DQ [15:8] are supported in x16 only. DQ15 through DQ8 are 0 during erase operation, and 1 after completion of erase operation.

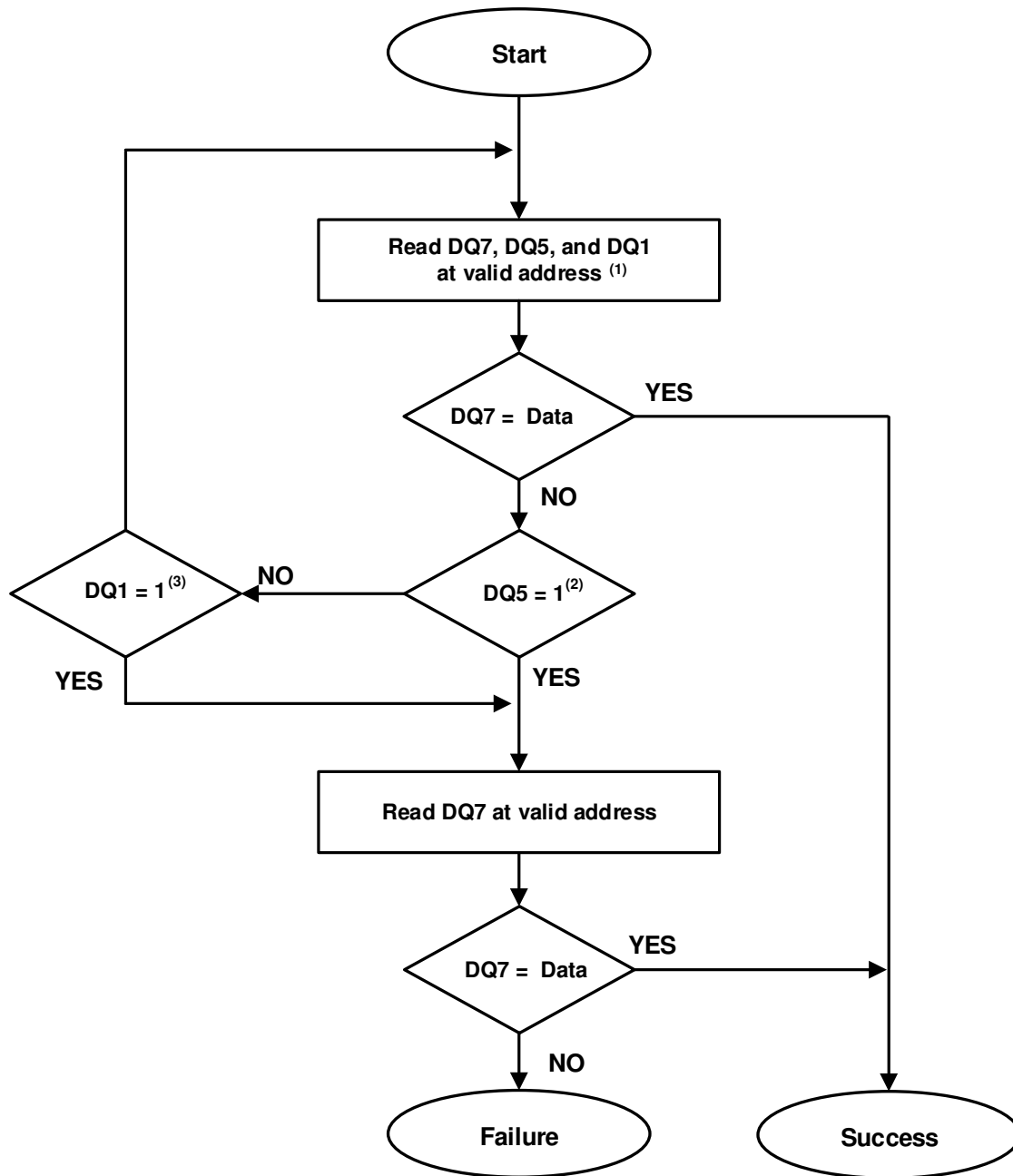
Table 7.2. Operations and Corresponding Bit Settings

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	DQ1	RY/BY#	Notes
PROGRAM	Any address	DQ7#	Toggle	0	-	-	0	0	2
BLANK CHECK	Any address	0	Toggle	0	-	-	0	0	
CHIP ERASE	Any address	0	Toggle	0	1	Toggle	-	0	
SECTOR ERASE before time-out	Erasing sector	0	Toggle	0	0	Toggle	-	0	
	Non-erasing sector	0	Toggle	0	0	No Toggle	-	0	
SECTOR ERASE	Erasing sector	0	Toggle	0	1	Toggle	-	0	3
	Non-erasing sector	0	Toggle	0	1	No Toggle	-	0	
PROGRAM SUSPEND	Programming sector	Invalid operation						High-Z	
	Non-programming sector	Outputs memory array data as if in read mode						High-Z	
SECTOR ERASE SUSPEND	Erasing blk	1	No Toggle	0	-	Toggle	-	High-Z	
	Non-erasing blk	Outputs memory array data as if in read mode						High-Z	
PROGRAM during SECTOR ERASE SUSPEND	Erasing sector	DQ7#	Toggle	0	-	Toggle	-	0	2
	Non-erasing sector	DQ7#	Toggle	0	-	No Toggle	-	0	2
BUFFERED PROGRAM ABORT	Any address	DQ7#	Toggle	0	-	-	1	0	
PROGRAM Error	Any address	DQ7#	Toggle	1	-	-	-	0	2
ERASE Error	Erase success sector	0	Toggle	1	1	No Toggle	-	0	
	Erase fail sector	0	Toggle	1	1	Toggle	-	0	
BLANK CHECK Error	Any address	0	Toggle	1	1	Toggle	-	0	

Notes:

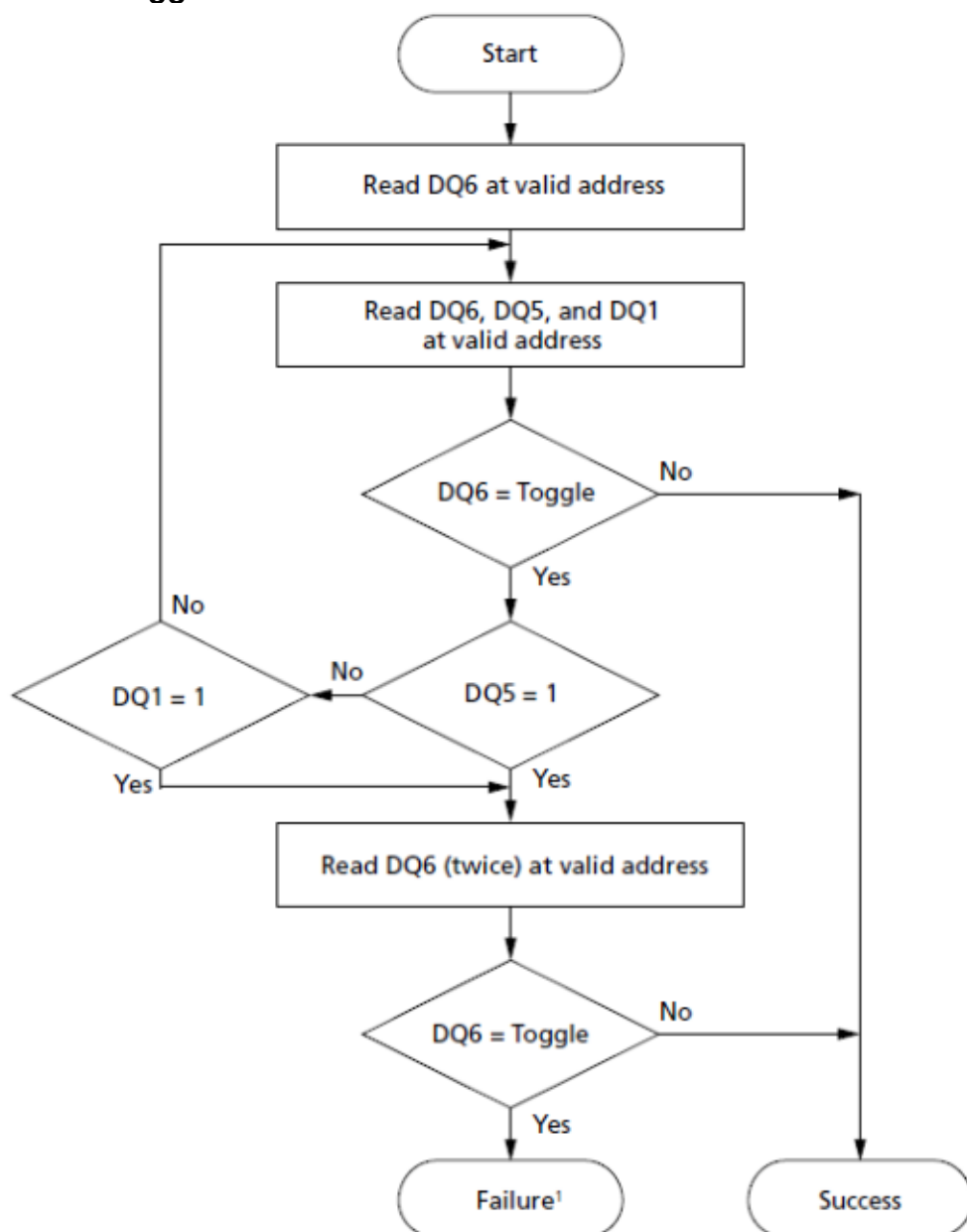
1. Unspecified data bits should be ignored.
2. DQ7# for buffer program is related to the last address location loaded.
3. DQ2 toggles only for actively erasing sector during SECTOR ERASE operation.

Figure 7.1. Data Polling Flowchart

**Notes:**

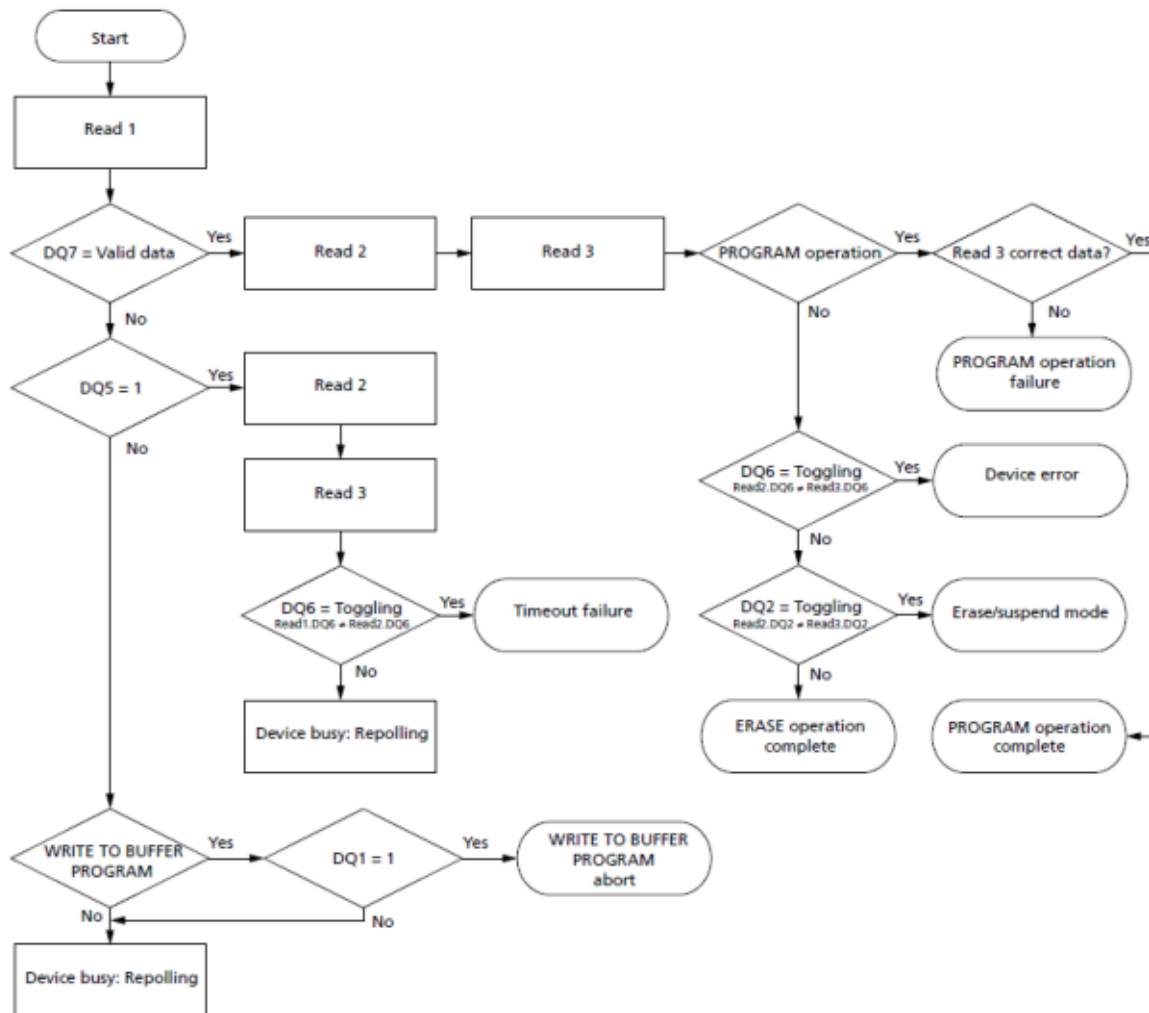
1. Valid address is the address being programmed or an address within the sector being erased.
2. Failure results: DQ5 = 1 indicates an operation error.
3. DQ1 = 1 indicates a WRITE BUFFER PROGRAM ABORT operation.

Figure 7.2. Toggle Bit Flowchart

**Note:**

1. Failure results: DQ5 = 1 indicates an operation error; DQ1 = 1 indicates a BUFFER PROGRAM ABORT operation.

Figure 7.3. Status Register Polling Flowchart



8. PROTECTION

8.1 Device Protection Methods

8.1.1 Low V_{CC} Write Inhibit

When V_{CC} is less than VLKO (Lock-Out Voltage), the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down.

The command register and all internal program/erase circuits are disabled, and the device resets to reading array data. Subsequent writes are ignored until V_{CC} is greater than VLKO. The system must provide the proper signals to the control inputs to prevent unintentional writes when V_{CC} is greater than VLKO.

8.1.2 Power-Up Write Inhibit

If WE# = CE# = RESET# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

8.2 Sector Protection Methods

8.2.1 WP#/ACC Method

The WP#/ACC function provides a hardware method of protecting either the highest/lowest sector or the top/bottom two sectors. When WP#/ACC is LOW, PROGRAM/ERASE operations on either of these sector options is ignored to provide protection.

When WP#/ACC is HIGH, either the highest/lowest sector or the top/bottom two sectors are not protected from PROGRAM/ERASE operations. WP#/ACC has an internal pull-up; when unconnected, WP#/ACC is at V_{IH}. WP#/ACC should not change between V_{IL} and V_{IH} during any embedded operation.

8.2.2 Advanced Sector Protection

Advanced Sector Protection (ASP) is a set of protection methods used to disable or enable programming or erase operations, individually, in any or all sectors.

Every sector has a non-volatile (PPB) and a volatile (DYB) protection bit associated with it.

As for PPB bits, they are protected when PPB Lock bit is "0". There are two methods for managing the state of the PPB Lock bit; Persistent Lock and Password Lock.

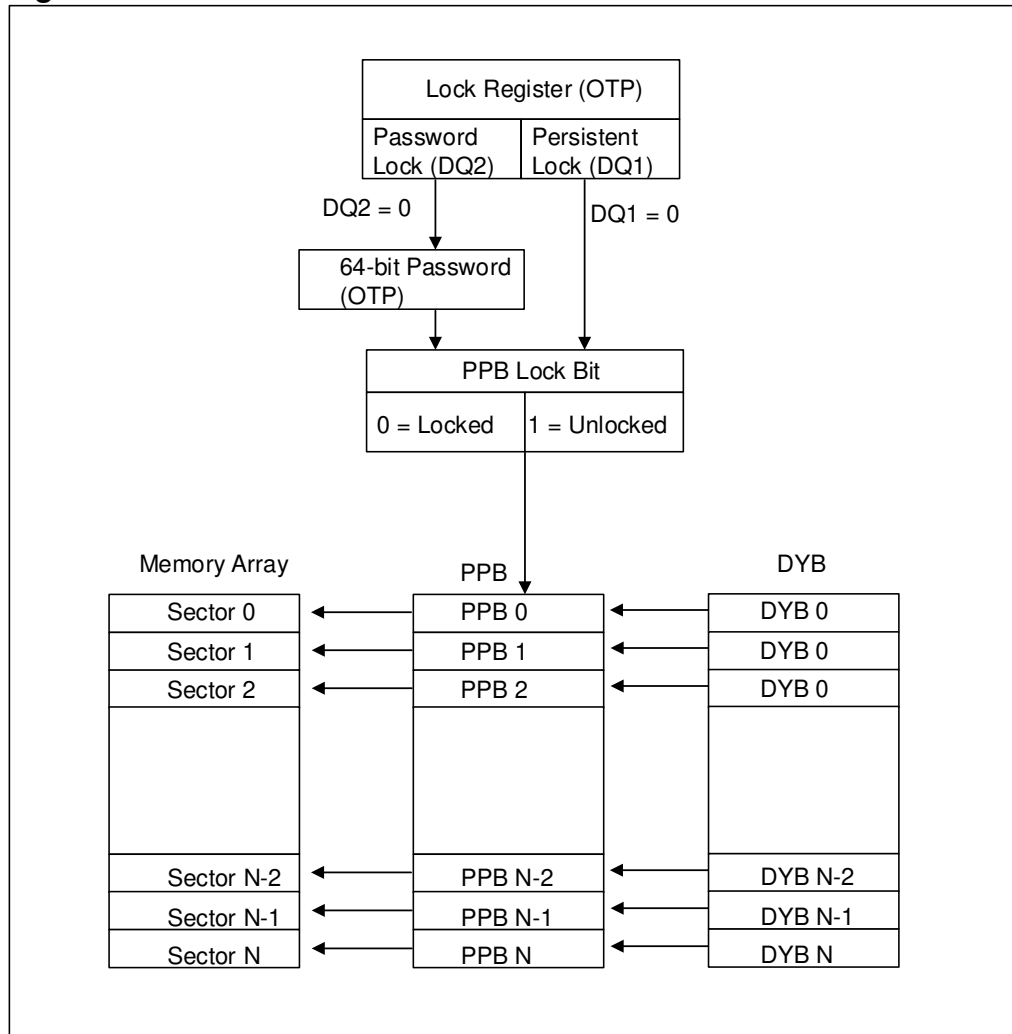
The selection of method for managing the state of PPB Lock bit is made by programming OTP bits in the Lock Register.

The Persistent Lock method sets the PPB Lock bit to 1 during POR or Hardware Reset, so PPB bits are unlocked by a device reset. In Persistent Lock mode, there is a command to set the PPB Lock bit to "0", but no command to clear to "1", so PPB Lock bit remains 0 until the next power-off or hardware reset.

The Password Lock method sets the PPB Lock bit to "0" during POR or Hardware Reset to protect all PPB bits. A command together with correct 64-bit password must be used to clear PPB Lock bit to "1".

Sectors with DYB and PPB protection can coexist within the memory array. If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode.

The sector protection status can be read by performing a read electronic signature or by issuing an AUTO SELECT command.

Figure 8.1. Advanced Sector Protection


8.3 Dynamic Protection Bits

Dynamic Protection Bits are volatile and unique for each sector and can be individually modified. DYBs only control the protection scheme for unprotected sectors that have their PPBs erased to “1”. By issuing the DYB Set or Clear command sequences, the DYBs are set to “0” or cleared to “1”, thus placing each sector in the protected or unprotected state respectively. This feature allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed.

Notes

1. The DYBs are programmed or cleared individually. When the parts are first shipped from the factory, the all DYBs are set to “1” (Unprotected).
2. If all DYBs are cleared to “1” after power up, then the sectors may be modified if PPB of that sector is also cleared to “1”.
3. It is possible to have sectors that are persistently locked with sectors that are left in the dynamic state.
4. The DYB Set or Clear commands for the dynamic sectors signify protected or unprotected state of the sectors respectively. However, if there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock Bit must be cleared by either putting the device through a power-cycle, or hardware reset. The PPBs can then be changed to reflect the desired settings. Setting the PPB Lock Bit once again locks the PPBs, and the device operates normally again.
5. To achieve the best protection, it is recommended to execute the PPB Lock Bit Set command early in the boot code and protect the boot code by holding $WP\#/ACC = V_{IL}$.
Note that the PPB and DYB bits have the same function when $WP\#/ACC = V_{HH}$ as they do when $WP\#/ACC = V_{IH}$.

8.4 Persistent Protection Bits

The Persistent Protection Bits are unique for each sector and nonvolatile. It has the same endurance as the Flash memory. Preprogramming and verification prior to erasure are handled by the device, and therefore do not require system monitoring. There is a command to set the PPB Lock bit to 0 to protect the PPB. However, there is no command in the Persistent Protection method to clear the PPB Lock bit to 1 therefore the PPB Lock bit will remain at 0 until the next power up or reset.

Notes

1. Each PPB is individually programmed individually, but cleared collectively. When the parts are first shipped from the factory, the all PPBs are set to “1” (Unprotected).
2. While programming PPB and data polling on programming PPB address, array data cannot be read from any sectors.
3. Entry command disables reads and writes for all sectors.
4. Reads within that sector return the PPB status for that sector.
5. If the PPB Lock Bit is set to “0”, the PPB Program or erase command does not execute and times-out without programming or erasing the PPB.
6. Exit command must be issued after the execution which resets the device to read mode and re-enables reads and writes for all sectors.

8.5 Lock Register

Host can choose the method for managing the state of PPB Lock bit via setting Lock Register bits as DQ1 and DQ2. Lock Register is an OTP bits. Once programming either DQ2 or DQ1, they will be locked in that mode permanently.

Table 8.1. Lock Register Bit Definitions

Bit	Name	Settings	Description
DQ15-3	Reserved	1	Reserved
DQ2	Password lock bit	0 = Password Lock mode enabled with persistent Lock mode disabled. 1 = Password Lock mode disabled (Default)	The device will be permanently in Password Lock mode.
DQ1	Persistent lock bit	0 = Persistent Lock mode disabled with Password Lock mode disabled 1 = Persistent Lock mode enabled (Default)	The device will be permanently in Persistent Lock mode. When shipped from the factory, the device is in Persistent Lock mode.
DQ0	Secured Silicon Region protection bit	0 = Protected 1 = Unprotected (Default)	If the device is shipped with the Secured Silicon Region unlocked, the sector can be protected by setting this bit to 0. The Secured Silicon Region protection status can be read in auto select mode by issuing an AUTO SELECT command.

Notes:

1. The password lock bit (DQ2) and persistent lock bit (DQ1) cannot both be programmed to 0. Any attempt to program one while the other is programmed causes the operation to abort, and the device returns to read mode. The device is shipped from the factory with the default setting.

8.6 PPB Lock Bit

The PPB Lock Bit is a global volatile bit for all sectors. When set (programmed to “0”), it locks all PPBs and when cleared (erased to “1”), allows the PPBs to be changed. There is only one PPB Lock Bit per device.

The PPB Lock command is used to set to 0.

There are two methods for managing the state of the PPB Lock bit, Persistent Lock Mode and Password Lock mode.

Notes

1. No software command sequence to clear this bit, but only a hardware reset or a power-up clears this bit.
2. The PPB Lock Bit must be set (programmed to “0”) only after all PPBs are configured to the desired settings.

8.7 Persistent Lock mode

The Persistent Lock Mode clears the PPB Lock bit to “1” during POR or Hardware Reset so that all PPB bits are unprotected by a device reset. The PPB Lock command is used to set PPB Lock bit to 0, but there is no command to clear PPB Lock bit to 1, so PPB Lock bit will remain at 0 until the next power-off or Hardware reset.

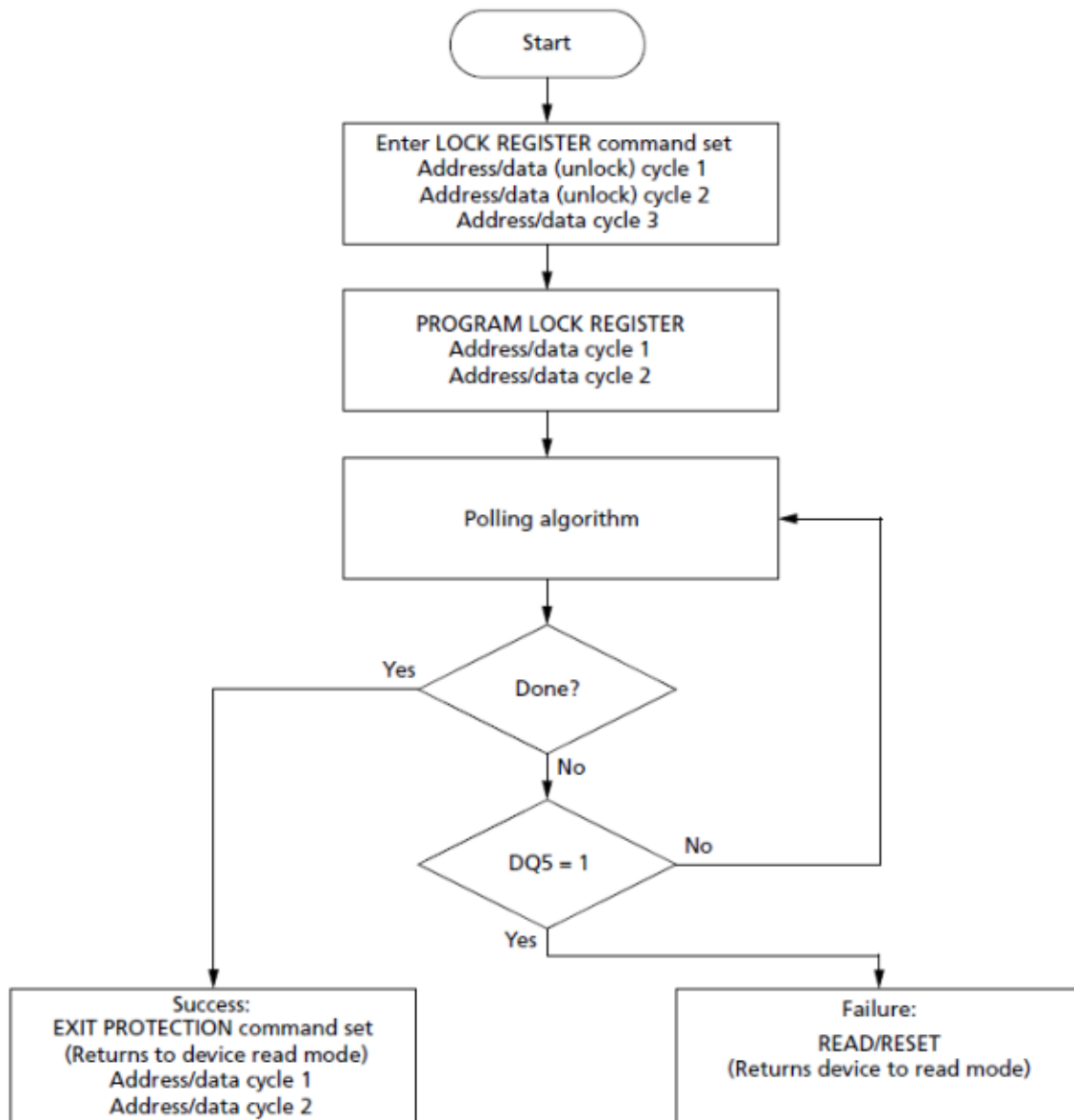
8.8 Password Lock mode

The Password Lock Mode allows an even higher level of security than the Persistent Sector Protection Mode by requiring a 64-bit password for unlocking the device PPB Lock Bit. In addition to this password requirement, after power up and reset, the PPB Lock Bit is set “0” to maintain the password mode of operation. Successful execution of the Password Unlock command by entering the entire password clears the PPB Lock Bit, allowing for sector PPBs modifications.

Notes

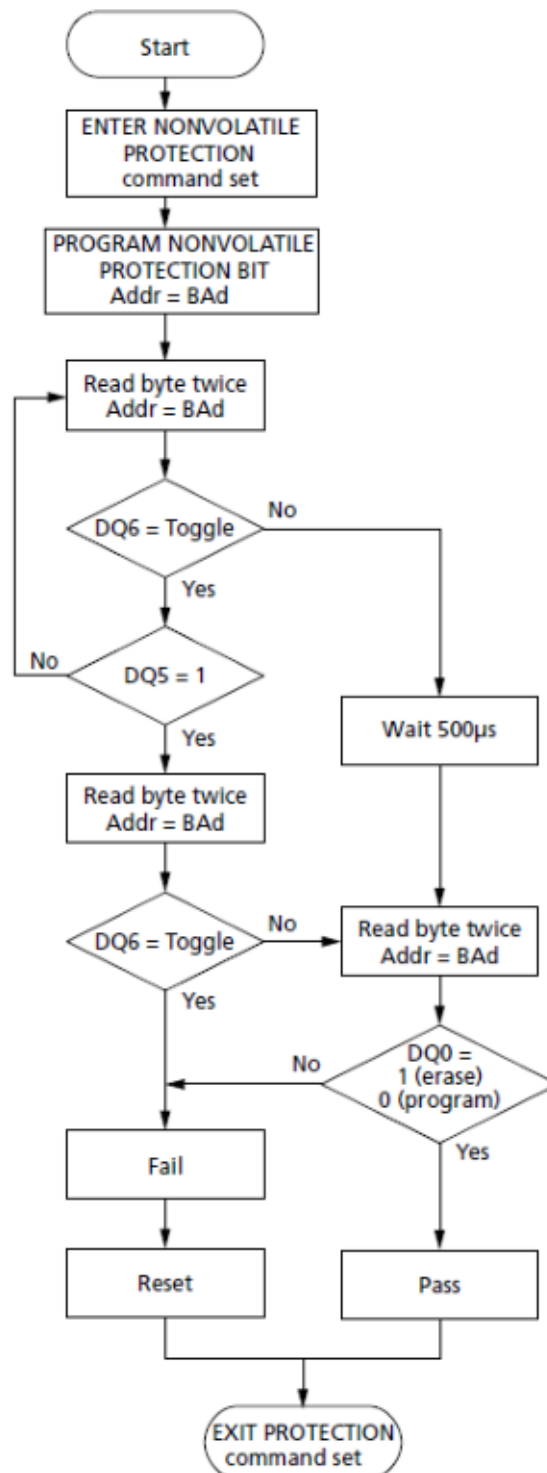
1. The Password Program Command is only capable of programming 0's.
2. The password is all 1's when shipped from factory. It is located in its own memory space and is accessible through the use of the Password Program and Password Read commands.
3. All 64-bit password combinations are valid as a password.
4. Once the Password is programmed and verified, the Password Lock mode bit must be set in order to prevent reading or modification of the password.
5. The Password Lock mode bit, once programmed, prevents reading the 64-bit password on the data bus and further password programming. All further program and read commands to the password region are disabled (data is read as 1's) and these commands are ignored. There is no means to verify what the password is after the Password Lock mode bit is programmed. Password verification is only allowed before selecting the Password Lock mode.
6. The Password Mode Lock bit is not erasable.
7. The exact password must be entered in order for the unlocking function to occur.
8. The addresses can be loaded in any order but all 4 words are required for a successful match to occur.
9. If the password is lost after setting the Password Lock mode bit, there is no way to clear the PPB Lock.

Figure 8.2. Lock Register Program Flowchart

**Notes:**

1. Each lock register bit can be programmed only one.

Figure 8.3 PPB Program/Erase Algorithm



8.9 Sector Protection Command Definitions

Table 8.4. Sector Protection Command Definitions

Command	Bus Size	Address and Data Cycles											Notes
		1st		2nd		3rd		4th		...	nth		
		A	D	A	D	A	D	A	D		A	D	
LOCK REGISTER Commands													
ENTER LOCK REGISTER COMMAND SET (40h)	X8	AAA	AA	555	55	AAA	40						3
	X16	555		2AA		555							
PROGRAM LOCK REGISTER (A0h)	X8	X	A0	X	Data							5	
	X16												
READ LOCK REGISTER	X8	X	Data									4, 5, 6	
	X16												
EXIT LOCK REGISTER (90h/00h)	X8	X	90	X	00							3	
	X16												
PASSWORD LOCK MODE Commands													
ENTER PASSWORD LOCK MODE COMMAND SET (60h)	X8	AAA	AA	555	55	AAA	60						3
	X16	555	AA	2AA	55	555							
PROGRAM PASSWORD (A0h)	X8	X	A0	PWA _n	PWD _n							7	
	X16												
READ PASSWORD	X8	00	PWD ₀	01	PWD ₁	02	PWD ₂	03	PWD ₃	...	07	PWD ₇	4, 6, 8, 9
	X16	00	PWD ₀	01	PWD ₁	02	PWD ₂	03	PWD ₃				
UNLOCK PASSWORD (25h/03h)	X8	00	25	00	03	00	PWD ₀	01	PWD ₁	...	00	29	8, 10
	X16												
EXIT PASSWORD LOCK MODE (90h/00h)	X8	X	90	X	00							3	
	X16												

Table 8.4. Sector Protection Command Definitions (Continued)

Command	Bus Size	Address and Data Cycles											Notes
		1st		2nd		3rd		4th		...	nth		
		A	D	A	D	A	D	A	D		A	D	
PPB Commands													
ENTER PPB (C0h)	X8	AAA	AA	555	55	AAA	C0						3
	X16	555		2AA		555							
PROGRAM PPB (A0h)	X8	X	A0	BAd	00						11		
	X16												
READ PPB STATUS	X8	BAd	READ (DQ0)								4, 6, 11		
	X16												
CLEAR ALL PPBs (80h/30h)	X8	X	80	00	30								
	X16												
EXIT PPB (90h/00h)	X8	X	90	X	00						3		
	X16												
PERSISTENT LOCK MODE Commands													
ENTER PERSISTENT LOCK MODE (50h)	X8	AAA	AA	555	55	AAA	50						3
	X16	555		2AA		555							
PROGRAM PERSISTENT LOCK BIT (A0h)	X8	X	A0	X	00						11		
	X16												
READ PERSISTENT LOCK BIT STATUS	X8	X	READ (DQ0)								4, 6, 11		
	X16												
EXIT PERSISTENT LOCK MODE (90h/00h)	X8	X	90	X	00						3		
	X16												

Table 8.4. Sector Protection Command Definitions (Continued)

Command	Bus Size	Address and Data Cycles											Notes
		1st		2nd		3rd		4th		...	nth		
		A	D	A	D	A	D	A	D		A	D	
DYB Commands													
ENTER DYB (E0h)	X8	AAA	AA	555	55	AAA	E0						3
	X16	555		2AA		555							
PROGRAM DYB (A0h)	X8	X	A0	BAd	00						11		
	X16												
READ DYB STATUS	X8	BAd	READ (DQ0)								4, 6, 12		
	X16												
CLEAR DYB (A0h)	X8	X	A0	BAd	01						11		
	X16												
EXIT DYB (90h/00h)	X8	X	90	X	00						3		
	X16												
Secured Silicon Region Operations													
ENTER Secured Silicon Region (88h)	X8	AAA	AA	555	55	AAA	88						
	X16	555		2AA		555							
PROGRAM Secured Silicon Region (A0h)	X8	AAA	AA	555	55	AAA	A0	Word address	data				
	X16	555		2AA		555							
READ Secured Silicon Region	X8	Word addresses	data										
	X16												
EXIT Secured Silicon Region (90h/00h)	X8	AAA	AA	555	55	555	90	X	00				
	X16	555		2AA									

Notes:

- Key: A = Address and D = Data; X = "Don't Care; BAd = Any address in the sector; PWDn = Password bytes, n = 0 to 7 (x8)/ words 0 to 3 (x16); PWA_n = Password address, n = 0 to 3(x16); Gray = Not applicable. All values in the table are hexadecimal.
- DQ[15:8] are "Don't Care" during UNLOCK and COMMAND cycles. A[_{MAX}:16] are "Don't Care" during UNLOCK and COMMAND cycles, unless an address is required

3. The ENTER command sequence must be issued prior to any operation. It disables READ and WRITE operations from and to all sectors in the main array. Also, when an ENTER COMMAND SET command is issued, an EXIT COMMAND SET command must be issued to return the device to READ mode.
4. READ REGISTER/PASSWORD commands have no command code; CE# and OE# are driven LOW and data is read according to a specified address.
5. Data = Lock Register content
6. All address cycles shown for this command are READ cycles
7. Only one portion of the password can be entered or read in any order as long as the entire 64-bit password is entered or read.
8. Each portion of the password can be entered or read in any order as long as the entire 64-bit password is entered or read.
9. For the x8 READ PASSWORD command, the nth (and final) address cycle equals the 8th address cycle. From the 5th to the 8th address cycle, the values for each address and data pair continue the pattern shown in the table as follows: for x8, address and data = 04 and PWD4; 05 and PWD5; 06 and PWD6; 07 and PWD7.
10. For the x8 UNLOCK PASSWORD command, the nth (and final) address cycle equals the 11th address cycle. From the 5th to the 10th address cycle, the values for each address and data pair continue the pattern shown in the table as follows: address and data = 02 and PWD2; 03 and PWD3; 04 and PWD4; 05 and PWD5; 06 and PWD6; 07 and PWD7.

For x16 UNLOCK PASSWORD command, the nth (and final) address cycle equals the 7th address cycle. For the 5th and 6th address cycles, the values for the address and data pair continue the pattern shown in the table as follows: address and data = 02 and PWD2; 03 and PWD3.

11. Both PPB and DYB settings are as follows: Protected state = 00; Unprotected state = 01.
12. DYB read status also includes WP#/ACC=L effect.

9. Secured Silicon Region Command Sequence

The device has one extra 128-word Secured Silicon Region (SSR) that can be accessed only by the ENTER Secured Silicon Region (88h) command. The Secured Silicon Region is 128 words (x16) or 256 bytes (x8). It is used as a security sector to provide a permanent 128-bit security identification number or to store additional information. The device can be shipped with the Secured Silicon Region prelocked permanently by ISSI, including 128-bit security identification number. Or, the device can be shipped with the Secured Silicon Region unlocked, enabling customers to permanently program and lock it.

After the ENTER SECURED SILICON REGION command has been issued, the device enters the Secured Silicon Region mode. All bus READ or PROGRAM operations are conducted on the Secured Silicon Region, and the Secured Silicon Region is addressed using the address occupied by the sector 0 in other operating modes.

In Secured Silicon Region mode, ERASE, CHIP ERASE, CHIP ERASE SUSPEND, and ERASE RESUME commands are not allowed. The Secured Silicon Region cannot be erased, and each bit of the Secured Silicon Region can only be programmed once.

The Secured Silicon Region is protected from further modification by programming lock register bit 0. Once invoked, this protection cannot be undone.

The device remains in Secured Silicon Region mode until EXIT PROTECTION COMMAND SET (90/00h) command is issued, which returns the device to read mode, or until power is removed from the device. After a power-up sequence or hardware reset, the device will revert to reading memory sectors in the main array.

Table 9.1. Secured Silicon Region Address and Data

Address			Data	
X8	X16	ISSI prelocked	Customer Lockable	
000000h-00000Fh	000000h-000007h	Secure ID number	Determined by customer	Secure ID number
000010h-0000FFh	000008h-00007Fh	Protected and unavailable		Determined by customer

10. COMMON FLASH INTERFACE (CFI)

The common flash interface (CFI) specification outlines device and host systems software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the READ CFI QUERY command is issued, and the data structure is read from memory. The following tables show the address (A-1, A [7:0]) used to retrieve the data. The query data is always presented on the lowest order data outputs (DQ [7:0]), and the other data outputs (DQ [15:8]) are set to 0.

Table 10.1. Query Structure Overview

Addresses		Subsection Name	Description
X16	X8		
10h	20h	CFI query identification string	Command set ID and algorithm data offset
1Bh	36h	System Interface information	Device timing and voltage information
27h	4Eh	Device geometry definition	Flash device layout
40h	80h	Primary algorithm-specific extended query table	Additional information specific to the primary algorithm (optional)

Note: Query data are always presented on the lowest order data outputs (DQ [7:0]). DQ [15:8] are set to 0.

Table 10.2. CFI Query Identification String

Addresses		Data	Description
X16	X8		
10h	20h	0051h	Query Unique ASCII string "QRY"
11h	22h	0052h	
12h	24h	0059h	
13h	26h	0002h	Primary algorithm command set and control interface ID code 16-bit ID code defining a specific algorithm
14h	28h	0000h	
15h	2Ah	0040h	Address for primary algorithm extended query table
16h	2Ch	0000h	
17h	2Eh	0000h	Alternate vendor command set and control interface ID code second vendor-specified algorithm supported
18h	30h	0000h	
19h	32h	0000h	Address for Alternate algorithm extended query table
1Ah	34h	0000h	

Note: Query data are always presented on the lowest order data outputs (DQ [7:0]). DQ [15:8] are set to 0.

Table 10.3. System Interface String

Addresses		Data	Description	Value
X16	X8			
1Bh	36h	0027h	V _{CC} Min (write/erase) DQ7-DQ4: volt, DQ3-DQ0: 100mV	2.7V
1Ch	38h	0036h	V _{CC} Max (write/erase) DQ7-DQ4: volt, DQ3-DQ0: 100mV	3.6V
1Dh	3Ah	0095h	V _{HH} Min voltage (00h = no V _{pp} pin present)	9.5V
1Eh	3Ch	00A5h	V _{HH} Max voltage (00h = no V _{pp} pin present)	10.5V
1Fh	3Eh	0004h	Typical timeout per single byte/word write 2 ^N μ s	16us
20h	40h	000Ah	Typical timeout for min size buffer write 2 ^N μ s (00h = not supported)	1024us
21h	42h	0009h	Typical timeout per individual sector erase 2 ^N ms	0.5s
22h	44h	000Fh	Typical timeout for full chip erase 2 ^N ms (00h = not supported)	32Mb:33s
		0010h		64Mb:66s
23h	46h	0004h	Max timeout for byte/word write 2 ^N times typical	256us
24h	48h	0002h	Max timeout for buffer write 2 ^N times typical	4096us
25h	4Ah	0003h	Max timeout per individual sector erase 2 ^N times typical	4s
26h	4Ch	0002h	Max timeout for full chip erase 2 ^N times typical (00h = not supported)	32Mb:131s
		0002h		64Mb:262s

Table 10.4. Device Geometry Definition

Addresses		Data	Description	Value
X16	X8			
27h	4Eh	0016h 0017h	Device Size = 2 ^N bytes, 0016h for 32Mb	4MB 8MB
28h 29h	50h 52h	0002h 0000h	Flash Device Interface Description 01h = X16 only; 02h = x8/x16	X8, x16 as- ynchronous
2Ah 2Bh	54h 56h	0008h ⁽¹⁾ 0000h	Max number of bytes in multi-byte program or page = 2 ^N (00h = not supported)	256
2Ch	58h	See table below	Number of Erase Sector Regions. It specifies the number of regions containing contiguous sectors of the same size. 01h = Uniform device, 02h = Boot device	-
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	See table below	Erase Sector Region 1 Information Bits[15:0] = y, y+1 = Number of identical-size erase sectors Bits[31:16] = z, sector size in region 1 is z x 256 bytes	-
31h 32h 33h 34h	62h 64h 66h 68h	See table below	Erase Sector Region 2 Information Bits[15:0] = y, y+1 = Number of identical-size erase sectors Bits[31:16] = z, sector size in region 1 is z x 256 bytes	-
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0000h 0000h	Erase Sector Region 3 Information	-
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase Sector Region 3 Information	-

Note: The value at 2Ah in the CFI region is set to 08h (256 bytes) due to compatibility issues. The maximum 256-word program buffer can be used to optimize system program performance.

Table 10.5. Erase Sector Region Information

Address	32Mb			64Mb		
	Top	Bottom	Uniform	Top	Bottom	Uniform
2Ch	02h	02h	01h	02h	02h	01h
2Dh	07h	07h	3Fh	07h	07h	7Fh
2Eh	00h	00h	00h	00h	00h	00h
2Fh	20h	20h	00h	20h	20h	00h
30h	00h	00h	01h	00h	00h	01h
31h	3Eh	3Eh	00h	7Eh	7Eh	00h
32h	00h	00h	00h	00h	00h	00h
33h	00h	00h	00h	00h	00h	00h
34h	01h	01h	00h	01h	01h	00h

Table 10.6. Primary Algorithm-specific Extended Query

Addresses		Data	Description	Value
X16	X8			
40h	80h	0050h	Primary algorithm extended query table unique ASCII string "PRI"	"P"
41h	82h	0052h		"R"
42h	84h	0049h		"I"
43h	86h	0031h	Major version number, ASCII	"1"
44h	88h	0033h	Minor version number, ASCII	"3"
45h	8Ah	0100h	Address Sensitive Unlock (bits [1:0]) 00 = Required, 01 = Not Required Silicon revision number (bits [5:2]) 0001 = 0.18um, 0010 = 0.13um, 0011 = 90nm, 0100 = 65nm	Required
46h	8Ch	0002h	Erase Suspend: 00 = Not Supported, 01 = To Read Only, 02 = To Read & Write	2
47h	8Eh	0001h	Sector Protection: 00 = Not Supported, X = Minimum number of sectors per group	1
48h	90h	0000h	Temporary sector unprotect: 00 = Not Supported, 01 = Supported	Not supported
49h	92h	0008h	Sector Protect/Unprotect: 08 = Advanced sector Protection	8
4Ah	94h	0000h	Simultaneous operations: 00 = Not Supported	Not supported
4Bh	96h	0000h	Burst mode: 00 = Not Supported	Not supported
4Ch	98h	0002h	Page Mode : 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page 03 = 16 Word Page	8 Word Page
4Dh	9Ah	0095h	V _{HH} supply minimum program/erase voltage: Bits [7:4] hex value in volts, Bits [3:0] BCD value in 100mV.	9.5V
4Eh	9Ch	00A5h	V _{HH} supply maximum program/erase voltage: Bits [7:4] hex value in volts, Bits [3:0] BCD value in 100mV.	10.5V
4Fh	9Eh	00xxh	Top/Bottom boot sector flag: xx = 02h: Bottom boot device, HW protection for bottom two sectors xx = 03h: Top boot device, HW protection for top two sectors xx = 04h: Uniform device, HW protection for lowest sector xx = 05h: Uniform device, HW protection for highest sector	Device type (bottom boot, top boot, uniform)
50h	A0h	0001h	Program suspend: 00 = Not supported 01 = supported	Supported

11. POWER-UP AND RESET CHARACTERISTICS

Table 11.1: Power-Up Timings

Parameter	Symbol		Min	Unit	Notes
	Legacy	JEDEC			
V _{CC} HIGH to V _{CCQ} HIGH	-	tVCHVCQH	0	us	1
V _{CC} HIGH to rising edge of RESET#	tVCS	tVCHPH	60	us	2
V _{CCQ} HIGH to rising edge of RESET#	tVIOS	tVCQHPH	0	us	2
V _{CC} HIGH to CE# LOW	-	tVCS	60		

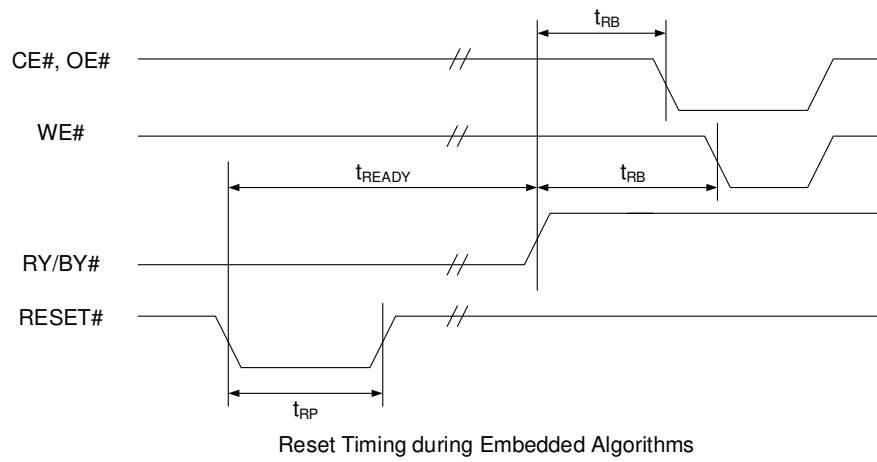
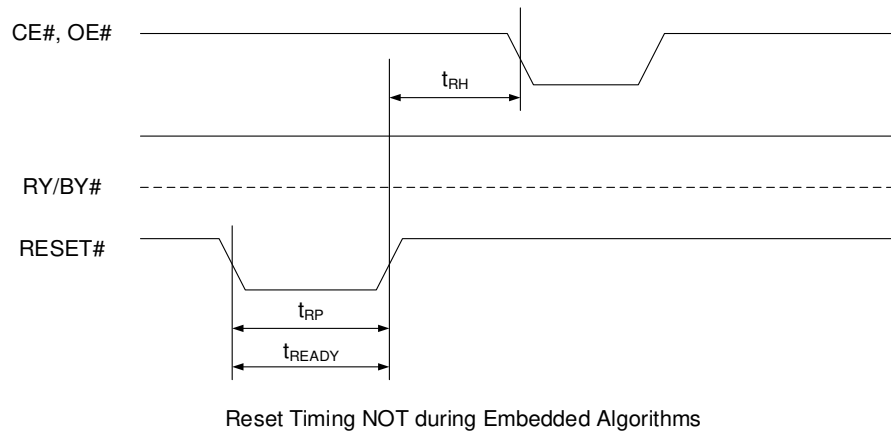
Notes:

1. V_{CC} and V_{CCQ} ramps must be synchronized during power-up.
2. If RESET# is not stable for tVCS or tVIOS, the device will not allow any READ or WRITE operations, and a hardware reset is required.

Table 11.2 Hardware Reset (RESET#) Timings

Parameter	Description	Test Setup	Value	Unit
t _{RP}	RESET# Pulse	Min	100	ns
t _{RH}	RESET# High to CE#, OE# LOW	Min	50	ns
T _{PHWL}	RESET# High to WE# LOW	Min	150	ns
t _{RB}	RY/BY# HIGH to CE#, OE# LOW	Min	0	ns
t _{READY}	RESET# LOW to Read mode during program/erase	Max	25	us
t _{RPD}	RESET# LOW to standby mode during read mode	Min	10	us
	RESET# LOW to standby mode during program/erase mode	Min	50	us

Figure11.1. AC Waveforms for RESET#



12. ELECTRICAL CHARACTERISTICS

12.1 ABSOLUTE MAXIMUM RATINGS

Table 12.1: ABSOLUTE MAXIMUM RATINGS

Parameter		Value	Notes
Storage Temperature		-65°C to +150°C	
Voltage with Respect to Ground	V _{CC} , V _{CCQ}	-0.5V to 4.0V	
	Input/output voltage	-0.5V to V _{CCQ} + 0.5V	1, 2
	V _{HH}	-0.5V to 10.5V	1, 2

Notes:

1. During signal transition, minimum voltage may undershoot to -2V during periods less than 20ns.
2. During signal transition, maximum voltage may overshoot to V_{CC} + 2V during periods less than 20ns.

12.2 OPERATING RANGE

Table 12.2 Operating Range

Parameter		Value
Ambient Operating Temperature (T _A)	Extended Grade	-40°C to 105°C
	Automotive Grade A3	-40°C to 125°C
V _{CC} Power Supply		2.7V (V _{CCmin}) – 3.6V (V _{CCmax}); 3.3V (Typ)
V _{CCQ} Power Supply		1.65V (V _{CCQ min}) – V _{CC} (V _{CCQ max}); 3.3V (Typ)

12.3 DC CHARACTERISTICS

Table 12.3. DC Characteristics

(Under recommended operating ranges)

Symbol	Parameter		Test Conditions		Min	Typ ⁽⁴⁾	Max	Unit
I _{LI} ⁽¹⁾	Input Leakage Current		0V≤ V _{IN} ≤ V _{CC}				±1	μA
I _{LO}	Output Leakage Current		0V≤ V _{OUT} ≤ V _{CC}				±1	μA
I _{CC1}	V _{CC} Active Read Current	Random	CE# = V _{IL} ; OE# = V _{IH} , V _{CC} = V _{CCmax} , f=5MHz			20	25	mA
		Page	CE# = V _{IL} ; OE# = V _{IH} , V _{CC} = V _{CCmax} , f=13MHz			12	16	mA
I _{CC2} ⁽³⁾	V _{CC} Standby Current	64Mb	CE#, RESET# = V _{CCQ} ± 0.3 V, V _{CC} = V _{CC} max			35	120	μA
		32Mb				35	120	
I _{CC3} ⁽²⁾	V _{CC} Program/ Erase/Blank V _{CC}		program/erase controller active	WP#/ACC = V _{IL} or V _{IH}		35	50	mA
				WP#/ACC = V _{HH}		26	33	
I _{ACC1}	V _{ACC} Current	Read	WP#/ACC ≤ V _{CC}		-	2	15	μA
		Standby			-	0.2	5	μA
I _{ACC2}		Reset	RESET# = V _{SS} ± 0.2 V			0.2	5	μA
I _{ACC3}		Program operation ongoing	WP#/ACC = 10V ± 5%		-	5	10	mA
			WP#/ACC = V _{CC}		-	0.05	0.10	mA
I _{ACC4}		Erase operation ongoing	WP#/ACC = 10V ± 5%		-	5	10	mA
			WP#/ACC = V _{CC}		-	0.05	0.10	mA
V _{IL}	Input Low Voltage		-		-0.1		0.3 x V _{CCQ}	V
V _{IH}	Input High Voltage		-		0.7 x V _{CCQ}		V _{CCQ} + 0.3	V
V _{OL}	Output Low Voltage		I _{OL} = 100μA		-	-	0.15 x V _{CCQ}	V
V _{OH}	Output High Voltage CMOS		I _{OH} = -100μA		0.85 x V _{CCQ}		-	V
V _{HH}	Acceleration Program Voltage		-		9.5		10.5	V
V _{ACCL}	V _{ACC} logic level		-		2.7		3.6	
V _{LKO} ⁽²⁾	Program/erase lockout supply voltage		-		2.3	-	-	V

Notes:

- The maximum input leakage current is $\pm 5 \mu A$ on the WP#/ACC pin.
- Sampled only; not 100% tested.
- BYTE#, WP#/ACC = V_{IH} or V_{IL} at ICC2 test for 48-pin TSOP package.

12.4 AC MEASUREMENT CONDITIONS

Table 12.4. AC MEASUREMENT CONDITIONS

Symbol	Parameter	Min	Max	Units
CL	Load Capacitance		30	pF
TR,TF	Input Rise and Fall Times		2.5	ns
VIN	Input Pulse Voltages	0 to V _{CCQ}		V
VREFI	Input Timing Reference Voltages	0.3V _{CC} to 0.7V _{CC}		V
VREFO	Output Timing Reference Voltages	V _{CCQ} /2		V

Figure 12.1 Test Conditions

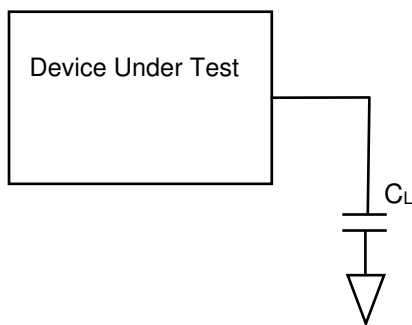


Figure 12.1. Input Waveforms and Measurement Levels

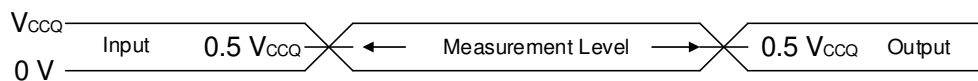


Table 12.5 Input/Output Capacitance

Parameter	Symbol	Test Condition	Package	Typ.	Max.	Unit
Input Capacitance	C _{IN}	V _{IN} = 0V	TSOP	6	7.5	pF
			BGA	TBD	TBD	pF
Control Pin Capacitance	C _{IN2}	V _{IN} = 0V	TSOP	6	7.5	pF
			BGA	TBD	TBD	pF
RESET#, WP#/ACC Pin Capacitance	C _{IN3}	V _{IN} = 0V	TSOP	13	18	pF
			BGA	TBD	TBD	pF
Output Capacitance	C _{OUT}	V _{OUT} = 0V	TSOP	7	8.5	pF
			BGA	TBD	TBD	pF

12.5 AC CHARACTERISTICS

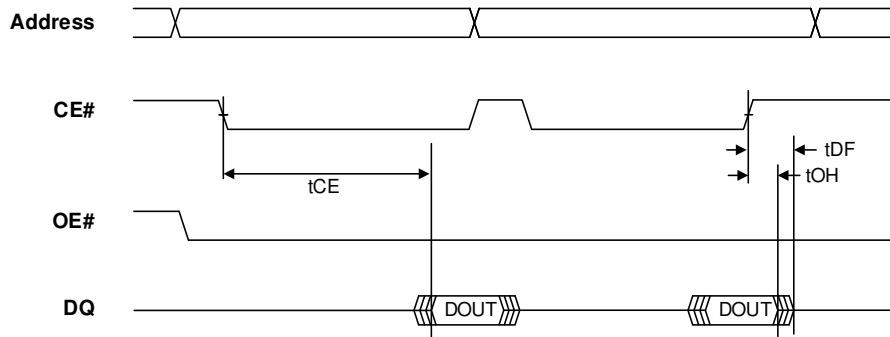
Table 12.6 Read Operations Characteristics

Parameter Symbols		Description	Condition	Min	Max	Unit
JEDEC	Legacy					
t_{AVAV}	t_{RC}	Read Cycle Time	$V_{CCQ} \geq 2.7V$, $CE\# = V_{IL}$, $OE\# = V_{IL}$	70	-	ns
			$V_{CCQ} \leq 2.7V$, $CE\# = V_{IL}$, $OE\# = V_{IL}$	75	-	ns
t_{AVQV}	t_{ACC}	Address valid to output valid	$V_{CCQ} \geq 2.7V$, $CE\# = V_{IL}$, $OE\# = V_{IL}$	-	70	ns
			$V_{CCQ} \leq 2.7V$, $CE\# = V_{IL}$, $OE\# = V_{IL}$	-	75	ns
	t_{PACC}	Address to output valid (page)	$CE\# = V_{IL}$, $OE\# = V_{IL}$	-	25	ns
t_{ELQX}	$t_{LZ}^{(1)}$	CE# LOW to output transition	$OE\# = V_{IL}$	0	-	ns
t_{ELQV}	t_{CE}	CE# LOW to output valid	$V_{CCQ} \geq 2.7V$, $OE\# = V_{IL}$	-	70	ns
			$V_{CCQ} \leq 2.7V$, $OE\# = V_{IL}$	-	75	ns
T_{OLZ}	$T_{OLZ}^{(1)}$	OE# LOW to output transition	$CE\# = V_{IL}$	0	-	ns
T_{GLQV}	T_{OE}	OE# LOW to output valid	$CE\# = V_{IL}$	-	25	ns
t_{EHQZ}	$T_{DF}^{(1)}$	CE# HIGH to output transition	$OE\# = V_{IL}$	-	20	ns
T_{GHQZ}	$T_{DF}^{(1)}$	OE# HIGH to output transition	$CE\# = V_{IL}$	-	15	ns
t_{EHQX} , t_{EHQX} , t_{EHQX}	T_{OH}	CE#, OE#, or address transition to output transition.	-	0	-	ns

Notes:

1. High Z is Not 100% tested.
2. t_{OE} parameter will meet specification value when the interval between CE# LOW and OE# LOW or Valid address to OE# LOW is equal to or longer than $(t_{CE} - t_{OE})$ or $(t_{ACC} - t_{OE})$.

Figure 12.2.1 READ to READ Operation Timing Diagram (WE#=HIGH, CE# Toggle)



Note:

1. Please [click here](#) to refer to Application Note (AN25D012, Understanding and Interpreting Read Timing of Parallel NOR FLASH).

Figure 12.2.2 READ to READ Operation Timing Diagram (OE# Toggle)

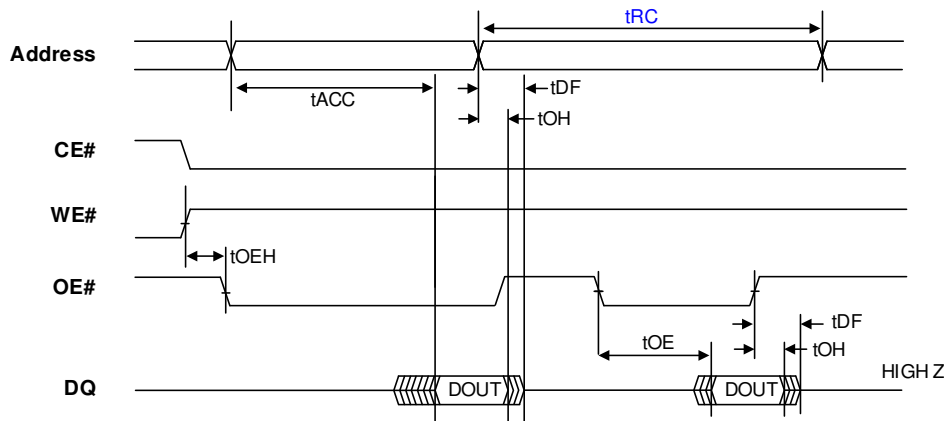
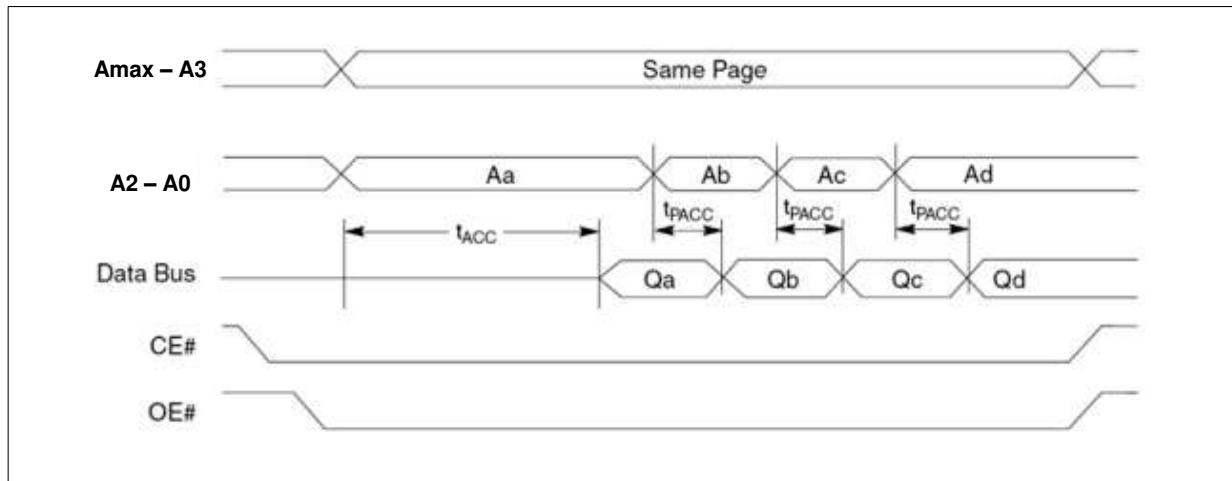


Figure 12.3 Page Read Operation Timings

Note: Addresses are A2:A-1 for byte mode.

Table 12.7 Word / Byte Configuration (BYTE#)

(Under recommended operating ranges)

Std Parameter	Description	Test Setup	Speed	Unit
			70ns	
t_{BCS}	Byte# to CE# switching setup time	Min	0	ns
t_{CBH}	CE# to Byte# switching hold time	Min	0	ns
t_{RBH}	RY/BY# to Byte# switching hold time	Min	0	ns

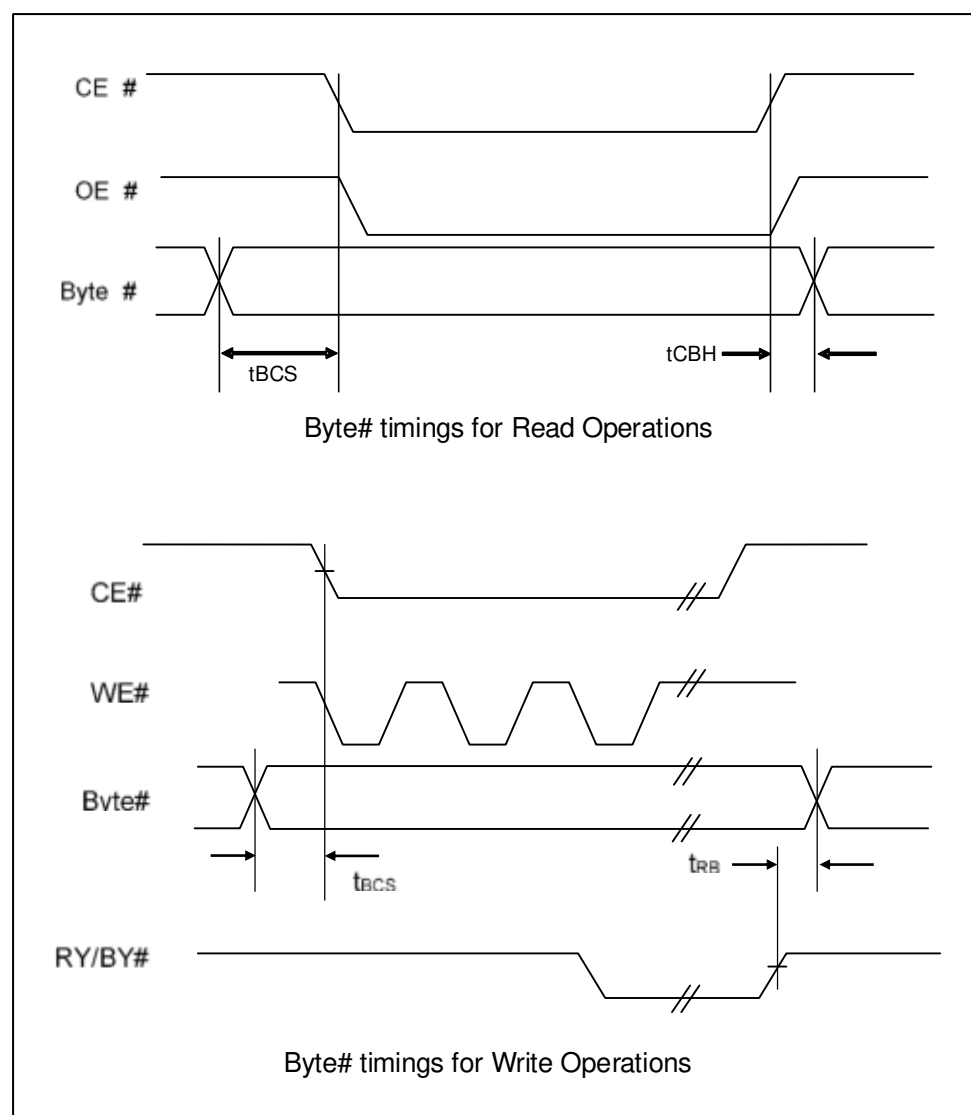
Figure 12.4 BYTE# Operation Timings

Note: Switching Byte# pin not allowed during embedded operations.

Table 12.8 WE#-Controlled Write AC Characteristics

Parameter Symbols		Description	Condition	Min	Max	Unit
JEDEC	Legacy					
T _{AVAV}	T _{WC}	Write Cycle Time	V _{CCQ} ≥ 2.7V	70	-	ns
			V _{CCQ} ≤ 2.7V	75	-	ns
T _{ELWL}	T _{CS}	CE# LOW to WE# LOW	-	0	-	ns
T _{WLWH}	T _{WP}	WE# LOW to WE# HIGH	-	35	-	ns
T _{WHWL}	T _{WPH}	WE# HIGH to WE# LOW	-	20	-	ns
T _{DVWH}	T _{DS}	Input valid to WE# HIGH	-	30	-	ns
T _{WHDX}	T _{DH}	WE# HIGH to input transition	-	0	-	ns
T _{WHEH}	T _{CH}	WE# HIGH to CE# HIGH	-	0	-	ns
T _{AVWL}	T _{AS}	Address valid to WE# LOW	-	0	-	ns
T _{WLAX}	T _{AH}	WE# LOW to Address transition	-	45	-	ns
T _{GHWL}	T _{GHWL}	OE# HIGH to WE# LOW.	-	0	-	ns
T _{WHGL}	T _{OEH}	OE# Hold (Read)	-	0	-	us
	T _{VHH}	V _{HH} Rise and Fall Time		250	-	ns
	T _{BUSY} ⁽¹⁾	Program/erase valid to RY/BY# LOW	-	-	90	us

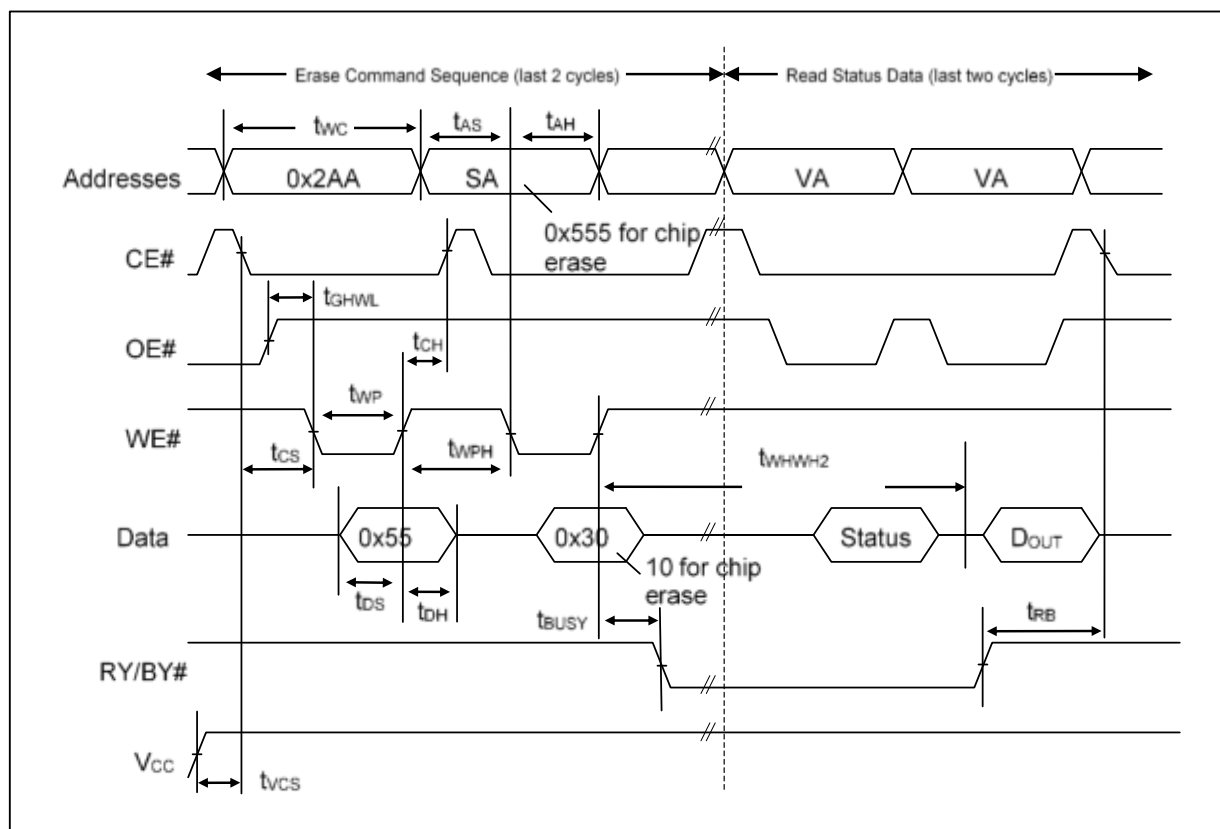
Note:

1. Sampled only; not 100% tested.

Table 12.9. Alternate CE#-Controlled Write AC Characteristics

Parameter Symbols		Description	Condition	Min	Max	Unit
JEDEC	Legacy					
T _{AVAV}	T _{WC}	Write Cycle Time	V _{CCQ} ≥ 2.7V	70	-	ns
			V _{CCQ} ≤ 2.7V	75	-	ns
T _{WLEL}	T _{WS}	WE# LOW to CE# LOW	-	0	-	ns
T _{ELEH}	T _{CP}	CE# LOW to CE# HIGH	-	35	-	ns
T _{DVEH}	T _{DS}	Input valid to CE# HIGH	-	30	-	ns
T _{EHDx}	T _{DH}	CE# HIGH to input transition	-	0	-	ns
T _{EHWH}	T _{WH}	CE# HIGH to WE# HIGH	-	0	-	ns
T _{EHEL}	T _{CPH}	CE# HIGH to CE# LOW	-	20	-	ns
T _{AVEL}	T _{AS}	Address valid to CE# LOW	-	0	-	ns
T _{ELAX}	T _{AH}	CE# LOW to Address transition	-	45	-	ns
T _{GHEL}	-	OE# HIGH to CE# LOW.	-	0	-	ns

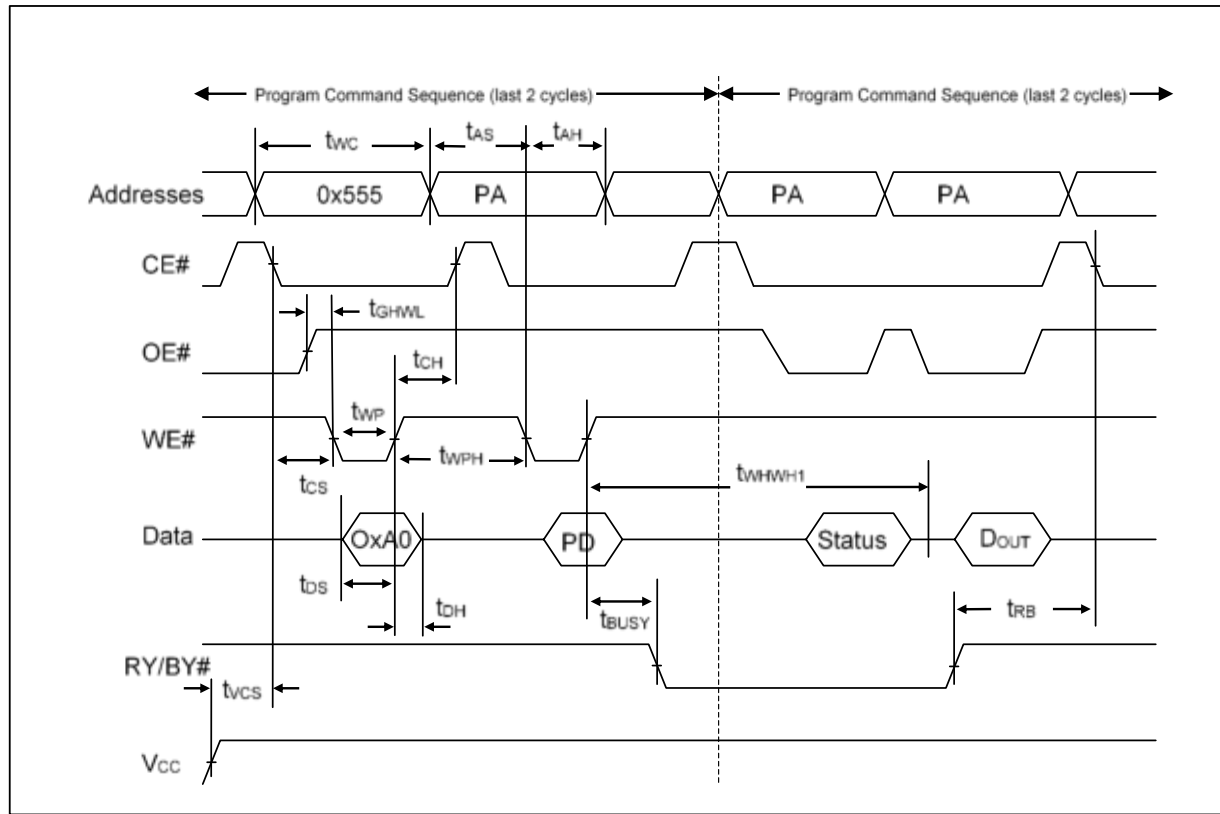
Figure 12.5 AC Waveforms for Chip/Sector Erase Operations Timings(x16)



Notes:

1. SA=Sector Address (for sector erase), VA=Valid Address for reading status, D_{OUT}=true data at read address.
2. V_{CC} shown only to illustrate t_{VCS} measurement references. It cannot occur as shown during a valid command sequence.

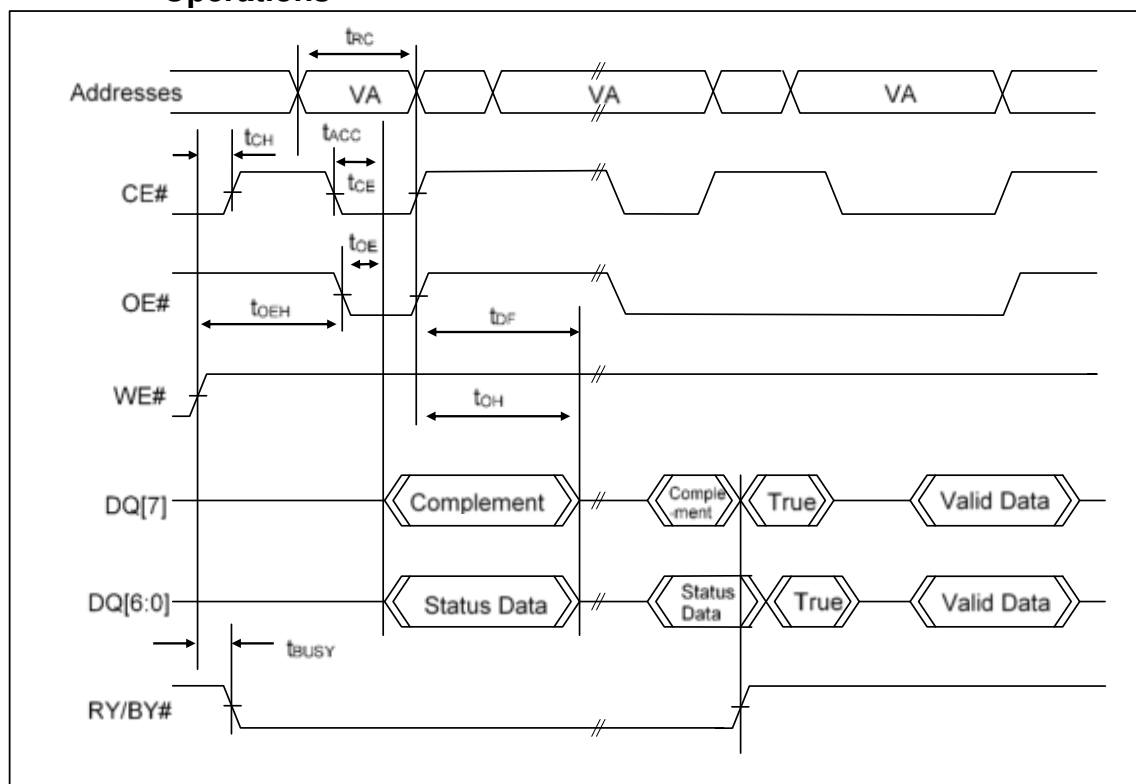
Figure 12.6 Program Operation Timings (x16)



Notes:

1. PA=Program Address, PD=Program Data, D_{OUT} is the true data at the program address.
2. V_{CC} shown in order to illustrate t_{VCS} measurement references. It cannot occur as shown during a valid command sequence.

Figure 12.7 AC Waveforms for /DATA Polling During Embedded Algorithm Operations



Notes:

1. VA=Valid Address for reading Data# Polling status data
2. This diagram shows the first status cycle after the command sequence, the last status read cycle and the array data read cycle.

Figure 12.8 AC Waveforms for Toggle Bit During Embedded Algorithm Operations

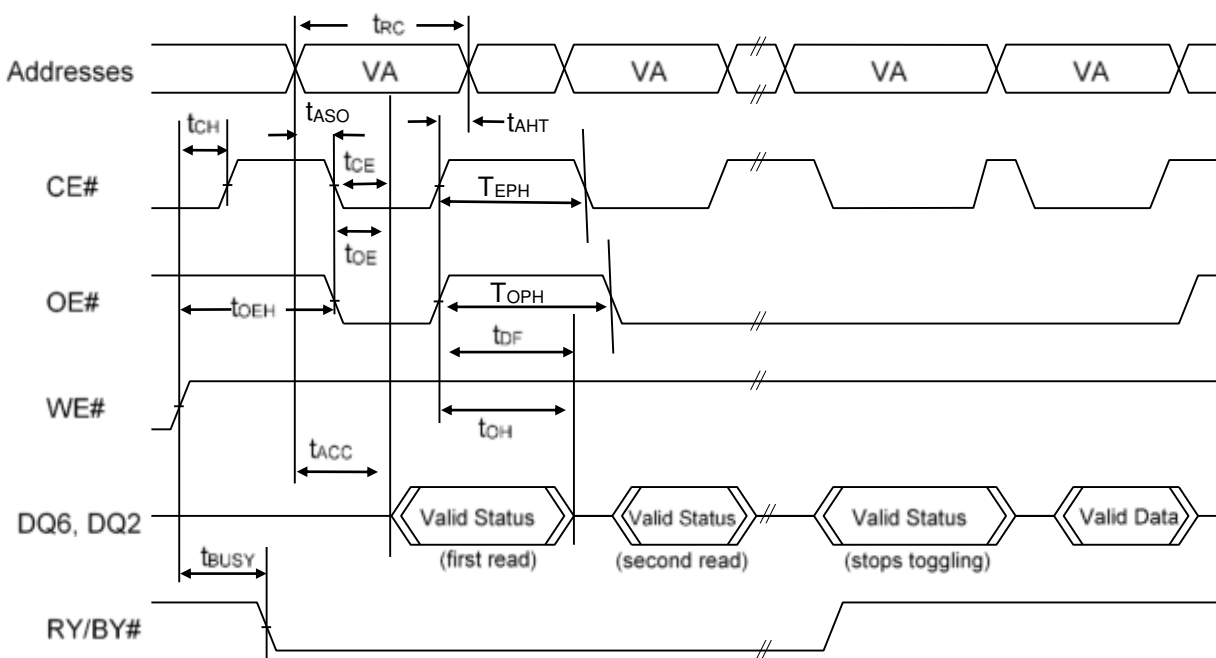
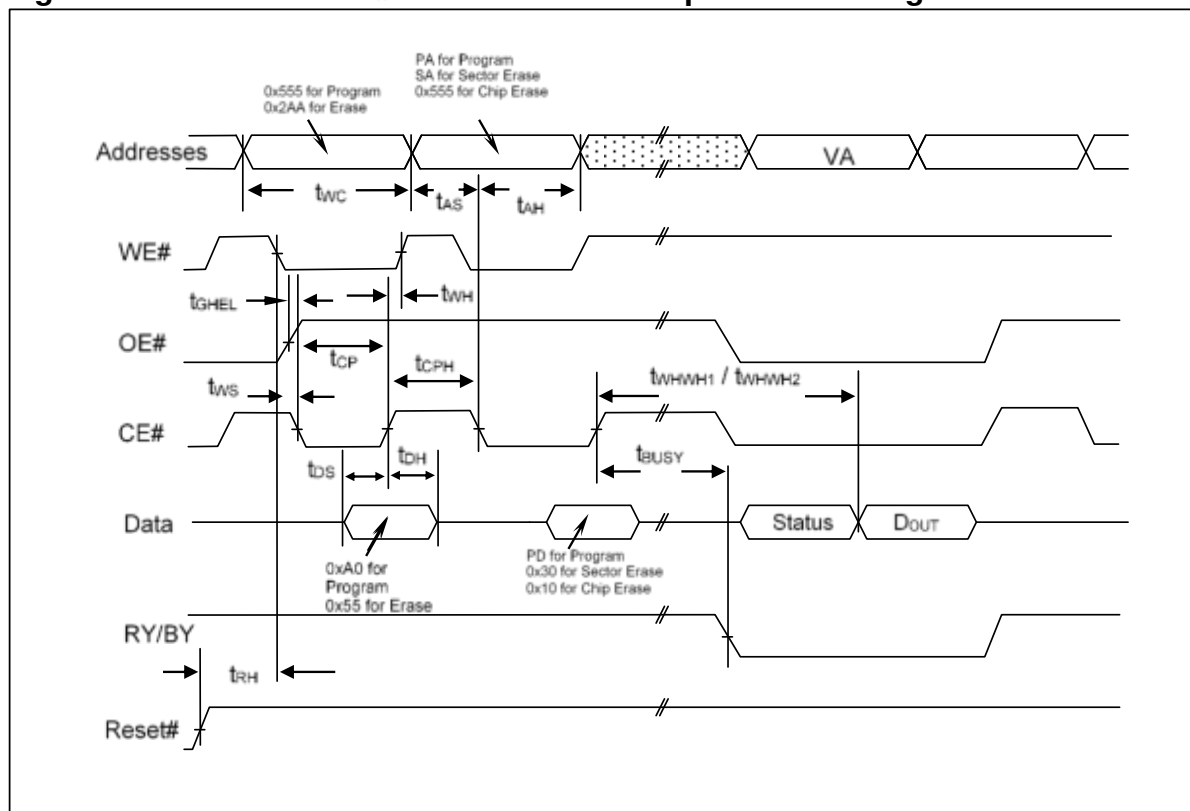


Figure 12.9 Alternate CE# Controlled Write Operation Timings

Notes:

PA = address of the memory location to be programmed.

PD = data to be programmed at byte address.

VA = Valid Address for reading program or erase status

D_{out} = array data read at VA

Shown above are the last two cycles of the program or erase command sequence and the last status read cycle

Reset# shown to illustrate t_{RH} measurement references. It cannot occur as shown during a valid command sequence.

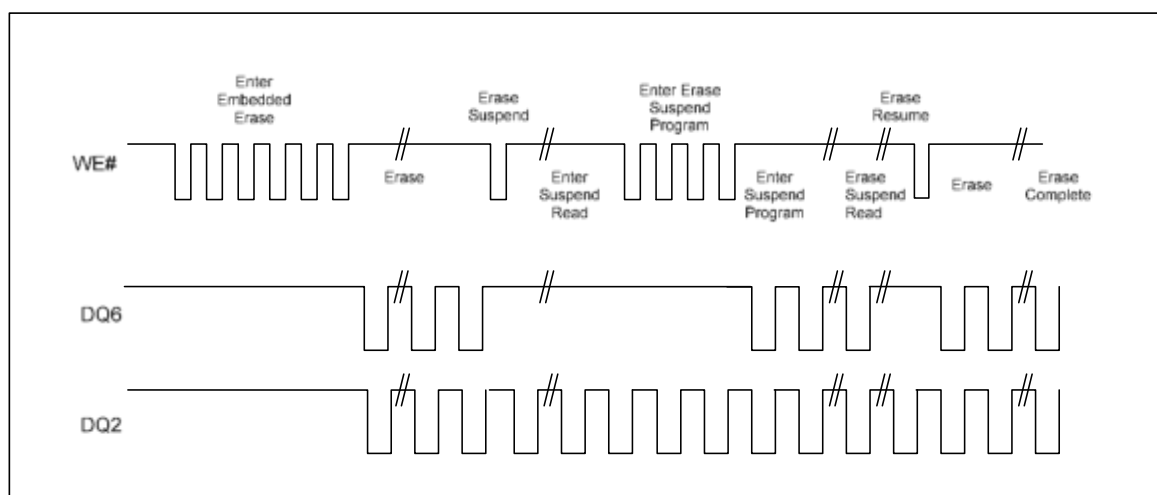
Figure 12.10 DQ2 vs. DQ6


Table 12.10. Accelerated Program and Data Polling/Data Toggle AC Characteristics

Parameter Symbols		Description	Min	Max	Unit
JEDEC	Legacy				
T_{VHVPP}	-	WP#/ACC rising or falling time	250	-	ns
T_{VHHWH}	-	Valid V_{HH} on WP#/ACC to WE# HIGH	50	-	ns
T_{AXGL}	T_{ASO}	Address setup time to OE# LOW during toggle bit polling	15	-	ns
T_{GHAX}, T_{EHAX}	T_{AHT}	Address hold time from OE# HIGH or CE# HIGH during toggle bit polling	0	-	ns
T_{EHEL2}	T_{EPH}	CE# HIGH during toggle bit polling	20	-	ns
	T_{OPH}	OE# HIGH during toggle bit polling	20	-	ns
T_{WHRL}	T_{BUSY}	Program/erase valid to RY#/BY# LOW	-	90	ns

Note: 1. Sampled only; not 100% tested.

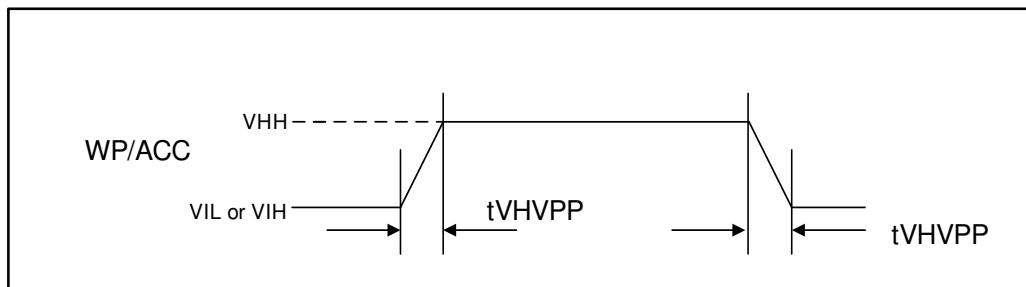
Figure 12.11 Accelerated Program AC Timing


Table 12.11 Program/Erase Characteristics

Parameter		Buffer Size	Byte	Word	Min	Typ ^(1,2)	Max ⁽²⁾	Unit
Sector Erase		-	-	-		0.5	4	s
Erase suspend latency		-	-	-		20	25	us
Sector erase timeout					50	-		us
Byte program	Single-byte program	-	-	-	-	15	175	us
	Double-/ Quadruple-/ Octuple-byte program	-	-	-	-	10	200	us
	Byte buffer program	32B	32	-	-	80	250	us
		64B	64	-	-	160	500	us
		256B	256	-	-	640	2000	us
Word program	Single-word program	-	-	-	-	15	175	us
	Word buffer program	16W	-	16	-	80	250	us
		32W	-	32	-	160	500	us
		128W	-	128	-	640	2000	us
		256W	-	256	-	1280	4000	us
	Full buffer program with V _{HH}	256	-	256	-	480	1200	us
	Effective buffer program per word	16	-	1	-	5	15.6	us
		32	-	1	-	5	15.6	us
		128	-	1	-	5	15.6	us
		256	-	1	-	5	15.6	us
	Effective full buffer program per word with V _{HH}	256	-	1	-	1.9	4.7	us
Program suspend latency		-	-	-	-	20	25	us
Blank check		-	-	-	-	20	-	ms
PROGRAM/ERASE cycles (per sector)		-	-		100,000	-	-	cycles

Notes:

1. Typical values measured at room temperature and nominal voltages.
2. Sampled, but not 100% tested.

13. PACKAGE INFORMATION

FIGURE 13.1 56-pin TSOP 14mmx20mm (S)

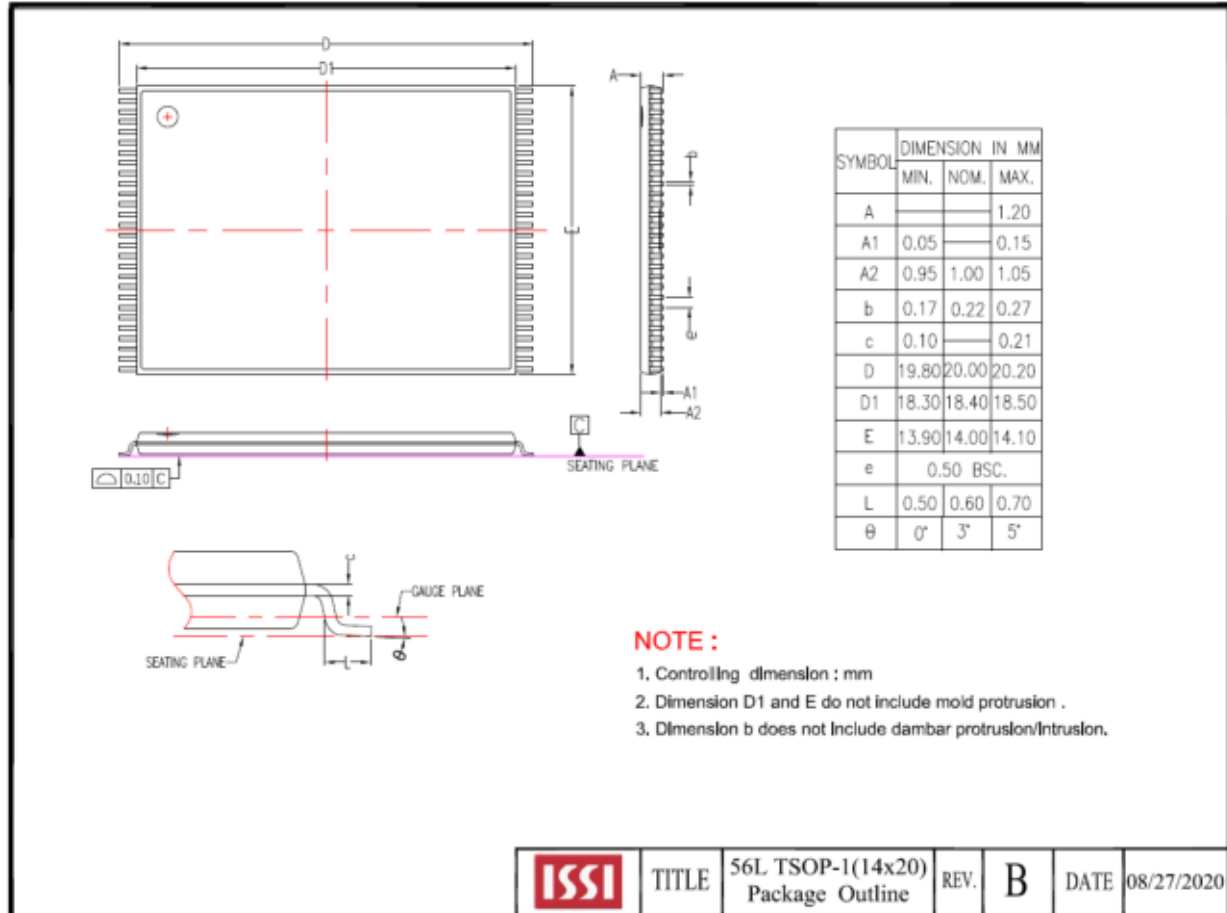


FIGURE 13.2. 48-pin TSOP 12mmx20mm (T)

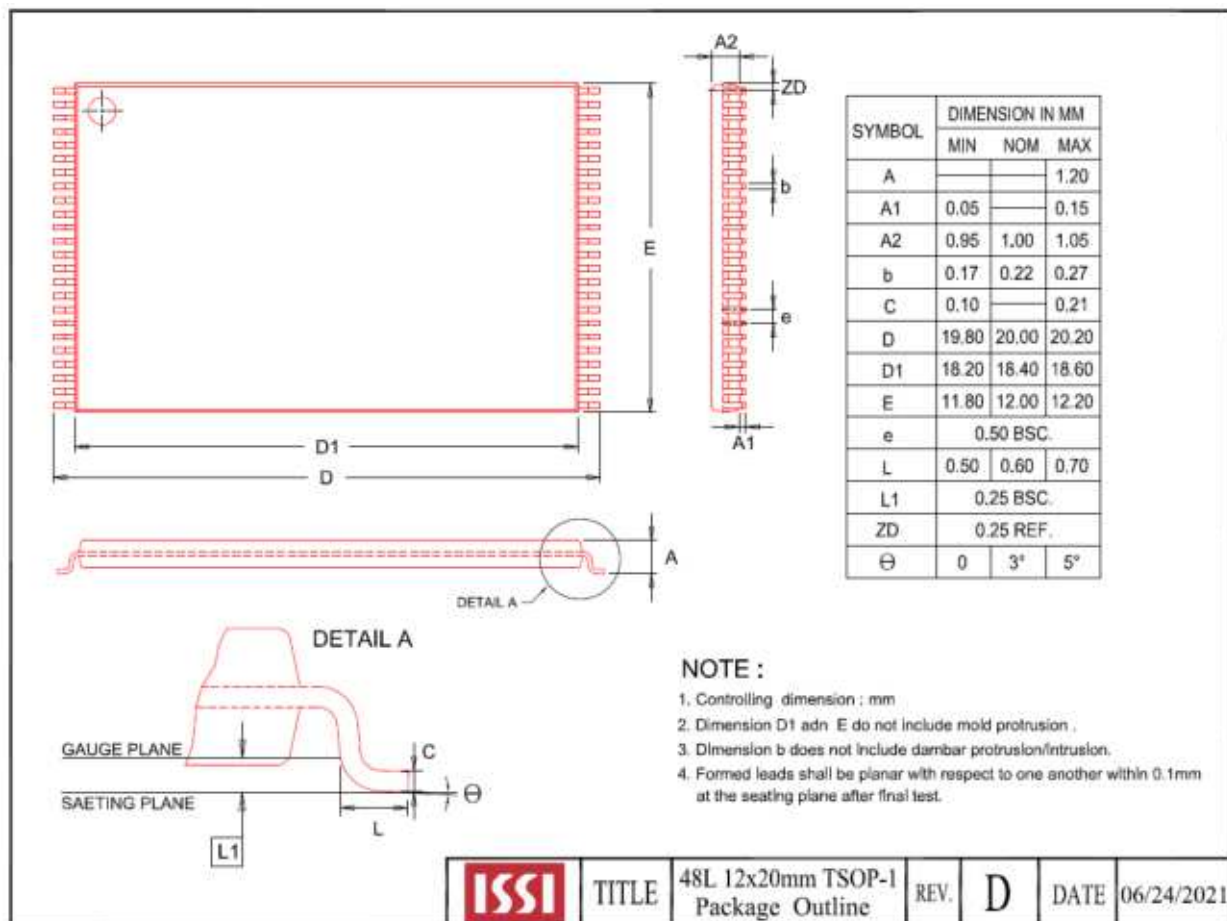


FIGURE 13.3. 64-ball Ball Grid Array (BGA), 11x13 mm, Pitch 1mm (F)

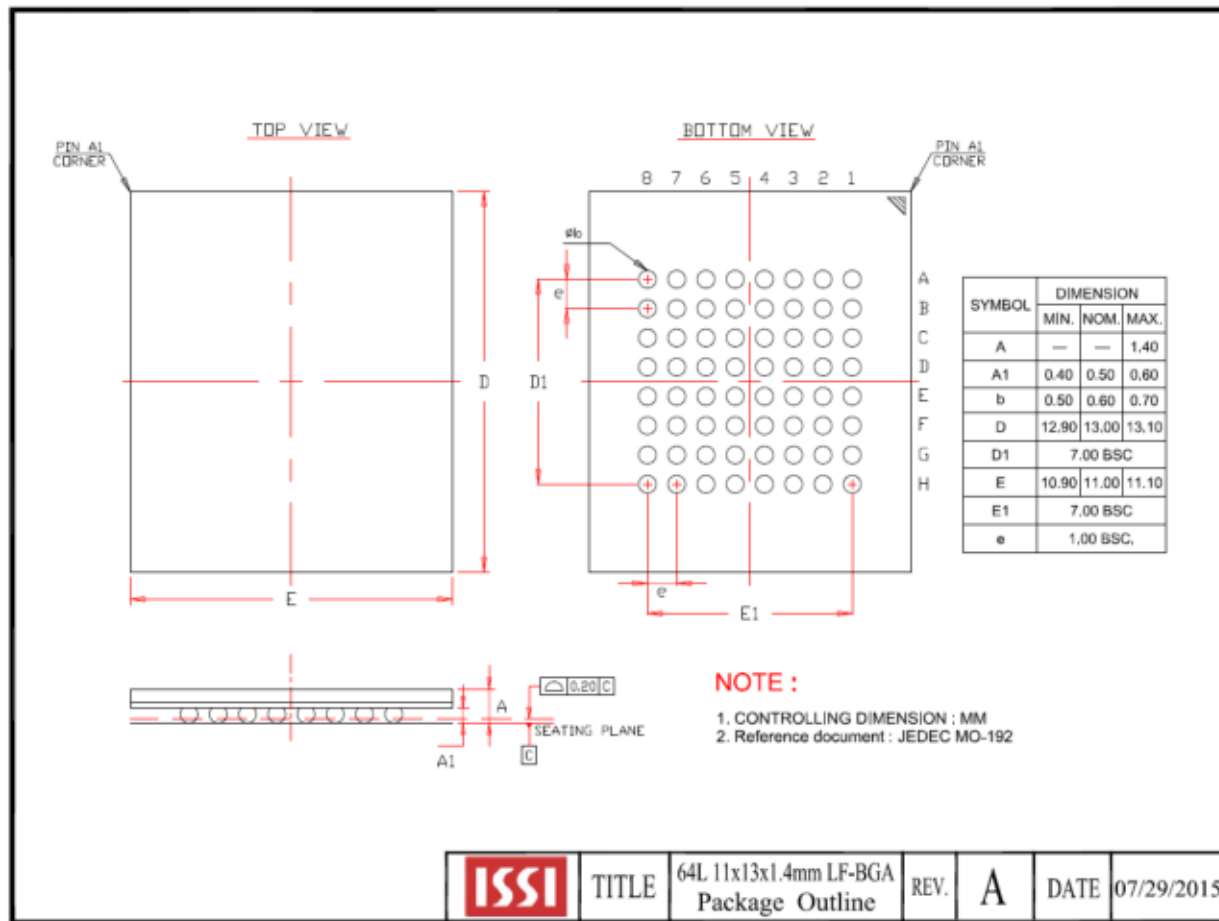


FIGURE 13.4. 48-ball Ball Grid Array (BGA), 6x8x1.2mm, Pitch 0.8mm (B)

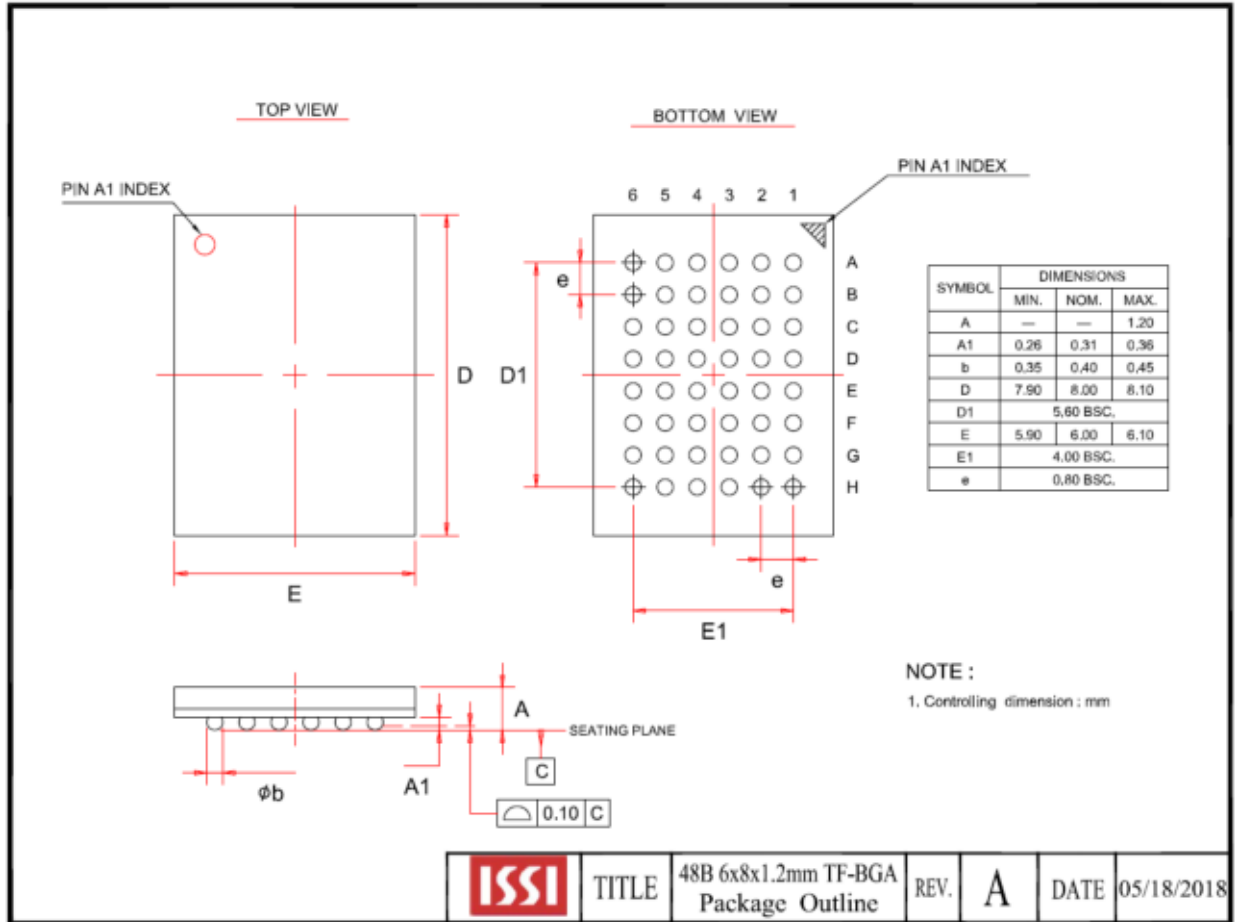
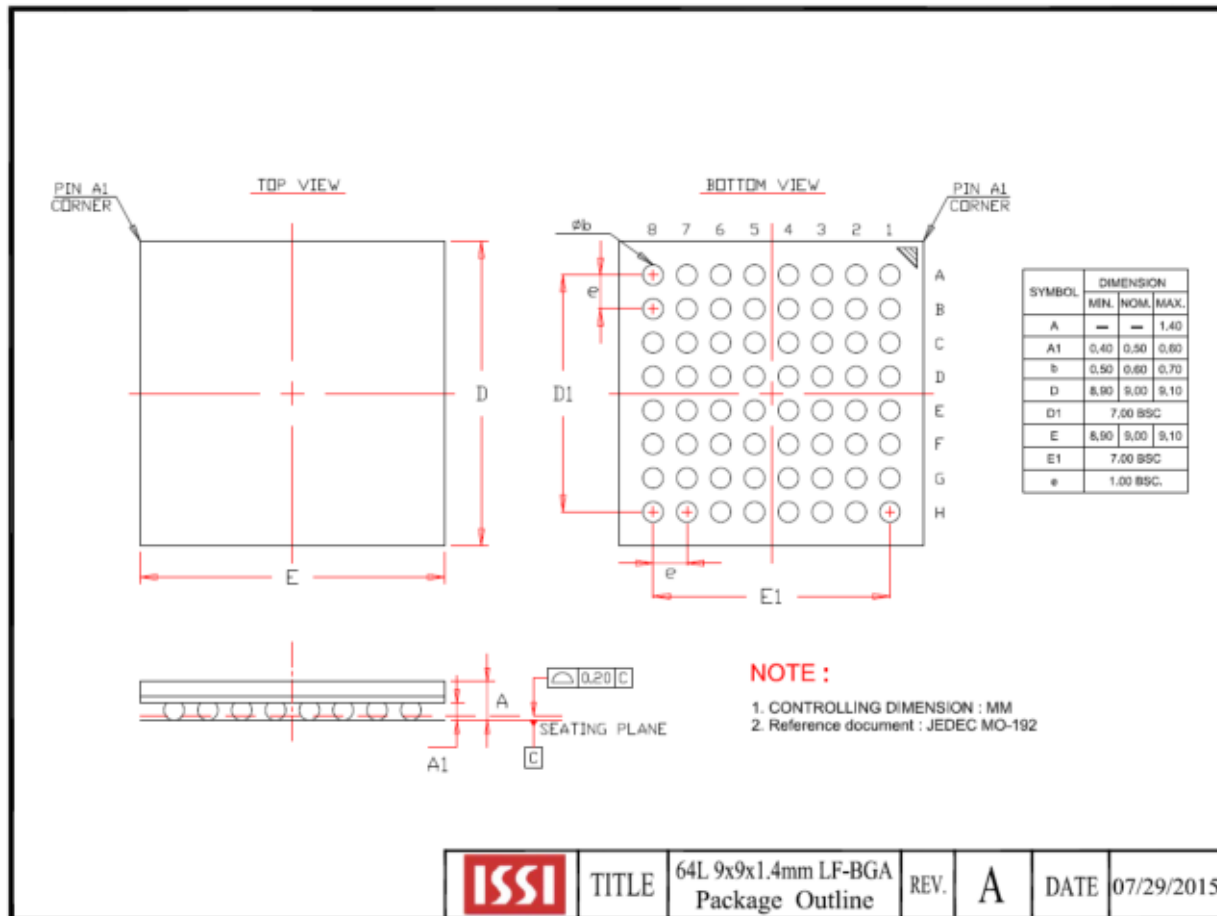
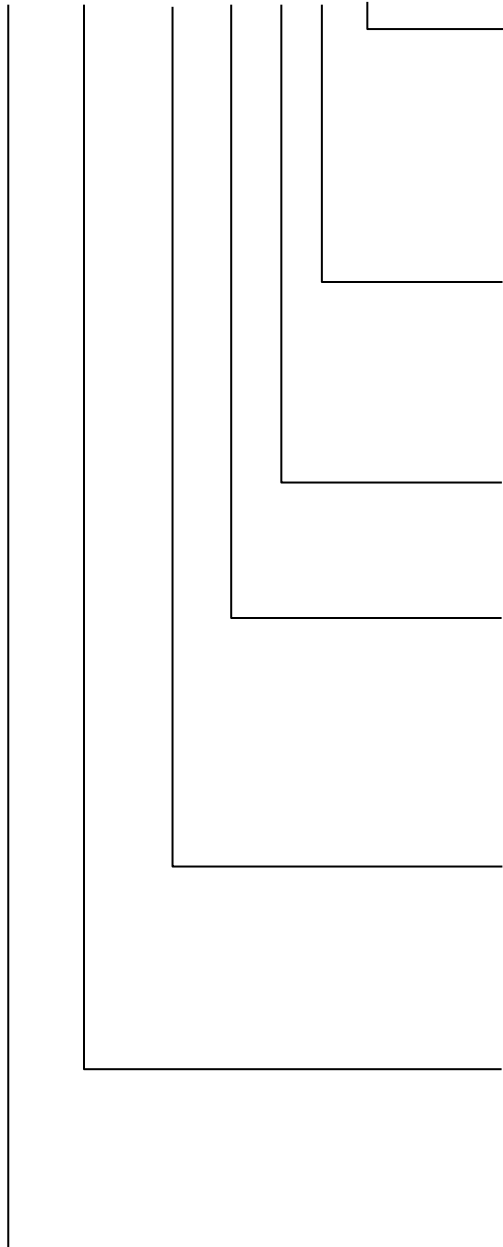


FIGURE 13.5. 64-ball Ball Grid Array (BGA), 9 X 9 mm, Pitch 1mm package outline



14. ORDERING INFORMATION

IS29GL 064 - 70 T L E T



SECTOR for WRITE PROTECT (WP#/ACC=L)

T = Highest sector protected, uniform sector by WP#/ACC
 B = Lowest sector protected, uniform sector by WP#/ACC
 U = Top boot; top two sectors protected by WP#/ACC
 D = Bottom boot; bottom two sectors protected by WP#/ACC

TEMPERATURE RANGE

E = Extended Grade (-40°C to +105°C)
 A3 = Automotive Grade (-40°C to +125°C)

PACKAGING CONTENT

L = RoHS compliant

PACKAGE

S = 56-pin TSOP
 T = 48-pin TSOP
 F = 64-ball BGA 1.0mm pitch, 11mm x 13mm
 D = 64-ball BGA 1.0mm pitch, 9mm x 9mm (Call Factory)
 B = 48-ball BGA 0.8mm pitch, 6mm x 8mm
 W = KGD (Call Factory)

SPEED at VCCQ=2.7~3.6V.

70 = 70ns

Density

064 = 64 Mb (4M x 16) ⁽¹⁾
 032 = 32 Mb (2M x 16) ⁽¹⁾

BASE PART NUMBER

IS = Integrated Silicon Solution Inc.
 29GL = FLASH, 3V Page Mode Flash Memory

Note:

1. Word mode (x16) only supported. Please contact Factory for Byte mode and Word mode.

64Mb

Temperature	Order Part Number	Sector Protection ⁽²⁾	Package
Extended (-40°C to +105°C)	IS29GL064-70SLET	Highest Sector, Uniform Sector	56-pin TSOP
	IS29GL064-70SLEB	Lowest Sector, Uniform Sector	
	IS29GL064-70SLEU	Top Two Sector, Top Boot	
	IS29GL064-70SLED	Bottom Two Sector, Bottom Boot	
	IS29GL064-70TLET	Highest Sector, Uniform Sector	48-pin TSOP
	IS29GL064-70TLEB	Lowest Sector, Uniform Sector	
	IS29GL064-70TLEU	Top Two Sector, Top Boot	
	IS29GL064-70TLED	Bottom Two Sector, Bottom Boot	
	IS29GL064-70FLET	Highest Sector, Uniform Sector	64-ball BGA (11x13mm)
	IS29GL064-70FLEB	Lowest Sector, Uniform Sector	
	IS29GL064-70FLEU	Top Two Sector, Top Boot	
	IS29GL064-70FLED	Bottom Two Sector, Bottom Boot	
	IS29GL064-70BLET	Highest Sector, Uniform Sector	48-ball BGA (6x8mm)
	IS29GL064-70BLEB	Lowest Sector, Uniform Sector	
	IS29GL064-70BLEU	Top Two Sector, Top Boot	
	IS29GL064-70BLED	Bottom Two Sector, Bottom Boot	
Automotive. A3 (-40°C to +125°C)	IS29GL064-70SLA3T	Highest Sector, Uniform Sector	56-pin TSOP
	IS29GL064-70SLA3B	Lowest Sector, Uniform Sector	
	IS29GL064-70SLA3U	Top Two Sector, Top Boot	
	IS29GL064-70SLA3D	Bottom Two Sector, Bottom Boot	
	IS29GL064-70TLA3T	Highest Sector, Uniform Sector	48-pin TSOP
	IS29GL064-70TLA3B	Lowest Sector, Uniform Sector	
	IS29GL064-70TLA3U	Top Two Sector, Top Boot	
	IS29GL064-70TLA3D	Bottom Two Sector, Bottom Boot	
	IS29GL064-70FLA3D	Bottom Two Sector, Bottom Boot	64-ball BGA (11x13mm)
	IS29GL064-70FLA3T	Highest Sector, Uniform Sector	
	IS29GL064-70FLA3B	Lowest Sector, Uniform Sector	
	IS29GL064-70FLA3U	Top Two Sector, Top Boot	
	IS29GL064-70FLA3D	Bottom Two Sector, Bottom Boot	48-ball BGA (6x8mm)
	IS29GL064-70BLA3T	Highest Sector, Uniform Sector	
	IS29GL064-70BLA3B	Lowest Sector, Uniform Sector	
	IS29GL064-70BLA3U	Top Two Sector, Top Boot	
	IS29GL064-70BLA3D	Bottom Two Sector, Bottom Boot	

32Mb

Temperature	Order Part Number	Sector Protection ⁽²⁾	Package
Extended (-40°C to +105°C)	IS29GL032-70SLET	Highest Sector, Uniform Sector	56-pin TSOP
	IS29GL032-70SLEB	Lowest Sector, Uniform Sector	
	IS29GL032-70SLEU	Top Two Sector, Top Boot	
	IS29GL032-70SLED	Bottom Two Sector, Bottom Boot	
	IS29GL032-70TLET	Highest Sector, Uniform Sector	48-pin TSOP
	IS29GL032-70TLEB	Lowest Sector, Uniform Sector	
	IS29GL032-70TLEU	Top Two Sector, Top Boot	
	IS29GL032-70TLED	Bottom Two Sector, Bottom Boot	
	IS29GL032-70BLET	Highest Sector, Uniform Sector	48-ball BGA (6x8mm)
	IS29GL032-70BLEB	Lowest Sector, Uniform Sector	
	IS29GL032-70BLEU	Top Two Sector, Top Boot	
	IS29GL032-70BLED	Bottom Two Sector, Bottom Boot	
Automotive. A3 (-40°C to +125°C)	IS29GL032-70SLA3T	Highest Sector, Uniform Sector	56-pin TSOP
	IS29GL032-70SLA3B	Lowest Sector, Uniform Sector	
	IS29GL032-70SLA3U	Top Two Sector, Top Boot	
	IS29GL032-70SLA3D	Bottom Two Sector, Bottom Boot	
	IS29GL032-70TLA3T	Highest Sector, Uniform Sector	48-pin TSOP
	IS29GL032-70TLA3B	Lowest Sector, Uniform Sector	
	IS29GL032-70TLA3U	Top Two Sector, Top Boot	
	IS29GL032-70TLA3D	Bottom Two Sector, Bottom Boot	
	IS29GL032-70BLA3T	Highest Sector, Uniform Sector	48-ball BGA (6x8mm)
	IS29GL032-70BLA3B	Lowest Sector, Uniform Sector	
	IS29GL032-70BLA3U	Top Two Sector, Top Boot	
	IS29GL032-70BLA3D	Bottom Two Sector, Bottom Boot	

Notes:

- A3: Meet AEC-Q100 requirements with PPAP
Temp Grades: E= -40 to 105°C, A3= -40 to 125°C
- WP#/ACC=L