Very Low Power 8-Bit 32 kHz RTC Module with Digital Trimming, User RAM and Battery Switch-over

Description

The V3025 is a low power CMOS real time clock with an integrated battery switch-over. The standby current is typically 2.5 µA and the access time is 50 ns. The interface is a multiplexed address and data 8 bits bus. Multiplexing of address and data is handled by the input line $\overline{A}$ /D. There are no busy flags in the V3025, internal time update cycles are invisible to the user's software. Time data can be read from the V3025 in 12 or 24 hour data formats. An external signal puts the V3025 in standby mode. Even in standby, the V3025 pulls the $\overline{IRQ}$ pin active low on an internal alarm interrupt. Calendar functions include leap year correction and week number calculation. The V3025 can be synchronized to an external 50 Hz signal or to the nearest second or minute. The integrated battery switch-over supply the real time clock part by V_{DD} as long as V_{DD} is higher than V_{BAT}. When V_{DD} decreases under V_{BAT}, the output $\overline{PFO}$ comes active and the real clock is supplied by the battery or the supercap.

Applications

- Industrial controllers
- Alarm systems with periodic wake up
- PABX and telephone systems
- Point of sale terminals
- Automotive electronics
- Personal computers

Features

- **Built-in quartz with digital trimming and temperature compensation facilities**
- INTEL and MOTOROLA interface compatibility
- 15 ns typical access time at 5.0V
- 1.2 µA typical standby current at 3.0V
- Wide supply voltage range, 2.0 ≤ V_{DD} ≤ 5.5V
- Integrated battery switch-over
- Battery voltage range, 2.0 ≤ V_{BAT} ≤ 4.0V
- No busy state
- No external components required
- BCD format
- Frequency measurements
- Time set lock mode
- Week number calculation
- Clock counts up to 99 years
- Leap year correction
- 12 or 24 hour data format
- Output programmable interrupts
- Alarm interrupt, programmable up to one month
- Timer interrupt, programmable up to 24 hours
- Time to 1/100 of a second
- To external time reference synchronisation
- 50 Hz or nearest s/min synchronisation
- Power fail input $\overline{PFI}$
- Power fail output or Reset output $\overline{PFO}$
- Tri-state bus capability when power fail ($\overline{PFI}$ = 0)
- User RAM
- Temperature range -40 to +85°C
- Package SO28

Typical Operating Configuration

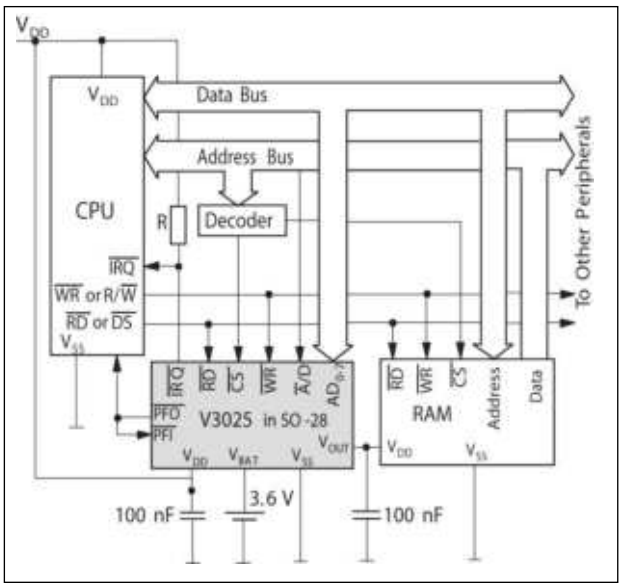


Fig. 1

Pin Assignment

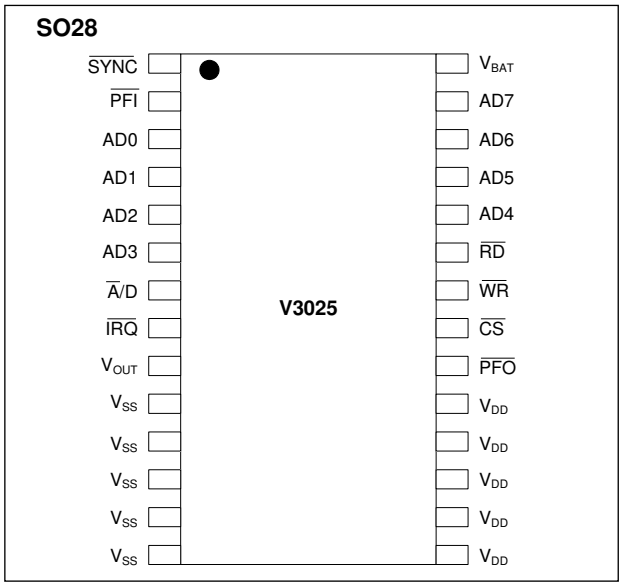


Fig. 2

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Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum voltage at V_{DD} and V_{BAT}	V_{SUPmax}	V_{SS} + 7.0V
Max. voltage at remaining pins	V_{SUP}	V_{DD} + 0.3V
Min. voltage on all pins	V_{min}	V_{SS} – 0.3V
Maximum storage temperature	T_{STOmax}	+85°C
Minimum storage temperature	T_{STOmin}	-55°C
Maximum electrostatic discharge to MIL-STD-883C method 3015.7 with ref. to V_{SS}	V_{Smax}	1000V
Maximum soldering conditions	T_{Smax}	260°C x 10s
Shock resistance		5000 g. 0.3ms, ½ sine

Table 1

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating temperature	T_A	-40		+85	°C
Main supply voltage	V_{DD}	2		5.5	V
Battery supply voltage	V_{BAT}	2		4	V
Logic supply voltage	V_{SUP}	2.0	5.0	5.5	V
Supply voltage dv/dt (power-up & down)	dv/dt			6 (note 1)	V/µs
Decoupling capacitor			100		nF

Table 2

Electrical Characteristics

V_{DD} = 5.0V ±10%, V_{BAT} = 3V, T_A = -40 to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Standby current (note 2)	I_{DD1}	V_{DD} = 3 V, V_{BAT} = 0V, $\overline{PFI}$ = 0		1.2	10	µA
	I_{DD2}	V_{DD} = 5.5 V, $\overline{PFI}$ = 0		2.5	15	µA
Standby current (note 2)	I_{BAT}	V_{DD} = 0 V, $\overline{PFI}$ = 0		1.3	10	µA
Dynamic current (note 3)	I_{DYN}	$\overline{CS}$ = 4 MHz, $\overline{RD}$ = V_{SS} $\overline{WR}$ = V_{DD}			1.5	mA
$\overline{IRQ}$ (open drain)						
Output low voltage	V_{OL}	I_{OL} = 6 mA			0.4	V
Output low voltage	V_{OL}	I_{OL} = 1 mA, V_{DD} = 2 V			0.4	V
Inputs and Outputs						
Input logic low	V_{IL}	T_A = +25°C			0.2 V_{SUP}	V
Input logic high	V_{IH}	T_A = +25°C	0.8 V_{SUP}			V
Output logic low	V_{OL}	I_{OL} = 6 mA			0.4	V
Output logic high	V_{OH}	I_{OH} = 6 mA	2.4			V
$\overline{PFI}$ activation voltage	V_{PFL}			0.5 V_{DD}		V
$\overline{PFI}$ hysteresis	V_H	T_A = +25°C		100		mV
Pullup on $\overline{SYNC}$	I_{LS}	V_{ILS} = 0.8 V	20	40		µA
Input leakage	I_{IN}	V_{SS} < V_{IN} < V_{DD}		5	1000	nA
Output tri-state leakage	I_{TS}	$\overline{CS}$ = 1		5	1000	nA
Oscillator Characteristics						
Starting voltage	V_{STA}	T_A ≥ +25°C	2			V
	V_{STA}			2.5		V
Frequency Characteristics						
Start-up time	T_{STA}			1		s
Frequency tolerance	Δf/f	T_A = +25°C addr. 10 hex = 00 hex	150	210 (note 4)	251	ppm
Frequency stability	f_{sta}	2.0 ≤ V_{DD} ≤ 5.5 V (note 5)		1	5	ppm/V
Temperature stability	t_{sta}	addr. 10 hex = 00 hex		see Fig.6		ppm
Aging	t_{ag}	T_A = +25°C, first year			±5	ppm/year
Accuracy versus switch-over	A_{SW}	V_{BAT} = 3V, 10 pulses of V_{DD} switching between 2 to 5V in 70ms		0.2		ppm

Table 3

Note 1: For temperature below -20°C, dv/dt max 0.1V/ms.

Note 2: With $\overline{PFO}$ = 0 (V_{SS}) all I/O pads can be tri-state, tested.
With $\overline{PFO}$ = 1 (V_{DD}), $\overline{CS}$ = 1 (V_{DD}) and all other I/O pads fixed to V_{DD} or V_{SS}: same standby current, not tested.

Note 3: All other inputs to V_{DD} and all outputs open.

Note 4: See Fig. 4

Note 5: At a given temperature.

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Switch-over Electrical Characteristics

T_A = -40 to +85°C, inputs to V_{DD}, outputs not connected, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ON resistance of V_{DD} to V_{OUT}	R_{VDD}	V_{DD} = 3V, V_{BAT} = 0V, I_{OUT} = 100mA		4	8	Ω
ON resistance of V_{BAT} to V_{OUT}	R_{BAT}	V_{DD} = 0V, V_{BAT} = 3V, I_{OUT} = 20mA		24	40	Ω
V_{DD} voltage over V_{BAT} for switching	V_{SVDD}	V_{BAT} = 3V, V_{OUT} open	3.00	3.21	3.45	V
V_{DD} voltage under V_{BAT} for switching	V_{SBAT}	V_{BAT} = 3V, V_{OUT} open	2.98	3.08	3.18	V
V_{DD} rising edge switching delay to $\overline{PFO}$ and V_{OUT}	T_{RDD}	V_{BAT} = 3V, V_{DD} rise from 2.8V to 3.5V		14	100	µs
VDD falling edge switching delay to $\overline{PFO}$ and V_{OUT}	T_{FDD}	V_{BAT} = 3V, V_{DD} falling from 3.5V to 2.8V		8	60	µs

Table 4

Timing Characteristics

V_{DD} = 5.0V ±10%, V_{BAT} = 0V, V_{SS} = 0V and T_A = -40 to +85°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Chip select duration, write cycle	t_{CS}		50			ns
Write pulse duration	t_{WR}		50			ns
Time between two transfers	t_W		100			ns
RAM access time (note 1)	t_{ACC}	C_{LOAD} = 50pF		50	60	ns
Data valid to Hi-impedance (note 2)	t_{DF}		10	30	40	ns
Write data settle time (note 3)	t_{DW}		50			ns
Data hold time (note 4)	t_{DH}		10			ns
Advance write time	t_{ADW}		10			ns
$\overline{PF}$ response delay	t_{PF}				100	ns
Rise time (all inputs)	t_R				200	ns
Fall time (all inputs)	t_F				200	ns
$\overline{CS}$ delay after $\overline{A}$ /D (note 5)	$t_{\overline{A}/Ds}$		5			ns
$\overline{CS}$ delay to $\overline{A}$ /D	$t_{\overline{A}/Dt}$		10			ns

Table 5

Note 1: t_{ACC} starts from $\overline{RD}$ ($\overline{DS}$) or $\overline{CS}$, whichever activates last
Typically, t_{ACC} = 5 + 0.9 C_{EXT} in ns; where C_{EXT} (external parasitic capacitance) is in pF

Note 2: t_{DF} starts from $\overline{RD}$ ($\overline{DS}$) or $\overline{CS}$, whichever deactivates first

Note 3: t_{DW} ends at $\overline{WR}$ (R/$\overline{W}$) or $\overline{CS}$, whichever deactivates first

Note 4: t_{DH} starts from $\overline{WR}$ (R/$\overline{W}$) or $\overline{CS}$, whichever deactivates first

Note 5: $\overline{A}$ /D must come before a $\overline{CS}$ and $\overline{RD}$ or a $\overline{CS}$ and $\overline{WR}$ combination. The user has to guarantee this.

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Typical V_{DD} Current vs. Temperature

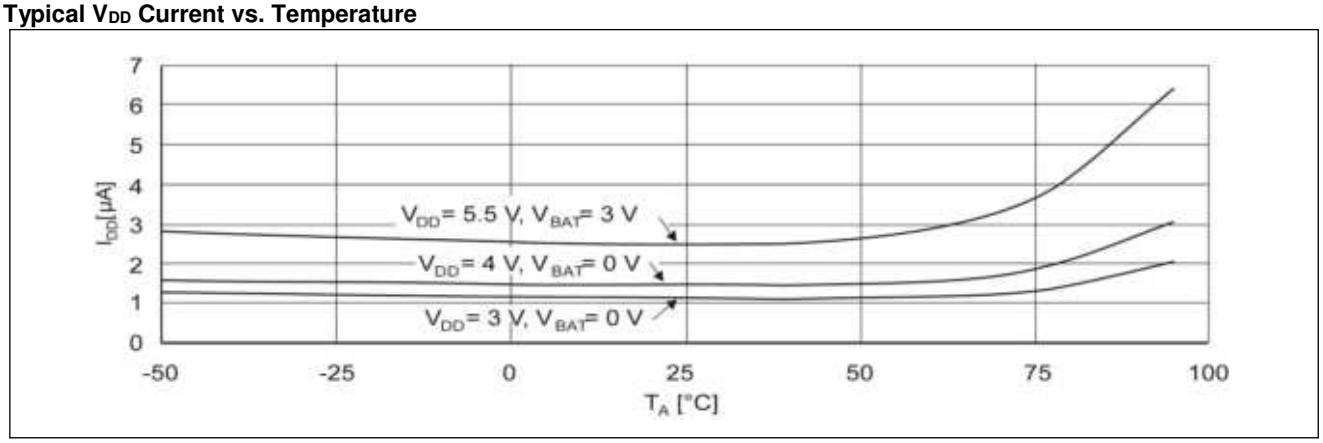


Fig. 3

Typical V_{BAT} Current vs. Temperature

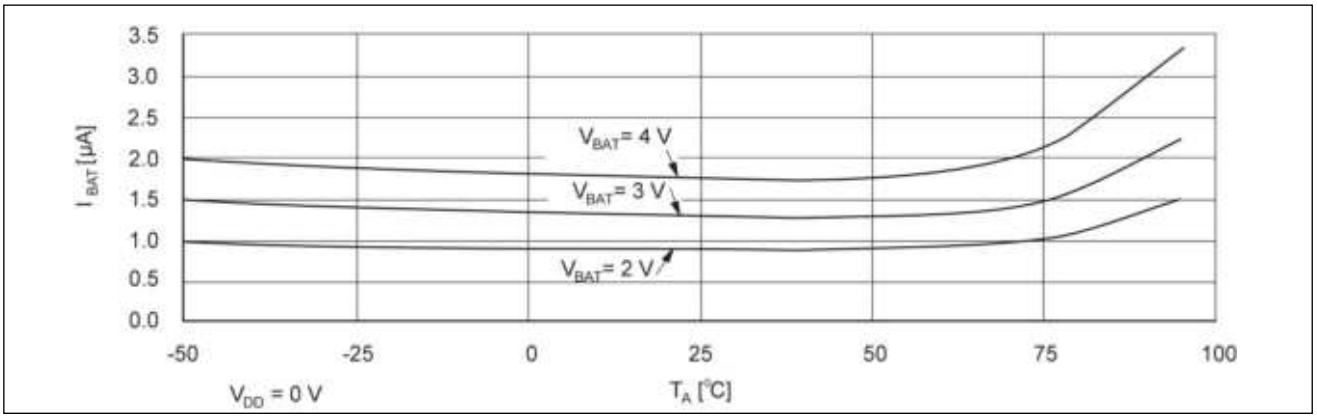


Fig. 4

Typical Frequency on $\overline{IRQ}$

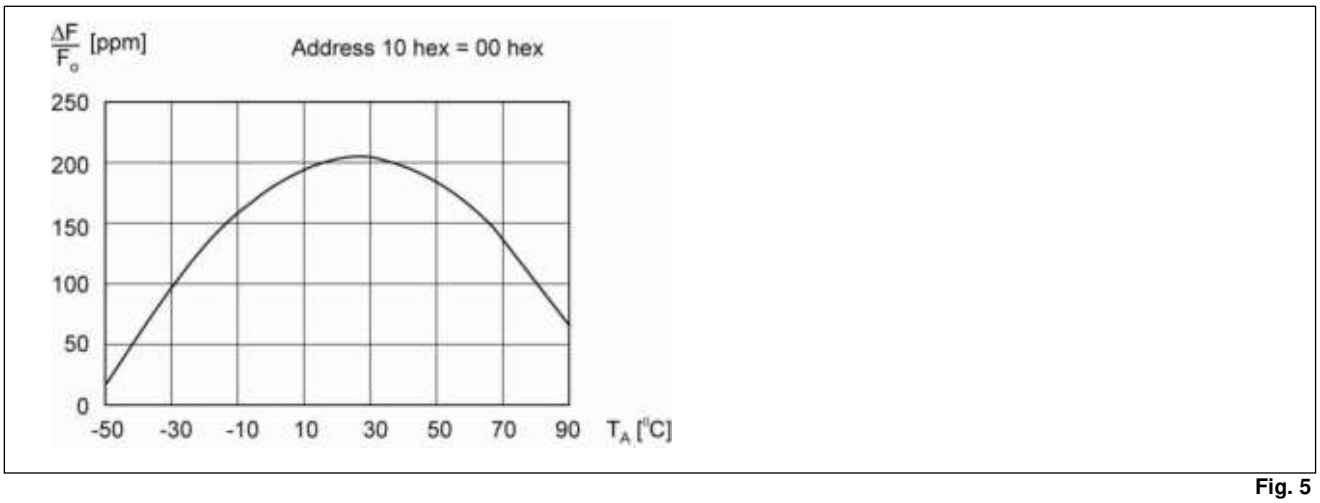
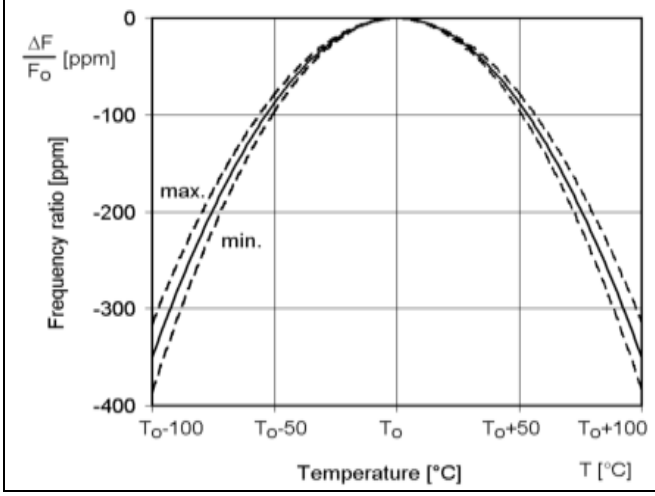


Fig. 5

Module Characteristic



$$\frac{\Delta F}{F_O} = -0.035 \frac{ppm}{°C^2} (T - T_O)^2 \pm 10\%$$

$\Delta F/F_O$ = the ratio of the change in frequency to the nominal value expressed in ppm (it can be thought of as the frequency deviation at any temperature)

T = the temperature of interest in °C

T_O = the turnover temperature (25 ± 5°C)

To determine the clock error (accuracy) at a given temperature, add the frequency tolerance at 25°C to the value obtained from the formula above.

Fig. 6

Typical V_{DD} Switch Resistance vs. Temperature

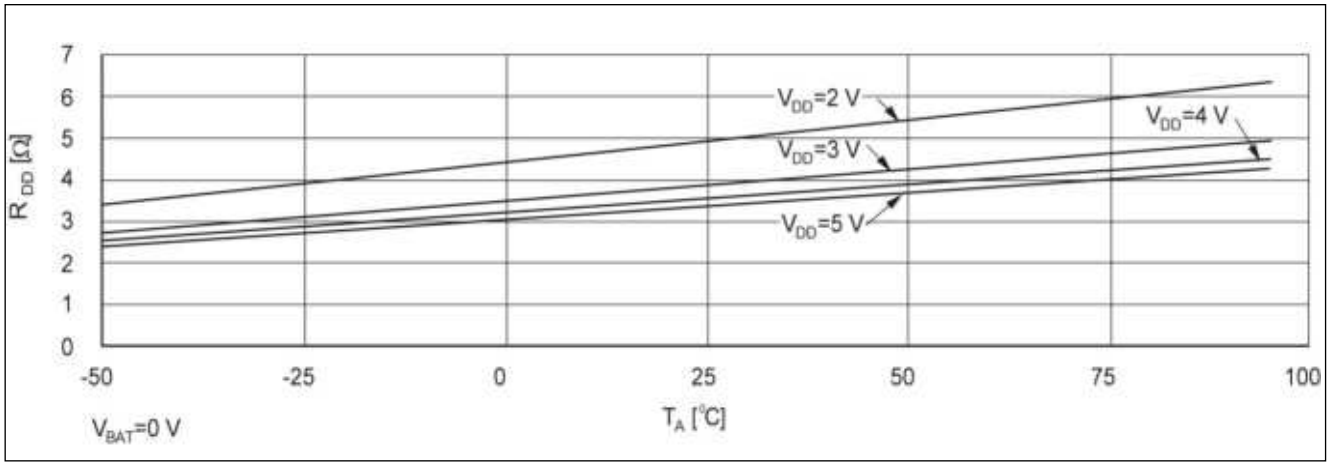


Fig. 7

Typical Battery Switch Resistance vs. Temperature

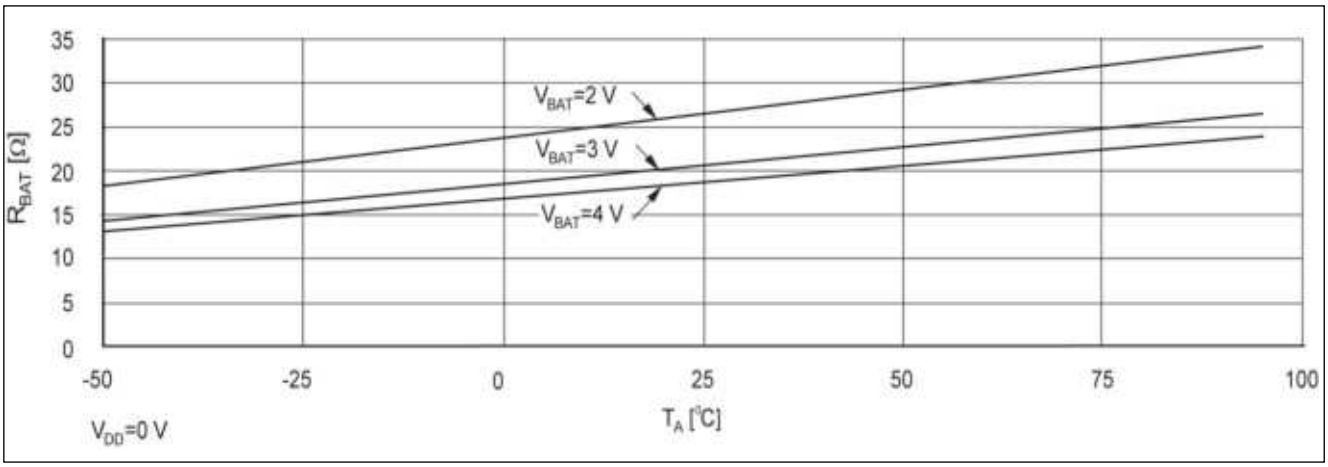


Fig. 8

Timing Waveforms

Read Timing for Intel ($\overline{RD}$ and $\overline{WR}$ Pulse) and Motorola ($\overline{DS}$ or $\overline{RD}$ pin tied to $\overline{CS}$ and R/$\overline{W}$)

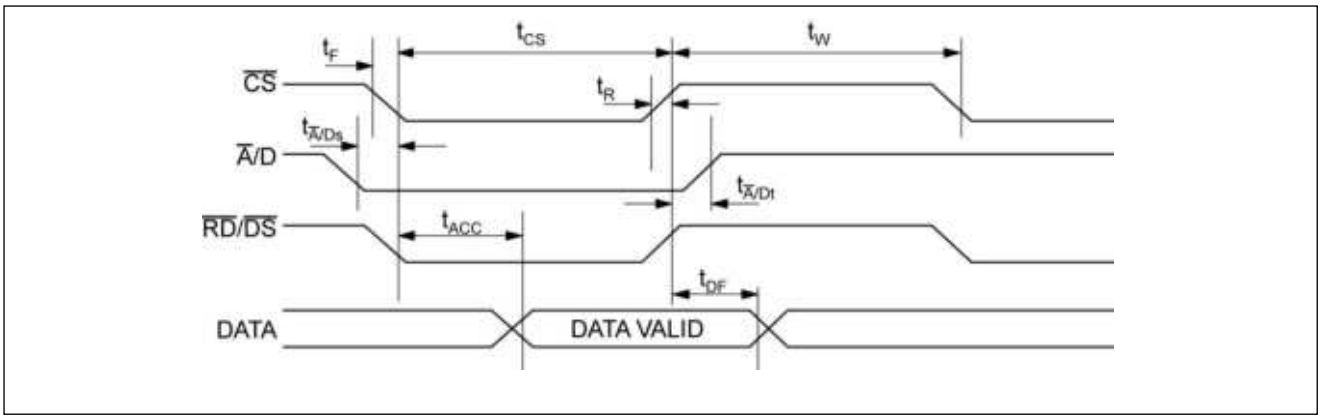


Fig. 9a

Intel Interface
Write Timing

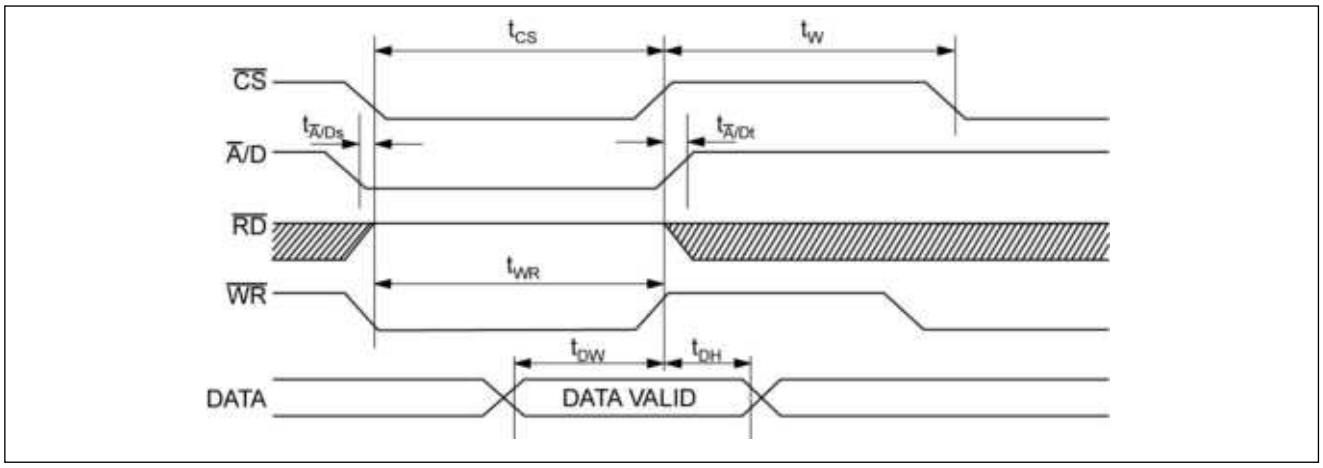


Fig. 9b

Write

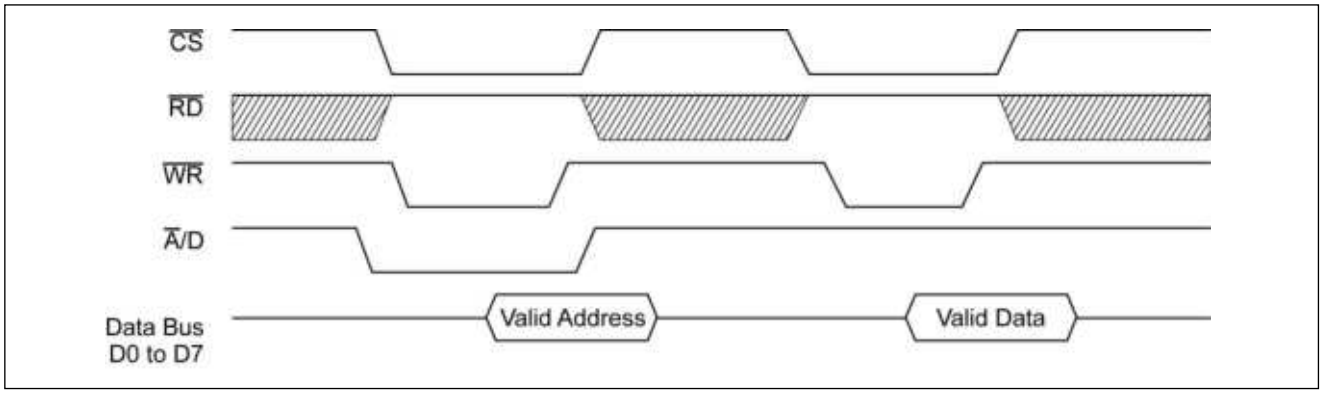


Fig. 9c

Read

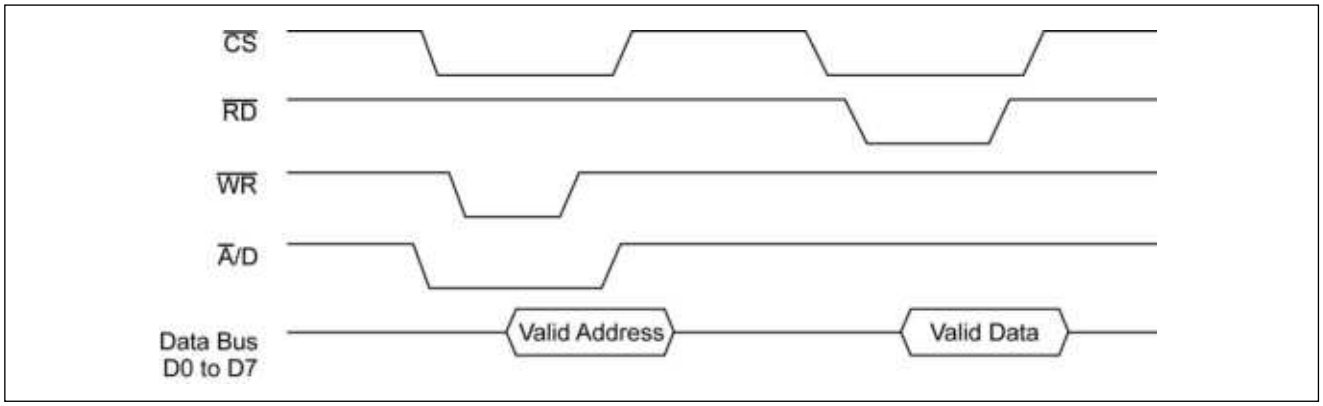


Fig. 9d

Motorola Interface
Motorola Write

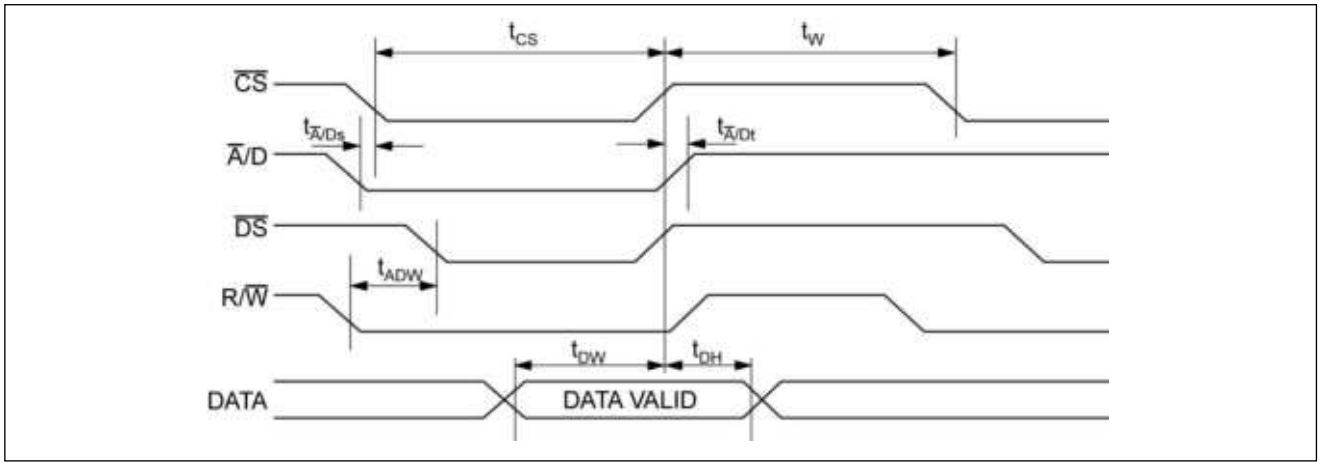


Fig. 9e

Write

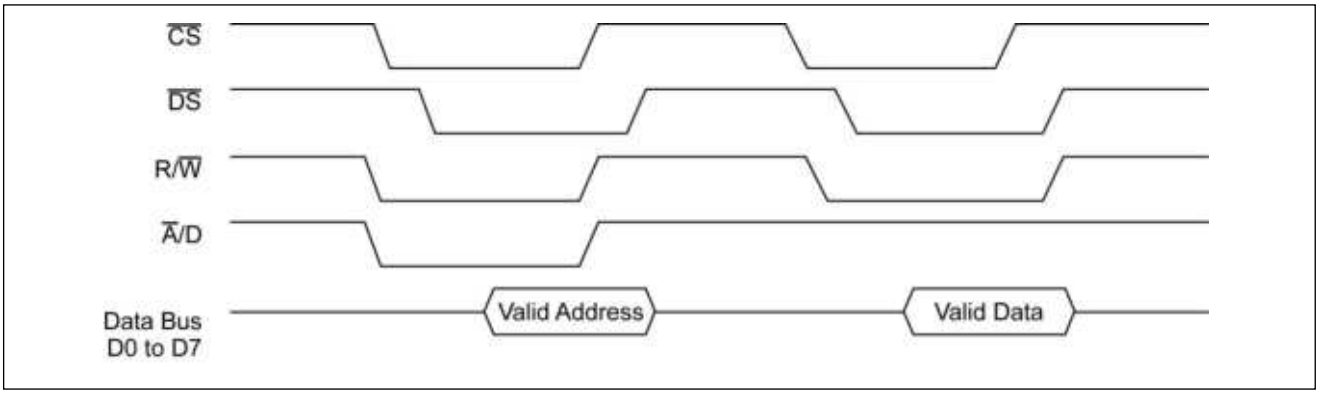


Fig. 9f

Read

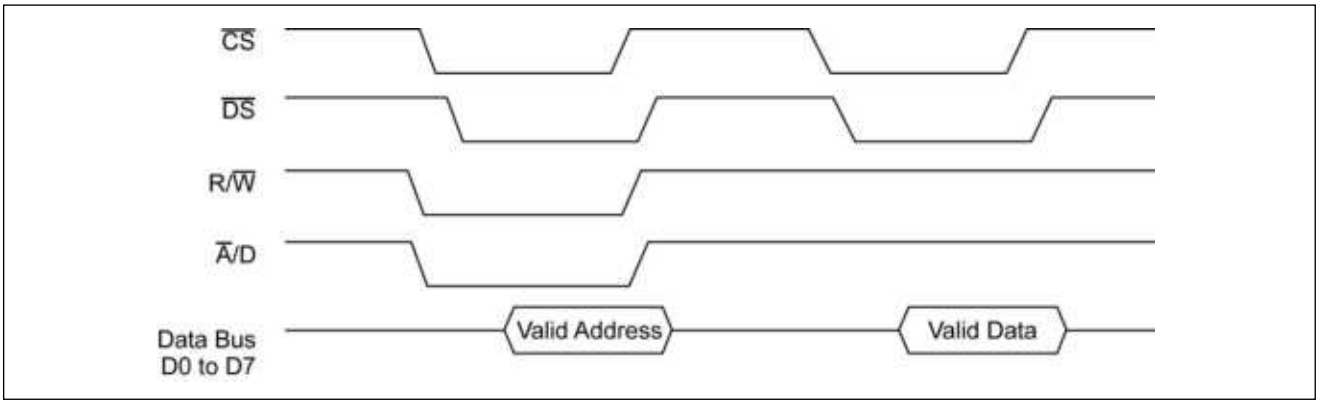


Fig. 9g

General Block Diagram

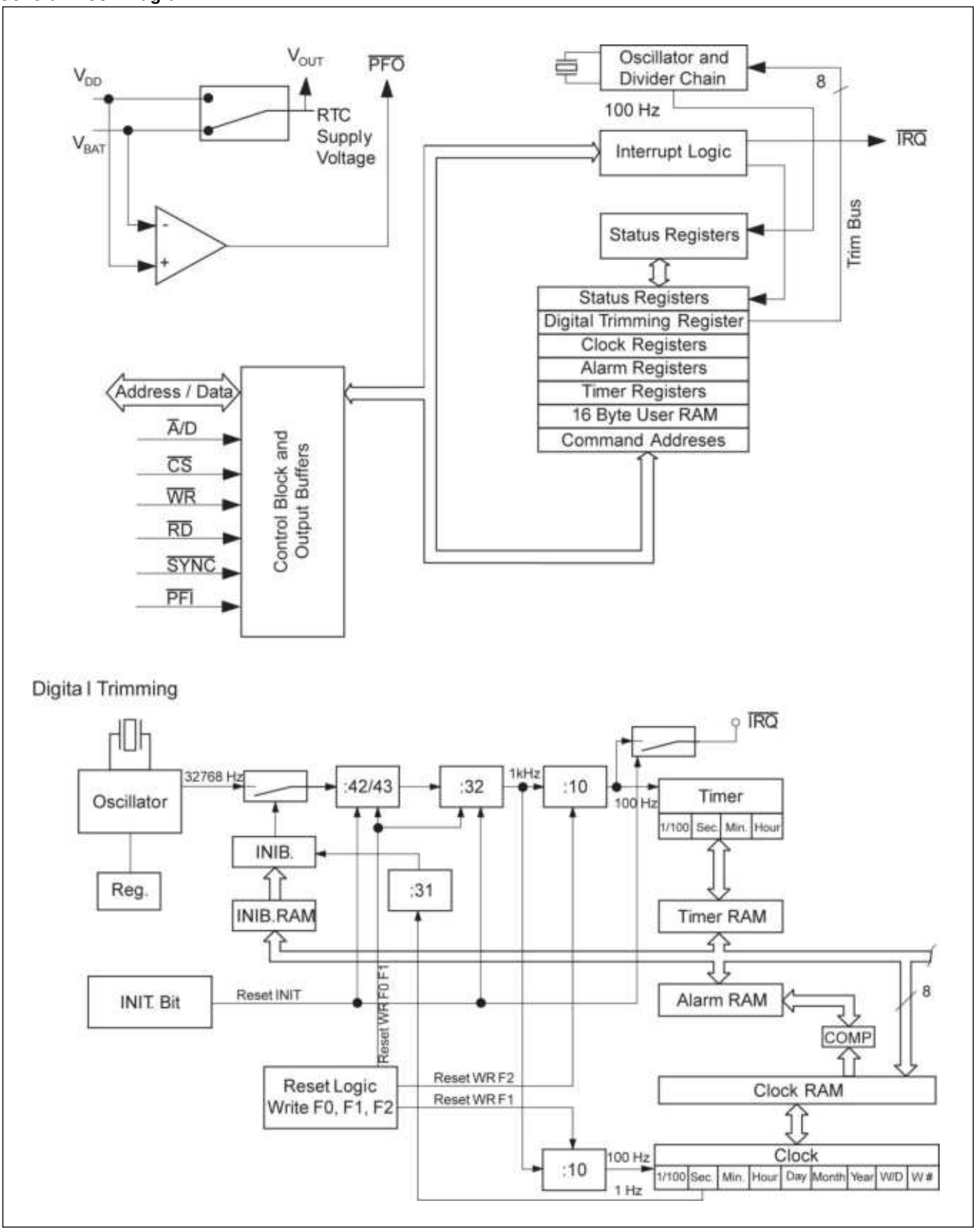


Fig. 10

Pin Description
SO28 Package

Pin	Name	Description	
1	$\overline{SYNC}$	Time synchronization	I
2	$\overline{PFI}$	Power fail	I
3	AD0	Bit 0 from MUX address / data bus	I/O
4	AD1	Bit 1 from MUX address / data bus	I/O
5	AD2	Bit 2 from MUX address / data bus	I/O
6	AD3	Bit 3 from MUX address / data bus	I/O
7	$\overline{A}$ /D	Address / data decode	I
8	$\overline{IRQ}$	Interrupt request	O
9	V_{OUT}	Switch-over output	O
10-14	V_{SS}	Supply ground (substrate)	GND
15-19	V_{DD}	Positive supply terminal	PWR
20	$\overline{PFO}$	Power fail output	O
21	$\overline{CS}$	Chip select	I
22	$\overline{WR}$	$\overline{WR}$ (Intel) or R/$\overline{W}$ (Motorola)	I
23	$\overline{RD}$	$\overline{RD}$ (Intel) or $\overline{DS}$ (Motorola)	I
24	AD4	Bit 4 from MUX address / data bus	I/O
25	AD5	Bit 5 from MUX address / data bus	I/O
26	AD6	Bit 6 from MUX address / data bus	I/O
27	AD7	Bit 7 from MUX address / data bus	I/O
28	V_{BAT}	Battery supply	PWR

Table 6

Functional Description
Power Supply, Data Retention and Standby

The V3025 is put in standby mode by activating the $\overline{PFI}$ input. When pulled logic low, $\overline{PFI}$ will disable the input lines, and immediately take to high impedance the lines AD 0-7. Input states must be under control whenever $\overline{PFI}$ is deactivated. If no specific power fail signal can be provided, $\overline{PFI}$ can be tied to the system $\overline{RESET}$. Even in standby the interrupt request pin $\overline{IRQ}$ will pull to ground upon an unmasked alarm interrupt occurring.

Switch-over

The switch-over supplies the core of the RTC. The I/O pads are supplied by V_{DD}, except for $\overline{IRQ}$ and $\overline{SYNC}$. The $\overline{SYNC}$ input is internally pulled-up to V_{OUT}, $\overline{IRQ}$ can be externally pulled-up between 2 and 5.5V. The switch-over circuitry works in recovery mode. During switching, both transistors (V_{DD} to V_{OUT} and V_{BAT} to V_{OUT}) are ON. This is to guarantee that the RTC is always supplied. The power fail signal becomes active ($\overline{PFO}$ = 0) when $V_{DD} < V_{BAT}$ (see Table 4).

Initialisation

When power is first applied to the V3025 all registers have a random value.
To initialise the V3025, software must first write a 1 to the initialisation bit (addr. 2 bit 4) and then a 0. This sets the Frequency Tuning bit and clears all other status bits.
The time and date parameters should then be loaded into the RAM (addr. 20 to 28 hex) and then transferred to the reserved clock area using the clock command followed by a write.
The digital trimming register must then be initialised by writing 210 (D2 hex) to it, if Frequency Tuning is not required. After having written a value to the digital trimming register the frequency tuning mode bit can be cleared.

RAM Configuration

The RAM area of the V3025 has a reserved clock and time area, a data space, user RAM and an address command space (see Table 10 or Fig. 10). The reserved clock and timer area is not directly accessible to the user, it is used for internal time keeping and contains the current time and date plus the timer parameters.

Data Space

All locations in the data space are Read/Write. The data space is directly accessible to the user and is divided into five areas:
Status Registers – three registers used for status and control data for the device (see Table 7, 8 and 9).
Reserved bits must be set to 0.
Digital Trimming Register – a special function described under "Frequency Tuning".
Time and Date Registers – 9 time and date locations which are loaded with, either the current time and date parameters from the reserved clock area or the time and date parameters to be transferred to the reserved clock area.
Alarm Registers – 5 locations used for setting the alarm parameters.
Timer Registers – 4 locations which are loaded with either the timer parameters from the reserved timer area or the timer parameters to be transferred to the reserved timer area.

User RAM

The V3025 has 16 bytes of general purpose RAM available for the users applications. This RAM block is located at addresses 50 to 5F hex and is maintained even in the standby mode ($\overline{PFI}$ active). The commands, or the time set lock bit, have no effect on the user RAM block. Reading or writing to the user RAM is similar to reading or writing to any system RAM address.

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Status Words

Status 0 - Address 00 Hex

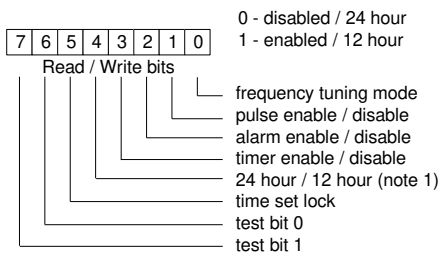


Table 7

Status 1 - Address 01 Hex

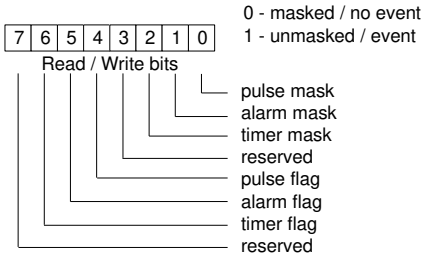


Table 8

Status 2 - Address 02 Hex

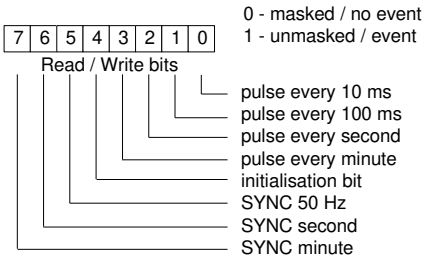


Table 9

Address Command Space

This space contains the three commands used for carrying out the transfers between the Time and Data Register and / or the Timer Registers and the reserved clock and timer area.

RAM Map

Address Dec	Address Hex	Parameter	Range
Data Space			
Status			
00	00	status 0	
01	01	status 1	
02	02	status 2	
Special purpose			
16	10	digital trimming	0-255
Clock			
32	20	1/100 second	00-99
33	21	seconds	00-59
34	22	minutes	00-59
35	23	hours (note 1)	00-23
36	24	date	01-31
37	25	month	01-12
38	26	year	00-99
39	27	week day	01-07
40	28	week number	00-53
Alarm			
48	30	1/100 second	00-99
49	31	seconds	00-59
50	32	minutes	00-59
51	33	hours (note 1 & 2)	00-23
52	34	date	01-31
Timer			
64	40	1/100 second	00-99
65	41	seconds	00-59
66	42	minutes	00-59
67	43	hours	00-23
User RAM			
80	50	user RAM, byte 0	
81	51	user RAM, byte 1	
82	52	user RAM, byte 2	
83	53	user RAM, byte 3	
84	54	user RAM, byte 4	
85	55	user RAM, byte 5	
86	56	user RAM, byte 6	
87	57	user RAM, byte 7	
88	58	user RAM, byte 8	
89	59	user RAM, byte 9	
90	5A	user RAM, byte 10	
91	5B	user RAM, byte 11	
92	5C	user RAM, byte 12	
93	5D	user RAM, byte 13	
94	5E	user RAM, byte 14	
95	5F	user RAM, byte 15	
Address Command Space			
240	F0	clock and timer transfer	
241	F1	clock transfer	
242	F2	timer transfer	

Table 10

Note 1: The MSB (bit 7) of the hours byte (addr. 23 hex for the clock and 33 hex for the alarm) are used as AM/PM indicators in the 12 hour time data format and reading of the hours byte must be preceded by masking of the AM/PM bit. A set AM/PM bit indicates PM. In the 24 hour time data format the bit will always be zero.

Note 2: The alarm hours, addr. 33 hex, must always be rewritten after a change between 12 and 24 hour modes.

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Communication
Data transfer is in 8 bit parallel form. All time data is in packed BCD format with tens data on lines AD7-4 and units on lines AD3-0. To access information within the RAM (see Fig.10) first write the RAM address, then read or write from or to this location. Fig.11 shows the two steps needed.
The lines AD0-7 will be treated as an address when pin $\overline{A}$/D is low, and as data when $\overline{A}$/D is high. Pin $\overline{A}$/D must not change state during any single read or write access. One line of the address bus (e.g. A0) can be used to implement the $\overline{A}$/D signal (see "Typical Operating Configuration", Fig.1). Until a new address is written, data accesses ($\overline{A}$/D high) will always be to the same RAM address.

Communication Sequence

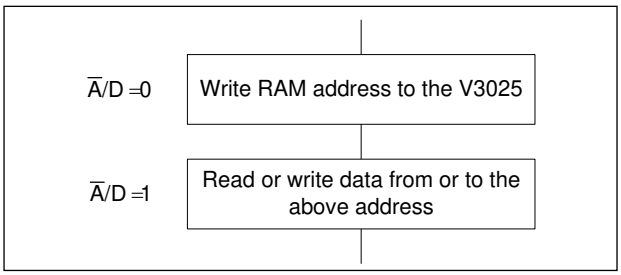


Fig. 11

Access Considerations
The communication sequence shown in Fig.11 is re-entrant. When the address is written to the V3025 (ie. first step of the communication sequence) it is stored in an internal address latch. Software can read the internal address latch at any time by holding the $\overline{A}$/D line low during a read from the V3025. So, for example, an interrupt routine can read the address latch and push it on to a stack, popping it when finished to restore the V3025.
N.B. Alarm and timer interrupt routines can reprogram the alarm and timer without it being necessary to read or reprogram the clock.

Commands
The commands allow software to transfer the clock and timer parameters in a sequence (eg. seconds, minutes, hours, etc.) without any danger of an internal time update with carry over corrupting the data. They also avoid delaying internal time updates while using the V3025, as updates occurring in the reserved clock and timer area are invisible to software. Software writes or reads parameters to or from the RAM only.
There are three commands that occupy the command address space in the RAM. The function of these commands is to transfer data from the reserved clock and timer area to the RAM or to transfer data in the opposite direction, from the RAM to the reserved clock and timer area.
The commands take place in two steps as do all other communications. The command address is sent with $\overline{A}$/D low. This is followed by either a read ($\overline{RD}$) or a write ($\overline{WR}$), with $\overline{A}$/D high, to determine the direction of the transfer. If the second step is a read then the data is transferred from the reserved clock and timer area to the RAM and if the second step is a write then the data that has already been loaded into the RAM clock and/or timer locations is transferred to the reserved clock and/or timer area.

Clock and Calendar
The time and date locations in RAM (see Table 10) provide access to the 1/100 seconds, seconds, minutes, hours, date, month, year, week day and week number. These parameters have the ranges indicated in Table 10. The V3025 may be programmed for 12 or 24 hour time format (see section "12/24 Data Format"). If a parameter is found to be out of range, it will be cleared when the units value on its being next incremented is equal to or greater than 9 eg. B2 will be set to 00 after the units have incremented to 9 (ie. B9 to 00). The device incorporates leap year correction and week number calculation at the beginning of a year. If the first day of the year is day 05, 06 or 07 of the week, then it is given a zero week number, otherwise it becomes week 1. Week days are numbered from 1 to 7 with Monday as day 1.
Reading of the current time and date must be preceded by a clock command. The time and date from the last clock command is held unchanged in RAM.
When transferring data to the reserved clock and timer area remember to clear the time set lock bit first.

Timer
The timer can be used either for counting elapsed time, or for giving an interrupt ($\overline{IRQ}$) on being incremented from 23:59:59:99 to 00:00:00:00. The timer counts up with a resolution of 1/100 second in the timer reserved areas. The timer enable/disable bit (addr. 00 hex, bit 3) must be set by software to allow the timer to be incremented. The timer is incremented in the reserved timer area, every internal time update (10 ms). The timer flag (addr. 01 hex, bit 6) is set when the timer rolls over from 23:59:59:99 to 00:00:00:00 and the $\overline{IRQ}$ becomes active if the timer mask bit (addr. 01, bit 2) is set. The $\overline{IRQ}$ will remain active until software acknowledges the interrupt by clearing the timer flag. The timer is incremented in the standby mode, however it will not cause $\overline{IRQ}$ to become active until power (V_{DD}) has been restored.

Note: The user should ensure that a time lapse of at least 60 microseconds exists between the falling edge of the $\overline{IRQ}$ and the clearing of the timer flag.

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Reading the Clock

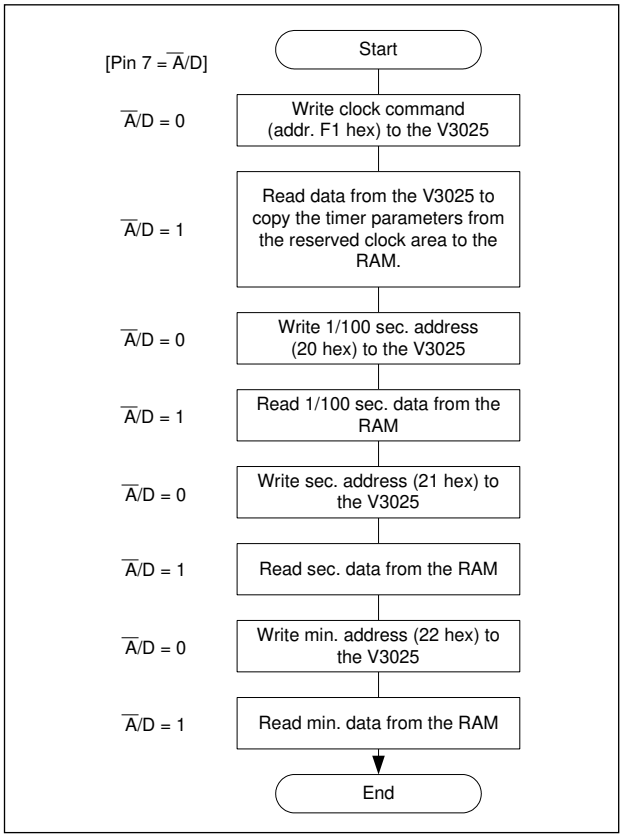


Fig. 12

Setting the Timer (Time Set Lock Bit = 0)

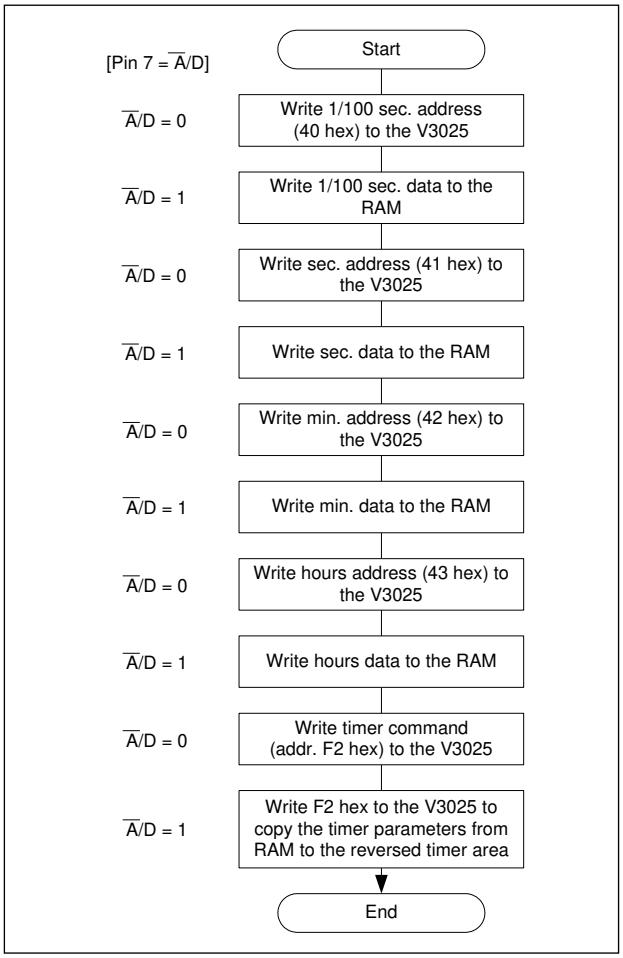


Fig. 13

Note: Commands are only valid as commands when the $\overline{A}$/D line is low. Writing F2 hex with the $\overline{A}$/D line high, as in the last box of Fig. 11, serves only to activate the V3025 write pin which determines the direction of transfer.

Alarm

An alarm date and time may be preset in RAM addresses 30 to 34 hex. The alarm function can be activated by setting the alarm enable / disable bit (addr. 00 hex, bit 2). Once enabled the preset alarm time and date are compared, every internal time update cycle (10 ms), with the clock parameters in the reserved clock area. When the clock parameters equal the alarm parameters the alarm flag (addr. 01 hex, bit 5) is set. If the alarm mask bit (addr. 01 hex, bit 1) is set, the $\overline{IRQ}$ pin goes active. The alarm flag indicates to software the source of the interrupt. $\overline{IRQ}$ will remain active until software acknowledges the interrupt by clearing the alarm flag. If the alarm is enabled, and an alarm address set to FF hex, this parameters is not compared with the associated clock parameter. Thus it is possible to achieve a repeat feature where an alarm occurs every programmed number of seconds, or seconds and minutes, or seconds, minutes and hours. The V3025 pulls the open drain $\overline{IRQ}$ line active low during standby when an alarm interrupt occurs.

If the 12/24 hour mode is changed then the alarm hours must be re-initialised.

Note: The user should ensure that a time lapse of at least 60 microseconds exists between the falling edge of the $\overline{IRQ}$ and the clearing of the alarm flag.

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$\overline{IRQ}$

The $\overline{IRQ}$ output is used by 4 of the V3025's features.
These are:

1. Pulse, to provide periodic interrupts to the microprocessors at pre-programmed intervals;
2. Alarm to provide an interrupt to the microprocessor at a pre-programmed time and date;
3. Timer, to provide an interrupt to the microprocessor when the time rolls over from 23:59:59:99 to 00:00:00:00; and
4. Frequency trimming (see section "Frequency Trimming").

The first 3 features listed are similar in the way they provide interrupts to the microprocessor. Each of the 3 has an enable / disable bit, a flag bit, and an interrupt mask bit. The enable / disable bit allows software to select a feature or not. A set flag bit indicates that an enable feature has reached its interrupt condition. Software must clear the flag bit. The interrupt mask bit allows or disallows the $\overline{IRQ}$ output to become active when the flag bit is se. The $\overline{IRQ}$ output becomes active whenever any interrupt flag is set which also has its mask bit set. For all sources of maskable interrupts within the V3025, the $\overline{IRQ}$ output will remain active until software clears the interrupt flag. The $\overline{IRQ}$ output is the logical OR of all the unmasked interrupt flags. The $\overline{IRQ}$ output is open drain so an external pullup to V_{DD} is needed. In standby ($\overline{PF}$ active) the $\overline{IRQ}$ output will be active if the alarm mask bit (addr, 01 hex, bit 1) is set and the alarm flag is also set. The timer or the pulse feature cannot cause the $\overline{IRQ}$ output to become active while in standby.

Snychronization

There are 3 ways to synchronize the V3025. It can be synchronized to 50 Hz, the nearest second, or the nearest minute. Synchronization mode is selected by setting one of the bits 5 to 7 at addr. 02 hex, in accordance with Table 8. If more than one bit is set then all the synchronization bits are disabled. If the $\overline{SYNC}$ input is set low for longer than 200 µs, while in the synchronization mode, the clock will synchronize to the falling edge of the signal. Synchronization to the nearest second implies that the 1/100 seconds are cleared to zero and if the contents were > 50, the seconds register is incremented. Synchronization to the nearest minute implies that the seconds are cleared to zero and if the contents were > 30, the minutes register is incremented. Fractions of seconds are cleared.

Pulse

There are 4 programmable pulse frequencies available on the V3025, these are every 10 ms, 100 ms, second or minute. The pulse feature is activated by setting the pulse enable / disable bit at address 00, bit 1. The pulse frequency is selected by setting one of the bit 0 to 3 at address 02 hex (see Table 9). If more than one of the pulse bits is set then the feature is disabled. At the selected interval the pulse flag bit (addr. 01 hex, bit 4) is set. If the pulse mask bit (addr. 01 hex, bit 0) is set then the $\overline{IRQ}$ pin goes active. The pulse flag indicates to software the source of the interrupt. $\overline{IRQ}$ will remain active until software acknowledges the interrupt by clearing the pulse flag. The pulse feature is disabled while in standby. Upon power restoration the pulse feature is enabled if enabled prior to standby. See also the section "Frequency Tuning".
Note: The user should ensure that a time lapse of at least 60 microseconds exists between the falling edge of the $\overline{IRQ}$ and the clearing of the pulse flag.

Time Set Lock

The time set lock control bit is located at address 00 hex, bit 5 (see Table 7). When set by software, this bit disables any transfer from the RAM to the reserved clock and timer area as well as inhibiting any write to the digital trimming register at address 10 hex. When the time set lock bit is set the following transfer operations are disabled:

The clock command followed by write,
the timer command followed by write,
the clock and timer command followed by write, and
writing to the digital trimming register

A set bit prevents unauthorized overwriting of the reserved clock and timer area. Reading of the reserved clock and timer area, using the commands, is not affected by the time set lock bit. Clearing the time set lock bit by software will re-enable the above listed commands. On initialisation the time set lock bit is cleared. The time set lock bit does not affect the user RAM (addr. 50 to 5F hex).

Frequency Tuning

The V3025 offers a key feature called "Digital Trimming", which is used for the clock accuracy adjustment. Unlike the traditional capacitor trimming method which tunes the crystal oscillator, the digital trimming acts on the divider chain, allowing the clock adjustment by software. The oscillator frequency itself is not affected.

The Principle of Digital Trimming

With the digital trimming disabled (ie. digital trimming register set to 00 hex), the oscillator and the first stages of the divider chain will run slightly too fast (typ. 210 ppm: ppm = parts per million), and will generate a 100 Hz signal with a frequency of typically 100.021 Hz. To correct this frequency, the digital trimming logic will inhibit every 31 seconds, a number of clock pulses, as set in the digital trimming register. Since the duration of 31 seconds corresponds to 1'015'808 oscillator cycles, the digital trimming has a resolution of 0.984 ppm. In other words every increment by 1 of the digital trimming value will slow down the clock by 0.984 ppm, which permits the accuracy of ± 0.5 ppm to be reached. Note that a 1 ppm error will result in a 1 second difference after 11.5 days, or a 1 minute difference after 694 days ! The trimming range of the V3025 is from 0 to 251 ppm. The 251 ppm correction is obtained by writing 255 (FFhex) into the digital trimming register.

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How to Determine the Digital Trimming Value
The value to write into the digital trimming register has to be determined by the following procedure:

1. Initialise the V3025 by writing a 1 and then a 0 into the "Initialisation Bit" of the status register 2 (addr. 02 hex, bit 4). This activates the frequency tuning mode in status register 0 (addr. 00 hex, bit 1) and clears the other status bits.
2. Write the value 00 hex into the digital trimming register (addr 10 hex). From now, the $\overline{IRQ}$ output (open drain) will deliver the 100 Hz signal, which has a 20% duty cycle.
3. Measure the duration of 21 pulses at the $\overline{IRQ}$ output, with the trigger set for the falling edge. It is possible also to divide the $\overline{IRQ}$ frequency by 21, using a TTL or CMOS external circuit.
4. Compute the frequency error in ppm:
   $$\text{freq. error} = \frac{210\text{ms} - \text{measuredvalueinms}}{210\text{ms}} \times 10^6$$
5. Compute the corrective value to write into the digital trimming register.
   Digital trimming value = frequency error / 0.984
6. Write this value into the digital trimming register.
7. Switch off the frequency tuning mode in status 0 (addr. 00 hex, bit 0 set to 0).

The Real Time Clock circuit will now run accurately at an operating temperature equal to the calibration temperature. If the operating temperature differs from the one at calibration time, the graphs shown on Fig. 5 and 6 will help in determining the definitive value. If the mean operating temperature of the equipment is not known at calibration time, the equipment user will do the final correction with a software provided by the system designer. To avoid the calibration procedure, it is possible also to set the digital trimming register to 210 (D2 hex) as a standard starting value, and let the final equipment user perform the final adjustment on site, which will take the real temperature into account.

Time Correction at Room Temperature
Let us consider that the duration of 21 pulses of the $\overline{IRQ}$ signal is 209.960 ms at room temperature.

The frequency error is:
$(210 - 209.960) / 210 \times 10^6 = 190.476$ ppm

The value for the digital trimming register is:
190.476 / 0.984 = 193.57, rounded to 194 (B2 hex)

Time Correction with Change of Temperature
If the mean temperature on site is known to be 45°C, the frequency error determined at room temperature has to be modified using the graphs or the equation of Fig. 6

$$\Delta f/f = -0.035 \times (45-25)^2 = -14.0 \text{ ppm}$$

The trimming value for 45°C will be:
(190.476 ppm – 14.0 ppm) / 0.984 = 179.34, rounded to 179 (A3 hex)

12 / 24 Hour Data Format
The V3025 can run in 12 hour data format. On initialisation the 12/24 hour bit addr. 00 bit 4 is cleared putting the V3025 in 24 hour data format. If the 12 hour data format is required then bit 4 at addr. 00 must be set. In the 12 hour data format the AM/PM indicator is the MSB of the hours register addr. 23 bit 7. A set bit indicates PM. When reading the hours in the 12 hour data format software should mask the MSB of the hours register. In the 24 hour data format the MSB is always zero.
The internal clock registers change automatically between 12 and 24 hour mode when the 24/12 hour bit is changed. **The alarm hours however must be rewritten.**

Test
From the various test features added to the V3025 some may be activated by the user. Table 7 shows the test bits. Table 11 shows the three available modes and how they may be activated.
The first accelerates the incrementing of the parameters in the reserved clock and timer area by 32.
The second causes all clock and timer parameters, in the reserved clock and timer area, to be incremented in parallel at 100 Hz with no carry over, ie. independently of each other.
The third test mode combines the previous two resulting in parallel incrementing at 3.2 kHz.
While test bit 1 is set (addr. 00 hex, bit 7) the digital trimming action is disabled and no pulses are removed from the divider chain. Test bit 0 (addr. 00 hex, bit 6) can be combined with digital trimming (see section "Frequency Tuning").
To leave test, the test bits (addr 00 hex, bits 6 and 7) must be cleared by software. Test corrupts the clock and timer parameters and so all parameters should be re-initialised after a test session.

Test Modes

Addr. 00hex bit 7	Addr. 00hex bit 6	Function
0	0	Normal operation
0	1	Acceleration by 32
1	0	Parallel increment of all clock and timer parameters at 100 Hz with no carry over; dependent on the status of bit 3 at address 00 hex
1	1	Parallel increment of all clock and timer parameters at 3.2 kHz with no carry over; dependent on the status of bit 3 at address 00 hex

Table 11

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Typical Operating Configuration

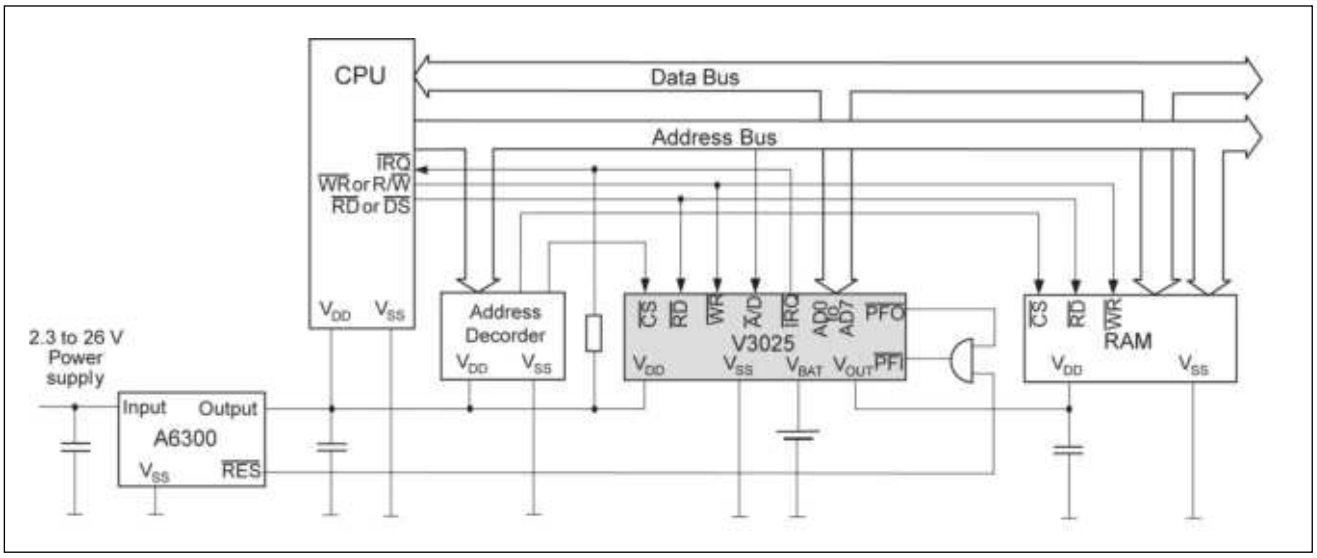


Fig. 14

Process Application

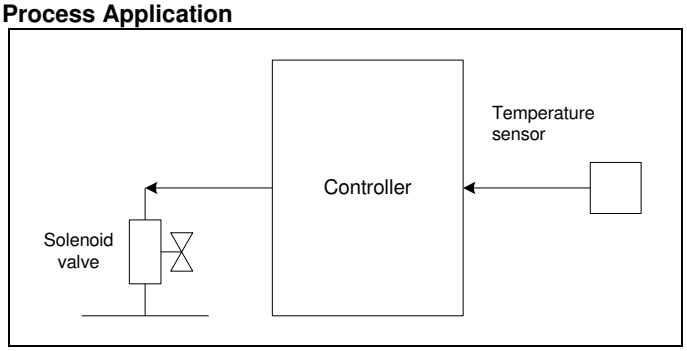


Fig. 15

- The formula in Fig. 5 is used by software to continually update the digital trimming register and so compensate the V3025 for the ambient temperature.
- The timer is used to measure the duration the valve is on.
- The alarm feature is used to turn the controller power on and off at the time programmed by software. The V3025 pulls $\overline{IRQ}$ active low on an alarm even in standby and thus can control the power on/off switch for the controller.

Typical Applications

V3025 Interfaced with Intel CPU ($\overline{RD}$ and $\overline{WR}$ pulse)

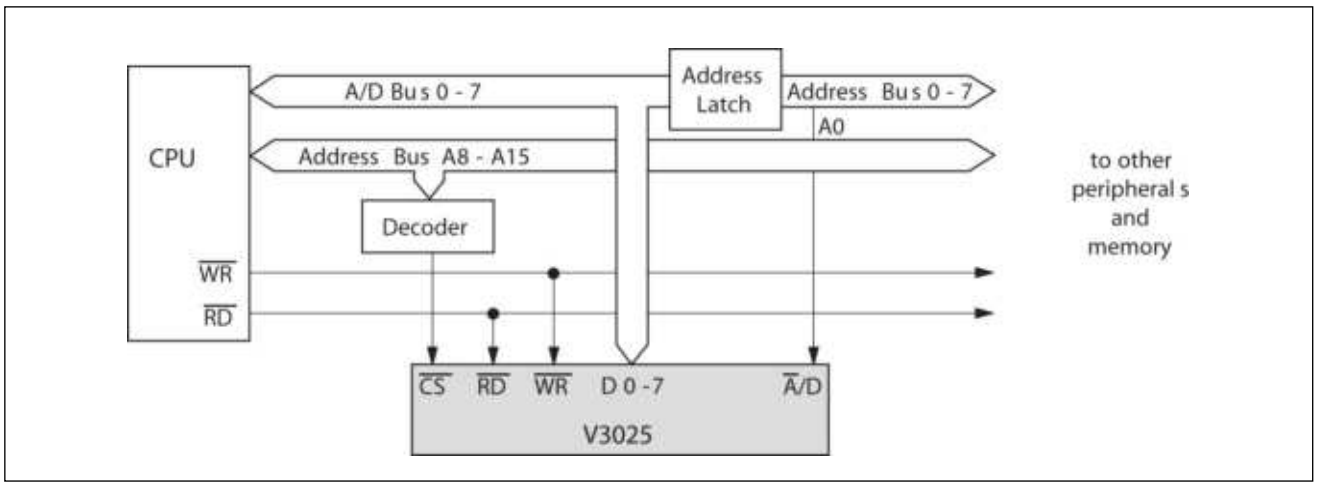


Fig. 16

V3025 Interfaced with Motorola CPU ($\overline{DS}$ or $\overline{RD}$ pin tied to $\overline{CS}$, and R/ $\overline{W}$)

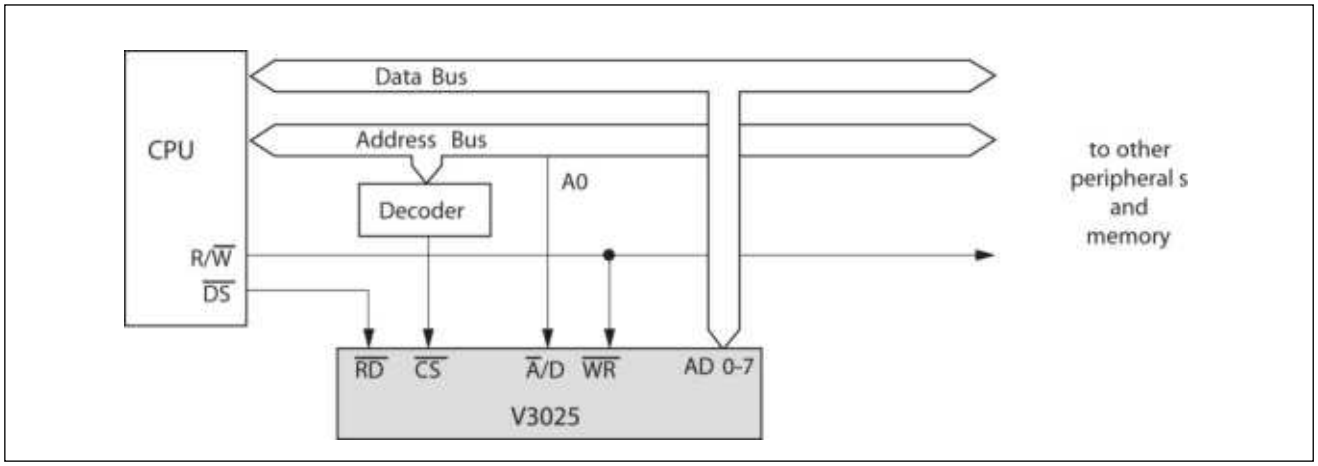
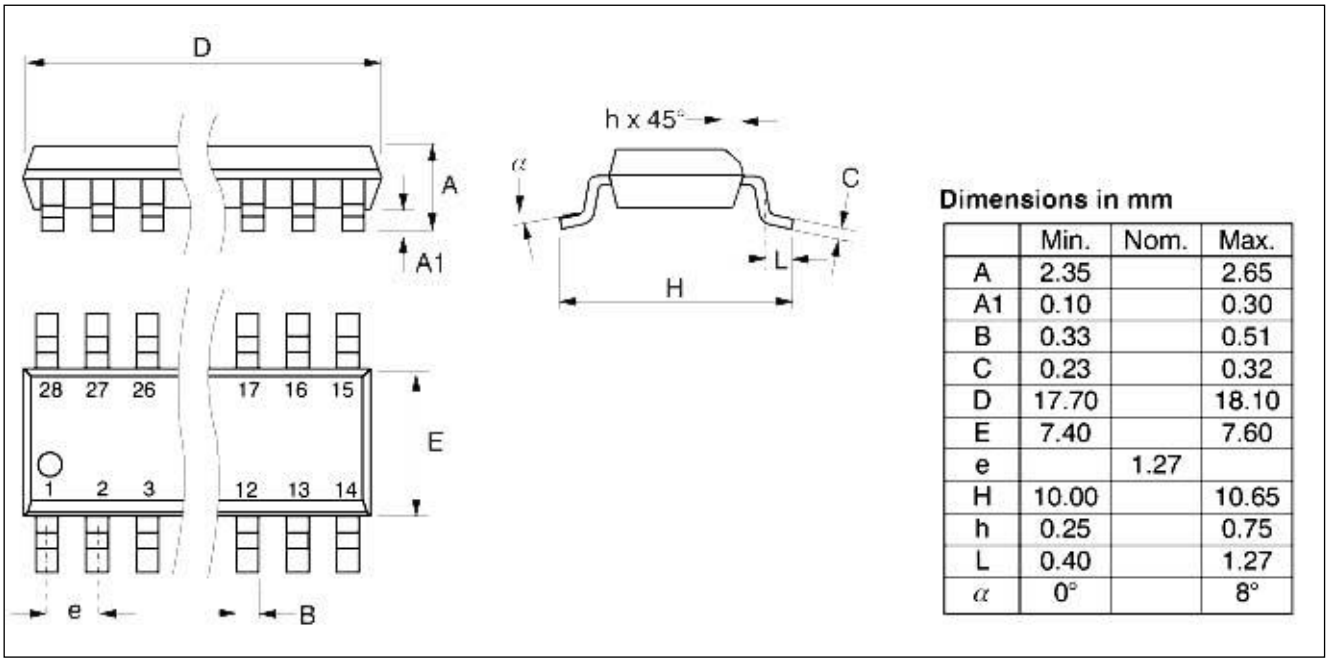


Fig. 17

Ordering and Package Information

Dimensions of 28-pin SOIC Package



Dimensions in mm

	Min.	Nom.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D	17.70		18.10
E	7.40		7.60
e		1.27	
H	10.00		10.65
h	0.25		0.75
L	0.40		1.27
α	0°		8°

Fig. 18

Ordering Information

When ordering, please specify the complete part number.

Part Number	**Package**	**Delivery Form**	**Package Marking** (first line)
V3025SO28B+	28-pin SOIC	Tape & Reel	V3025A 28SI
V3025SO28A+	28-pin SOIC	Stick	V3025A 28SI

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