Dual 150mA Positive/Negative Low Noise Low Dropout Linear Regulator

FEATURES

- **Low Noise: 20μV_{RMS} (Positive) and 30μV_{RMS} (Negative)**
- **Low Quiescent Current: 30μA/Channel**
- **Wide Input Voltage Range: ±2.3V to ±20V**
- **Output Current: ±150mA**
- **Low Shutdown Current: <3μA Total (Typical)**
- **Low Dropout Voltage: 300mV/Channel**
- Fixed Output Voltages: ±3.3V, ±5V, ±12V, ±15V
- Adjustable Outputs from ±1.22V to ±20V
- No Protection Diodes Needed
- Stable with 2.2μF Output Capacitors
- Stable with Ceramic, Tantalum or Aluminum Capacitors
- Starts into Reverse Output Voltage
- Current Limit and Thermal Limit
- Low Profile 14-Lead 4mm × 3mm × 0.75mm DFN Package

APPLICATIONS

- Battery-Powered Instruments
- Bipolar Power Supplies
- Low Noise Power Supplies

DESCRIPTION

The LT®3032 is a dual, low noise, positive and negative low dropout voltage linear regulator. Each regulator delivers up to 150mA with a typical 300mV dropout voltage. Each regulator's quiescent current is low (30μA operating and <3μA in shutdown) and well-controlled in dropout, making it an excellent choice for battery-powered circuits.

Another key feature of the LT3032 is low output noise. Adding an external 10nF bypass capacitor to each regulator reduces output noise to 20μV_{RMS}/30μV_{RMS} over a 10Hz to 100kHz bandwidth. The LT3032 is stable with minimum output capacitors of 2.2μF. The regulators do not require the addition of ESR as is common with other regulators.

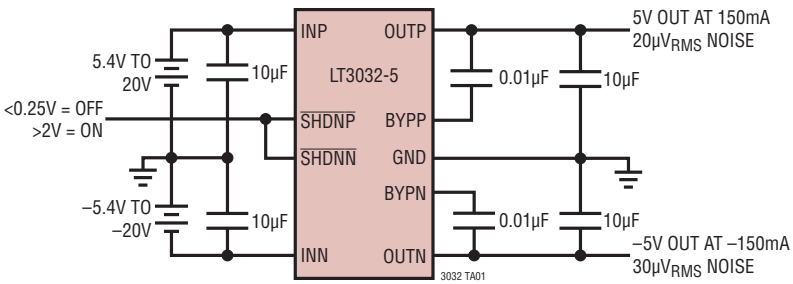
The regulators are offered as adjustable output devices with an output voltage down to the ±1.22V reference voltage or in fixed voltages of ±3.3V, ±5V, ±12V and ±15V. Internal protection circuitry includes reverse-output protection, current limiting and thermal limiting.

The LT3032 is available in a unique low profile 14-lead 4mm × 3mm × 0.75mm DFN package with exposed back-side pads for each regulator, allowing optimum thermal performance.

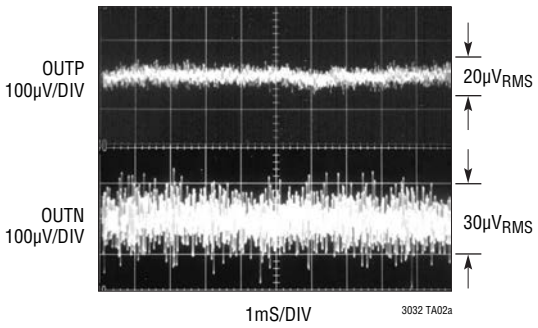
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TYPICAL APPLICATION

Dual Polarity Low Noise 150mA Power Supply



10Hz to 100kHz Output Noise

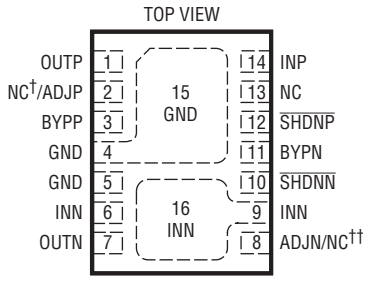


ABSOLUTE MAXIMUM RATINGS

(Note 1)

INP Pin Voltage ..... ±20V
INN Pin Voltage ..... ±20V
OUTP Pin Voltage ..... ±20V
OUTN Pin Voltage (Note 3) ..... ±20V
INP Pin to OUTP Pin Differential Voltage ..... ±20V
OUTN Pin to INN Pin Differential Voltage
(Note 3) ..... –0.5V, 20V
ADJP Pin Voltage ..... ±7V
ADJN Pin Voltage
(with Respect to INN Pin, Note 3) ..... –0.5V, 20V
BYPP Pin Voltage ..... ±0.5V
BYPN Pin Voltage
(with Respect to INN Pin) ..... ±20V
$\overline{\text{SHDNP}}$ Pin Voltage ..... ±20V
$\overline{\text{SHDNN}}$ Pin Voltage
(with Respect to INN Pin, Note 3) ..... –0.5V, 35V
$\overline{\text{SHDNN}}$ Pin Voltage
(with Respect to GND Pin) ..... –20V, 15V
Output Short-Circuit Duration ..... Indefinite
Operating Junction Temperature Range (Note 2)
E, I Grades ..... –40°C to 125°C
MP-Grade ..... –55°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DE14MA PACKAGE
14-LEAD (4mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 30°C/W TO 43°C/W*, θ_{JC} = 10°C/W*

*SEE APPLICATIONS INFORMATION FOR MORE DETAIL

†PIN 2: NC FOR LT3032-3.3/LT3032-5/LT3032-12/LT3032-15, ADJP FOR LT3032
††PIN 8: NC FOR LT3032-3.3/LT3032-5/LT3032-12/LT3032-15, ADJN FOR LT3032

EXPOSED PAD (PIN 15) IS GND, MUST BE SOLDERED TO PINS 4, 5 ON PCB
EXPOSED PAD (PIN 16) IS INN, MUST BE SOLDERED TO PINS 6, 9 ON PCB

ORDER INFORMATION

http://www.linear.com/product/LT3032#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3032EDE#PBF	LT3032EDE#TRPBF	3032	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LT3032IDE#PBF	LT3032IDE#TRPBF	3032	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LT3032MPDE#PBF	LT3032MPDE#TRPBF	3032	14-Lead (4mm × 3mm) Plastic DFN	–55°C to 125°C
LT3032EDE-3.3#PBF	LT3032EDE-3.3#TRPBF	03233	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LT3032IDE-3.3#PBF	LT3032IDE-3.3#TRPBF	03233	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LT3032MPDE-3.3#PBF	LT3032MPDE-3.3#TRPBF	03233	14-Lead (4mm × 3mm) Plastic DFN	–55°C to 125°C
LT3032EDE-5#PBF	LT3032EDE-5#TRPBF	30325	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LT3032IDE-5#PBF	LT3032IDE-5#TRPBF	30325	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LT3032MPDE-5#PBF	LT3032MPDE-5#TRPBF	30325	14-Lead (4mm × 3mm) Plastic DFN	–55°C to 125°C
LT3032EDE-12#PBF	LT3032EDE-12#TRPBF	30322	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LT3032IDE-12#PBF	LT3032IDE-12#TRPBF	30322	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LT3032MPDE-12#PBF	LT3032MPDE-12#TRPBF	30322	14-Lead (4mm × 3mm) Plastic DFN	–55°C to 125°C

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3032EDE-15#PBF	LT3032EDE-15#TRPBF	03215	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LT3032IDE-15#PBF	LT3032IDE-15#TRPBF	03215	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LT3032MPDE-15#PBF	LT3032MPDE-15#TRPBF	03215	14-Lead (4mm × 3mm) Plastic DFN	–55°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Minimum INP Operating Voltage		LT3032 I_{LOAD} = 150mA	●		1.8	2.3	V
Minimum INN Operating Voltage		LT3032 I_{LOAD} = –150mA	●	–2.3	–1.6		V
Regulated Output Voltage (Notes 4, 10)	LT3032-3.3	V_{INP} = 3.8V, I_{LOAD} = 1mA		3.250	3.300	3.350	V
		4.3V ≤ V_{INP} ≤ 20V, 1mA ≤ I_{LOAD} ≤ 150mA	●	3.200	3.300	3.400	V
	LT3032-3.3	V_{INN} = –3.8V, I_{LOAD} = –1mA		–3.250	–3.300	–3.350	V
		–4.3V ≤ V_{INN} ≤ –20V, –1mA ≥ I_{LOAD} ≥ –150mA	●	–3.200	–3.300	–3.400	V
	LT3032-5	V_{INP} = 5.5V, I_{LOAD} = 1mA		4.925	5.00	5.075	V
		6V ≤ V_{INP} ≤ 20V, 1mA ≤ I_{LOAD} ≤ 150mA	●	4.850	5.00	5.150	V
	LT3032-5	V_{INN} = –5.5V, I_{LOAD} = –1mA		–5.075	–5.00	–4.925	V
		–6V ≤ V_{INN} ≤ –20V, –1mA ≥ I_{LOAD} ≥ –150mA	●	–5.150	–5.00	–4.850	V
	LT3032-12	V_{INP} = 12.5V, I_{LOAD} = 1mA		11.82	12.00	12.18	V
		13V ≤ V_{INP} ≤ 20V, 1mA ≤ I_{LOAD} ≤ 150mA	●	11.64	12.00	12.36	V
	LT3032-12	V_{INN} = –12.5V, I_{LOAD} = –1mA		–12.18	–12.00	–11.82	V
		–13V ≤ V_{INN} ≤ –20V, –1mA ≥ I_{LOAD} ≥ 150mA	●	–12.36	–12.00	–11.64	V
	LT3032-15	V_{INP} = 15.5V, I_{LOAD} = 1mA		14.775	15.00	15.225	V
		16V ≤ V_{INP} ≤ 20V, 1mA ≤ I_{LOAD} ≤ 150mA	●	14.550	15.00	15.450	V
	LT3032-15	V_{INN} = –15.5V, I_{LOAD} = –1mA		–15.225	–15.00	–14.775	V
		–16V ≤ V_{INN} ≤ –20V, –1mA ≥ I_{LOAD} ≥ 150mA	●	–15.450	–15.00	–14.550	V
ADJP Pin Voltage (Notes 4, 5)	LT3032	V_{INP} = 2V, I_{LOAD} = 1mA		1.202	1.22	1.238	V
		2.3V ≤ V_{INP} ≤ 20V, 1mA ≤ I_{LOAD} ≤ 150mA	●	1.184	1.22	1.256	V
ADJN Pin Voltage (Notes 4, 5, 10)	LT3032	V_{INN} = –2V, I_{LOAD} = –1mA		–1.238	–1.22	–1.202	V
		–2.3V ≤ V_{INN} ≤ –20V, –1mA ≤ I_{LOAD} ≤ –150mA	●	–1.256	–1.22	–1.184	V
Line Regulation (Note 5)	LT3032-3.3	OUTP ΔV_{INP} = 3.8V to 20V, I_{LOAD} = 1mA	●		1	6	mV
		OUTN ΔV_{INN} = –3.8V to –20V, I_{LOAD} = –1mA	●		9	30	mV
	LT3032-5	OUTP ΔV_{INP} = 5.5V to 20V, I_{LOAD} = 1mA	●		1	6	mV
		OUTN ΔV_{INN} = –5.5V to –20V, I_{LOAD} = –1mA	●		15	50	mV
	LT3032-12	OUTP ΔV_{INP} = 12.5V to 20V, I_{LOAD} = 1mA	●		1.5	15	mV
		OUTN ΔV_{INN} = –12.5V to –20V, I_{LOAD} = –1mA	●		13	75	mV
	LT3032-15	OUTP ΔV_{INP} = 15.5V to 20V, I_{LOAD} = 1mA	●		2	20	mV
		OUTN ΔV_{INN} = –15.5V to 20V, I_{LOAD} = –1mA	●		10	75	mV
	LT3032	ADJP ΔV_{INP} = 2V to 20V, I_{LOAD} = 1mA	●		1	6	mV
		ADJN ΔV_{INN} = –2V to –20V, I_{LOAD} = –1mA	●		1	12	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
Load Regulation (Notes 5, 13)	LT3032-3.3	OUTP	V_{INP} = 4.3V, ΔI_{LOAD} = 1mA to 150mA			–5		mV
	LT3032-3.3	OUTN	V_{INN} = –4.3V, ΔI_{LOAD} = –1mA to –150mA			10		mV
	LT3032-5	OUTP	V_{INP} = 6V, ΔI_{LOAD} = 1mA to 150mA			–9		mV
	LT3032-5	OUTN	V_{INN} = –6V, ΔI_{LOAD} = –1mA to –150mA			15		mV
	LT3032-12	OUTP	V_{INP} = 13V, ΔI_{LOAD} = 1mA to 150mA			–20		mV
	LT3032-12	OUTN	V_{INN} = –13V, ΔI_{LOAD} = –1mA to –150mA			20		mV
	LT3032-15	OUTP	V_{INP} = 16V, ΔI_{LOAD} = 1mA to 150mA			–25		mV
	LT3032-15	OUTN	V_{INN} = –16V, ΔI_{LOAD} = –1mA to –150mA			27		mV
	LT3032	ADJP	V_{INP} = 2.3V, ΔI_{LOAD} = 1mA to 150mA			–1.5	–7	mV
			V_{INP} = 2.3V, ΔI_{LOAD} = 1mA to 150mA	●			–15	mV
	LT3032	ADJN	V_{INN} = –2.3V, ΔI_{LOAD} = –1mA to –150mA			1.5	7	mV
			V_{INN} = –2.3V, ΔI_{LOAD} = –1mA to –150mA	●			15	mV
Dropout Voltage $V_{INP} = V_{OUTP(NOMINAL)}$ (Notes 6, 7)		I_{LOAD} = 1mA		●		0.09	0.20	V
		I_{LOAD} = 10mA		●		0.15	0.27	V
		I_{LOAD} = 50mA				0.21		V
		I_{LOAD} = 150mA				0.27		V
Dropout Voltage $V_{INN} = V_{OUTN(NOMINAL)}$ (Notes 6, 7)		I_{LOAD} = –1mA		●		0.10	0.20	V
		I_{LOAD} = –10mA		●		0.15	0.27	V
		I_{LOAD} = –50mA				0.21		V
		I_{LOAD} = –150mA				0.30		V
GND Pin Current $V_{INP} = V_{OUTP(NOMINAL)}$, V_{INN} = 0V (Notes 6, 8, 9)		I_{LOAD} = 0mA (LT3032, LT3032-3.3, LT3032-5)		●		–25	–65	µA
		I_{LOAD} = 0mA (LT3032-12, LT3032-15)		●		–50	–120	µA
		I_{LOAD} = 1mA (LT3032, LT3032-3.3, LT3032-5)		●		–70	–120	µA
		I_{LOAD} = 1mA (LT3032-12, LT3032-15)		●		–80	180	µA
		I_{LOAD} = 10mA		●		–350	–500	µA
		I_{LOAD} = 50mA		●		–1.3	–1.8	mA
		I_{LOAD} = 150mA		●		–4	–7	mA
GND Pin Current $V_{INN} = V_{OUTN(NOMINAL)}$, V_{INP} = 0V (Notes 6, 8, 9, 10)		I_{LOAD} = 0mA (LT3032, LT3032-3.3, LT3032-5)		●		30	70	µA
		I_{LOAD} = 0mA (LT3032-12, LT3032-15)		●		50	130	µA
		I_{LOAD} = –1mA (LT3032, LT3032-3.3, LT3032-5)		●		85	180	µA
		I_{LOAD} = –1mA (LT3032-12, LT3032-15)		●		90	180	µA
		I_{LOAD} = –10mA		●		300	600	µA
		I_{LOAD} = –50mA		●		0.75	1.5	mA
		I_{LOAD} = –150mA		●		2	5	mA
ADJP Pin Bias Current	LT3032	(Notes 5, 9)				30	100	nA
ADJN Pin Bias Current	LT3032	(Notes 5, 9)				–30	–100	nA
Shutdown Threshold		$\overline{SHDNP}$	V_{OUTP} = Off to On	●		0.7	2	V
		$\overline{SHDNP}$	V_{OUTP} = On to Off	●	0.25	0.6		V
		$\overline{SHDNN}$	V_{OUTN} = Off to On (Positive)	●		1.4	2	V
		$\overline{SHDNN}$	V_{OUTN} = Off to On (Negative)	●	–2.8	–1.9		V
		$\overline{SHDNN}$	V_{OUTN} = On to Off (Positive)	●	0.25	1.4		V
		$\overline{SHDNN}$	V_{OUTN} = On to Off (Negative)	●		–1.9	–0.25	V
$\overline{SHDNP}$ Pin Current (Note 9)		$V_{\overline{SHDNP}}$ = 0V			–1		1	µA
		$V_{\overline{SHDNP}}$ = 20V				1	4	µA
$\overline{SHDNN}$ Pin Current (Note 9)		$V_{\overline{SHDNN}}$ = 0V			–1		1	µA
		$V_{\overline{SHDNN}}$ = 15V				6	15	µA
		$V_{\overline{SHDNN}}$ = -15V				–3	–9	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Current in Shutdown		V_{INP} = 6V, $V_{\overline{SHDNP}}$ = 0V, V_{INN} = 0V	●		0.1	8	µA
		V_{INN} = –6V, $V_{\overline{SHDNN}}$ = 0V, V_{INP} = 0V (LT3032, LT3032-3.3, LT3032-5)	●		–3	–10	µA
		V_{INN} = $V_{OUT(NOMINAL)}$ –1V, $V_{\overline{SHDNN}}$ = 0V, V_{INP} = 0V (LT3032-12/ LT3032-15)	●		10	20	µA
Output Voltage Noise (10Hz to 100kHz)		C_{OUTP} = 10µF, C_{BYPP} 0.01µF, I_{LOAD} = 150mA			20		μV_{RMS}
		C_{OUTN} = 10µF, C_{BYPN} 0.01µF, I_{LOAD} = –150mA			30		μV_{RMS}
Ripple Rejection V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz		V_{INP} to V_{OUTP} = 1.5V (Average), I_{LOAD} = 100mA		50	68		dB
		V_{INN} to V_{OUTN} = –1.5V (Average), I_{LOAD} = –100mA		46	54		dB
Current Limit (Note 12)		V_{INP} = 7V, V_{OUTP} = 0V			400		mA
		V_{INN} = –7V, V_{OUTN} = 0V			350		mA
		V_{INP} = 2.3V or $V_{OUTP(NOMINAL)}$ + 1V, ΔV_{OUTP} = –0.1V	●	170			mA
		V_{INN} = –2.3V or $V_{OUTP(NOMINAL)}$ – 1V, ΔV_{OUTN} = 0.1V	●	170			mA
INP Reverse Leakage Current		V_{INP} = –20V, V_{OUTP} = 0V	●			–1	mA
INN Reverse Leakage Current		V_{INN} = 20V, V_{OUTN}, V_{ADJN}, $V_{\overline{SHDNN}}$ = Open Circuit	●			1	mA
Reverse Output Current (Notes 5, 11)	LT3032-3.3	V_{OUTP} = 3.3V, V_{INP} < 3.3V			10	20	µA
	LT3032-5	V_{OUTP} = 5V, V_{INP} < 5V			10	20	µA
	LT3032-12	V_{OUTP} = 12V, V_{INP} < 12V			25	50	µA
	LT3032-15	V_{OUTP} = 15V, V_{INP} < 15V			25	50	µA
	LT3032	V_{OUTP} = V_{ADJP} = 1.22V, V_{INP} < 1.22V			5	10	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3032 is tested and specified under pulse load conditions such that $T_J \cong T_A$. The LT3032E is 100% tested at T_A = 25°C. Performance of the LT3032E over the full –40°C to 125°C operating junction temperature range is assured by design, characterization, and correlation with statistical process controls. The LT3032I regulators are guaranteed over the full –40°C to 125°C operating junction temperature range.

Note 3: Parasitic diodes exist internally between the INN pin and the OUTN, ADJN, and $\overline{SHDNN}$ pins. These pins cannot be pulled more than 0.5V below the INN pin during fault conditions, and must remain at a voltage more positive than the INN pin during operation.

Note 4: Operating conditions are limited by maximum junction temperature. Specifications do not apply for all possible combinations of input voltages and output currents. When operating at maximum input voltages, the output current ranges must be limited. When operating at maximum output currents, the input voltage ranges must be limited.

Note 5: The LT3032 is tested and specified for these conditions with the ADJP pin tied to the OUTP pin and the ADJN pin tied to the OUTN pin.

Note 6: To satisfy requirements for minimum input voltage, the LT3032 is tested and specified for these conditions with an external resistor divider (two 250k resistors) from OUTP/OUTN to the corresponding ADJP/ADJN pin to give an output voltage of ±2.44V. The external resistor divider adds a 5µA DC load on the output. The LT3032-12/LT3032-15 have higher internal resistor divider current, resulting in higher GND pin current at light/no load.

Note 7: Dropout voltage is the minimum input-to-output voltage differential needed to maintain regulation at a specified output current. In dropout, output voltage equals:

$V_{INP/INN} – V_{DROPOUT}$

For lower output voltages, dropout voltage is limited by the minimum input voltage specification under some output voltage/load conditions; see curves for Minimum INN Voltage and Minimum INP Voltage in Typical Performance Characteristics. LTC is unable to guarantee Maximum Dropout Voltage specifications at 50mA and 150mA due to production test limitations with Kelvin-Sensing the package pins. Please consult the Typical Performance Characteristics for curves of Dropout Voltage as a function of Output Load Current and Temperature.

Note 8: GND pin current is tested with V_{INP} = $V_{OUTP(NOMINAL)}$ or V_{INN} = $V_{OUTN(NOMINAL)}$ and a current source load. This means the device is tested while operating in its dropout region. This is the worst-case GND pin current. GND pin current decreases slightly at higher input voltages.

Note 9: Positive current flow is into the pin. Negative current flow is out of the pin.

Note 10: For input-to-output differential voltages from INN to OUTN greater than –7V, a –50µA load is needed to maintain regulation.

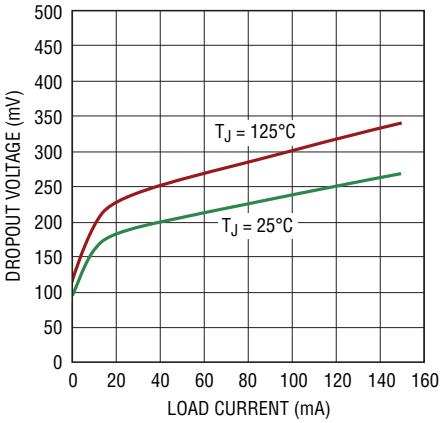
Note 11: Reverse output current is tested with the INP pin grounded and the OUTP pin forced to the nominal output voltage. This current flows into the OUTP pin and out the GND pin.

Note 12: Positive side current limit is tested at V_{INP} = 2.3V or $V_{OUTP(NOMINAL)}$ + 1V (whichever is more positive). Negative side current limit is tested at V_{INN} = –2.3V or $V_{OUTN(NOMINAL)}$ – 1V (whichever is more negative).

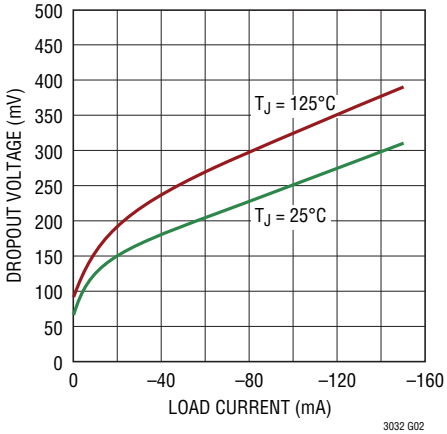
Note 13: LTC is unable to guarantee load regulation specifications on fixed voltage versions of the LT3032 due to production test limitations with Kelvin-Sensing the package pins. Please consult the Typical Performance Characteristics for curves of Load Regulation as a function of Temperature.

TYPICAL PERFORMANCE CHARACTERISTICS

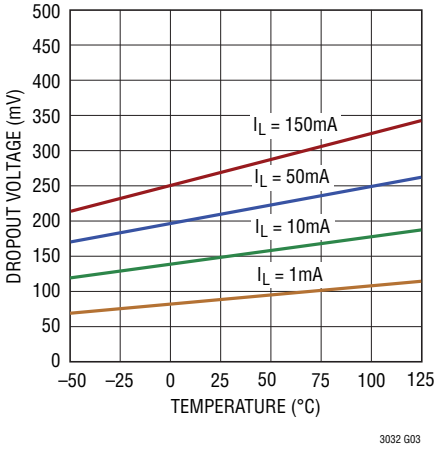
INP-to-OUTP Typical Dropout Voltage



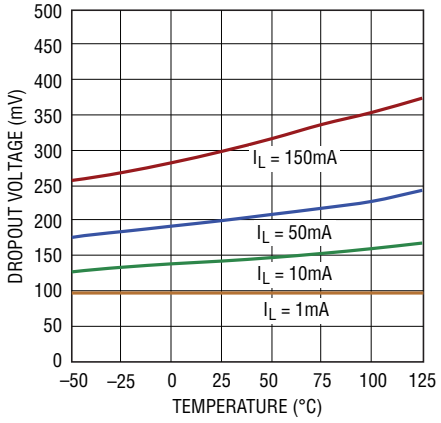
INN-to-OUTN Typical Dropout Voltage



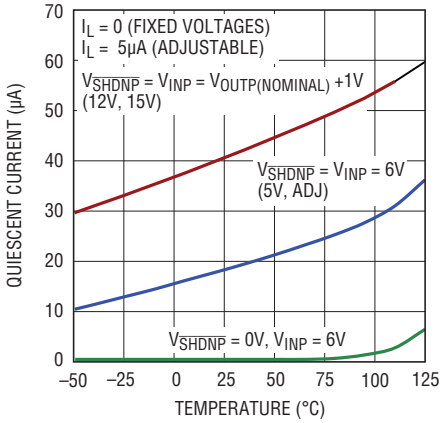
INP-to-OUTP Dropout Voltage



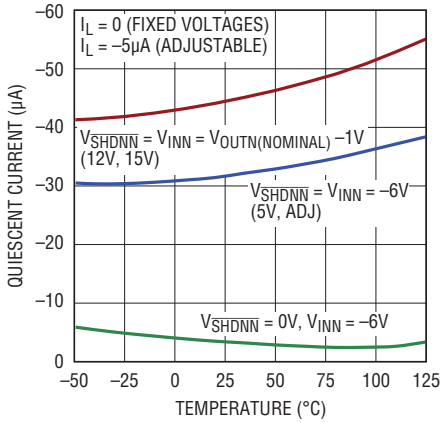
INN-to-OUTN Dropout Voltage



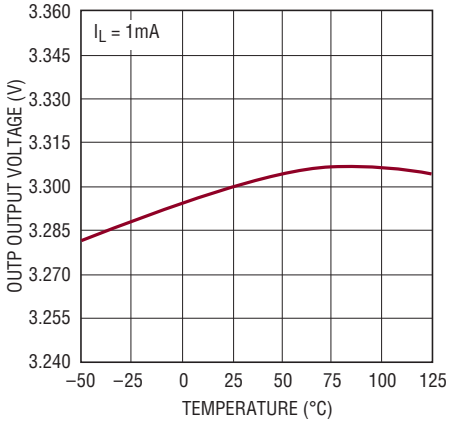
INP Quiescent Current



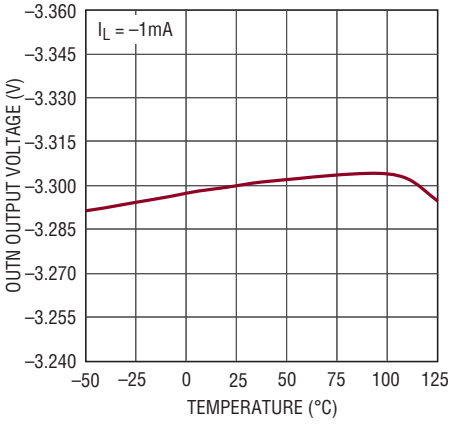
INN Quiescent Current



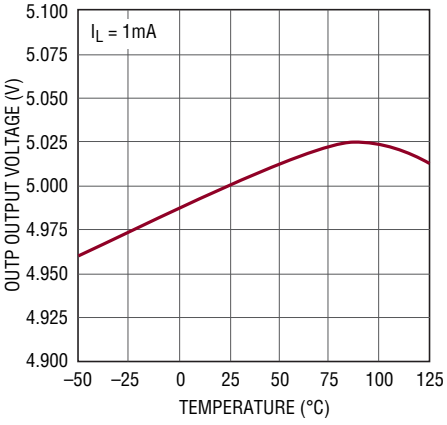
LT3032-3.3 OUTP Output Voltage



LT3032-3.3 OUTN Output Voltage

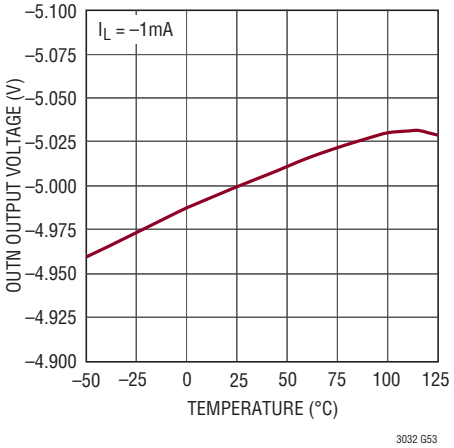


LT3032-5 OUTP Output Voltage

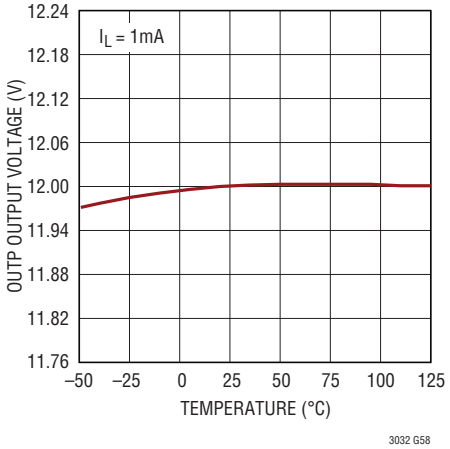


TYPICAL PERFORMANCE CHARACTERISTICS

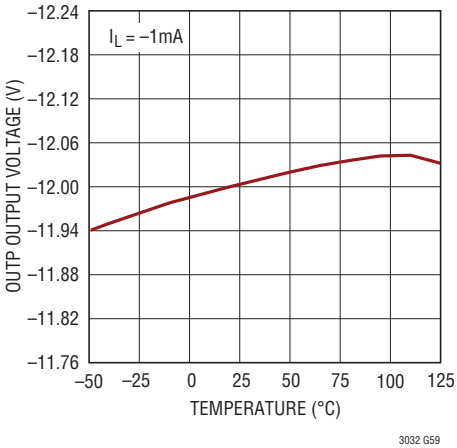
LT3032-5 OUTN Output Voltage



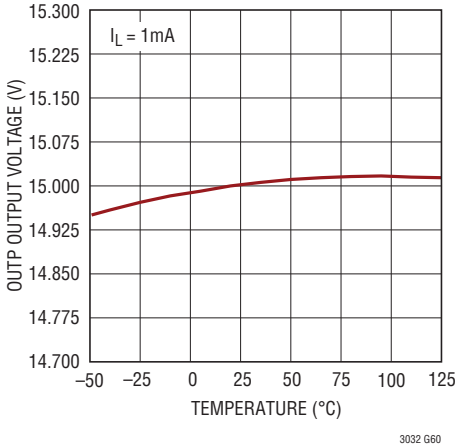
LT3032-12 OUTP Output Voltage



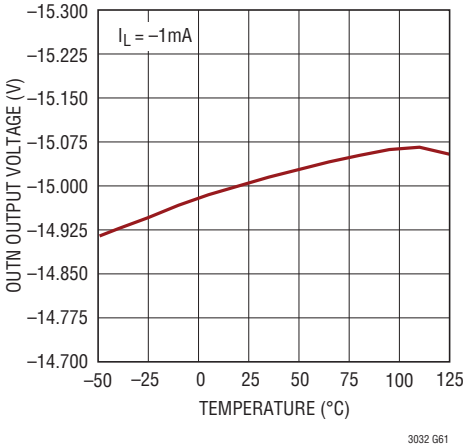
LT3032-12 OUTN Output Voltage



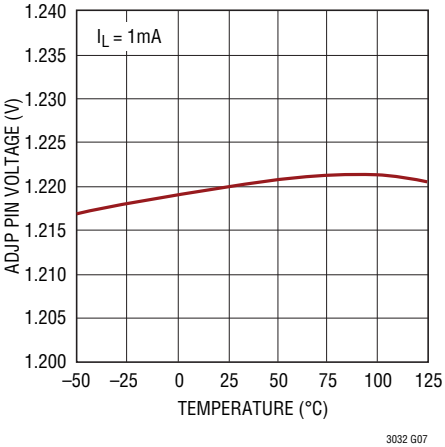
LT3032-15 OUTP Output Voltage



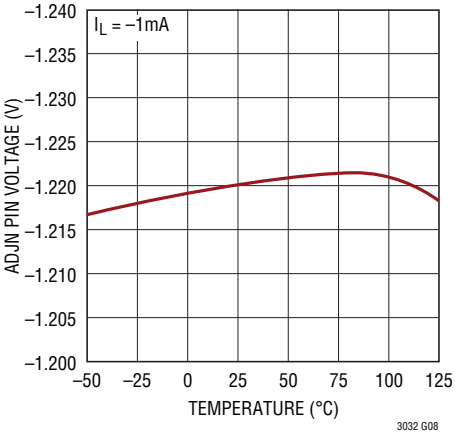
LT3032-15 OUTN Output Voltage



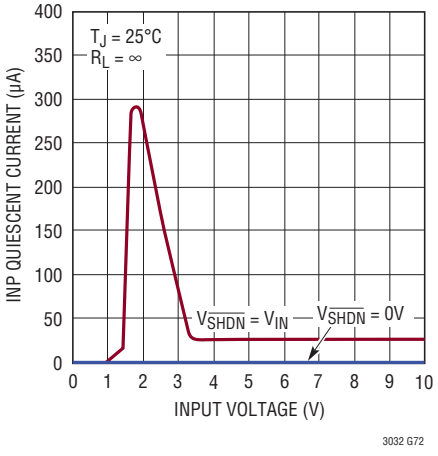
LT3032 ADJP Pin Voltage



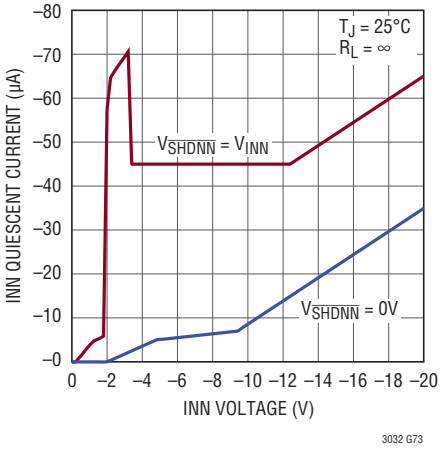
LT3032 ADJN Pin Voltage



LT3032-3.3 INP Quiescent Current

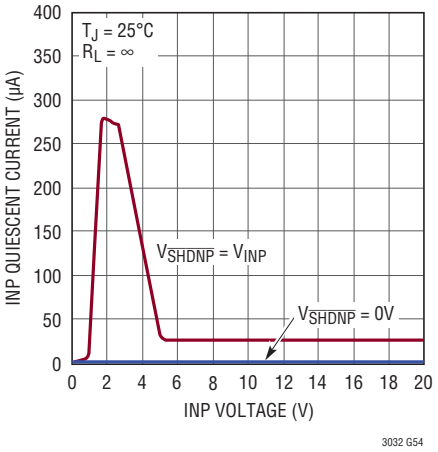


LT3032-3.3 INN Quiescent Current

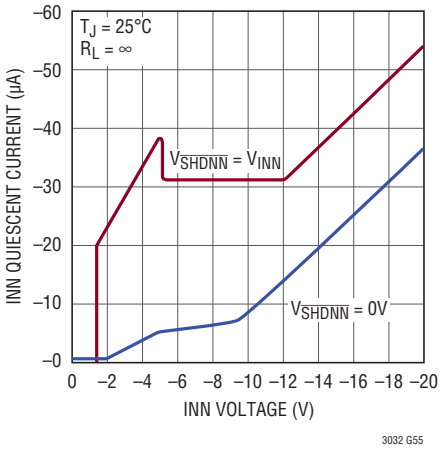


TYPICAL PERFORMANCE CHARACTERISTICS

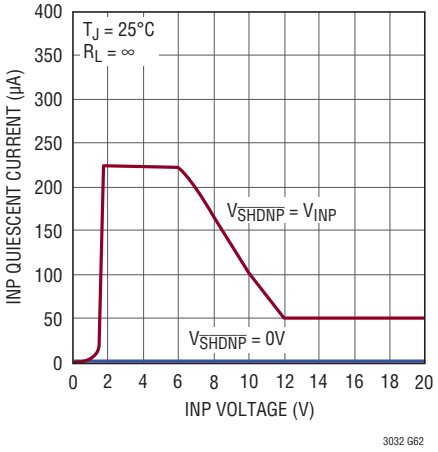
LT3032-5 INP Quiescent Current



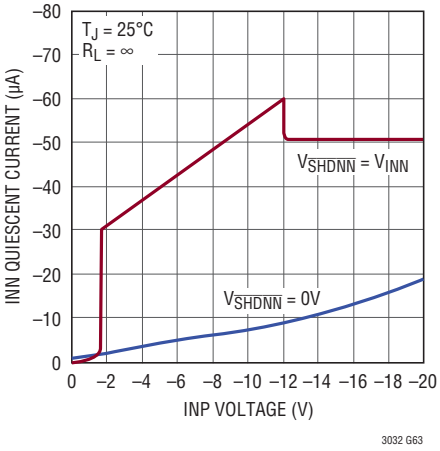
LT3032-5 INN Quiescent Current



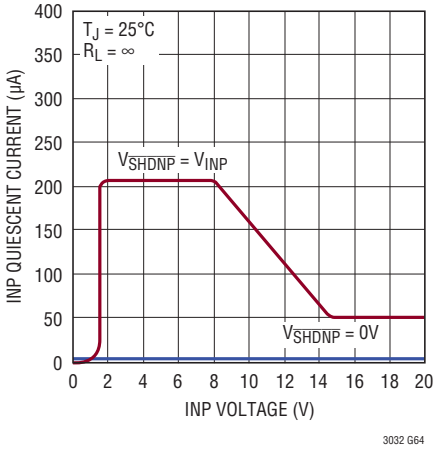
LT3032-12 INP Quiescent Current



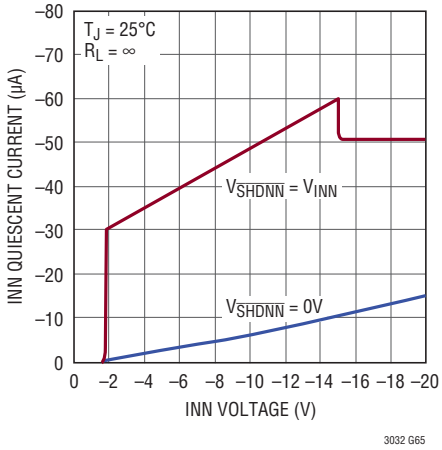
LT3032-12 INN Quiescent Current



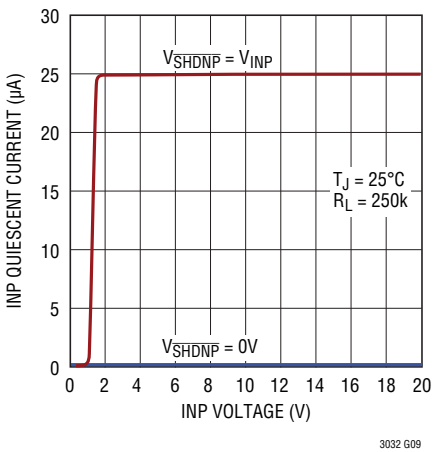
LT3032-15 INP Quiescent Current



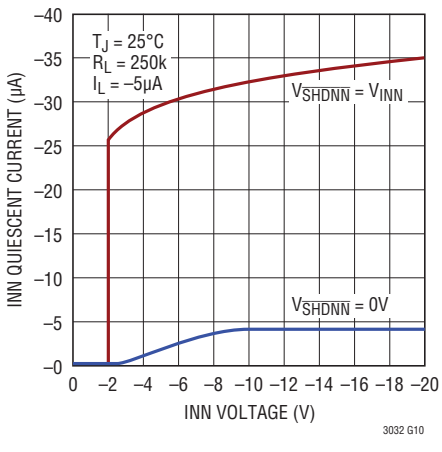
LT3032-15 INN Quiescent Current



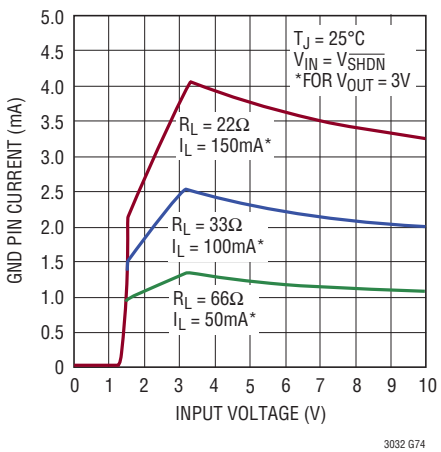
LT3032 INP Quiescent Current



LT3032 INN Quiescent Current

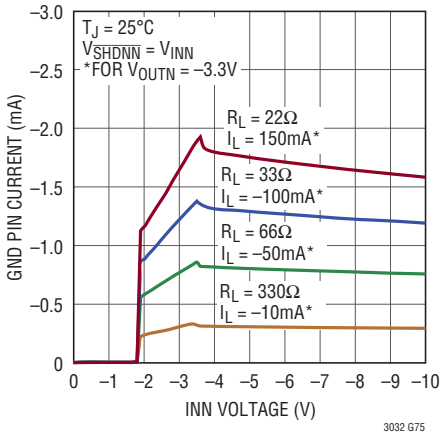


LT3032-3.3 Positive Side GND Pin Current

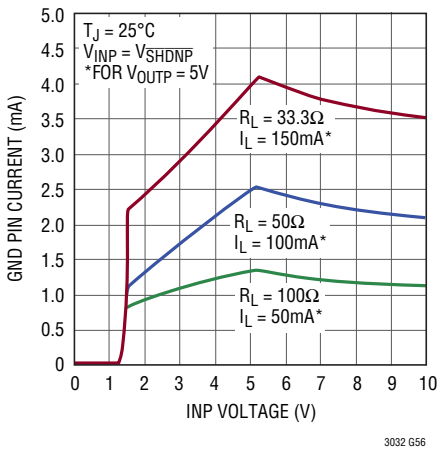


TYPICAL PERFORMANCE CHARACTERISTICS

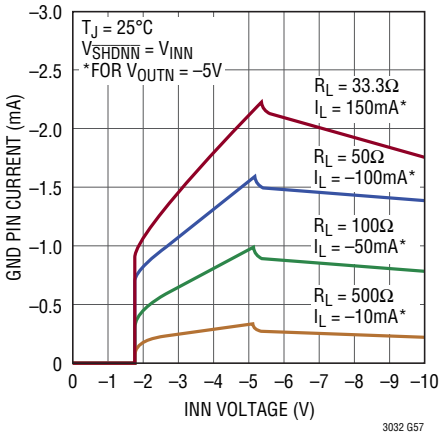
LT3032-3.3
Negative Side GND Pin Current



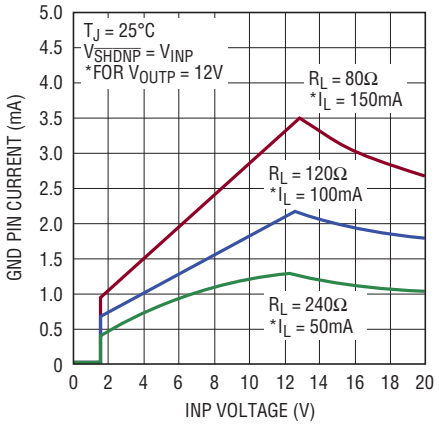
LT3032-5
Positive Side GND Pin Current



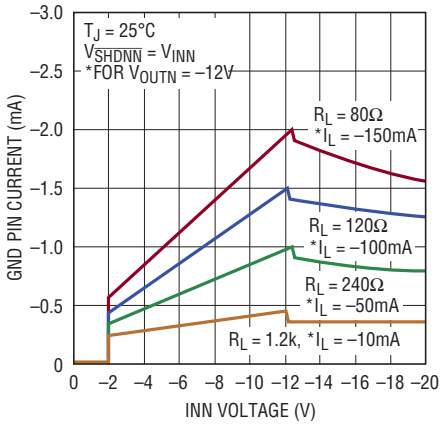
LT3032-5
Negative Side GND Pin Current



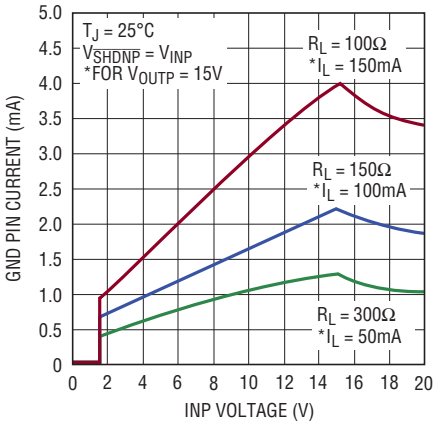
LT3032-12
Positive Side GND Pin Current



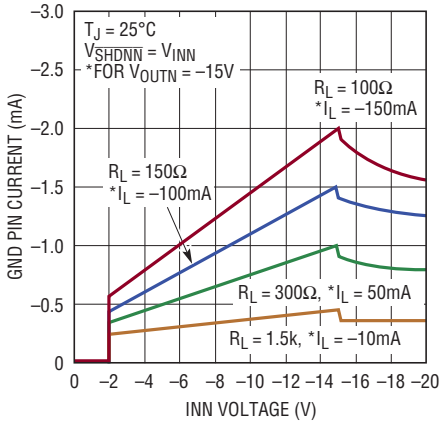
LT3032-12
Negative Side GND Pin Current



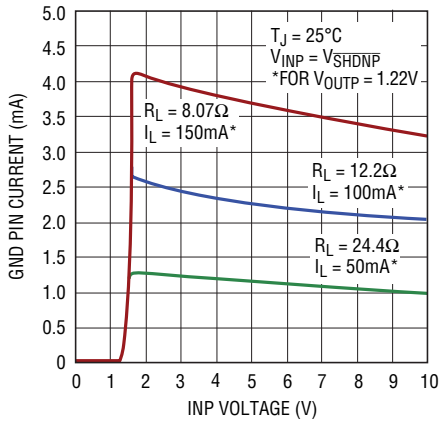
LT3032-15
Positive Side GND Pin Current



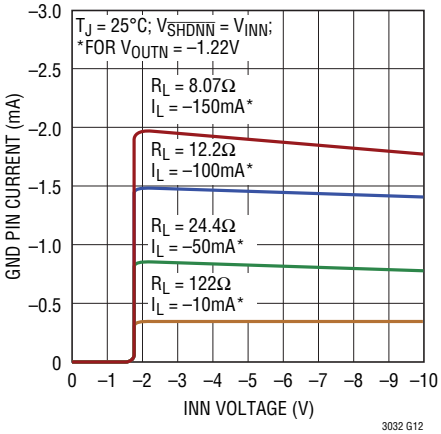
LT3032-15
Negative Side GND Pin Current



LT3032
Positive Side GND Pin Current

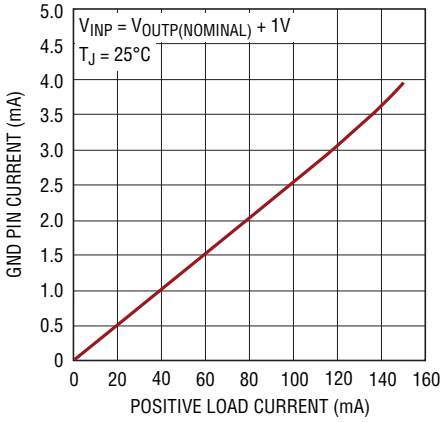


LT3032
Negative Side GND Pin Current

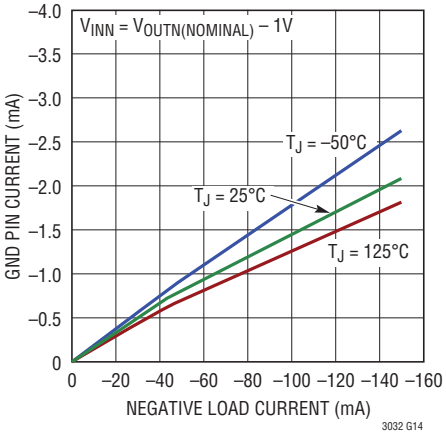


TYPICAL PERFORMANCE CHARACTERISTICS

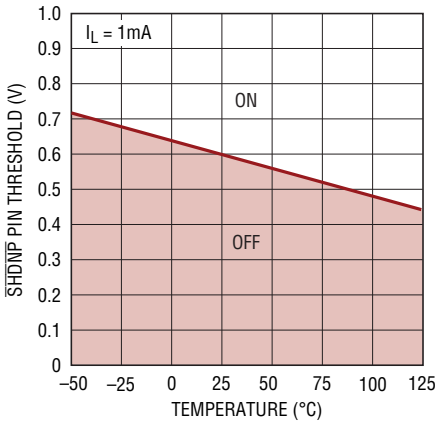
Positive Side GND Pin Current vs I_{LOAD}



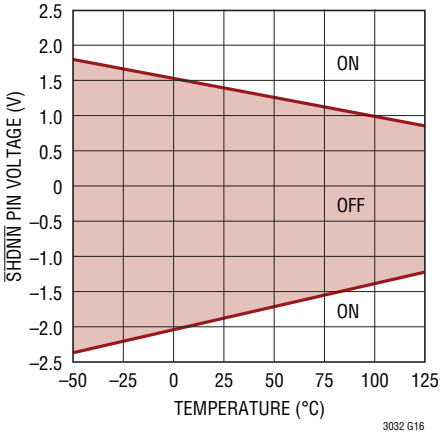
Negative Side GND Pin Current vs I_{LOAD}



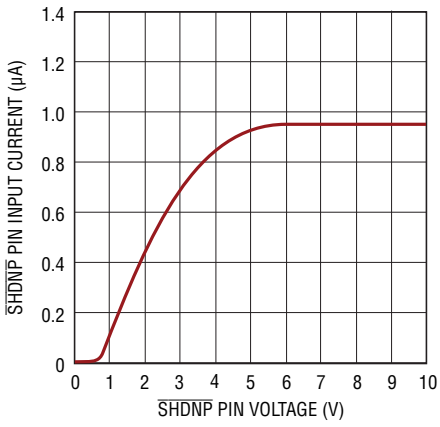
$\overline{SHDNP}$ Pin Threshold



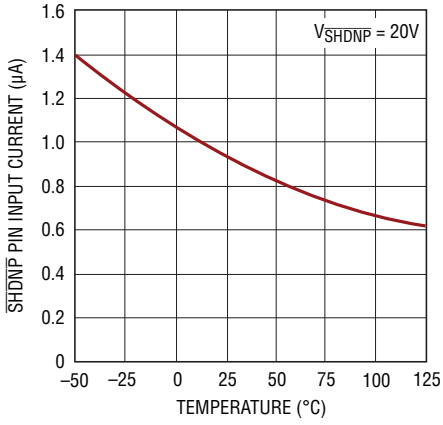
$\overline{SHDNN}$ Pin Thresholds



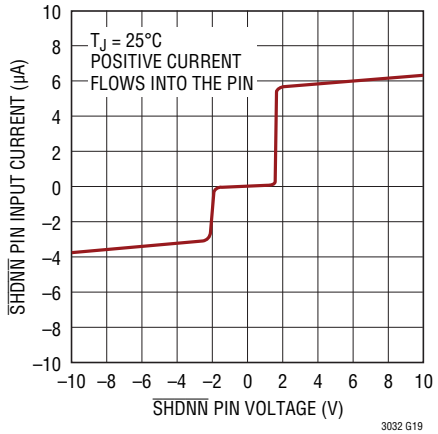
$\overline{SHDNP}$ Pin Input Current



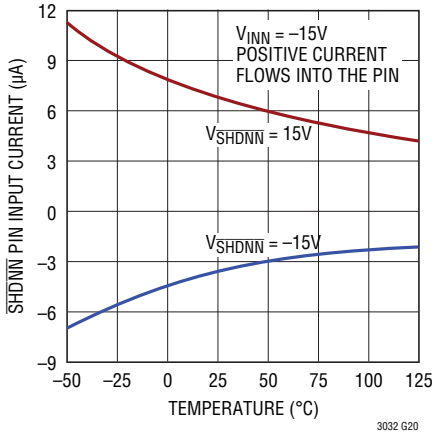
$\overline{SHDNP}$ Pin Input Current



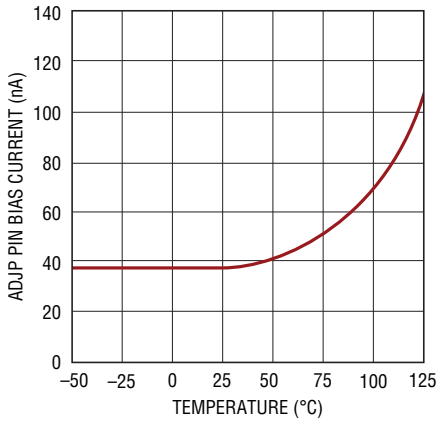
$\overline{SHDNN}$ Pin Input Current



$\overline{SHDNN}$ Pin Input Current

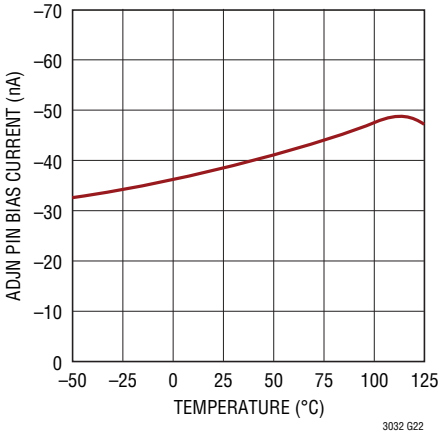


ADJP Pin Bias Current

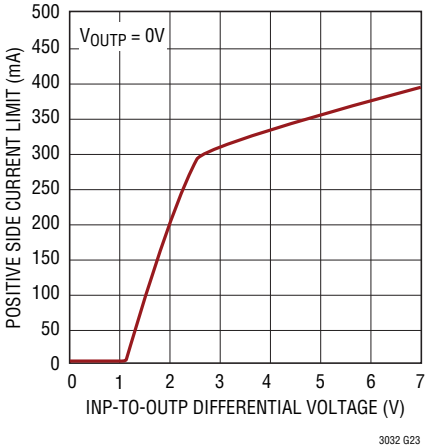


TYPICAL PERFORMANCE CHARACTERISTICS

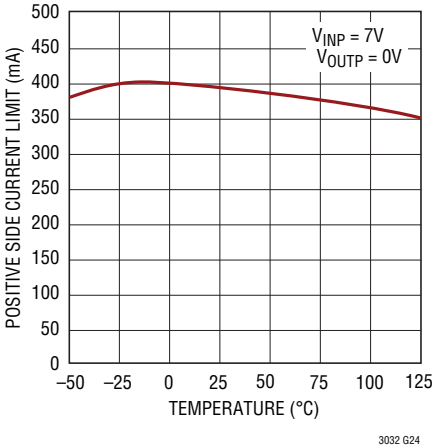
ADJN Pin Bias Current



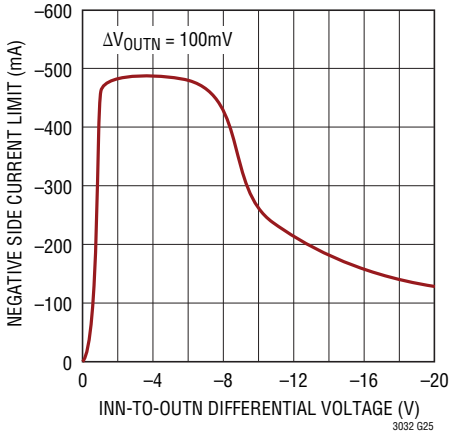
Positive Side Current Limit



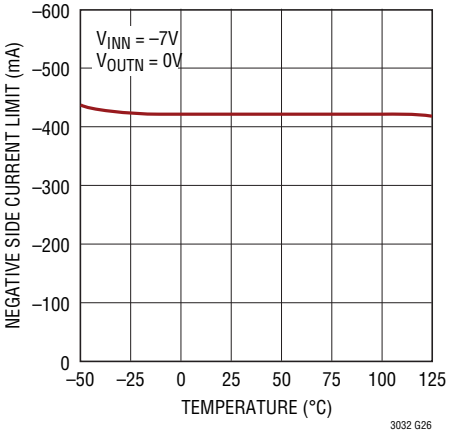
Positive Side Current Limit



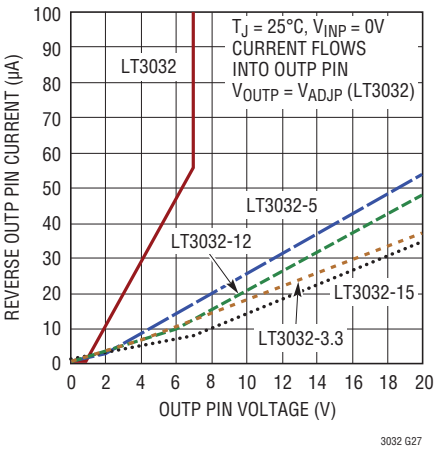
Negative Side Current Limit



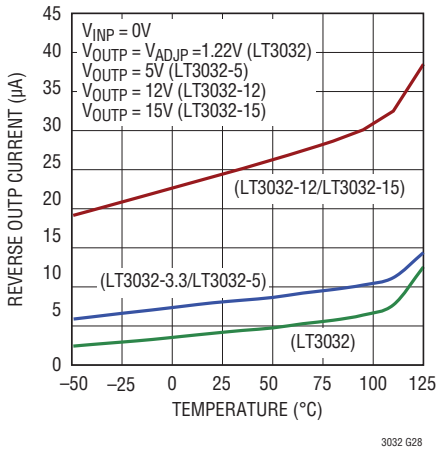
Negative Side Current Limit



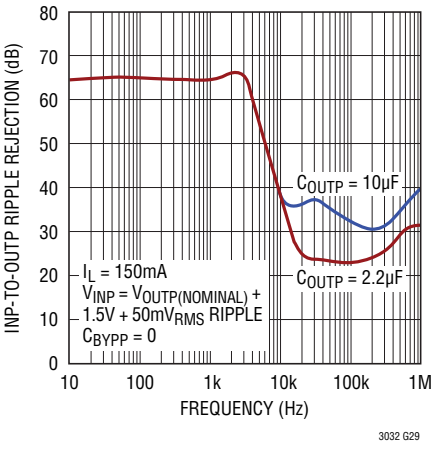
Reverse OUTP Pin Current



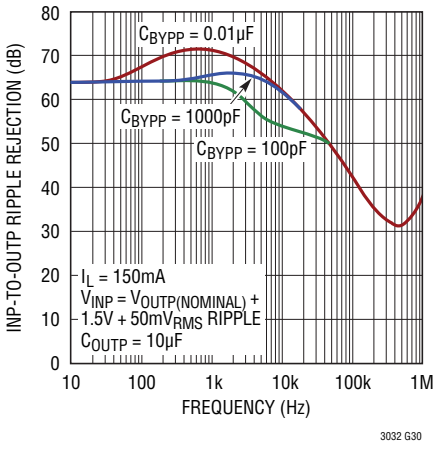
Reverse OUTP Pin Current



INP-to-OUTP Ripple Rejection

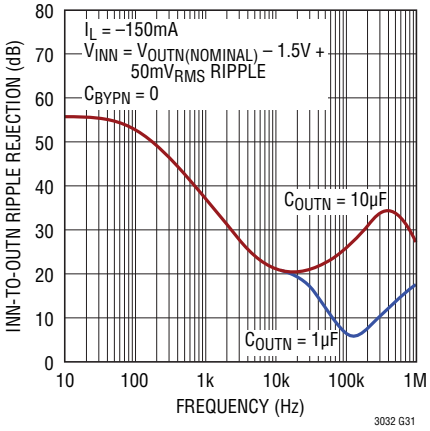


INP-to-OUTP Ripple Rejection

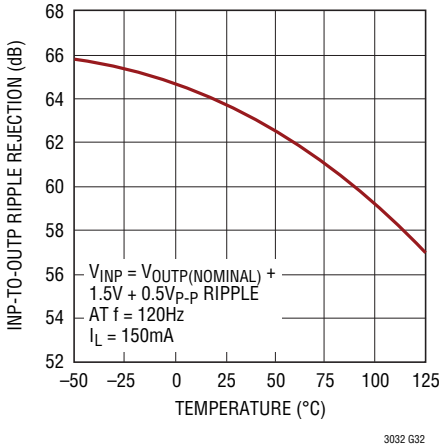


TYPICAL PERFORMANCE CHARACTERISTICS

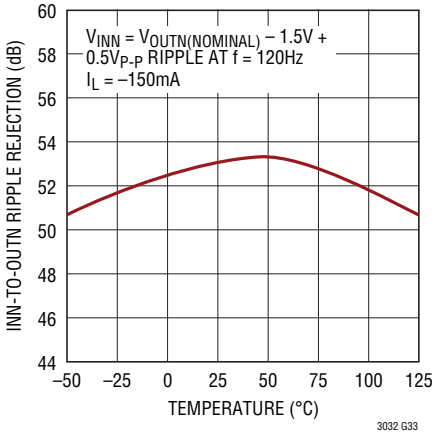
INN-to-OUTN Ripple Rejection



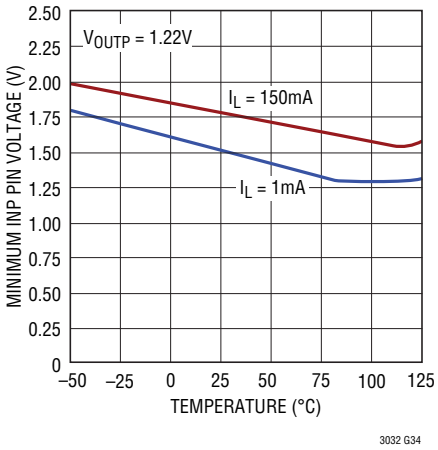
INP-to-OUTP Ripple Rejection



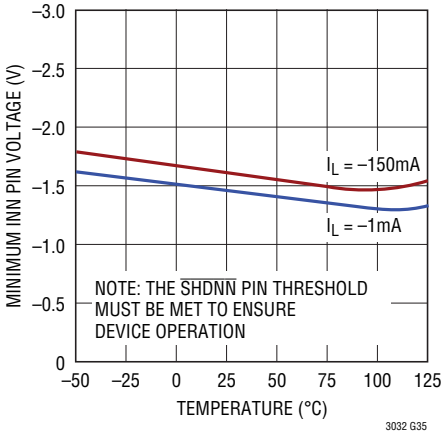
INN-to-OUTN Ripple Rejection



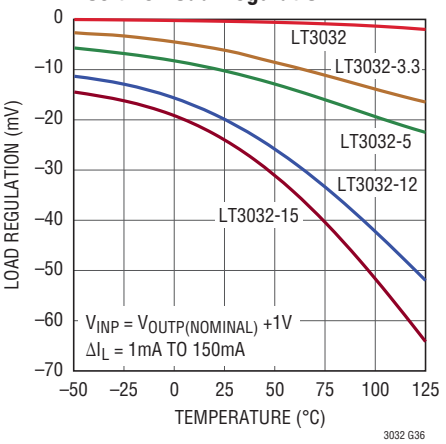
LT3032 Minimum INP Pin Voltage



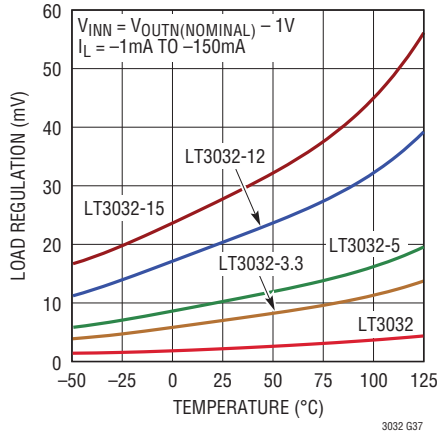
LT3032 Minimum INN Pin Voltage



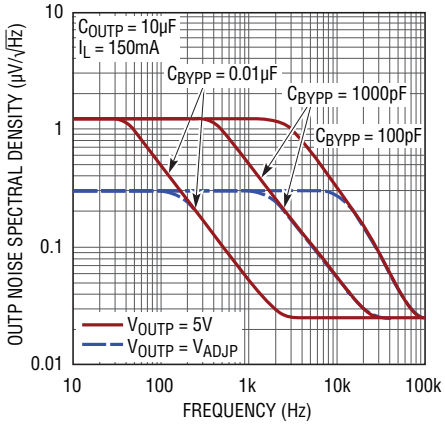
Positive Load Regulation



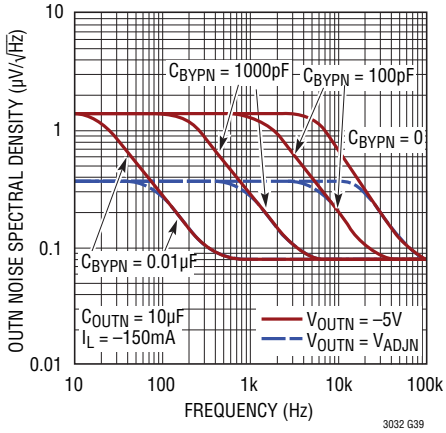
Negative Load Regulation



OUTP Noise Spectral Density

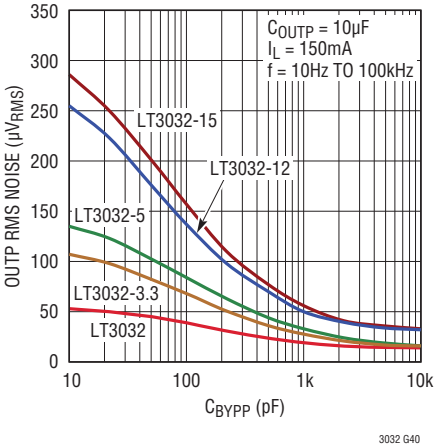


OUTN Noise Spectral Density

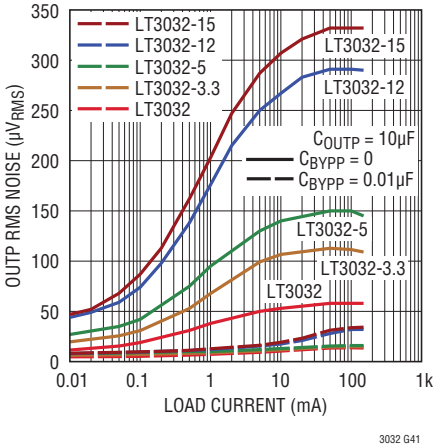


TYPICAL PERFORMANCE CHARACTERISTICS

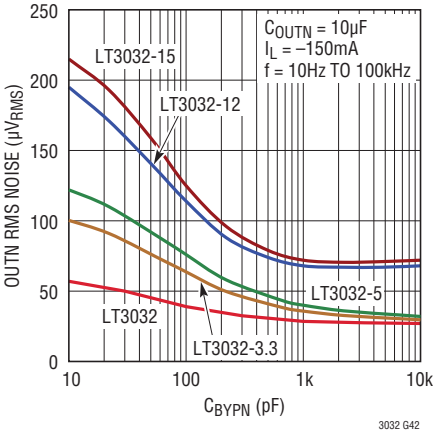
OUTP RMS Noise vs Bypass Capacitor



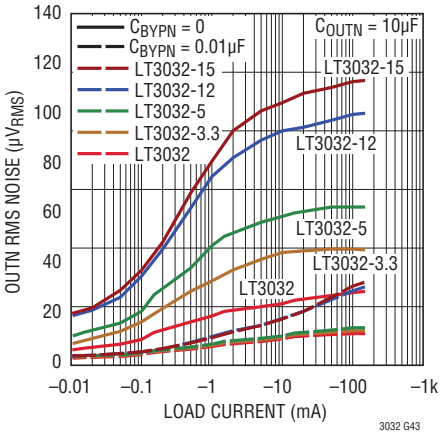
OUTP RMS Noise vs Load Current (10Hz to 100kHz)



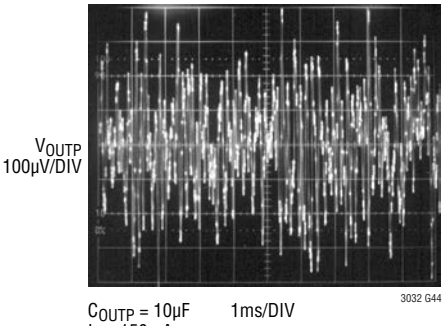
OUTN RMS Noise vs Bypass Capacitor



OUTN RMS Noise vs Load Current (10Hz to 100kHz)

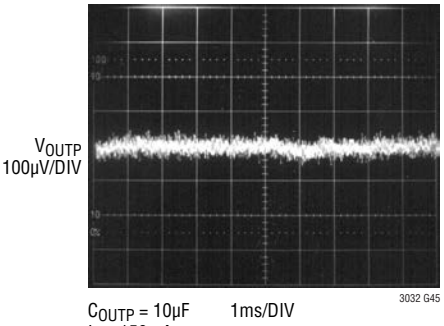


OUTP 10Hz to 100kHz Output Noise CBYPP = 0



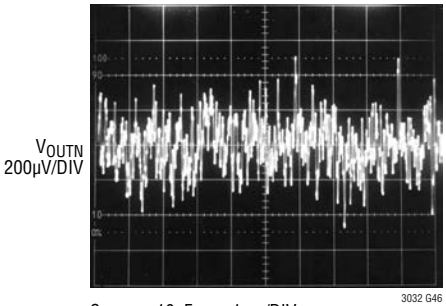
COUTP = 10µF 1ms/DIV
IL = 150mA
VOUTP = 5V

OUTP 10Hz to 100kHz Output Noise CBYPP = 0.01µF



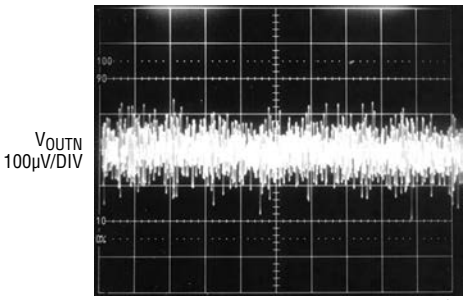
COUTP = 10µF 1ms/DIV
IL = 150mA
VOUTP = 5V

OUTN, 10Hz to 100kHz Output Noise, CBYPN = 0



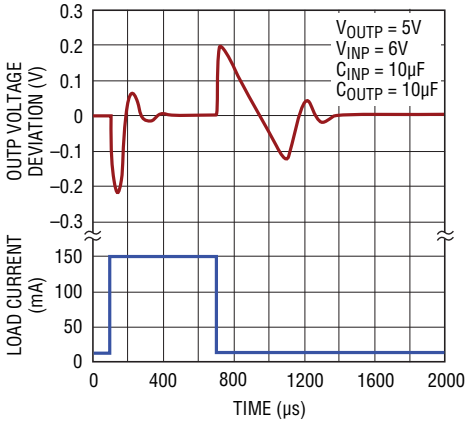
COUTN = 10µF 1ms/DIV
ILOAD = –150mA
VOUTN = –5V

OUTN, 10Hz to 100kHz Output Noise, CBYPN = 0.01µF



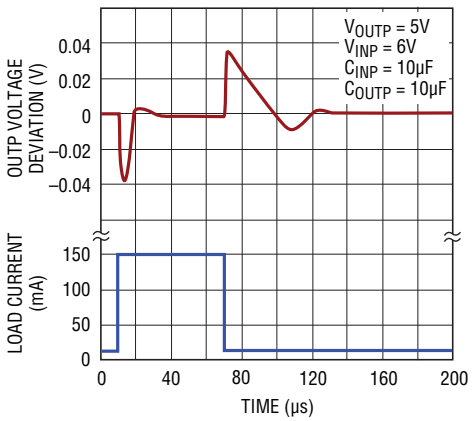
COUTN = 10µF 1ms/DIV
ILOAD = –150mA
VOUTN = –5V

OUTP Transient Response CBYPP = 0

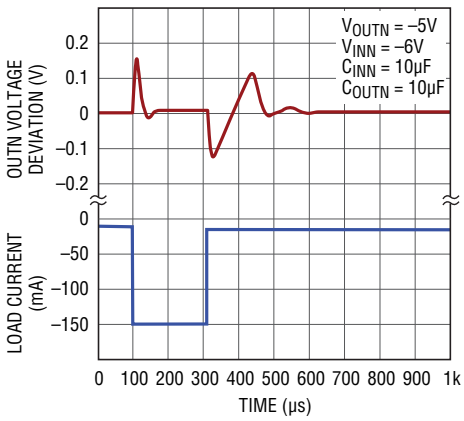


TYPICAL PERFORMANCE CHARACTERISTICS

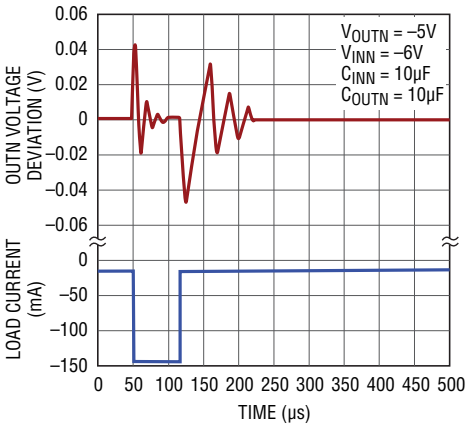
OUTP Transient Response
C_{BYPP} = 0.01µF



OUTN Transient Response
C_{BYPN} = 0



OUTN Transient Response
C_{BYPN} = 0.01µF



PIN FUNCTIONS

OUTP (Pin 1): Positive Output. This output supplies power to the positive side load. A minimum output capacitor of 2.2µF is required to prevent oscillations. Larger output capacitors are required for applications with large transient loads to limit peak voltage transients. See the Applications Information section for more information on output capacitance, bypass capacitance, and reverse output characteristics.

ADJP (Pin 2, Adjustable Part Only): Positive Adjust. This is the input to the positive side error amplifier. This pin is internally clamped to ±7V. It has a typical bias current of 30nA which flows into the pin (see curve of ADJP Pin Bias Current vs Temperature in the Typical Performance Characteristics). The ADJP pin voltage is 1.22V referenced to ground and the output voltage range is 1.22V to 20V.

BYPP (Pin 3): Positive Bypass. The BYPP pin is used to bypass the reference of the positive side regulator to achieve low noise performance. The BYPP pin is clamped internally to ±0.6V (one V_{BE}). A small capacitor from OUTP to this pin will bypass the reference to lower the output voltage noise. A maximum value of 0.01µF is used for reducing output voltage noise to a typical 20µV_{RMS} over the 10Hz to 100kHz bandwidth. If not used, this pin must be left unconnected.

GND (Pins 4, 5, Exposed Pad Pin 15): Ground. One of the DFN's exposed backside pads (Pin 15) is an electrical connection to ground. To ensure proper electrical and thermal performance, solder Pin 15 to the PCB's ground and tie directly to Pins 4 and 5. Connect the bottom of the positive and negative output voltage setting resistor dividers directly to Pins 4 and 5 for optimum load regulation performance.

INN (Pin 6, 9, Exposed Pad Pin 16): Negative Input. The DFN package's second exposed backside pad (Pin 16) is an electrical connection to INN. To ensure proper electrical and thermal performance, solder Pin 16 to the PCB's negative input supply and tie directly to Pins 6 and 9. Power is supplied to the negative side of the LT3032 through the INN pins. A bypass capacitor is required on this pin if it is more than six inches away from the main input filter capacitor. In general, the output impedance of a battery rises with frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor in the range of 1µF to 10µF is sufficient.

PIN FUNCTIONS

OUTN (Pin 7): Negative Output. This output supplies power to the negative side load. A minimum output capacitor of 1µF is required to prevent oscillations. Larger output capacitors are required for applications with large transient loads to limit peak voltage transients. A parasitic diode exists between OUTN and INN; OUTN can not be pulled more negative than INN during normal operation, or more than 0.5V below INN during a fault condition. See the Applications Information section for more information on output capacitance and bypass capacitors.

ADJN (Pin 8, Adjustable Part Only): Negative Adjust. This is the input to the negative side error amplifier. The ADJN pin has a typical bias current of 30nA that flows out of the pin. The ADJN pin voltage is –1.22V referenced to ground, and the output voltage range is –1.22V to –20V. A parasitic diode exists between ADJN and INN. The ADJN pin cannot be pulled more negative than INN during normal operation, or more than 0.5V below INN during a fault condition.

$\overline{\text{SHDNN}}$ (Pin 10): Negative Shutdown. The $\overline{\text{SHDNN}}$ pin puts the negative side into a low power shutdown state. The $\overline{\text{SHDNN}}$ pin is referenced to ground for regulator control, allowing the negative side to be driven by either positive or negative logic. The negative output will be off if the $\overline{\text{SHDNN}}$ pin is within ±0.8V(typical) of ground. Pulling the $\overline{\text{SHDNN}}$ pin more than –1.9V or +1.4V(typical) will turn the negative output on. The $\overline{\text{SHDNN}}$ pin can be driven by 5V logic or open-collector logic with a pull-up resistor. The pull-up resistor is required to supply the pull-up current of the open-collector device, normally several microamperes, and the $\overline{\text{SHDNN}}$ pin current, typically 3µA out of the pin (for negative logic) or 6µA into the pin (for positive logic). If unused, the $\overline{\text{SHDNN}}$ pin must be connected to INN. The negative output will be shut down if the $\overline{\text{SHDNN}}$ pin is open circuit. A parasitic diode exists between $\overline{\text{SHDNN}}$ and INN, the $\overline{\text{SHDNN}}$ pin cannot be pulled more negative than INN during normal operation, or more than 0.5V below INN during a fault condition.

BYPN (Pin 11): Negative Bypass. The BYPN pin is used to bypass the reference of the negative side regulator to achieve low noise performance. A small capacitor from OUTN to this pin will bypass the reference to lower the output voltage noise. A maximum value of 0.01µF is used for reducing output voltage noise to a typical 30μV_{RMS} over the 10Hz to 100kHz bandwidth. If not used, this pin must be left unconnected.

$\overline{\text{SHDNP}}$ (Pin 12): Positive Shutdown. The $\overline{\text{SHDNP}}$ pin puts the positive side into a low power shutdown state. The positive output will be off when the $\overline{\text{SHDNP}}$ pin is pulled below 0.6V(typical). The $\overline{\text{SHDNP}}$ pin can be driven by 5V logic or open-collector logic with a pull-up resistor. The pull-up resistor is required to supply the pull-up current of the open-collector device, normally several microamperes, and the $\overline{\text{SHDNP}}$ pin current, typically 1µA into the pin. If unused, the $\overline{\text{SHDNP}}$ pin must be connected to INP. The positive output will be shut down if the $\overline{\text{SHDNP}}$ pin is open circuit. The $\overline{\text{SHDNP}}$ pin can be tied directly to the $\overline{\text{SHDNN}}$ pin and both pins driven directly by positive logic for a single point control of both outputs.

NC (Pin 13/Pins 2, 8 for Fixed Voltage Devices): No Connect. The No Connect pin has no connection to internal circuitry and may be tied to INP, GND, INN, $\overline{\text{SHDNP}}$, $\overline{\text{SHDNN}}$, OUTP, OUTN, floated, or tied to any other point.

INP (Pin 14): Positive Input. Power is supplied to the positive side of the LT3032 through the INP pin. A bypass capacitor is required on this pin if it is more than six inches away from the main input filter capacitor. In general, the output impedance of a battery rises with frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor in the range of 1µF to 10µF is sufficient.

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The LT3032 is a dual 150mA positive and negative low noise low dropout linear regulator with micropower quiescent current and shutdown. It supplies ±150mA at a dropout of 300mV. Output voltage noise can be lowered on the positive side to 20μV_{RMS} and to 30μV_{RMS} on the negative side over the 10Hz to 100kHz bandwidth with the addition of 0.01μF reference bypass capacitors. Additionally, the reference bypass capacitors improve transient response, lowering the settling time for transient load conditions. Quiescent current is 25μA for the positive side and –30μA for the negative side (45μA each for the LT3032-12/ LT3032-15), typically dropping to less than 3μA total in shutdown. In addition to the low quiescent current, the LT3032 incorporates several protection features which make it ideal for use in battery-powered systems. If the load is common mode between the two outputs, it does not matter which output starts first; either output can be pulled to the opposing side of ground and the regulator will still start and operate.

Setting Output Voltage

The adjustable LT3032 has output voltage ranges of 1.22V to 20V for the positive side and –1.22V to –20V for the negative side. The output voltages are set by the ratio of two external resistor dividers as shown in Figure 1. The LT3032 servos the outputs to maintain the voltages at the ADJP and ADJN pins to 1.22V and –1.22V, respectively. The current in the bottom resistor of each divider (R1P or R1N) is equal to 1.22V/R1 and the current in the top resistor (R2P or R2N) is equal to the current in the bottom resistor plus the respective ADJP/ADJN pin bias current. The bias current for ADJP and ADJN is 30nA at 25°C, flowing into the pin for ADJP and flowing out of the pin for ADJN. The output voltages can then be calculated using the formulas shown in Figure 1. The value of R1P or R1N should be less than 250k to minimize errors in the resultant output voltage caused by the ADJP/ADJN pin bias current. Note that in shutdown the respective output is turned off and the divider current will be zero. Curves of ADJP Pin Voltage, ADJN Pin Voltage, ADJP Pin Bias Current, and ADJN Pin Bias Current (all vs Temperature) appear in the Typical Performance Characteristics.

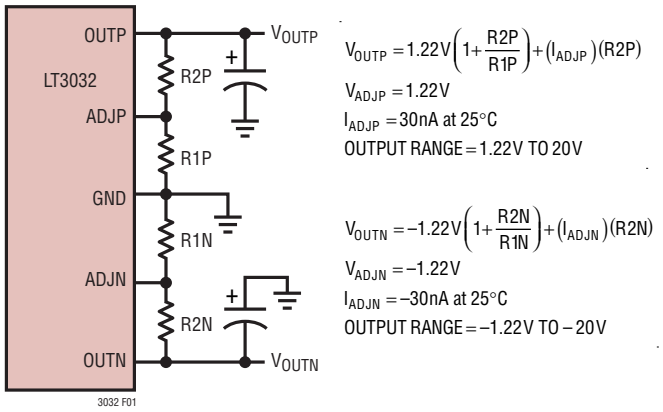


Figure 1. Setting Output Voltages

The LT3032 is tested and specified with the ADJP/ADJN pin tied to the respective OUTP/OUTN pin and a ±5μA DC load (unless otherwise specified) for an output voltage of ±1.22V. Specifications for output voltages greater than this will be proportional to ±1.22V; (V_{OUT}/±1.22V). For example, load regulation for an output current change of 1mA to 150mA is –2mV typical at V_{OUTN} = –1.22V. At V_{OUTN} = –12V, load regulation is:

(–12V/–1.22V)•(–2mV) = –19.6mV

Bypass Capacitors and Low Noise Performance

The LT3032 provides reasonable noise performance without reference bypass capacitors from OUTP/OUTN to the corresponding BYPP/BYPN pin. Using the LT3032 with the addition of reference bypass capacitors lowers output voltage noise. Good quality low leakage capacitors are recommended. These capacitors bypass the internal references for the positive and negative sides of the LT3032, providing low frequency noise poles. The noise poles provided by the bypass capacitors decrease the output voltage noise to as low as 20μV_{RMS} for the positive side and 30μV_{RMS} for the negative side with the use of 0.01μF bypass capacitors.

The BYPP pin and BYPN pin are high impedance nodes and leakage into or out of these pins affects the reference voltage. The BYPP pin operates at approximately 74mV at

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25°C during normal operation where the BYPN pin operates at approximately –60mV. DC leakages on the order of 1µA into or out of these pins can throw off the internal reference by 20% or more.

Output Capacitance and Transient Response

The LT3032 requires output capacitors for stability. It is designed to be stable with most low ESR capacitors (typically ceramic, tantalum or low ESR electrolytic). A minimum output capacitor of 2.2µF with an ESR of 3Ω or less is recommended to prevent oscillations on each output. The LT3032 is a micropower device and output transient response is a function of output capacitance. Larger values of output capacitance decrease peak deviations and provide improved transient response for larger load current changes. Additional capacitors, used to decouple individual components powered by the LT3032, increase the effective output capacitor value. When using bypass capacitors (for low noise operation), larger values of output capacitors are needed. For 100pF of bypass capacitance, 3.3µF of output capacitance is recommended. With a 330pF bypass capacitor or larger, a 4.7µF output capacitor is recommended. The shaded region of Figure 2 defines the range over which the LT3032 is stable. The minimum ESR needed is defined by the amount of bypass capacitance used, while the maximum ESR is 3Ω. These requirements are applicable to both the positive and negative linear regulator.

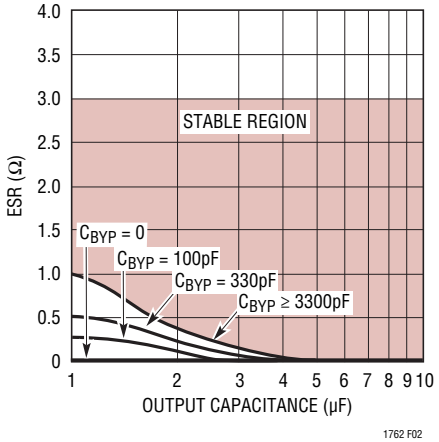


Figure 2. Stability

Give extra consideration to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but they tend to have strong voltage and temperature coefficients as shown in Figures 3 and 4. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied and over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values. Care still must be exercised when using X5R and X7R capacitors. The X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than Y5V and Z5U capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases, but expected capacitance at operating voltage should be verified in situ for a given application.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress. In a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients. Tapping on the ceramic bypass capacitor with a pencil generated the noise shown in Figure 5. Similar vibration induced behavior can masquerade as increased output voltage noise.

APPLICATIONS INFORMATION

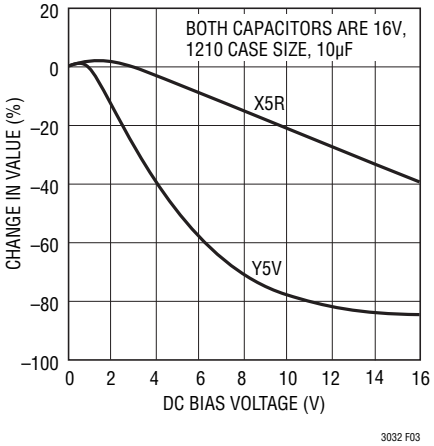


Figure 3. Ceramic Capacitor DC Bias Characteristics

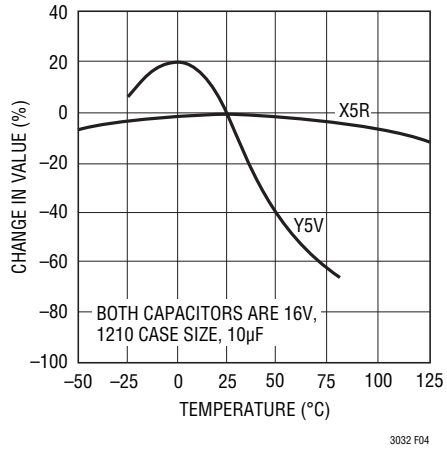


Figure 4. Ceramic Capacitor Temperature Characteristics

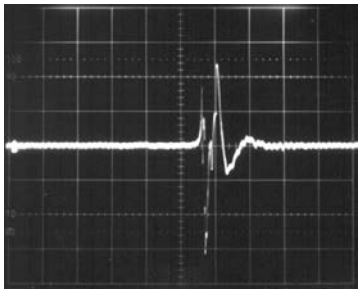


Figure 5. Noise Resulting From Tapping on a Ceramic Capacitor

Stability and Input Capacitance

Low ESR, ceramic input bypass capacitors are acceptable for applications without long input leads. However, applications connecting a power supply to an LT3032's circuit's INP/INN and GND pins with long input wires combined with low ESR, ceramic input capacitors are prone to voltage spikes, reliability concerns and application-specific board oscillations. The input wire inductance found in many battery-powered applications, combined with the low ESR ceramic input capacitor, forms a high-Q LC resonant tank circuit. In some instances this resonant frequency beats against the output current dependent LDO bandwidth and interferes with proper operation. Simple circuit modifications/solutions are then required. This behavior is not indicative of LT3032 instability, but is a common ceramic input bypass capacitor application issue.

The self-inductance, or isolated inductance, of a wire is directly proportional to its length. Wire diameter is not a major factor on its self-inductance. For example, the self-inductance of a 2-AWG isolated wire (diameter = 0.26") is about half the self-inductance of a 30-AWG wire (diameter = 0.01"). One foot of 30-AWG wire has about 465nH of self-inductance.

One of two ways reduces a wire's self-inductance. One method divides the current flowing towards the LT3032 between two parallel conductors. In this case, the farther apart the wires are from each other, the more the self-inductance is reduced; up to a 50% reduction when placed a few inches apart. Splitting the wires basically connects two equal inductors in parallel, but placing them in close proximity gives the wires mutual inductance adding to the self-inductance. The second and most effective way to reduce overall inductance is to place both forward and return current conductors (the input and GND wires) in very close proximity. Two 30-AWG wires separated by only 0.02", used as forward– and return– current conductors, reduce the overall self-inductance to approximately one-fifth that of a single isolated wire.

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If wiring modifications are not permissible for the applications, including series resistance between the power supply and the input of the LT3032 also stabilizes the application. As little as 0.1Ω to 0.5Ω, often less, is effective in damping the LC resonance. If the added impedance between the power supply and the input is unacceptable, adding ESR to the input capacitor also provides the necessary damping of the LC resonance. However, the required ESR is generally higher than the series impedance required.

Thermal Considerations

The power handling capability of the device is limited by the maximum rated junction temperature (125°C). The power dissipated by the device is made up of the following components:

1. Output current of each side multiplied by the respective input/output voltage differential: $(I_{OUT})(V_{IN}$ to $V_{OUT})$, and
2. GND pin current for each side multiplied by its input voltage: $(I_{GND})(V_{IN})$

The GND pin current of each side is found by examining the GND Pin Current curves in the Typical Performance Characteristics. Total power dissipation equals the sum for both channels of the components listed above.

The LT3032 has internal thermal limiting designed to protect each side of the regulator during overload conditions. For continuous normal conditions, the maximum junction temperature rating of 125°C must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

The LT3032 is a surface mount device and heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices.

Note that the exposed pads (Pins 15 and 16) are electrically connected to ground (GND) and the negative input (INN) respectively.

The following table lists thermal resistance as a function of copper area on a fixed board size. All measurements were taken in still air on a 4-layer FR-4 board with 1oz solid internal planes and 2oz external trace planes with a total finished board thickness of 1.6mm.

Table 3. DE Package, 14-Lead DFN

COPPER AREA			
TOPSIDE*	BACKSIDE	BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500mm^2	2500mm^2	2500mm^2	32°C/W
1000mm^2	2500mm^2	2500mm^2	33°C/W
225mm^2	2500mm^2	2500mm^2	38°C/W
100mm^2	2500mm^2	2500mm^2	43°C/W

*Device is mounted on topside

For further information on thermal resistance and using thermal information, refer to JEDEC standard JESD51, notably JESD51-12.

PCB layers, copper weight, board layout and thermal vias affect the resultant thermal resistance. This table provides thermal resistance numbers for best-case 4-layer boards with 1oz internal and 2oz external copper. Modern, multilayer PCBs may not be able to achieve quite the same level performance as found in this table.

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Calculating Junction Temperature

Example: Given a positive output voltage of 3.3V, a positive input voltage of 4V to 6V, output current range from 10mA to 150mA, negative output voltage of –3.3V, negative input voltage of –5V to –6V, a negative output current of –100mA, and a maximum ambient temperature of 50°C, what will the maximum junction temperature be for a 2500mm^2 board with topside copper of 1000mm^2?

The power in each side equals:

$$P_{SIDE} = (V_{IN(MAX)} - V_{OUT})(I_{OUT(MAX)}) + (V_{IN(MAX)} \bullet I_{GND})$$

where,

$I_{OUTP(MAX)}$ = 150mA

$V_{INP(MAX)}$ = 6V

I_{GND} at (I_{OUTP} = 150mA, V_{INP} = 6V) = 3.7mA

$I_{OUTN(MAX)}$ = –100mA

$V_{INN(MAX)}$ = –6V

I_{GND} at (I_{OUTN} = –100mA, V_{INN} = –6V) = –1.5mA

The total power equals:

$$P_{TOTAL} = P_{POSITIVE} + P_{NEGATIVE}$$

So,

$P_{POSITIVE}$ = 150mA(6V – 3.3V) + 3.7mA(6V) = 0.43W

$P_{NEGATIVE}$ = –100mA(–6V+3.3V)–1.5mA(–6V) = 0.28W

P_{TOTAL} = 0.43W + 0.28W = 0.71W

Junction Temperature equals:

$T_J = T_A + P_{TOTAL} \bullet \theta_{JA}$ (using tables)

T_J = 50°C + 0.71W • 33°C/W = 73.4°C

In this case, the junction temperature is below the maximum rating, ensuring reliable operation.

Protection Features

The LT3032 incorporates several protection features that make it ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the LT3032 is protected against reverse input voltages and reverse output voltages on both channels.

Current limit protection and thermal overload protection protect the device against current overload conditions at the outputs of the part. For normal operation, the junction temperature should not be allowed to exceed 125°C.

The positive input of the LT3032 withstands 20V reverse voltage. The negative input also withstands reverse voltage, but the negative input may not be more than 0.5V (one V_{BE}) higher than the OUTN and $\overline{SHDNN}$ pins. This provides protection against batteries that are plugged in backwards.

The outputs of the LT3032 can be pulled to opposing voltages without damaging the part. The outputs may be pulled to the opposing polarity with a load that is common mode between the two and one regulator starts before the other; in this condition, it does not matter which regulator started first. Both sides are capable of having the output pulled to the opposing polarity and both will still start and operate.

If an input is left open circuit or grounded, the corresponding output can be pulled to its opposing polarity by as much as 20V. The output will act like an open circuit; no current will flow into or out of the pin. If the input is powered by a voltage source, the output will source the short-circuit current and will protect itself by thermal limiting. In this case, grounding the respective $\overline{SHDNP}$/$\overline{SHDNN}$ pin will turn off that side of the LT3032 and stop the output from sourcing current.

The ADJP pin can be pulled above or below ground by ±7V without damage to the device. If the input is left open circuit or grounded, the ADJP pin acts like an open circuit when pulled below ground and like a large resistor (typically 100k) in series with a diode when pulled above ground.

APPLICATIONS INFORMATION

In situations where the ADJP pin is connected to a resistor divider that would pull the ADJP pin above its 7V clamp voltage if the output is pulled high, the ADJP pin input current must be limited to less than 5mA. For example, a resistor divider is used to provide a 1.5V output from the 1.22V reference and the output is forced to 20V. The top resistor of the divider must be chosen to limit the current into the ADJP pin to less than 5mA when the ADJP pin is at 7V. The 13V difference between OUTP and ADJP divided by the 5mA maximum current into the ADJP pin yields a minimum top resistor value of 2.6k.

In circuits where a backup battery is required on the positive output, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage or is left open circuit. Current flow back into OUTP follows the curve shown in Figure 6.

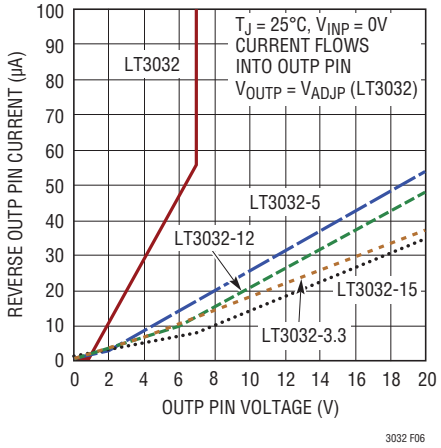


Figure 6. Reverse Output Current

If the INP pin is forced below the OUTP pin or the OUTP pin is pulled above the INP pin, input current typically drops to less than 2µA. This can happen if the device is connected to a discharged (low voltage) battery and the output is held up by a backup battery or a second regulator circuit. The state of the $\overline{\text{SHDNP}}$ pin has no effect on the reverse output current if OUTP is pulled above INP.

Like many IC power regulators, the negative side of the LT3032 has safe operating area (SOA) protection. The safe operating area protection activates when the differential voltage between INN and OUTN is greater than -7V. The SOA protection decreases current limit as a function of the voltage differential between INN and OUTN and keeps the power transistor inside a safe operating region for all values of forward input-to-output voltage. The protection is designed to provide some output current at all values of INN to OUTN differential voltage up to the Absolute Maximum Rating. A 50µA load is required to maintain regulation for INN to OUTN differential voltages greater than –7V. When in shutdown, protection circuitry remains active and will cause the output to rise slightly at zero load. A small pre-load is needed for zero output, if desired (see graph of Quiescent Current vs Input Voltage in Typical Performance Characteristics).

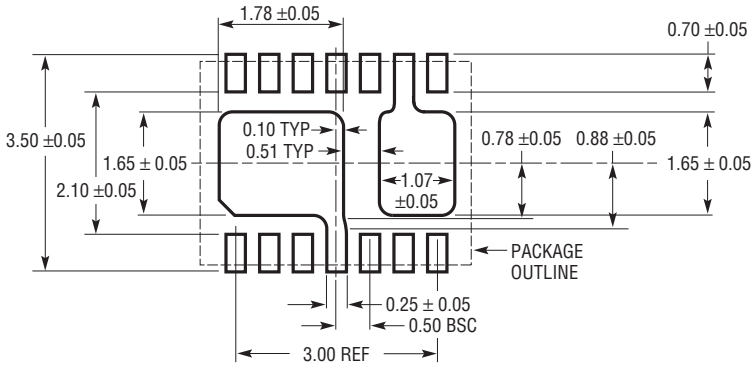
When power to the negative side is first turned on, as the input voltage rises, OUTN follows INN, allowing the regulator to start into very heavy loads. During start-up, as the INN voltage is rising, the differential voltage between INN and OUTN is small, allowing the negative side to supply large output currents. With a high INN voltage, a problem can occur wherein removal of an output short will not allow the output voltage to fully recover. Other regulators, such as the LT1175, LT1964, and LT3080 also exhibit this phenomenon, so it is not unique to the LT3032.

The problem occurs with a heavy output load when the INN voltage is high and the OUTN voltage is low. Common situations are immediately after the removal of a short-circuit or when the $\overline{\text{SHDNN}}$ pin is pulled high after the INN pin has already been turned on. The load line for such a load may intersect the output current curve at two points. If this happens, there are two stable operating points for the negative side of the LT3032. With this double intersection, the INN supply may need to be cycled down to zero and brought up again to make OUTN recover.

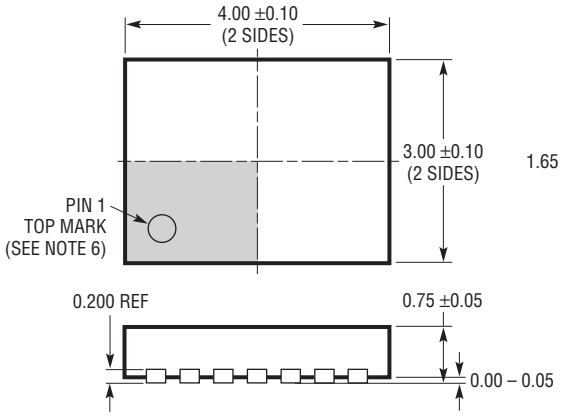
PACKAGE DESCRIPTION

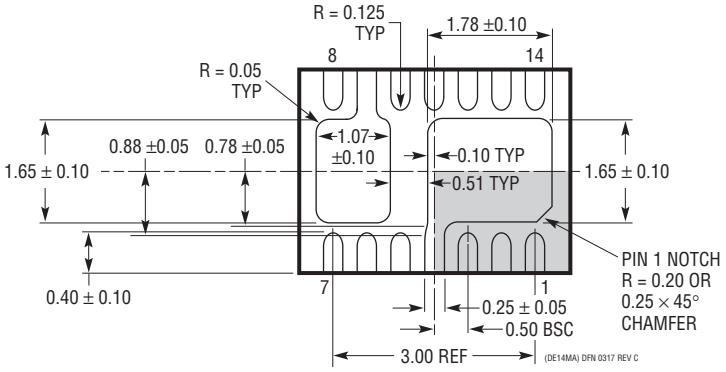
Please refer to http://www.linear.com/product/LT3032#packaging/ for the most recent package drawings.

DE14MA Package
14-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1731 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

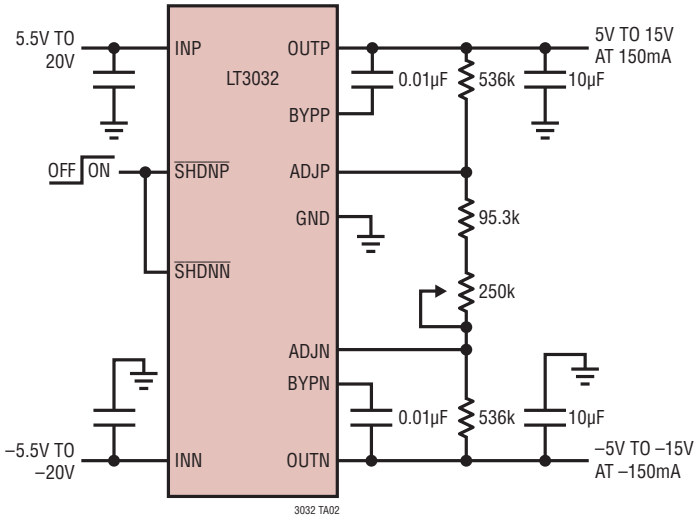
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	08/10	Updated all applicable sections to add fixed voltage ±5V option.	1-7, 9-14
B	01/11	Swapped OUTN and INN pins in Absolute Maximum Ratings. Revised values in $\overline{SHDNN}$ and $\overline{SHDNP}$ descriptions in Pin Functions. Revised quiescent current for the positive side up to 25µA in Applications Information.	2 12, 13 14
C	09/11	Updated to add 12V and 15V options.	1-12, 21
D	03/12	Added MP-Grade to Order Information and Absolute Maximum Ratings.	2, 3
E	08/14	Added ±3.3V option.	1-8, 10-12, 21, 24
F	04/17	Updated Package Description.	22

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

±5V to ±15V Tracking Supply



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1175	800mA Negative Low Dropout Micropower Regulator	V_{IN}: –4.5V to -20V, I_Q = 45µA, 0.5V Dropout Voltage, S8, DD-Pak, TO-220 and SOT-223 Packages
LT1761	100mA, Low Noise LDO	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, ThinSOT package
LT1762	150mA, Low Noise LDO	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, MS8 package
LTC1844	150mA, Very Low Dropout LDO	80mV Dropout Voltage, Low Noise <30µV_{RMS}, V_{IN} = 1.6V to 6.5V, Stable with 1µF Output Capacitors, ThinSOT Package
LT1962	300mA, Low Noise LDO	270mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, MS8 Package
LT1964	200mA, Low Noise, Negative LDO	340mV Dropout Voltage, Low Noise 30µV_{RMS}, V_{IN} = –1.8V to –20V, ThinSOT and DFN Packages
LT3023	Dual 100mA, Low Noise, Micropower LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, VDO = 0.30V, I_Q = 40µA, ISD < 1µA; DFN and MS10E Packages
LT3024	Dual 100mA/500mA, Low Noise, Micropower LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, VDO = 0.30V, I_Q = 60µA, ISD < 1µA; DFN and TSSOP-16E Packages
LT3027	Dual 100mA, Low Noise, Micropower LDO with Independent Inputs	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, VDO = 0.30V, I_Q = 50µA, ISD < 1µA; DFN and MS10E Packages
LT3028	Dual 100mA/500mA, Low Noise, Micropower LDO with Independent Inputs	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, VDO = 0.32V, I_Q = 60µA, ISD < 1µA; DFN and TSSOP-16E Packages
LT3029	Dual 500mA/500mA, Low Dropout, Low Noise, Micropower Linear Regulator	Low Noise: 20µV_{RMS} (10Hz to 100kHz), Low Quiescent Current: 55µA per Channel Wide Input Voltage Range: 1.8V to 20V (Common or Independent Input Supply) Adjustable Output: 1.215V Reference, Very Low Quiescent Current in Shutdown: <1µA per Channel Stable with 3.3µF Minimum Output Capacitor, Thermally Enhanced 16-Lead MSOP and 16-Lead (4mm × 3mm) DFN Packages
LT3082	200mA, Parallelable, Single Resistor, Low Dropout Linear Regulator	Wide Input Voltage Range: 1.2V to 40V Low Value Input/Output Capacitors Required: 0.22µF, Single Resistor Sets Output Voltage Initial Set Pin Current Accuracy: 1%, Low Output Noise: 40µV_{RMS} (10Hz to 100kHz) Reverse-Battery Protection, Reverse-Current Protection 8-Lead SOT-23, 3-Lead SOT-223 and 8-Lead 3mm × 3mm DFN Packages

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