

# 15V, 200mA Synchronous Buck-Boost DC/DC Converter with 1.3 $\mu$ A Quiescent Current

## FEATURES

- Regulates  $V_{OUT}$  Above, Below or Equal to  $V_{IN}$
- Wide  $V_{IN}$  Range: 2.42V to 15V, 1.92V to 15V After Start-Up (Bootstrapped)
- Wide  $V_{OUT}$  Range: 1.4V to 15.75V
- 200mA Output Current in Buck Mode
- Single Inductor
- 1.3 $\mu$ A Quiescent Current
- Programmable Maximum Power Point Control
- 1.2MHz Ultralow Noise PWM
- Current Mode Control
- Pin Selectable Burst Mode<sup>®</sup> Operation
- Up to 95% Efficiency
- Accurate RUN Pin Threshold
- Power Good Indicator
- 10nA Shutdown Current
- Thermally Enhanced 3mm  $\times$  3mm QFN and 16-Lead MSOP Packages

## APPLICATIONS

- Industrial Wireless Sensor Nodes
- Post-Regulator for Harvested Energy
- Solar Panel Post-Regulator/Charger
- Intrinsically Safe Power Supplies
- Wireless Microphones
- Avionics-Grade Wireless Headsets

## DESCRIPTION

The LTC<sup>®</sup>3129 is a high efficiency, 200mA buck-boost DC/DC converter with a wide  $V_{IN}$  and  $V_{OUT}$  range. It includes an accurate RUN pin threshold to allow predictable regulator turn-on and a maximum power point control (MPPC) capability that ensures maximum power extraction from non-ideal power sources such as photovoltaic panels.

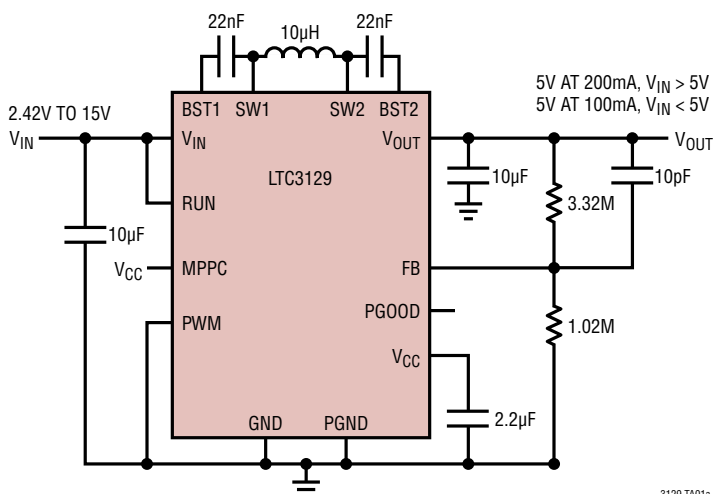
The LTC3129 employs an ultralow noise, 1.2MHz PWM switching architecture that minimizes solution footprint by allowing the use of tiny, low profile inductors and ceramic capacitors. Built-in loop compensation and soft-start simplify the design. For high efficiency operation at light loads, automatic Burst Mode operation can be selected, reducing the quiescent current to just 1.3 $\mu$ A.

Additional features include a power good output, less than 10nA of shutdown current and thermal shutdown.

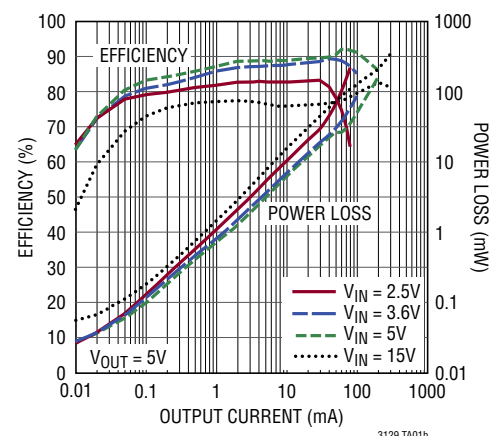
The LTC3129 is available in thermally enhanced 3mm  $\times$  3mm QFN and 16-lead MSOP packages. For fixed output voltage options, see the functionally equivalent LTC3129-1, which eliminates the need for an external feedback divider.

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## TYPICAL APPLICATION



Efficiency and Power Loss vs Load



3129 TA01a

3129 TA01b

3129fc

# LTC3129

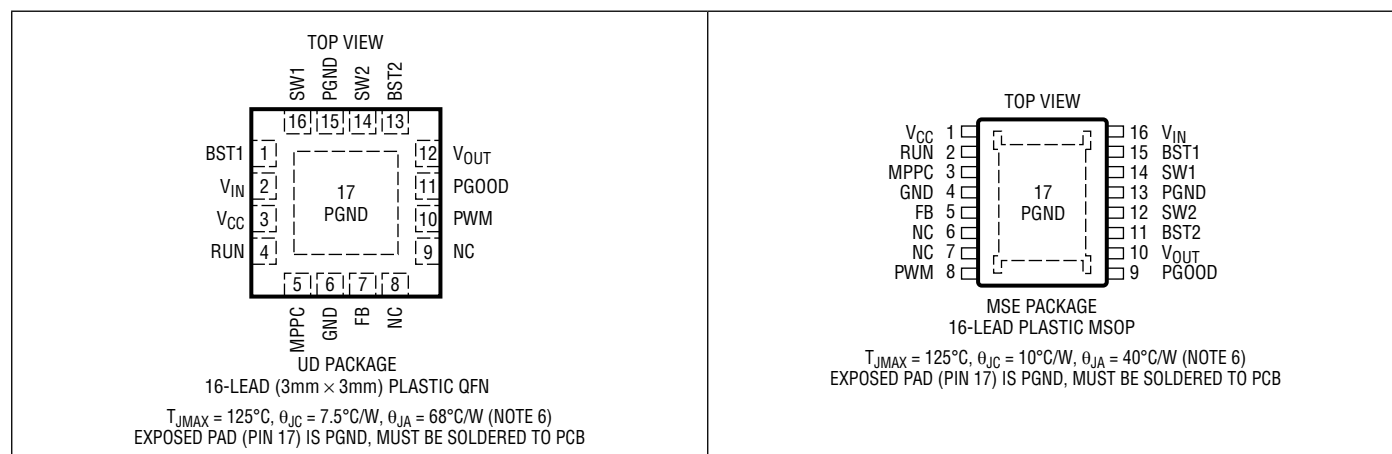
## ABSOLUTE MAXIMUM RATINGS

(Notes 1, 8)

$V_{IN}$ ,  $V_{OUT}$  Voltages ..... -0.3V to 18V  
 SW1 DC Voltage..... -0.3V to ( $V_{IN} + 0.3V$ )  
 SW2 DC Voltage..... -0.3V to ( $V_{OUT} + 0.3V$ )  
 SW1, SW2 Pulsed (<100ns) Voltage ..... -1V to 19V  
 BST1 Voltage ..... (SW1 - 0.3V) to (SW1 + 6V)  
 BST2 Voltage ..... (SW2 - 0.3V) to (SW2 + 6V)  
 RUN, PGOOD Voltages..... -0.3V to 18V

$V_{CC}$ , FB, PWM, MPPC Voltages..... -0.3V to 6V  
 PGOOD Sink Current ..... 15mA  
 Operating Junction Temperature Range  
 (Notes 2, 5)..... -40°C to 125°C  
 Storage Temperature Range ..... -65°C to 150°C  
 MSE Lead Temperature (Soldering, 10 sec) ..... 300°C

## PIN CONFIGURATION



## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL     | PART MARKING* | PACKAGE DESCRIPTION             | TEMPERATURE RANGE |
|------------------|-------------------|---------------|---------------------------------|-------------------|
| LTC3129EUD#PBF   | LTC3129EUD#TRPBF  | LGDR          | 16-Lead (3mm × 3mm) Plastic QFN | -40°C to 125°C    |
| LTC3129IUD#PBF   | LTC3129IUD#TRPBF  | LGDR          | 16-Lead (3mm × 3mm) Plastic QFN | -40°C to 125°C    |
| LTC3129EMSE#PBF  | LTC3129EMSE#TRPBF | 3129          | 16-Lead Plastic MSOP            | -40°C to 125°C    |
| LTC3129IMSE#PBF  | LTC3129IMSE#TRPBF | 3129          | 16-Lead Plastic MSOP            | -40°C to 125°C    |

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandree/>. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

# ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$  (Note 2). Unless otherwise noted,  $V_{IN} = 12\text{V}$ ,  $V_{OUT} = 5\text{V}$ .

| PARAMETER                                          | CONDITIONS                                                                                                   |   | MIN   | TYP     | MAX     | UNITS         |
|----------------------------------------------------|--------------------------------------------------------------------------------------------------------------|---|-------|---------|---------|---------------|
| $V_{IN}$ Start-Up Voltage                          |                                                                                                              | ● |       | 2.25    | 2.42    | V             |
| Input Voltage Range                                | $V_{CC} > 2.42\text{V}$ (Back-Driven)                                                                        | ● | 1.92  |         | 15      | V             |
| $V_{IN}$ UVLO Threshold (Rising)                   | $V_{CC} > 2.42\text{V}$ (Back-Driven)                                                                        | ● | 1.8   | 1.9     | 2.0     | V             |
| $V_{IN}$ UVLO Hysteresis                           |                                                                                                              | ● | 80    | 100     | 130     | mV            |
| Output Voltage Adjust Range                        |                                                                                                              | ● | 1.4   |         | 15.75   | V             |
| Feedback Voltage                                   |                                                                                                              | ● | 1.151 | 1.175   | 1.199   | V             |
| Feedback Input Current                             | $FB = 1.25\text{V}$                                                                                          |   |       | 0.1     | 10      | nA            |
| Quiescent Current ( $V_{IN}$ ) – Shutdown          | $RUN = 0\text{V}$ , Including Switch Leakage                                                                 |   |       | 10      | 100     | nA            |
| Quiescent Current ( $V_{IN}$ ) UVLO                | Either $V_{IN}$ or $V_{CC}$ Below Their UVLO Threshold, or $RUN$ Below the Threshold to Enable Switching     |   |       | 1.9     | 3       | $\mu\text{A}$ |
| Quiescent Current – Burst Mode Operation           | Measured on $V_{IN}$ , $FB > 1.25\text{V}$<br>$PWM = 0\text{V}$ , $RUN = V_{IN}$                             |   |       | 1.3     | 2.0     | $\mu\text{A}$ |
| N-Channel Switch Leakage on $V_{IN}$ and $V_{OUT}$ | $SW1 = 0\text{V}$ , $V_{IN} = 15\text{V}$<br>$SW2 = 0\text{V}$ , $V_{OUT} = 15\text{V}$<br>$RUN = 0\text{V}$ |   |       | 10      | 50      | nA            |
| N-Channel Switch On-Resistance                     | $V_{CC} = 4\text{V}$                                                                                         |   |       | 0.75    |         | $\Omega$      |
| Inductor Average Current Limit                     | $V_{OUT} > UV$ Threshold (Note 4)                                                                            | ● | 220   | 275     | 350     | mA            |
|                                                    | $V_{OUT} < UV$ Threshold (Note 4)                                                                            | ● | 80    | 130     | 200     | mA            |
| Inductor Peak Current Limit                        | (Note 4)                                                                                                     | ● | 400   | 500     | 680     | mA            |
| Maximum Boost Duty Cycle                           | $FB = 1.10\text{V}$ . Percentage of Period $SW2$ is Low in Boost Mode (Note 7)                               | ● | 85    | 89      | 95      | %             |
| Minimum Duty Cycle                                 | $FB = 1.25\text{V}$ . Percentage of Period $SW1$ is High in Buck Mode (Note 7)                               | ● |       |         | 0       | %             |
| Switching Frequency                                | $PWM = V_{CC}$                                                                                               | ● | 1.0   | 1.2     | 1.4     | MHz           |
| $SW1$ and $SW2$ Minimum Low Time                   | (Note 3)                                                                                                     |   |       | 90      |         | ns            |
| MPPC Voltage                                       |                                                                                                              | ● | 1.12  | 1.175   | 1.22    | V             |
| MPPC Input Current                                 | $MPPC = 5\text{V}$                                                                                           |   |       | 1       | 10      | nA            |
| $RUN$ Threshold to Enable $V_{CC}$                 |                                                                                                              | ● | 0.5   | 0.9     | 1.15    | V             |
| $RUN$ Threshold to Enable Switching (Rising)       | $V_{CC} > 2.4\text{V}$                                                                                       | ● | 1.16  | 1.22    | 1.28    | V             |
| $RUN$ (Switching) Threshold Hysteresis             |                                                                                                              |   | 50    | 80      | 120     | mV            |
| $RUN$ Input Current                                | $RUN = 15\text{V}$                                                                                           |   |       | 1       | 10      | nA            |
| PWM Input High                                     |                                                                                                              | ● | 1.6   |         |         | V             |
| PWM Input Low                                      |                                                                                                              | ● |       |         | 0.5     | V             |
| PWM Input Current                                  | $PWM = 5\text{V}$                                                                                            |   |       | 0.1     | 1       | $\mu\text{A}$ |
| Soft-Start Time                                    |                                                                                                              |   |       | 3       |         | ms            |
| $V_{CC}$ Voltage                                   | $V_{IN} > 4.85\text{V}$                                                                                      | ● | 3.4   | 4.1     | 4.7     | V             |
| $V_{CC}$ Dropout Voltage ( $V_{IN} - V_{CC}$ )     | $V_{IN} = 3.0\text{V}$ , Switching<br>$V_{IN} = 2.0\text{V}$ ( $V_{CC}$ in UVLO)                             |   |       | 35<br>0 | 60<br>2 | mV<br>mV      |
| $V_{CC}$ UVLO Threshold (Rising)                   |                                                                                                              | ● | 2.1   | 2.25    | 2.42    | V             |
| $V_{CC}$ UVLO Hysteresis                           |                                                                                                              |   |       | 60      |         | mV            |
| $V_{CC}$ Current Limit                             | $V_{CC} = 0\text{V}$                                                                                         | ● | 4     | 20      | 60      | mA            |
| $V_{CC}$ Back-Drive Voltage (Maximum)              |                                                                                                              | ● |       |         | 5.5     | V             |
| $V_{CC}$ Input Current (Back-Driven)               | $V_{CC} = 5.5\text{V}$ (Switching)                                                                           |   |       | 2       | 4       | mA            |
| $V_{CC}$ Leakage to $V_{IN}$ if $V_{CC} > V_{IN}$  | $V_{CC} = 5.5\text{V}$ , $V_{IN} = 1.8\text{V}$ , Measured on $V_{IN}$                                       |   |       | -27     |         | $\mu\text{A}$ |
| $V_{OUT}$ UV Threshold (Rising)                    |                                                                                                              | ● | 0.95  | 1.15    | 1.35    | V             |

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$  (Note 2). Unless otherwise noted,  $V_{IN} = 12\text{V}$ ,  $V_{OUT} = 5\text{V}$ .

| PARAMETER                    | CONDITIONS                                                   | MIN  | TYP  | MAX | UNITS         |
|------------------------------|--------------------------------------------------------------|------|------|-----|---------------|
| $V_{OUT}$ UV Hysteresis      |                                                              |      | 150  |     | mV            |
| $V_{OUT}$ Current – Shutdown | RUN = 0V, $V_{OUT} = 15\text{V}$ Including Switch Leakage    |      | 10   | 100 | nA            |
| $V_{OUT}$ Current – Sleep    | PWM = 0V, FB = 1.25V                                         |      | 10   |     | nA            |
| $V_{OUT}$ Current – Active   | PWM = $V_{CC}$ , $V_{OUT} = 15\text{V}$ (Note 4), FB = 1.25V |      | 5    | 9   | $\mu\text{A}$ |
| PGOOD Threshold, Falling     | Referenced to Programmed $V_{OUT}$ Voltage                   | -5.5 | -7.5 | -10 | %             |
| PGOOD Hysteresis             | Referenced to Programmed $V_{OUT}$ Voltage                   |      | 2.5  |     | %             |
| PGOOD Voltage Low            | $I_{SINK} = 1\text{mA}$                                      |      | 250  | 300 | mV            |
| PGOOD Leakage                | PGOOD = 15V                                                  |      | 1    | 50  | nA            |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC3129 is tested under pulsed load conditions such that  $T_J \approx T_A$ . The LTC3129E is guaranteed to meet specifications from  $0^\circ\text{C}$  to  $85^\circ\text{C}$  junction temperature. Specifications over the  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3129I is guaranteed over the full  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  operating junction temperature range. The junction temperature ( $T_J$ ) is calculated from the ambient temperature ( $T_A$ ) and power dissipation ( $P_D$ ) according to the formula:  $T_J = T_A + (P_D \cdot \theta_{JA})$ , where  $\theta_{JA}$  is the package thermal impedance. Note that the maximum ambient temperature consistent with these specifications, is determined by specific operating conditions in conjunction with board layout, the rated thermal package thermal resistance and other environmental factors.

**Note 3:** Specification is guaranteed by design and not 100% tested in production.

**Note 4:** Current measurements are made when the output is not switching.

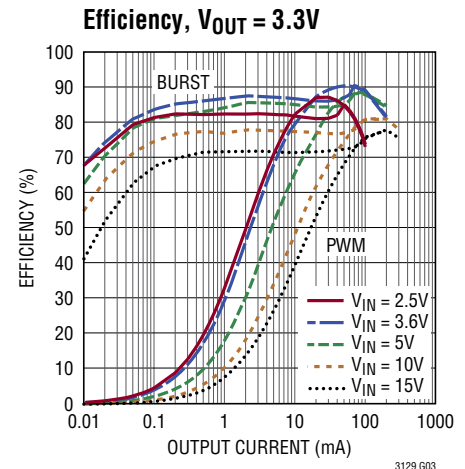
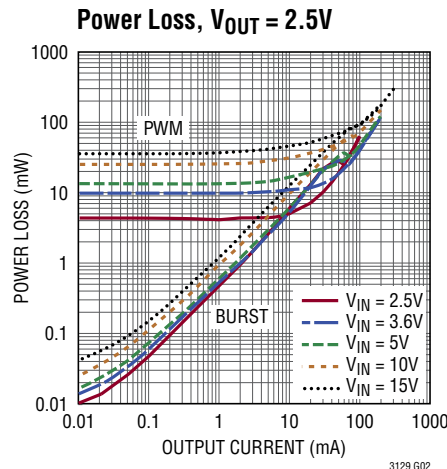
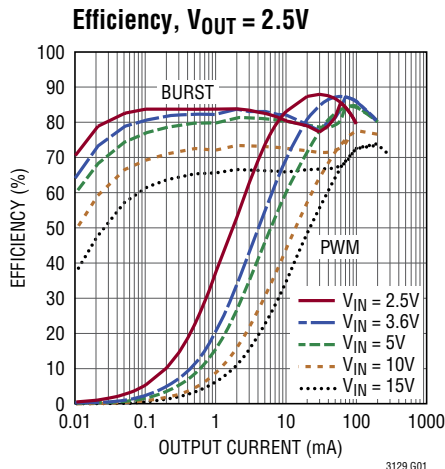
**Note 5:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed  $125^\circ\text{C}$  when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

**Note 6:** Failure to solder the exposed backside of the package to the PC board ground plane will result in a much higher thermal resistance.

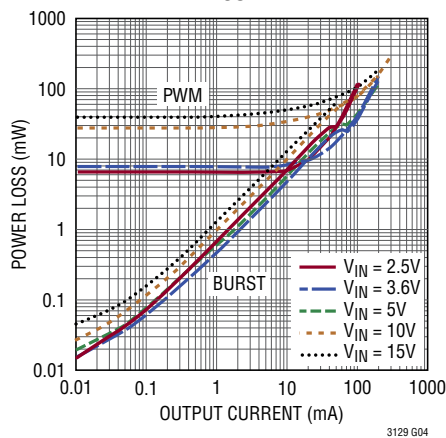
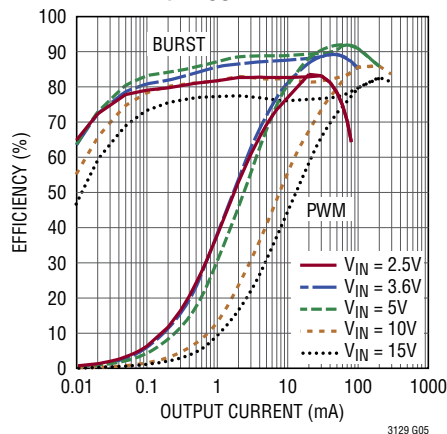
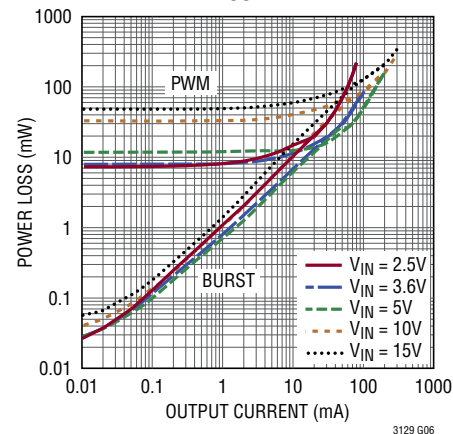
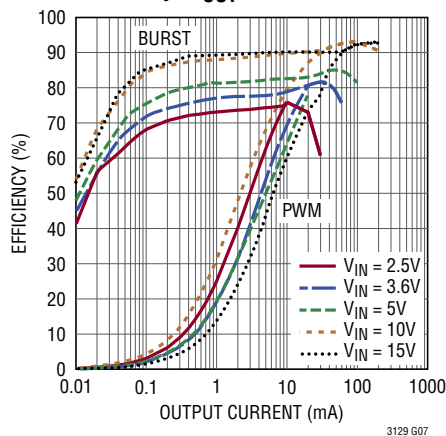
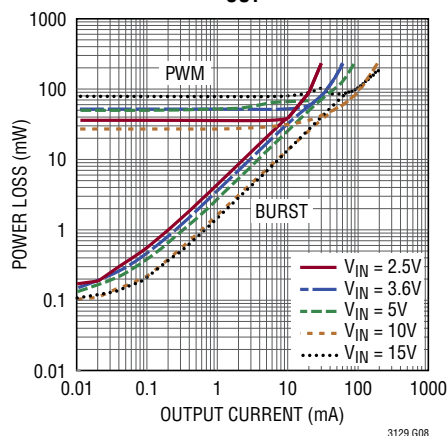
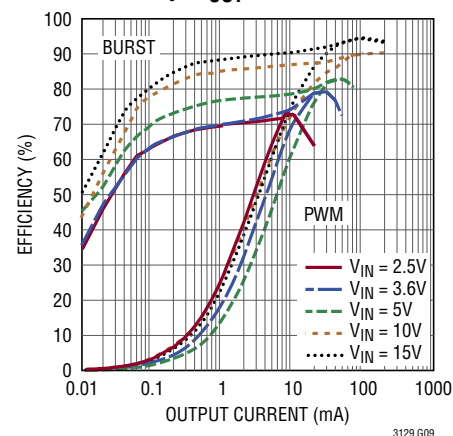
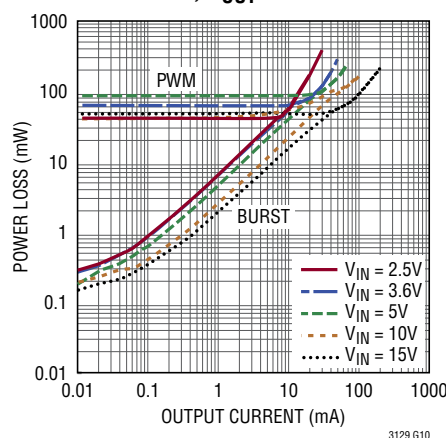
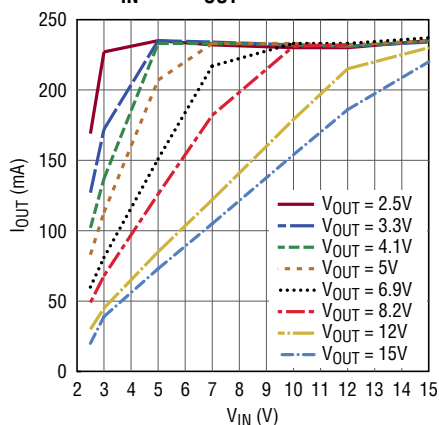
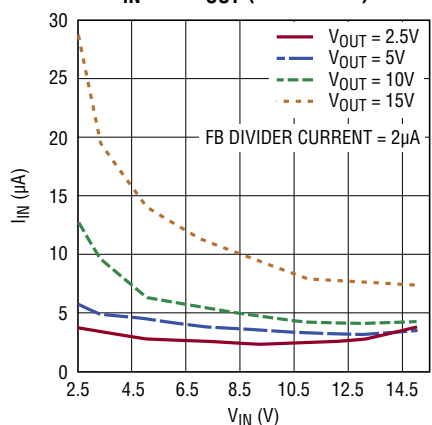
**Note 7:** Switch timing measurements are made in an open-loop test configuration. Timing in the application may vary somewhat from these values due to differences in the switch pin voltage during non-overlap durations when switch pin voltage is influenced by the magnitude and duration of the inductor current.

**Note 8:** Voltage transients on the switch pin(s) beyond the DC limits specified in the Absolute Maximum Ratings are non-disruptive to normal operation when using good layout practices as described elsewhere in the data sheet and application notes and as seen on the product demo board.

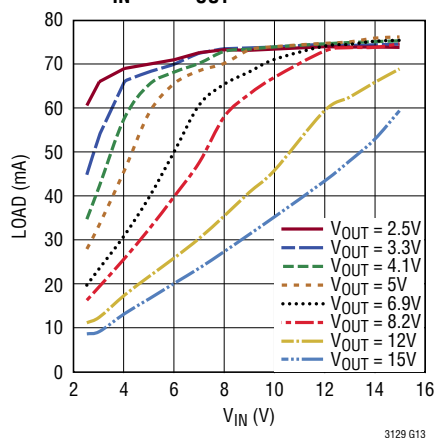
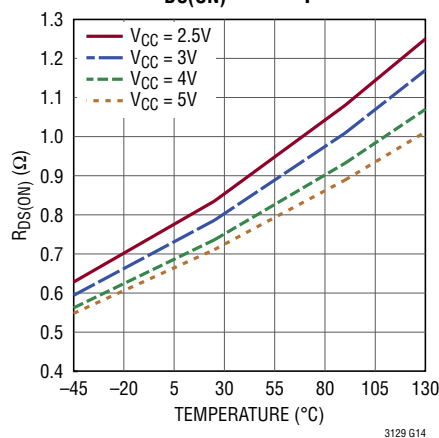
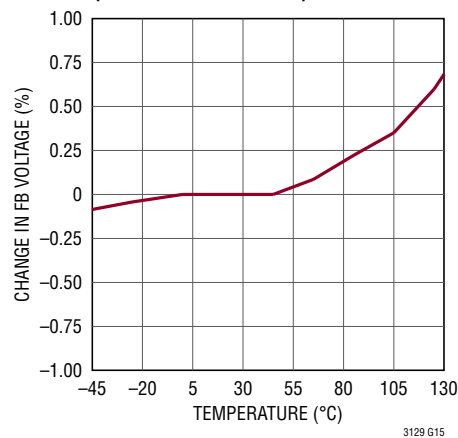
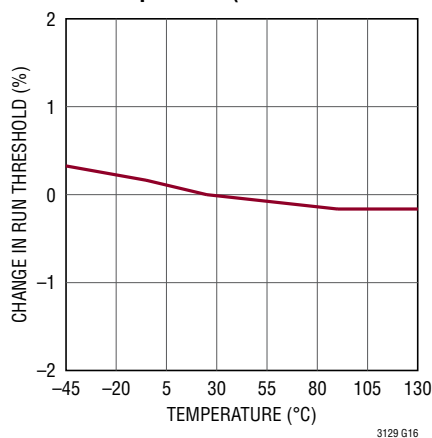
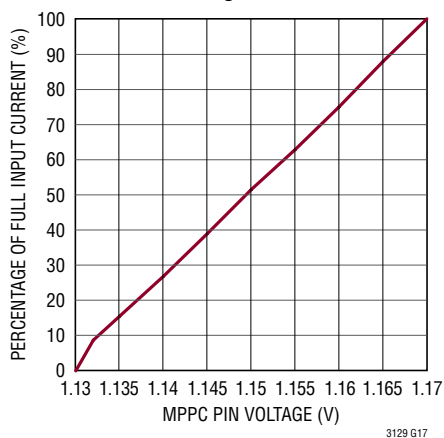
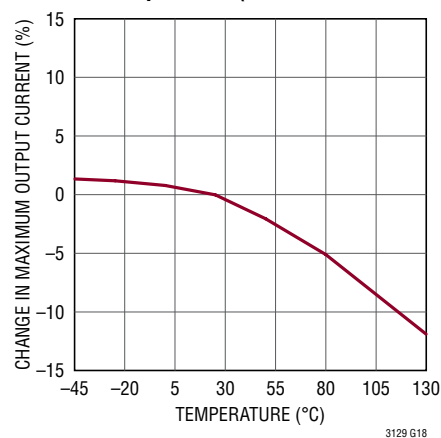
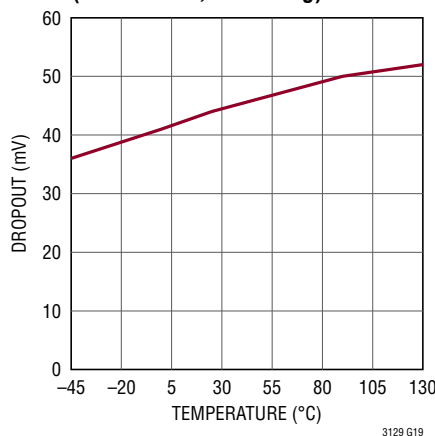
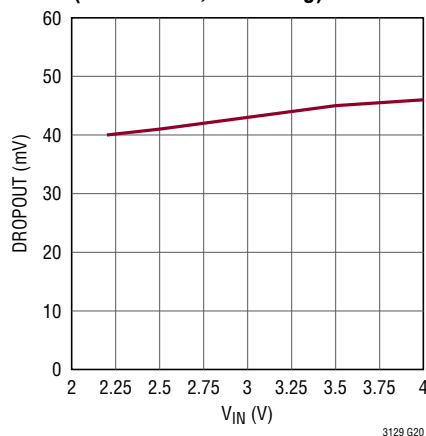
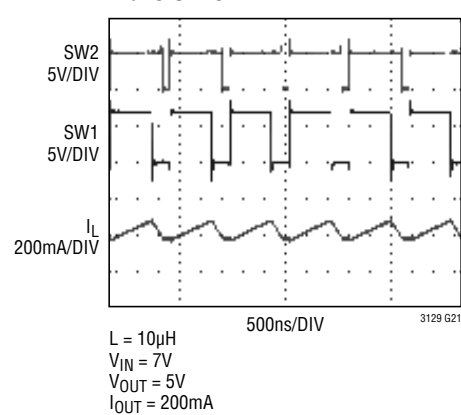
## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , unless otherwise noted.



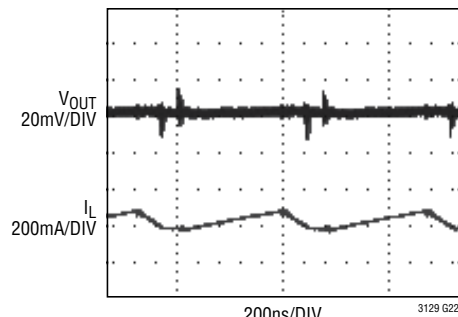
# TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Power Loss,  $V_{OUT} = 3.3\text{V}$ Efficiency,  $V_{OUT} = 5\text{V}$ Power Loss,  $V_{OUT} = 5\text{V}$ Efficiency,  $V_{OUT} = 12\text{V}$ Power Loss,  $V_{OUT} = 12\text{V}$ Efficiency,  $V_{OUT} = 15\text{V}$ Power Loss,  $V_{OUT} = 15\text{V}$ Maximum Output Current  
vs  $V_{IN}$  and  $V_{OUT}$ No Load Input Current  
vs  $V_{IN}$  and  $V_{OUT}$  (PWM = 0V)

# TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , unless otherwise noted.

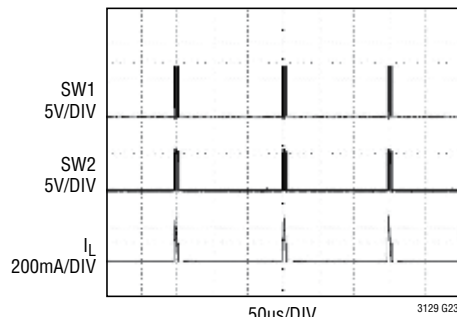
**Burst Mode Threshold vs  $V_{IN}$  and  $V_{OUT}$** 

**Switch  $R_{DS(ON)}$  vs Temperature**

**FB Voltage vs Temperature (Normalized to  $25^\circ\text{C}$ )**

**Accurate RUN Threshold vs Temperature (Normalized to  $25^\circ\text{C}$ )**

**Average Input Current Limit vs MPPC Voltage**

**Maximum Output Current vs Temperature (Normalized to  $25^\circ\text{C}$ )**

 **$V_{CC}$  Dropout Voltage vs Temperature (PWM Mode, Switching)**

 **$V_{CC}$  Dropout Voltage vs  $V_{IN}$  (PWM Mode, Switching)**

**Fixed Frequency PWM Waveforms**


# TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , unless otherwise noted.

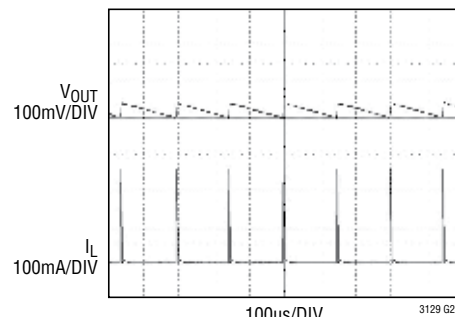
Fixed Frequency Ripple on  $V_{OUT}$ 

$L = 10\mu\text{H}$   
 $V_{IN} = 7\text{V}$   
 $V_{OUT} = 5\text{V}$   
 $I_{OUT} = 200\text{mA}$   
 $C_{OUT} = 10\mu\text{F}$

Burst Mode Waveforms

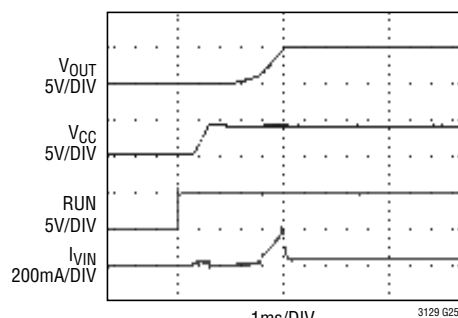


$L = 10\mu\text{H}$   
 $V_{IN} = 7\text{V}$   
 $V_{OUT} = 5\text{V}$   
 $I_{OUT} = 5\text{mA}$   
 $C_{OUT} = 22\mu\text{F}$

Burst Mode Ripple on  $V_{OUT}$ 

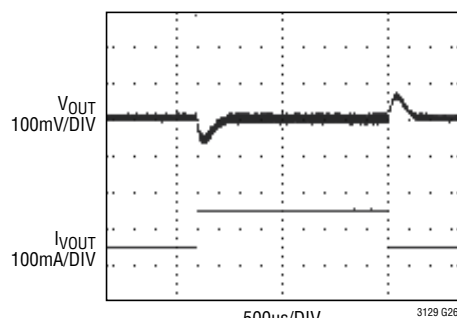
$L = 10\mu\text{H}$   
 $V_{IN} = 7\text{V}$   
 $V_{OUT} = 5\text{V}$   
 $I_{OUT} = 5\text{mA}$   
 $C_{OUT} = 22\mu\text{F}$  (WITH THE RECOMMENDED  
 FEEDFORWARD CAPACITOR)

Start-Up Waveforms



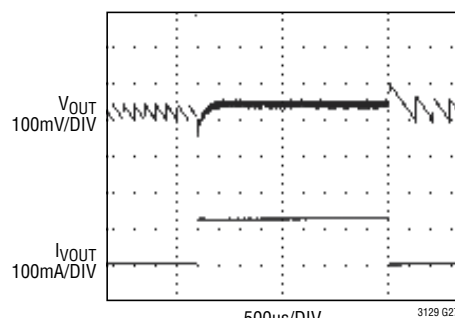
$V_{IN} = 7\text{V}$   
 $V_{OUT} = 5\text{V}$   
 $I_{OUT} = 50\text{mA}$   
 $C_{OUT} = 22\mu\text{F}$

Step Load Transient Response in Fixed Frequency

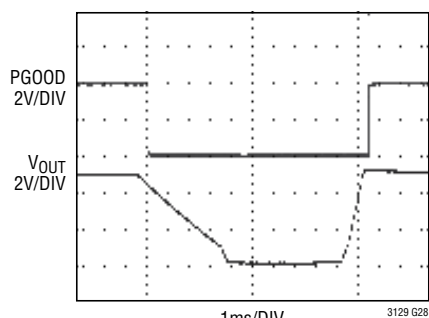


$L = 10\mu\text{H}$   
 $V_{IN} = 7\text{V}$   
 $V_{OUT} = 5\text{V}$   
 $C_{OUT} = 10\mu\text{F}$   
 $I_{OUT} = 50\text{mA}$  to  $150\text{mA}$  STEP

Step Load Transient Response in Burst Mode Operation

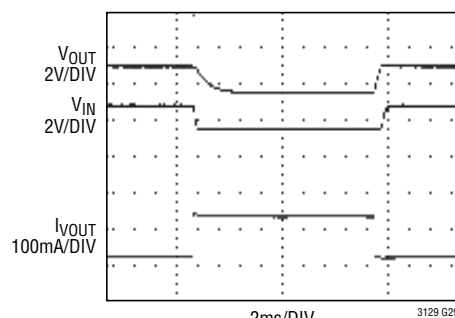


$L = 10\mu\text{H}$   
 $V_{IN} = 7\text{V}$   
 $V_{OUT} = 5\text{V}$   
 $C_{OUT} = 22\mu\text{F}$  (WITH THE RECOMMENDED  
 FEEDFORWARD CAPACITOR)  
 $I_{OUT} = 5\text{mA}$  to  $125\text{mA}$  STEP

PGOOD Response to a Drop On  $V_{OUT}$ 

$V_{OUT} = 5\text{V}$

MPPC Response to a Step Load



$V_{IN} = 5V_{OC}$   
 $V_{MPPC}$  SET TO  $3.5\text{V}$   
 $C_{IN} = 22\mu\text{F}$ ,  $R_{IN} = 10\Omega$ ,  
 $V_{OUT} = 5\text{V}$ ,  $C_{OUT} = 22\mu\text{F}$   
 $I_{OUT} = 25\text{mA}$  to  $125\text{mA}$  STEP

## PIN FUNCTIONS (QFN/MSOP)

**BST1 (Pin 1/Pin 15):** Bootstrapped Floating Supply for High Side NMOS Gate Drive. Connect to SW1 through a 22nF capacitor, as close to the part as possible. The value is not critical. Any value from 4.7nF to 47nF may be used.

**V<sub>IN</sub> (Pin 2/Pin 16):** Input Voltage for the Converter. Connect a minimum of 4.7μF ceramic decoupling capacitor from this pin to the ground plane, as close to the pin as possible.

**V<sub>CC</sub> (Pin 3/Pin 1):** Output voltage of the internal voltage regulator. This is the supply pin for the internal circuitry. Bypass this output with a minimum of 2.2μF ceramic capacitor close to the pin. This pin may be back-driven by an external supply, up to a maximum of 5.5V.

**RUN (Pin 4/Pin 2):** Input to the Run Comparator. Pull this pin above 1.1V to enable the V<sub>CC</sub> regulator and above 1.28V to enable the converter. Connecting this pin to a resistor divider from V<sub>IN</sub> to ground allows programming a V<sub>IN</sub> start threshold higher than the 1.8V (typical) V<sub>IN</sub> UVLO threshold. In this case, the typical V<sub>IN</sub> turn-on threshold is determined by  $V_{IN} = 1.22V \cdot [1 + (R3/R4)]$  (see Figure 2).

**MPPC (Pin 5/Pin 3):** Maximum Power Point Control Programming Pin. Connect this pin to a resistor divider from V<sub>IN</sub> to ground to enable the MPPC functionality. If the V<sub>OUT</sub> load is greater than what the power source can provide, the MPPC will reduce the inductor current to regulate V<sub>IN</sub> to a voltage determined by:  $V_{IN} = 1.175V \cdot [1 + (R5/R6)]$  (see Figure 3). By setting the V<sub>IN</sub> regulation voltage appropriately, maximum power transfer from the limited source is assured. Note this pin is very noise sensitive, therefore minimize trace length and stray capacitance. Please refer to the Applications Information section for more detail on programming the MPPC for different sources. If this function is not needed, tie the pin to V<sub>CC</sub>.

**GND (Pin 6/Pin 4):** Signal Ground. Provide a short direct PCB path between GND and the ground plane where the exposed pad is soldered.

**FB (Pin 7/Pin 5):** Feedback Input to the Error Amplifier. Connect to a resistor divider from V<sub>OUT</sub> to ground. The output voltage can be adjusted from 1.4V to 15.75V by:

$V_{OUT} = 1.175V \cdot [1 + (R1/R2)]$ . Note this pin is very noise sensitive, therefore minimize trace length and stray capacitance.

**NC (Pins 8, 9/Pins 6, 7):** Unused. These pins should be grounded.

**PWM (Pin 10/Pin 8):** Mode Select Pin.

PWM = Low (ground): Enables automatic Burst Mode operation.

PWM = High (tie to V<sub>CC</sub>): Fixed frequency PWM operation.

This pin should not be allowed to float. It has an internal 5M pull-down resistor.

**PGOOD (Pin 11/Pin 9):** Open drain output that pulls to ground when FB drops too far below its regulated voltage. Connect a pull-up resistor from this pin to a positive supply. This pin can sink up to the absolute maximum rating of 15mA when low. Refer to the Operation section of the data sheet for more detail.

**V<sub>OUT</sub> (Pin 12/Pin 10):** Output voltage of the converter. Connect a minimum value of 4.7μF ceramic capacitor from this pin to the ground plane, as close to the pin as possible.

**BST2 (Pin 13/Pin 11):** Bootstrapped floating supply for high side NMOS gate drive. Connect to SW2 through a 22nF capacitor, as close to the part as possible. The value is not critical. Any value from 4.7nF to 47nF may be used.

**SW2 (Pin 14/Pin 12):** Switch Pin. Connect to one side of the inductor. Keep PCB trace lengths as short and wide as possible to reduce EMI.

**PGND (Pin 15, Exposed Pad Pin 17/Pin 13, Exposed Pad Pin 17):** Power Ground. Provide a short direct PCB path between PGND and the ground plane. **The exposed pad must also be soldered to the PCB ground plane.** It serves as a power ground connection, and as a means of conducting heat away from the die.

**SW1 (Pin 16/Pin 14):** Switch Pin. Connect to one side of the inductor. Keep PCB trace lengths as short and wide as possible to reduce EMI.



## OPERATION

### INTRODUCTION

The LTC3129 is a 1.3 $\mu$ A quiescent current, monolithic, current mode, buck-boost DC/DC converter that can operate over a wide input voltage range of 1.92V to 15V and provide up to 200mA to the load. Internal, low  $R_{DS(ON)}$  N-channel power switches reduce solution complexity and maximize efficiency. A proprietary switch control algorithm allows the buck-boost converter to maintain output voltage regulation with input voltages that are above, below or equal to the output voltage. Transitions between the step-up or step-down operating modes are seamless and free of transients and sub-harmonic switching, making this product ideal for noise sensitive applications. The LTC3129 operates at a fixed nominal switching frequency of 1.2MHz, which provides an ideal trade-off between small solution size and high efficiency. Current mode control provides inherent input line voltage rejection, simplified compensation and rapid response to load transients.

Burst Mode capability is also included in the LTC3129 and is user-selected via the PWM input pin. In Burst Mode operation, the LTC3129 provides exceptional efficiency at light output loading conditions by operating the converter only when necessary to maintain voltage regulation. The Burst Mode quiescent current is a miserly 1.3 $\mu$ A. At higher loads, the LTC3129 automatically switches to fixed frequency PWM mode when Burst Mode operation is selected. (Please refer to the Typical Performance Characteristics curves for the mode transition point at different input and output voltages.) If the application requires extremely low noise, continuous PWM operation can also be selected via the PWM pin.

A MPPC (maximum power point control) function is also provided that allows the input voltage to the converter to be servo'd to a programmable point for maximum power when operating from various non-ideal power sources such as photovoltaic cells. The LTC3129 also features an accurate RUN comparator threshold with hysteresis, allowing the buck-boost DC/DC converter to turn on and off at user-selected  $V_{IN}$  voltage thresholds. With a wide voltage range, 1.3 $\mu$ A Burst Mode current and programmable RUN and MPPC pins, the LTC3129 is well suited for many diverse applications.

### PWM MODE OPERATION

If the PWM pin is high or if the load current on the converter is high enough to command PWM mode operation with PWM low, the LTC3129 operates in a fixed 1.2MHz PWM mode using an internally compensated average current mode control loop. PWM mode minimizes output voltage ripple and yields a low noise switching frequency spectrum. A proprietary switching algorithm provides seamless transitions between operating modes and eliminates discontinuities in the average inductor current, inductor ripple current and loop transfer function throughout all modes of operation. These advantages result in increased efficiency, improved loop stability and lower output voltage ripple in comparison to the traditional buck-boost converter.

Figure 1 shows the topology of the LTC3129 power stage which is comprised of four N-channel DMOS switches and their associated gate drivers. In PWM mode operation both switch pins transition on every cycle independent of the input and output voltages. In response to the internal control loop command, an internal pulse width modulator generates the appropriate switch duty cycle to maintain regulation of the output voltage.

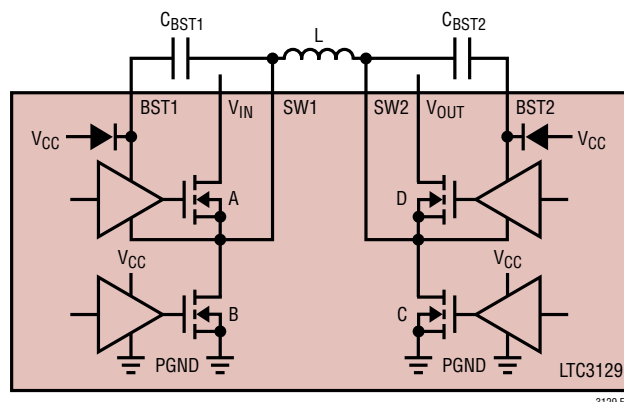


Figure 1. Power Stage Schematic

## OPERATION

When stepping down from a high input voltage to a lower output voltage, the converter operates in buck mode and switch D remains on for the entire switching cycle except for the minimum switch low duration (typically 90ns). During the switch low duration, switch C is turned on which forces SW2 low and charges the flying capacitor,  $C_{BST2}$ . This ensures that the switch D gate driver power supply rail on BST2 is maintained. The duty cycle of switches A and B are adjusted to maintain output voltage regulation in buck mode.

If the input voltage is lower than the output voltage, the converter operates in boost mode. Switch A remains on for the entire switching cycle except for the minimum switch low duration (typically 90ns). During the switch low duration, switch B is turned on which forces SW1 low and charges the flying capacitor,  $C_{BST1}$ . This ensures that the switch A gate driver power supply rail on BST1 is maintained. The duty cycle of switches C and D are adjusted to maintain output voltage regulation in boost mode.

### Oscillator

The LTC3129 operates from an internal oscillator with a nominal fixed frequency of 1.2MHz. This allows the DC/DC converter efficiency to be maximized while still using small external components.

### Current Mode Control

The LTC3129 utilizes average current mode control for the pulse width modulator. Current mode control, both average and the better known peak method, enjoy some benefits compared to other control methods including: simplified loop compensation, rapid response to load transients and inherent line voltage rejection.

Referring to the Block Diagram, a high gain, internally compensated transconductance amplifier monitors  $V_{out}$  through a voltage divider connected to the FB pin. The error amplifier output is used by the current mode control loop to command the appropriate inductor current level. The inverting input of the internally compensated average current amplifier is connected to the inductor current sense circuit. The average current amplifier's output is compared to the oscillator ramps, and the comparator

outputs are used to control the duty cycle of the switch pins on a cycle-by-cycle basis.

The voltage error amplifier monitors the output voltage,  $V_{OUT}$  through a voltage divider and makes adjustments to the current command as necessary to maintain regulation. The voltage error amplifier therefore controls the outer voltage regulation loop. The average current amplifier makes adjustments to the inductor current as directed by the voltage error amplifier output via  $V_C$  and is commonly referred to as the inner current loop amplifier.

The average current mode control technique is similar to peak current mode control except that the average current amplifier, by virtue of its configuration as an integrator, controls average current instead of the peak current. This difference eliminates the peak to average current error inherent to peak current mode control, while maintaining most of the advantages inherent to peak current mode control.

Average current mode control requires appropriate compensation for the inner current loop, unlike peak current mode control. The compensation network must have high DC gain to minimize errors between the actual and commanded average current level, high bandwidth to quickly change the commanded current level following transient load steps and a controlled mid-band gain to provide a form of slope compensation unique to average current mode control. The compensation components required to ensure proper operation have been carefully selected and are integrated within the LTC3129.

### Inductor Current Sense and Maximum Output Current

As part of the current control loop required for current mode control, the LTC3129 includes a pair of current sensing circuits that measure the buck-boost converter inductor current.

The voltage error amplifier output,  $V_C$ , is internally clamped to a nominal level of 0.6V. Since the average inductor current is proportional to  $V_C$ , the 0.6V clamp level sets the maximum average inductor current that can be programmed by the inner current loop. Taking into account the current sense amplifier's gain, the maximum average

## OPERATION

inductor current is approximately 275mA (typical). In Buck mode, the output current is approximately equal to the inductor current  $I_L$ .

$$I_{OUT(BUCK)} \approx I_L \cdot 0.89$$

The 90ns SW1/SW2 forced low time on each switching cycle briefly disconnects the inductor from  $V_{OUT}$  and  $V_{IN}$  resulting in about 11% less output current in either buck or boost mode for a given inductor current. In boost mode, the output current is related to average inductor current and duty cycle by:

$$I_{OUT(BOOST)} \approx I_L \cdot (1 - D) \cdot \text{Efficiency},$$

where D is the converter duty cycle.

Since the output current in boost mode is reduced by the duty cycle (D), the output current rating in buck mode is always greater than in boost mode. Also, because boost mode operation requires a higher inductor current for a given output current compared to buck mode, the efficiency in boost mode will be lower due to higher  $I_L^2 \cdot R_{DS(ON)}$  losses in the power switches. This will further reduce the output current capability in boost mode. In either operating mode, however, the inductor peak-to-peak ripple current does not play a major role in determining the output current capability, unlike peak current mode control.

With peak current mode control, the maximum output current capability is reduced by the magnitude of inductor ripple current because the peak inductor current level is the control variable, but the average inductor current is what determines the output current. The LTC3129 measures and controls average inductor current, and therefore, the inductor ripple current magnitude has little effect on the maximum current capability in contrast to an equivalent peak current mode converter. Under most conditions in buck mode, the LTC3129 is capable of providing a minimum of 200mA to the load. In boost mode, as described previously, the output current capability is related to the boost ratio or duty cycle (D). For example, for a 3.6V  $V_{IN}$  to 5V output application, the LTC3129 can provide up to 150mA to the load. Refer to the Typical Performance characteristics section for more detail on output current capability.

### Overload Current Limit and $I_{ZERO}$ Comparator

The internal current sense waveform is also used by the peak overload current ( $I_{PEAK}$ ) and zero current ( $I_{ZERO}$ ) comparators. The  $I_{PEAK}$  current comparator monitors  $I_{sense}$  and turns off switch A if the inductor current level exceeds its maximum internal threshold, which is approximately 500mA. An inductor current level of this magnitude will occur during a fault, such as an output short-circuit, or during large load or input voltage transients.

The LTC3129 features near discontinuous inductor current operation at light output loads by virtue of the  $I_{ZERO}$  comparator circuit. By limiting the reverse current magnitude in PWM mode, a balance between low noise operation and improved efficiency at light loads is achieved. The  $I_{ZERO}$  comparator threshold is set near the zero current level in PWM mode, and as a result, the reverse current magnitude will be a function of inductance value and output voltage due to the comparator's propagation delay. In general, higher output voltages and lower inductor values will result in increased reverse current magnitude.

In automatic Burst Mode operation (PWM pin low), the  $I_{ZERO}$  comparator threshold is increased so that reverse inductor current does not normally occur. This maximizes efficiency at very light loads.

### Burst Mode OPERATION

When the PWM pin is held low, the LTC3129 is configured for automatic Burst Mode operation. As a result, the buck-boost DC/DC converter will operate with normal continuous PWM switching above a predetermined minimum output load and will automatically transition to power saving Burst Mode operation below this output load level. Note that if the PWM pin is low, reverse inductor current is not allowed at any load. Refer to the Typical Performance Characteristics section to determine the Burst Mode transition threshold for various combinations of  $V_{IN}$  and  $V_{OUT}$ . If PWM is low, at light output loads, the LTC3129 will go into a standby or sleep state when the output voltage achieves its nominal regulation level. The sleep state halts PWM switching and powers down all non-essential

## OPERATION

functions of the IC, significantly reducing the quiescent current of the LTC3129 to just 1.3 $\mu$ A typical. This greatly improves overall power conversion efficiency when the output load is light. Since the converter is not operating in sleep, the output voltage will slowly decay at a rate determined by the output load resistance and the output capacitor value. When the output voltage has decayed by a small amount, typically 1%, the LTC3129 will wake and resume normal PWM switching operation until the voltage on  $V_{OUT}$  is restored to the previous level. If the load is very light, the LTC3129 may only need to switch for a few cycles to restore  $V_{OUT}$  and may sleep for extended periods of time, significantly improving efficiency. If the load is suddenly increased above the burst transition threshold, the part will automatically resume continuous PWM operation until the load is once again reduced.

A feedforward capacitor on the feedback divider can be used to reduce Burst Mode  $V_{OUT}$  ripple. This is discussed in more detail in the Applications Information section of this data sheet.

Note that Burst Mode operation is inhibited until soft-start is done, the MPPC pin is greater than 1.175V and  $V_{OUT}$  has reached regulation.

### Soft-Start

The LTC3129 soft-start circuit minimizes input current transients and output voltage overshoot on initial power up. The required timing components for soft-start are internal to the LTC3129 and produce a nominal soft-start duration of approximately 3ms. The internal soft-start circuit slowly ramps the error amplifier output,  $V_C$ . In doing so, the current command of the IC is also slowly increased, starting from zero. It is unaffected by output loading or output capacitor value. Soft-start is reset by the UVLO on both  $V_{IN}$  and  $V_{CC}$ , the RUN pin and thermal shutdown.

### $V_{CC}$ Regulator

An internal low dropout regulator (LDO) generates a nominal 4.1V  $V_{CC}$  rail from  $V_{IN}$ . The  $V_{CC}$  rail powers the internal control circuitry and the gate drivers of the LTC3129. The  $V_{CC}$  regulator is disabled in shutdown to reduce quiescent current and is enabled by raising the RUN pin above its

logic threshold. The  $V_{CC}$  regulator includes current-limit protection to safeguard against accidental short-circuiting of the  $V_{CC}$  rail.

### Undervoltage Lockout (UVLO)

There are two undervoltage lockout (UVLO) circuits within the LTC3129 that inhibit switching; one that monitors  $V_{IN}$  and another that monitors  $V_{CC}$ . Either UVLO will disable operation of the internal power switches and keep other IC functions in a reset state if either  $V_{IN}$  or  $V_{CC}$  are below their respective UVLO thresholds.

The  $V_{IN}$  UVLO comparator has a falling voltage threshold of 1.8V (typical). If  $V_{IN}$  falls below this level, IC operation is disabled until  $V_{IN}$  rises above 1.9V (typical), as long as the  $V_{CC}$  voltage is above its UVLO threshold.

The  $V_{CC}$  UVLO has a falling voltage threshold of 2.19V (typical). If the  $V_{CC}$  voltage falls below this threshold, IC operation is disabled until  $V_{CC}$  rises above 2.25V (typical) as long as  $V_{IN}$  is above its nominal UVLO threshold level.

Depending on the particular application, either of these UVLO thresholds could be the limiting factor affecting the minimum input voltage required for operation. Because the  $V_{CC}$  regulator uses  $V_{IN}$  for its power input, the minimum input voltage required for operation is determined by the  $V_{CC}$  minimum voltage, as input voltage ( $V_{IN}$ ) will always be higher than  $V_{CC}$  in the normal (non-bootstrapped) configuration. Therefore, the minimum  $V_{IN}$  for the part to startup is 2.25V (typical).

In applications where  $V_{CC}$  is bootstrapped (powered through a Schottky diode by either  $V_{OUT}$  or an auxiliary power rail), the minimum input voltage for operation will be limited only by the  $V_{IN}$  UVLO threshold (1.8V typical). *Please note that if the bootstrap voltage is derived from the LTC3129  $V_{OUT}$  and not an independent power rail, then the minimum input voltage required for initial startup is still 2.25V (typical).*

Note that if either  $V_{IN}$  or  $V_{CC}$  are below their UVLO thresholds, or if RUN is below its accurate threshold of 1.22V (typical), then the LTC3129 will remain in a soft shutdown state, where the  $V_{IN}$  quiescent current will be only 1.9 $\mu$ A typical.

## OPERATION

### V<sub>OUT</sub> Undervoltage

There is also an undervoltage comparator that monitors the output voltage. Until V<sub>OUT</sub> reaches 1.15V (typical), the average current limit is reduced by a factor of two. This reduces power dissipation in the device in the event of a shorted output. In addition, N-channel switch D, which feeds V<sub>OUT</sub>, will be disabled until V<sub>OUT</sub> exceeds 1.15V.

### RUN Pin Comparator

In addition to serving as a logic level input to enable certain functions of the IC, the RUN pin includes an accurate internal comparator that allows it to be used to set custom rising and falling ON/OFF thresholds with the addition of an optional external resistor divider. When RUN is driven above its logic threshold (0.9V typical), the V<sub>CC</sub> regulator is enabled, which provides power to the internal control circuitry of the IC. If the voltage on RUN is increased further so that it exceeds the RUN comparator's accurate analog threshold (1.22V typical), all functions of the buck-boost converter will be enabled and a start-up sequence will ensue, assuming the V<sub>IN</sub> and V<sub>CC</sub> UVLO thresholds are satisfied.

If RUN is brought below the accurate comparator threshold, the buck-boost converter will inhibit switching, but the V<sub>CC</sub> regulator and control circuitry will remain powered unless RUN is brought below its logic threshold. Therefore, in order to completely shut down the IC and reduce the V<sub>IN</sub> current to 10nA (typical), it is necessary to ensure that RUN is brought below its worst case low logic threshold of 0.5V. RUN is a high voltage input and can be tied directly to V<sub>IN</sub> to continuously enable the IC when the input supply is present. Also note that RUN can be driven above V<sub>IN</sub> or V<sub>OUT</sub> as long as it stays within the operating range of the IC (up to 15V).

With the addition of an optional resistor divider as shown in Figure 2, the RUN pin can be used to establish a user-programmable turn-on and turn-off threshold. This feature can be utilized to minimize battery drain below a certain input voltage, or to operate the converter in a hiccup mode from very low current sources.

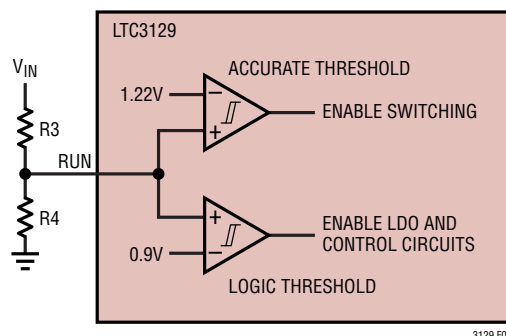


Figure 2. Accurate RUN Pin Comparator

Note that once RUN is above 0.9V typical, the quiescent input current on V<sub>IN</sub> (or V<sub>CC</sub> if back-driven) will increase to about 1.9μA typical until the V<sub>IN</sub> and V<sub>CC</sub> UVLO thresholds are satisfied.

The converter is enabled when the voltage on RUN exceeds 1.22V (nominal). Therefore, the turn-on voltage threshold on V<sub>IN</sub> is given by:

$$V_{IN(TURN-ON)} = 1.22V \cdot (1 + R3/R4)$$

The RUN comparator includes a built-in hysteresis of approximately 80mV, so that the turn off threshold will be 1.14V.

There may be cases due to PCB layout, very large value resistors for R3 and R4, or proximity to noisy components where noise pickup may cause the turn-on or turn-off of the IC to be intermittent. In these cases, a small filter capacitor can be added across R4 to ensure proper operation.

## OPERATION

### PGOOD Comparator

The LTC3129 provides an open-drain PGOOD output that pulls low if  $V_{OUT}$  falls more than 7.5% (typical) below its programmed value. When  $V_{OUT}$  rises to within 5% (typical) of its programmed value, the internal PGOOD pull-down will turn off and PGOOD will go high if an external pull-up resistor has been provided. An internal filter prevents nuisance trips of PGOOD due to short transients on  $V_{OUT}$ . Note that PGOOD can be pulled up to any voltage, as long as the absolute maximum rating of 18V is not exceeded, and as long as the maximum sink current rating is not exceeded when PGOOD is low. Note that PGOOD will also be driven low if  $V_{CC}$  is below its UVLO threshold or if the part is in shutdown (RUN below its logic threshold) while  $V_{CC}$  is being held up (or back-driven). PGOOD is not affected by  $V_{IN}$  UVLO or the accurate RUN threshold.

In cases where  $V_{CC}$  is not being back-driven in shutdown, PGOOD will not be held low indefinitely. The internal PGOOD pull-down will be disabled as the  $V_{CC}$  voltage decays below approximately 1V.

### Maximum Power-Point Control (MPPC)

The MPPC input of the LTC3129 can be used with an optional external voltage divider to dynamically adjust

the commanded inductor current in order to maintain a minimum input voltage when using high resistance sources, such as photovoltaic panels, so as to maximize input power transfer and prevent  $V_{IN}$  from dropping too low under load. Referring to Figure 3, the MPPC pin is internally connected to the non-inverting input of a  $g_m$  amplifier, whose inverting input is connected to the 1.175V reference. If the voltage at MPPC, using the external voltage divider, falls below the reference voltage, the output of the amplifier pulls the internal  $V_C$  node low. This reduces the commanded average inductor current so as to reduce the input current and regulate  $V_{IN}$  to the programmed minimum voltage, as given by:

$$V_{IN(MPPC)} = 1.175V \cdot (1 + R5/R6)$$

The MPPC feature provides capabilities to the LTC3129 that can ease the design of intrinsically safe power supplies.

Note that external compensation should not be required for MPPC loop stability if input filter capacitor,  $C_{IN}$ , is at least 22 $\mu$ F.

The divider resistor values can be in the M $\Omega$  range to minimize the input current in very low power applications. However, stray capacitance and noise pickup on the MPPC pin must also be minimized.

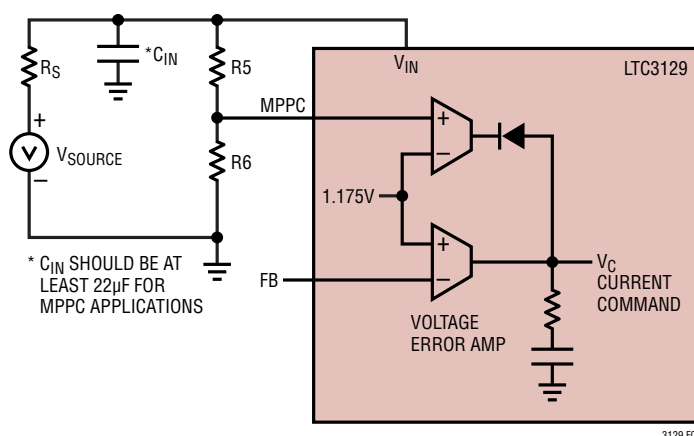


Figure 3. MPPC Amplifier with External Resistor Divider

## OPERATION

The MPPC pin controls the converter in a linear fashion when using sources that can provide a minimum of 5mA to 10mA of continuous input current. For operation from weaker input sources, refer to the Applications Information section to see how the programmable RUN pin can be used to control the converter in a hysteretic manner to provide an effective MPPC function for sources that can provide as little as 5 $\mu$ A or less. If the MPPC function is not required, the MPPC pin should be tied to  $V_{CC}$ .

### Thermal Considerations

The power switches of the LTC3129 are designed to operate continuously with currents up to the internal current limit thresholds. However, when operating at high current levels, there may be significant heat generated within the IC. In addition, the  $V_{CC}$  regulator can also generate wasted heat when  $V_{IN}$  is very high, adding to the total power dissipation of the IC. As described elsewhere in this data sheet, bootstrapping of the  $V_{CC}$  for 5V output applications can essentially eliminate the  $V_{CC}$  power dissipation term

and significantly improve efficiency. As a result, careful consideration must be given to the thermal environment of the IC in order to provide a means to remove heat from the IC and ensure that the LTC3129 is able to provide its full rated output current. Specifically, the exposed die attach pad of both the QFN and MSE packages must be soldered to a copper layer on the PCB to maximize the conduction of heat out of the IC package. This can be accomplished by utilizing multiple vias from the die attach pad connection underneath the IC package to other PCB layer(s) containing a large copper plane. A typical board layout incorporating these concepts is shown in Figure 4.

If the IC die temperature exceeds approximately 180°C, over temperature shutdown will be invoked and all switching will be inhibited. The part will remain disabled until the die temperature cools by approximately 10°C. The soft-start circuit is re-initialized in overtemperature shutdown to provide a smooth recovery when the IC die temperature cools enough to resume operation.

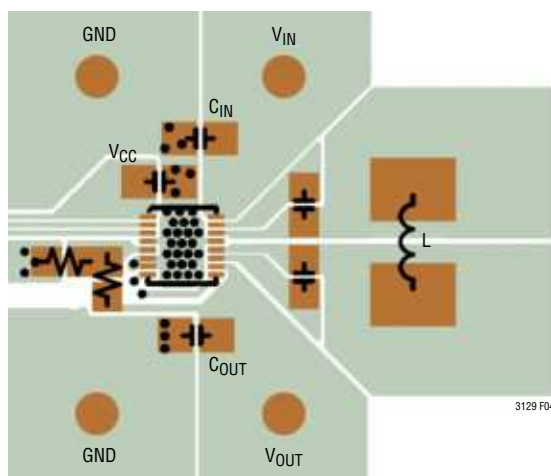


Figure 4. Typical 2-Layer PC Board Layout (MSE Package)

## APPLICATIONS INFORMATION

A standard application circuit for the LTC3129 is shown on the front page of this data sheet. The appropriate selection of external components is dependent upon the required performance of the IC in each particular application given considerations and trade-offs such as PCB area, input and output voltage range, output voltage ripple, transient response, required efficiency, thermal considerations and cost. This section of the data sheet provides some basic guidelines and considerations to aid in the selection of external components and the design of the applications circuit, as well as more application circuit examples.

### Programming $V_{OUT}$

The output voltage of the LTC3129 is set by connecting the FB pin to an external resistor divider from  $V_{OUT}$  to ground, as shown in Figure 5, according to the equation:

$$V_{OUT} = 1.175V \cdot (1 + R1/R2)$$

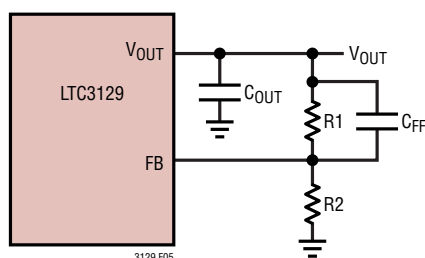


Figure 5.  $V_{OUT}$  Feedback Divider

A small feedforward capacitor can be added in parallel with R1 (in Figure 5) to reduce Burst Mode ripple and improve transient response. Details on selecting a feedforward capacitor are provided later in this data sheet.

### $V_{CC}$ Capacitor Selection

The  $V_{CC}$  output of the LTC3129 is generated from  $V_{IN}$  by a low dropout linear regulator. The  $V_{CC}$  regulator has been designed for stable operation with a wide range of output capacitors. For most applications, a low ESR capacitor of at least 2.2 $\mu$ F should be used. The capacitor should be located as close to the  $V_{CC}$  pin as possible and connected to the  $V_{CC}$  pin and ground through the shortest traces pos-

sible.  $V_{CC}$  is the regulator output and is also the internal supply pin for the LTC3129 control circuitry as well as the gate drivers and boost rail charging diodes. The  $V_{CC}$  pin is not intended to supply current to other external circuitry.

### Inductor Selection

The choice of inductor used in LTC3129 application circuits influences the maximum deliverable output current, the converter bandwidth, the magnitude of the inductor current ripple and the overall converter efficiency. The inductor must have a low DC series resistance, when compared to the internal switch resistance, or output current capability and efficiency will be compromised. Larger inductor values reduce inductor current ripple but may not increase output current capability as is the case with peak current mode control as described in the Maximum Output Current section. Larger value inductors also tend to have a higher DC series resistance for a given case size, which will have a negative impact on efficiency. Larger values of inductance will also lower the right half plane (RHP) zero frequency when operating in boost mode, which can compromise loop stability. Nearly all LTC3129 application circuits deliver the best performance with an inductor value between 3.3 $\mu$ H and 10 $\mu$ H. Buck mode-only applications can use the larger inductor values as they are unaffected by the RHP zero, while mostly boost applications generally require inductance on the low end of this range depending on how large the step-up ratio is.

Regardless of inductor value, the saturation current rating should be selected such that it is greater than the worst-case average inductor current plus half of the ripple current. The peak-to-peak inductor current ripple for each operational mode can be calculated from the following formula, where  $f$  is the switching frequency (1.2MHz),  $L$  is the inductance in  $\mu$ H and  $t_{LOW}$  is the switch pin minimum low time in  $\mu$ s. The switch pin minimum low time is typically 0.09 $\mu$ s.

$$\Delta I_{L(P-P)(BUCK)} = \frac{V_{OUT}}{L} \left( \frac{V_{IN} - V_{OUT}}{V_{IN}} \right) \left( \frac{1}{f} - t_{LOW} \right) A$$

$$\Delta I_{L(P-P)(BOOST)} = \frac{V_{IN}}{L} \left( \frac{V_{OUT} - V_{IN}}{V_{OUT}} \right) \left( \frac{1}{f} - t_{LOW} \right) A$$

## APPLICATIONS INFORMATION

It should be noted that the worst-case peak-to-peak inductor ripple current occurs when the duty cycle in buck mode is minimum (highest  $V_{IN}$ ) and in boost mode when the duty cycle is 50% ( $V_{OUT} = 2 \cdot V_{IN}$ ). As an example, if  $V_{IN}$  (minimum) = 2.5V and  $V_{IN}$  (maximum) = 15V,  $V_{OUT} = 5V$  and  $L = 10\mu H$ , the peak-to-peak inductor ripples at the voltage extremes (15V  $V_{IN}$  for buck and 2.5V  $V_{IN}$  for boost) are:

Buck = 248mA peak-to-peak

Boost = 93mA peak-to-peak

One half of this inductor ripple current must be added to the highest expected average inductor current in order to select the proper saturation current rating for the inductor.

To avoid the possibility of inductor saturation during load transients, an inductor with a saturation current rating of at least 600mA is recommended for all applications.

In addition to its influence on power conversion efficiency, the inductor DC resistance can also impact the maximum output current capability of the buck-boost converter particularly at low input voltages. In buck mode, the output current of the buck-boost converter is primarily limited by the inductor current reaching the average current limit threshold. However, in boost mode, especially at large step-up ratios, the output current capability can also be limited by the total resistive losses in the power stage. These losses include, switch resistances, inductor DC resistance and PCB trace resistance. Avoid inductors with a high DC resistance (DCR) as they can degrade the maximum output current capability from what is shown in the Typical Performance Characteristics section and from the Typical Application circuits.

As a guideline, the inductor DCR should be significantly less than the typical power switch resistance of 750m $\Omega$  each. The only exceptions are applications that have a maximum output current requirement much less than what the LTC3129 is capable of delivering. Generally speaking, inductors with a DCR in the range of 0.15 $\Omega$  to 0.3 $\Omega$  are recommended. Lower values of DCR will improve the efficiency at the expense of size, while higher DCR values will reduce efficiency (typically by a few percent) while allowing the use of a physically smaller inductor.

Different inductor core materials and styles have an impact on the size and price of an inductor at any given current rating. Shielded construction is generally preferred as it minimizes the chances of interference with other circuitry. The choice of inductor style depends upon the price, sizing, and EMI requirements of a particular application. Table 1 provides a wide sampling of inductors that are well suited to many LTC3129 applications.

**Table 1. Recommended Inductors**

| VENDOR                                  | PART                                                                        |
|-----------------------------------------|-----------------------------------------------------------------------------|
| Coilcraft<br>www.coilcraft.com          | EPL2014, EPL3012, EPL3015, LPS3015, LPS3314, XFL3012                        |
| Coiltronics<br>www.cooperindustries.com | SDH3812, SD3814, SD3114, SD3118                                             |
| Murata<br>www.murata.com                | LQH3NP, LQH32P, LQH44P                                                      |
| Sumida<br>www.sumida.com                | CDRH2D16, CDRH2D18, CDRH3D14, CDRH3D16                                      |
| Taiyo-Yuden<br>www.t-yuden.com          | NR3012T, NR3015T, NRS4012T, BRC2518                                         |
| TDK<br>www.tdk.com                      | VLS3012, VLS3015, VLF302510MT, VLF302512MT                                  |
| Toko<br>www.tokoam.com                  | DB3015C, DB3018C, DB3020C, DP418C, DP420C, DEM2815C, DFE322512C, DFE252012C |
| Würth<br>www.we-online.com              | WE-TPC 2813, WE-TPC 3816, WE-TPC 2828                                       |

Recommended inductor values for different operating voltage ranges are given in Table 2. These values were chosen to minimize inductor size while maintaining an acceptable amount of inductor ripple current for a given  $V_{IN}$  and  $V_{OUT}$  range.

**Table 2. Recommended Inductor Values**

| $V_{IN}$ AND $V_{OUT}$ RANGE        | RECOMMENDED INDUCTOR VALUES |
|-------------------------------------|-----------------------------|
| $V_{IN}$ and $V_{OUT}$ Both < 4.5V  | 3.3 $\mu H$ to 4.7 $\mu H$  |
| $V_{IN}$ and $V_{OUT}$ Both < 8V    | 4.7 $\mu H$ to 6.8 $\mu H$  |
| $V_{IN}$ and $V_{OUT}$ Both < 11V   | 6.8 $\mu H$ to 8.2 $\mu H$  |
| $V_{IN}$ and $V_{OUT}$ Up to 15.75V | 8.2 $\mu H$ to 10 $\mu H$   |

### Feedforward Capacitor

The use of a voltage feedforward capacitor, as shown in Figure 5, offers a number of performance advantages. A feedforward capacitor will reduce output voltage ripple in

## APPLICATIONS INFORMATION

Burst Mode operation and improve transient response. In addition, due to the wide  $V_{IN}$  and  $V_{OUT}$  operating range of the LTC3129 and its fixed internal loop compensation, some applications may require the use of a feedforward capacitor to assure light-load stability (less than ~15mA) when operating in PWM mode (PWM pin pulled high).

Therefore, to reduce Burst Mode ripple and improve phase margin at light load when PWM mode operation is selected, a feedforward capacitor is recommended for all applications. The recommended feedforward capacitor value can be calculated by:

$$C_{FF} = 66/R1$$

Where R1 is the top feedback divider resistor value in MΩ and  $C_{FF}$  is the recommended feedforward capacitor value in picofarads (use the nearest standard value). Refer to the application circuits for examples.

### Output Capacitor Selection

A low effective series resistance (ESR) output capacitor of 4.7μF minimum should be connected at the output of the buck-boost converter in order to minimize output voltage ripple. Multilayer ceramic capacitors are an excellent option as they have low ESR and are available in small footprints. The capacitor value should be chosen large enough to reduce the output voltage ripple to acceptable levels. Neglecting the capacitor's ESR and ESL (effective series inductance), the peak-to-peak output voltage ripple in PWM mode can be calculated by the following formula, where  $f$  is the frequency in MHz (1.2MHz),  $C_{OUT}$  is the capacitance in μF,  $t_{LOW}$  is the switch pin minimum low time in μs (0.09μs typical) and  $I_{LOAD}$  is the output current in amperes.

$$\Delta V_{P-P(BUCK)} = \frac{I_{LOAD} t_{LOW}}{C_{OUT}} V$$

$$\Delta V_{P-P(BOOST)} = \frac{I_{LOAD}}{f C_{OUT}} \left( \frac{V_{OUT} - V_{IN} + t_{LOW} f V_{IN}}{V_{OUT}} \right) V$$

Examining the previous equations reveals that the output voltage ripple increases with load current and is generally higher in boost mode than in buck mode. Note that these equations only take into account the voltage ripple that occurs from the inductor current to the output being discontinuous. They provide a good approximation to the ripple at any significant load current but underestimate the output voltage ripple at very light loads where the output voltage ripple is dominated by the inductor current ripple.

In addition to the output voltage ripple generated across the output capacitance, there is also output voltage ripple produced across the internal resistance of the output capacitor. The ESR-generated output voltage ripple is proportional to the series resistance of the output capacitor and is given by the following expressions where  $R_{ESR}$  is the series resistance of the output capacitor and all other terms as previously defined.

$$\Delta V_{P-P(BUCK)} = \frac{I_{LOAD} R_{ESR}}{1 - t_{LOW} f} \approx I_{LOAD} R_{ESR} V$$

$$\Delta V_{P-P(BOOST)} = \frac{I_{LOAD} R_{ESR} V_{OUT}}{V_{IN} (1 - t_{LOW} f)}$$

$$\approx I_{LOAD} R_{ESR} \left( \frac{V_{OUT}}{V_{IN}} \right) V$$

In most LTC3129 applications, an output capacitor between 10μF and 22μF will work well. To minimize output ripple in Burst Mode operation, or transients incurred by large step loads, values of 22μF or larger are recommended.

### Input Capacitor Selection

The  $V_{IN}$  pin carries the full inductor current and provides power to internal control circuits in the IC. To minimize input voltage ripple and ensure proper operation of the IC, a low ESR bypass capacitor with a value of at least 4.7μF should be located as close to the  $V_{IN}$  pin as possible. The traces connecting this capacitor to  $V_{IN}$  and the ground plane should be made as short as possible.

## APPLICATIONS INFORMATION

When powered through long leads or from a power source with significant resistance, a larger value bulk input capacitor may be required and is generally recommended. In such applications, a 47 $\mu$ F to 100 $\mu$ F low-ESR electrolytic capacitor in parallel with a 1 $\mu$ F ceramic capacitor generally yields a high performance, low cost solution.

Note that applications using the MPPC feature should use a minimum  $C_{IN}$  of 22 $\mu$ F. Larger values can be used without limitation.

### Recommended Input and Output Capacitor Types

The capacitors used to filter the input and output of the LTC3129 must have low ESR and must be rated to handle the AC currents generated by the switching converter. This is important to maintain proper functioning of the IC and to reduce output voltage ripple. There are many capacitor types that are well suited to these applications including multilayer ceramic, low ESR tantalum, OS-CON and POSCAP technologies. In addition, there are certain types of electrolytic capacitors such as solid aluminum organic polymer capacitors that are designed for low ESR and high AC currents and these are also well suited to some LTC3129 applications. The choice of capacitor technology is primarily dictated by a trade-off between size, leakage current and cost. In backup power applications, the input or output capacitor might be a super or ultra capacitor with a capacitance value measuring in the Farad range. The selection criteria in these applications are generally similar except that voltage ripple is generally not a concern. Some capacitors exhibit a high DC leakage current which may preclude their consideration for applications that require a very low quiescent current in Burst Mode operation. Note that ultra capacitors may have a rather high ESR, therefore a 4.7 $\mu$ F (minimum) ceramic capacitor is recommended in parallel, close to the IC pins.

Ceramic capacitors are often utilized in switching converter applications due to their small size, low ESR and low leakage currents. However, many ceramic capacitors intended for power applications experience a significant loss in capacitance from their rated value as the DC bias voltage on the capacitor increases. It is not uncommon for a small surface mount capacitor to lose more than 50%

of its rated capacitance when operated at even half of its maximum rated voltage. This effect is generally reduced as the case size is increased for the same nominal value capacitor. As a result, it is often necessary to use a larger value capacitance or a higher voltage rated capacitor than would ordinarily be required to actually realize the intended capacitance at the operating voltage of the application. X5R and X7R dielectric types are recommended as they exhibit the best performance over the wide operating range and temperature of the LTC3129. To verify that the intended capacitance is achieved in the application circuit, be sure to consult the capacitor vendor's curve of capacitance versus DC bias voltage.

### Using the Programmable RUN Function to Operate from Extremely Weak Input Sources

Another application of the programmable RUN pin is that it can be used to operate the converter in a hiccup mode from extremely low current sources. This allows operation from sources that can only generate microamps of output current, and would be far too weak to sustain normal steady-state operation, even with the use of the MPPC pin. Because the LTC3129 draws only 1.9 $\mu$ A typical from  $V_{IN}$  until it is enabled, the RUN pin can be programmed to keep the IC disabled until  $V_{IN}$  reaches the programmed voltage level. In this manner, the input source can trickle-charge an input storage capacitor, even if it can only supply microamps of current, until  $V_{IN}$  reaches the turn-on threshold set by the RUN pin divider. The converter will then be enabled using the stored charge in the input capacitor, until  $V_{IN}$  drops below the turn-off threshold, at which point the converter will turn off and the process will repeat.

This approach allows the converter to run from weak sources such as thin-film solar cells using indoor lighting. Although the converter will be operating in bursts, it is enough to charge an output capacitor to power low duty cycle loads, such as wireless sensor applications, or to trickle charge a battery. In addition, note that the input voltage will be cycling (with a small ripple as set by the RUN hysteresis) about a fixed voltage, as determined by the divider. This allows the high impedance source to operate at the programmed optimal voltage for maximum power transfer.

## APPLICATIONS INFORMATION

When using high value divider resistors (in the  $M\Omega$  range) to minimize current draw on  $V_{IN}$ , a small noise filter capacitor may be necessary across the lower divider resistor to prevent noise from erroneously tripping the RUN comparator. The capacitor value should be minimized so as not to introduce a time delay long enough for the input voltage to drop significantly below the desired  $V_{IN}$  threshold before the converter is turned off. Note that larger  $V_{IN}$  decoupling capacitor values will minimize this effect by providing more holdup time on  $V_{IN}$ .

### Programming the MPPC Voltage

As discussed in the previous section, the LTC3129 includes an MPPC function to optimize performance when operating from voltage sources with relatively high source resistance. Using an external voltage divider from  $V_{IN}$ , the MPPC function takes control of the average inductor current when necessary to maintain a minimum input voltage, as programmed by the user. Referring to Figure 3:

$$V_{IN(MPPC)} = 1.175V \cdot (1 + R5/R6)$$

This is useful for such applications as photovoltaic powered converters, since the maximum power transfer point occurs when the photovoltaic panel is operated at about 75% of its open-circuit voltage. For example, when operating from a photovoltaic panel with an open-circuit voltage of 5V, the maximum power transfer point will be when the panel is loaded such that its output voltage is about 3.75V. Choosing values of  $2M\Omega$  for  $R5$  and  $909k\Omega$  for  $R6$  will program the MPPC function to regulate the maximum input current so as to maintain  $V_{IN}$  at a minimum of 3.74V (typical). Note that if the panel can provide more power than the LTC3129 can draw, the input voltage will rise above the programmed MPPC point. This is fine as long as the input voltage doesn't exceed 15V.

For weak input sources with very high resistance (hundreds of Ohms or more), the LTC3129 may still draw more current than the source can provide, causing  $V_{IN}$  to drop below the UVLO threshold. For these applications, it is recommended that the programmable RUN feature be used, as described in the previous section.

### MPPC Compensation and Gain

When using MPPC, there are a number of variables that affect the gain and phase of the input voltage control loop. Primarily these are the input capacitance, the MPPC divider ratio and the  $V_{IN}$  source resistance (or current). To simplify the design of the application circuit, the MPPC control loop in the LTC3129 is designed with a relatively low gain, such that external MPPC loop compensation is generally not required when using a  $V_{IN}$  capacitor value of at least  $22\mu F$ . The gain from the MPPC pin to the internal VC control voltage is about 12, so a drop of 50mV on the MPPC pin (below the 1.175V MPPC threshold), corresponds to a 600mV drop on the internal VC voltage, which reduces the average inductor current all the way to zero. Therefore, the programmed input MPPC voltage will be maintained within about 4% over the load range.

Note that if large value  $V_{IN}$  capacitors are used (which may have a relatively high ESR) a small ceramic capacitor of at least  $4.7\mu F$  should be placed in parallel across the  $V_{IN}$  input, near the  $V_{IN}$  pin of the IC.

### Bootstrapping the $V_{CC}$ Regulator

The high and low side gate drivers are powered through the  $V_{CC}$  rail, which is generated from the input voltage,  $V_{IN}$ , through an internal linear regulator. In some applications, especially at high input voltages, the power dissipation in the linear regulator can become a major contributor to thermal heating of the IC and overall efficiency. The Typical Performance Characteristics section provides data on the  $V_{CC}$  current and resulting power loss versus  $V_{IN}$  and  $V_{OUT}$ .

A significant performance advantage can be attained in high  $V_{IN}$  applications where converter output voltage ( $V_{OUT}$ ) is programmed to 5V, if  $V_{OUT}$  is used to power the  $V_{CC}$  rail. Powering  $V_{CC}$  in this manner is referred to as bootstrapping. This can be done by connecting a Schottky diode (such as a BAT54) from  $V_{OUT}$  to  $V_{CC}$  as shown in Figure 6. With the bootstrap diode installed, the gate driver currents are supplied by the buck-boost converter at high efficiency rather than through the internal linear regulator. The internal linear regulator contains reverse blocking circuitry

APPLICATIONS INFORMATION

that allows  $V_{CC}$  to be driven above its nominal regulation level with only a very slight amount of reverse current. Please note that the bootstrapping supply (either  $V_{OUT}$  or a separate regulator) must be limited to less than 5.7V so as not to exceed the maximum  $V_{CC}$  voltage of 5.5V after the diode drop.

By maintaining  $V_{CC}$  above its UVLO threshold, bootstrapping, even to a 3.3V output, also allows operation down to the  $V_{IN}$  UVLO threshold of 1.8V (typical).

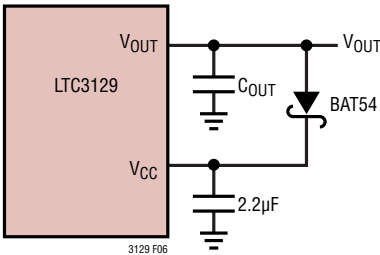


Figure 6. Example of  $V_{CC}$  Bootstrap

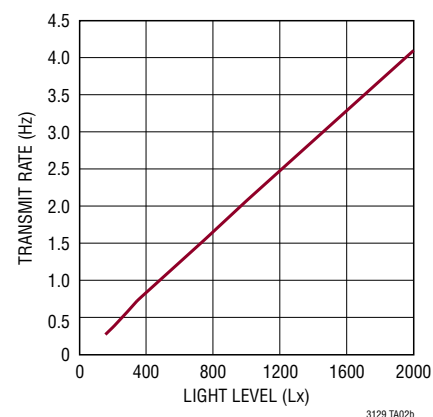
Sources of Small Photovoltaic Panels

A list of companies that manufacture small solar panels (sometimes referred to as modules or solar cell arrays) suitable for use with the LTC3129 is provided in Table 3.

Table 3. Small Photovoltaic Panel Manufacturers

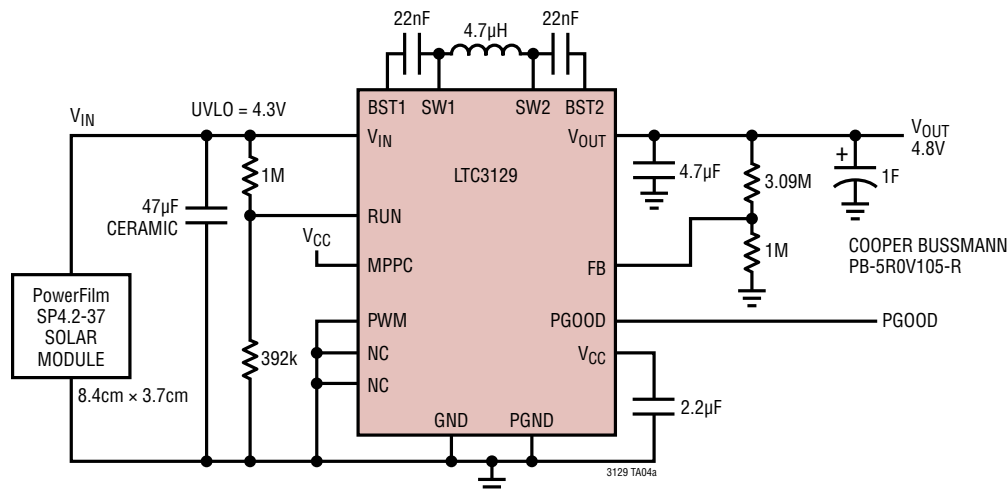
|                  |                                                                                                                           |
|------------------|---------------------------------------------------------------------------------------------------------------------------|
| Sanyo            | <a href="http://panasonic.net/energy/amorton/en/">http://panasonic.net/energy/amorton/en/</a>                             |
| PowerFilm        | <a href="http://www.powerfilmsolar.com/">http://www.powerfilmsolar.com/</a>                                               |
| Ixys Corporation | <a href="http://www.ixys.com/ProductPortfolio/GreenEnergy.aspx">http://www.ixys.com/ProductPortfolio/GreenEnergy.aspx</a> |
| G24 Innovations  | <a href="http://www.g24i.com/">http://www.g24i.com/</a>                                                                   |

### Transmit Rate vs Light Level (Fluorescent)

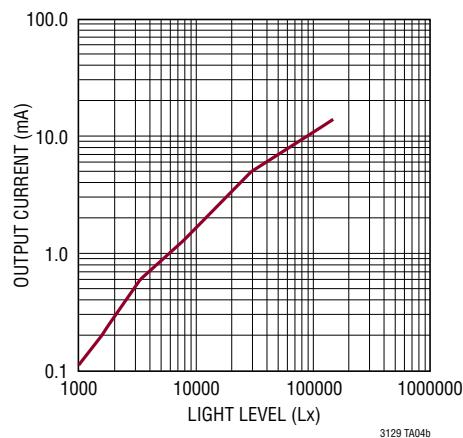


TYPICAL APPLICATIONS

Solar Powered Converter with MPPC Charges Storage Capacitor

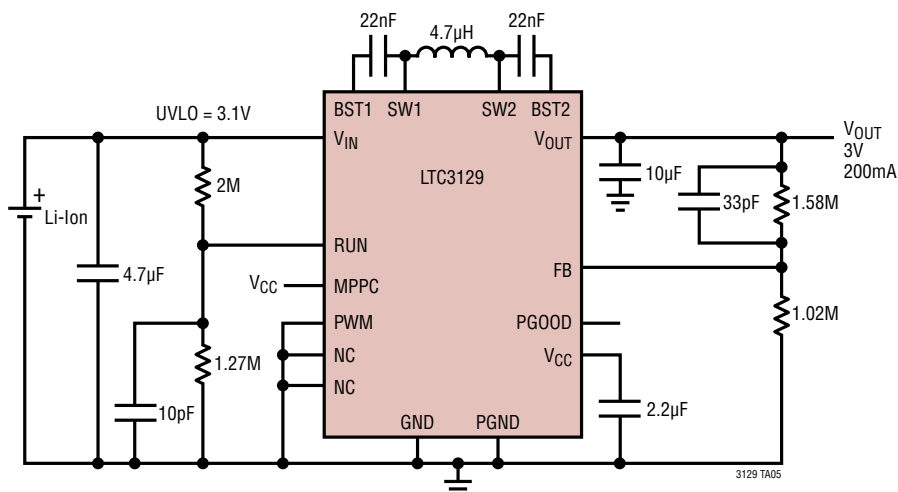


Average Output Current vs Light Level (Daylight)

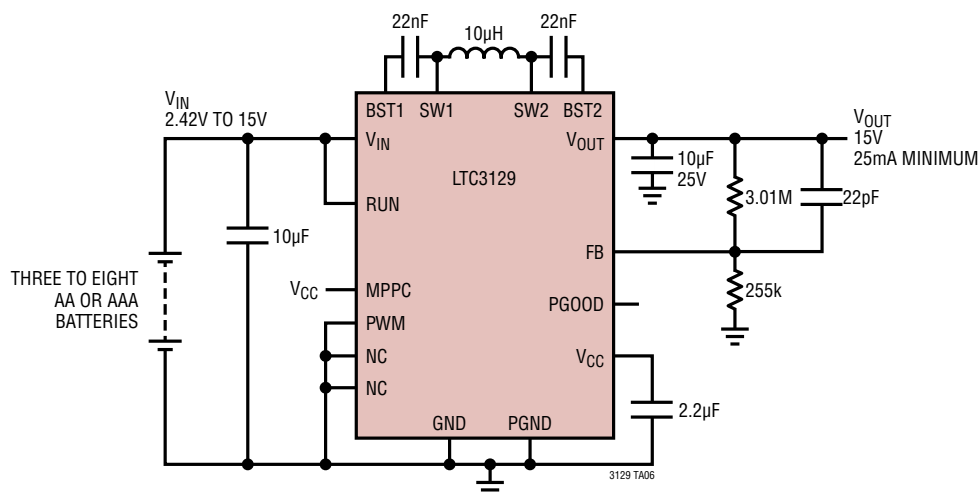


## TYPICAL APPLICATIONS

### Li-Ion Powered 3V Converter with 3.1V Input UVLO Reduces Low Battery $I_Q$ to 3 $\mu$ A

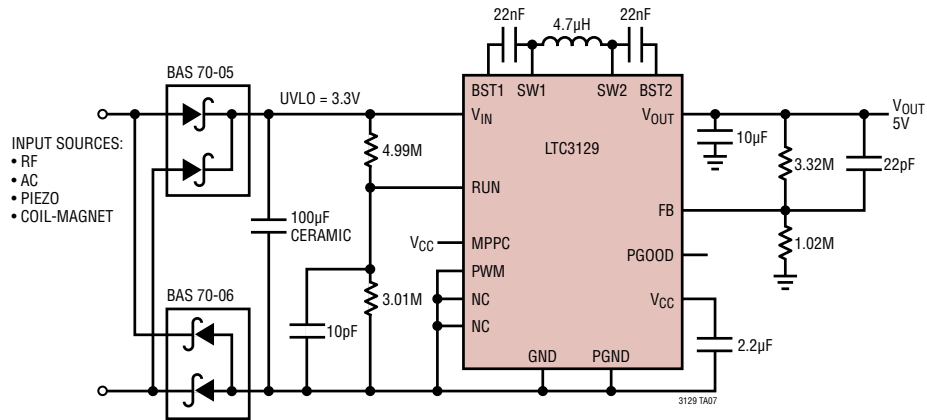


### 15V Converter Operates from Three to Eight AA or AAA Cells

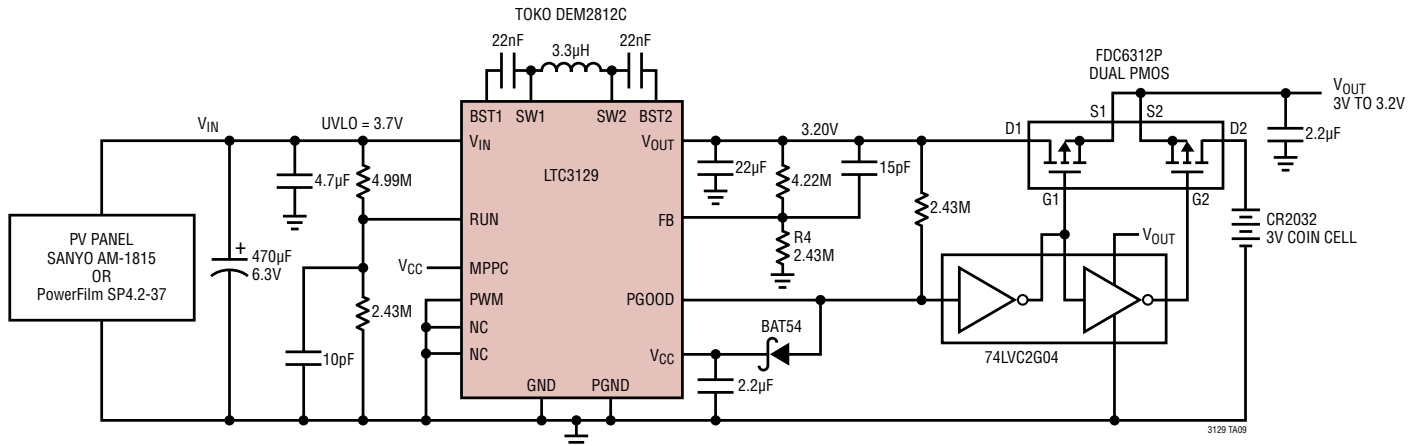


## TYPICAL APPLICATIONS

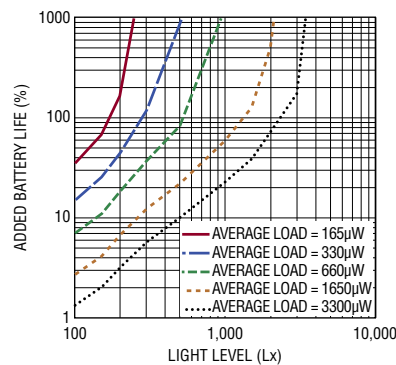
### Energy Harvesting Converter Operates from a Variety of Weak Sources



### Solar Powered Converter Extends Battery Life in Low Power 3V Primary Battery Applications



### Percentage of Added Battery Life vs Light Level and Load (PowerFilm SP4.2-37, 30sq cm Panel)



**UD Package**  
**16-Lead Plastic QFN (3mm × 3mm)**  
 (Reference LTC DWG # 05-08-1700 Rev A)

Top view of the package showing dimensions and pin locations. The package outline is a square with a side length of  $3.50 \pm 0.05$ . The pin pitch is  $1.65 \pm 0.05$  (4 SIDES). The distance from the package edge to the center of the pins is  $0.70 \pm 0.05$ . The distance from the package edge to the center of the pins is  $0.25 \pm 0.05$ . The distance from the package edge to the center of the pins is  $0.50$  BSC.

3.00 ± 0.10  
(4 SIDES)

PIN 1  
TOP MARK  
(NOTE 6)

0.75 ± 0.05

R = 0.115  
TYP

15 16

0.40 ± 0.10

1.65 ± 0.10  
(4-SIDES)

1 2

(UD16 VAR A) QFN 1207 REV A

0.200 REF

0.00 - 0.05

0.25 ± 0.05

0.50 BSC

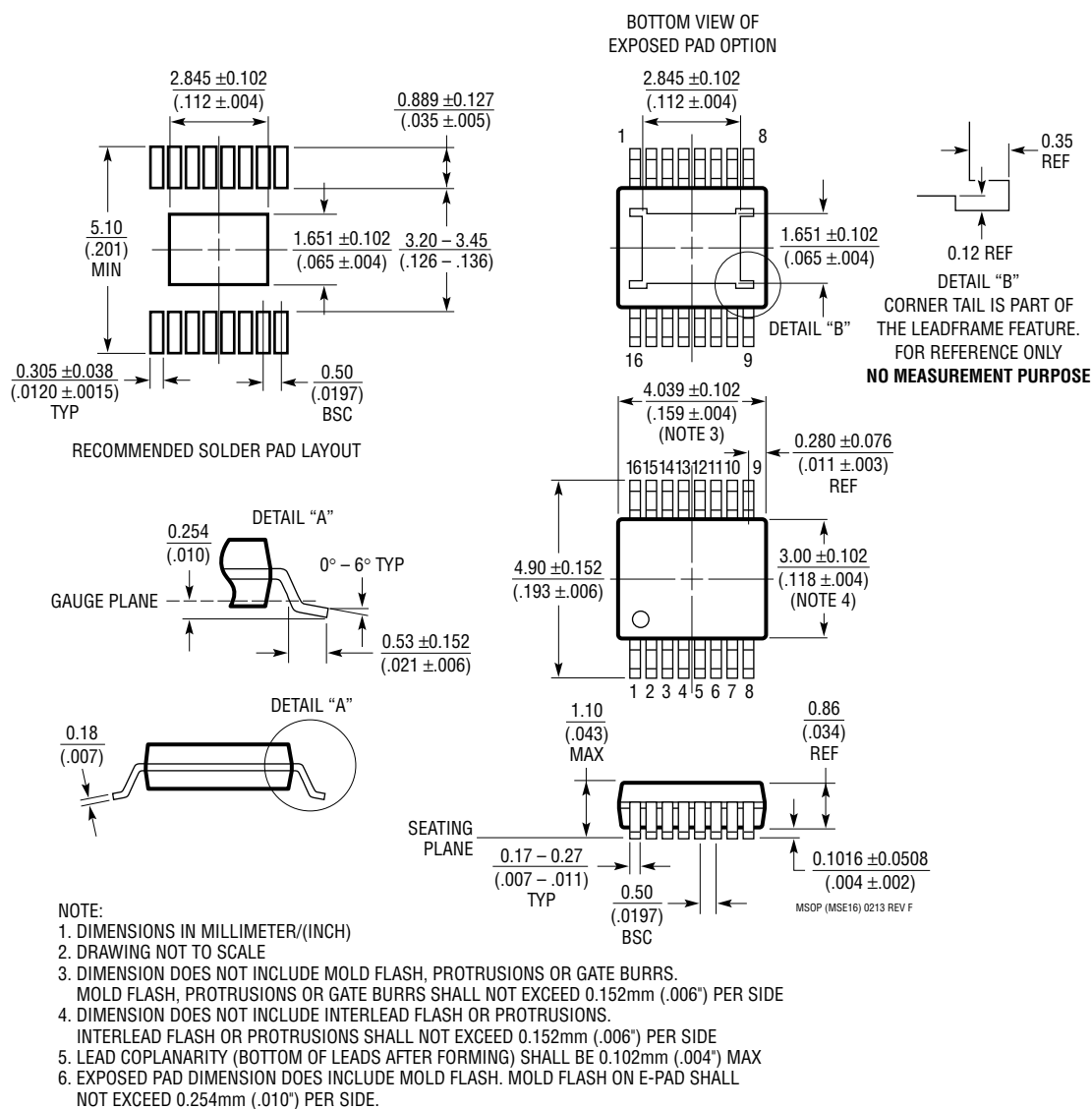
PIN 1 NOTCH R = 0.20 TYP  
OR 0.25 x 45° CHAMFER

1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-4)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTC3129#packaging> for the most recent package drawings.

### MSE Package 16-Lead Plastic MSOP, Exposed Die Pad (Reference LTC DWG # 05-08-1667 Rev F)



## REVISION HISTORY

| REV | DATE  | DESCRIPTION                                                                                | PAGE NUMBER |
|-----|-------|--------------------------------------------------------------------------------------------|-------------|
| A   | 5/14  | Clarified $V_{CC}$ Leakage to $V_{IN}$ if $V_{CC} > V_{IN}$ : from $-7\mu A$ to $-27\mu A$ | 4           |
| B   | 10/14 | Clarified typ $V_{OUT}$ Current in Sleep Mode                                              | 4           |
|     |       | Clarified PGOOD Pin Description                                                            | 8           |
|     |       | Clarified Operation Paragraph                                                              | 15          |
| C   | 10/15 | Changed MAX $V_{CC}$ Current Limit                                                         | 3           |
|     |       | Modified MPPC section                                                                      | 15          |
|     |       | Modified Table 3                                                                           | 22          |

