Dual 4MHz, ±3A Synchronous Buck Converter for DDR Termination

FEATURES

- **DDR Power Supply, Termination and Reference**
- **High Efficiency: Up to 94%**
- **Dual Outputs with ±3A Output Current Capability**
- **2.25V to 5.5V Input Voltage Range**
- **±1% Output Voltage Accuracy**
- **V_{TT} Output Voltage Down to 0.5V**
- Shutdown Current ≤1µA
- VTTR = VDDQIN/2, V_{FB2} = VTTR
- Adjustable Switching Frequency Up to 4MHz
- Internal or External Compensation
- Selectable 0°/90°/180° Phase Shift Between Channels
- Internal or External Soft-Start for V_{DDQ}, Internal Soft-Start for V_{TT}
- Power Good Status Outputs
- Low Profile 4mm × 4mm QFN-24 and TSSOP-24 Packages

APPLICATIONS

- DDR Memory
- Supports DDR, DDR2, and DDR3 Standards
- Tracking Supplies

DESCRIPTION

The LTC®3618 is a dual synchronous step-down regulator using a current mode, constant-frequency architecture. It provides a complete DDR solution with an input voltage range from 2.25V to 5.5V.

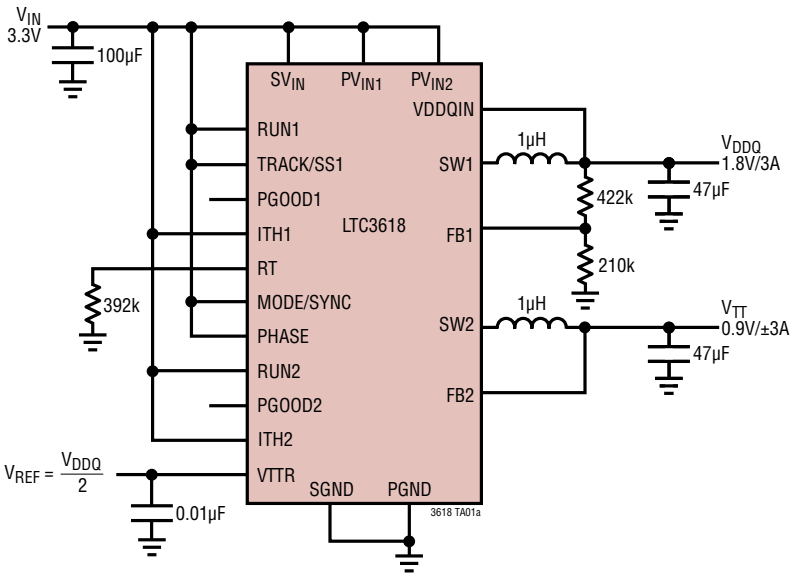
The output of the first step-down regulator offers a high accuracy V_{DDQ} supply. A buffered reference generates VTTR at 50% of VDDQIN and drives loads up to ±10mA. The second regulator generates the DDR termination voltage (V_{TT}) equal to VTTR. Both regulators are capable of delivering ±3A of load current at 1MHz switching frequency.

The operating frequency is externally programmable up to 4MHz, allowing the use of small surface mount inductors. 0°, 90°, or 180° of phase shift between the two channels can be selected to minimize input current ripple. For switching noise-sensitive applications, the LTC3618 can be synchronized to an external clock up to 4MHz.

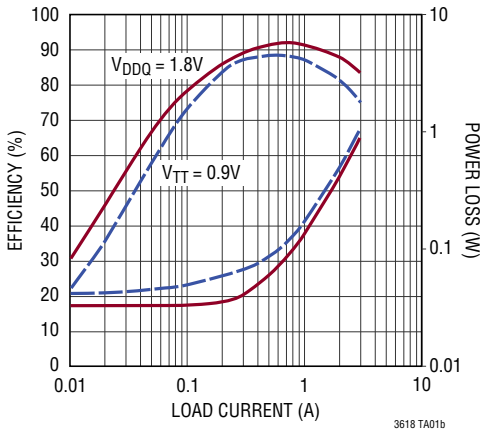
The LTC3618 is offered in leadless 24-pin 4mm × 4mm QFN and thermally enhanced 24-pin TSSOP packages.

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TYPICAL APPLICATION



Efficiency and Power Loss vs Load Current

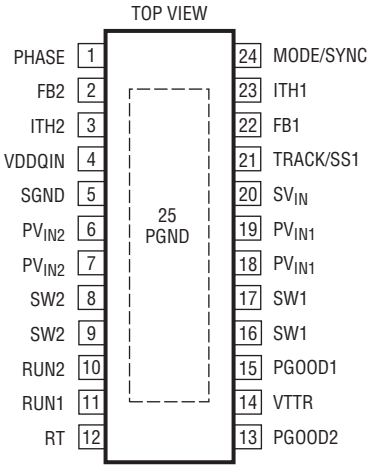


ABSOLUTE MAXIMUM RATINGS (Notes 1, 10)

PV_{IN1}, PV_{IN2} Voltages ..... –0.3V to 6V
SV_{IN} Voltage ..... –0.3V to 6V
SW1 Voltage ..... –0.3V to (PV_{IN1} + 0.3V)
SW2 Voltage ..... –0.3V to (PV_{IN2} + 0.3V)
RUN1 Voltage..... –0.3V to (SV_{IN} + 0.6V)
All Other Pins..... –0.3V to 6V

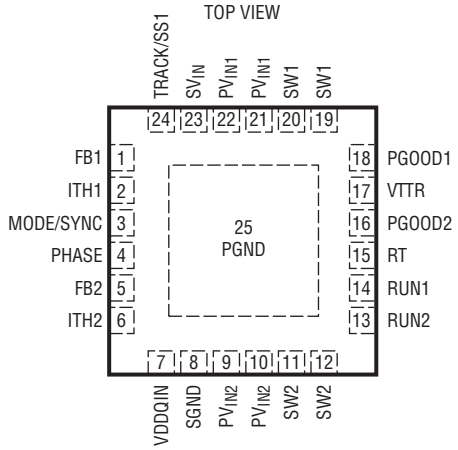
Operating Junction Temperature
Range (Note 2)..... –40°C to 125°C
Storage Temperature..... –65°C to 150°C
Lead Soldering Temperature (TSSOP) ..... 300°C
Reflow Peak Body Temperature (QFN) ..... 260°C

PIN CONFIGURATION



FE PACKAGE
24-LEAD PLASTIC TSSOP

T_{JMAX} = 125°C, θ_{JA} = 33°C/W
EXPOSED PAD (PIN 25) IS PGND, MUST BE SOLDERED TO PCB



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 46.9°C/W
EXPOSED PAD (PIN 25) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3618EFE#PBF	LTC3618EFE#TRPBF	LTC3618FE	24-Lead Plastic TSSOP	–40°C to 125°C
LTC3618IFE#PBF	LTC3618IFE#TRPBF	LTC3618FE	24-Lead Plastic TSSOP	–40°C to 125°C
LTC3618EUF#PBF	LTC3618EUF#TRPBF	3618	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C
LTC3618IUF#PBF	LTC3618IUF#TRPBF	3618	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2), SV_{IN} = PV_{INx} = 3.3V, R_T = 178k, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Voltage Range		●	2.25		5.5	V
V_{UVLO}	Undervoltage Lockout Threshold	SV_{IN} Ramping Down		1.8			V
		SV_{IN} Ramping Up				2.2	V
OVLO	Overvoltage Lockout Threshold	SV_{IN} Ramping Down Hysteresis			6.2 300		V mV
V_{FB1}	V_{DDQ} Feedback Voltage Internal Reference with Line and Load Regulation	(Note 3) $V_{TRACK/SS1}$ = SV_{IN} 0°C < T_J < 85°C –40°C < T_J < 125°C	 ●	 0.592 0.590	 0.6 	 0.608 0.610	 V V
	Feedback Voltage External Reference (Note 6)	(Note 3) $V_{TRACK/SS1}$ = 0.3V		0.289	0.3	0.311	V
		(Note 3) $V_{TRACK/SS1}$ = 0.5V		0.489	0.5	0.511	V
V_{FB2}	V_{TT} Feedback Reference Voltage with Line and Load Regulation	VDDQIN = 1.5V	●	VTTR – 6	VTTR	VTTR + 6	mV
VTTR	VTTR Output Voltage with Line and Load Regulation	VDDQIN = 1.5V, I_{LOAD} = ±10mA, C_{LOAD} = < 0.1µF	●	0.49 • V_{DDQ}	0.5 • V_{DDQ}	0.51 • V_{DDQ}	V
I_{FB}	Feedback Input Current	V_{FBx} = 0.6V	●		0	±30	nA
	VTTR Maximum Output Current					±10	mA
I_S	Input Supply Current, Active Mode	V_{FB1} = 0.5V, V_{MODE} = SV_{IN}, V_{RUN1} = SV_{IN}, V_{RUN2} = 0V, (Note 5)			2.4		mA
		V_{FBx} = 0.5V, V_{MODE} = SV_{IN}, V_{RUNx} = SV_{IN}, (Note 5)			2.8		mA
	Input Supply Current, Shutdown	SV_{IN} = PV_{IN} = 5.5V, V_{RUNx} = 0V			0.1	1	µA
$R_{DS(ON)}$	Top Switch On-Resistance	PV_{INx} = 3.3V (Note 9)			75		mΩ
	Bottom Switch On-Resistance	PV_{INx} = 3.3V (Note 9)			55		mΩ
I_{LIMX}	Peak Current Limit Positive Limit Negative Limit	 Sourcing (Note 7), V_{FBX} = 0.5V Sinking (Note 7), V_{FBX} = 0.7V		 4.2 –2.5	 5.5 –3.5	 8.0 –5.5	 A A
$I_{SW(LKG)}$	Switch Leakage Current	SV_{IN} = PV_{IN} = 5.5V, V_{RUNx} = 0V			0.01	1	µA
$g_{m(EA)}$	Error Amplifier Transconductance	–5µA < I_{TH} < 5µA			240		µmho
I_{EAO}	Error Amplifier Output Current	(Note 4)			±30		µA
$t_{SOFT-START1}$	V_{DDQ} Internal Soft-Start Time	V_{FB1} from 0.06V to 0.54V, TRACK/SS1 = SV_{IN}		0.5	1.1	2	ms
$t_{SOFT-START2}$	V_{TT} Internal Soft-Start Time	V_{FB2} from 0V to 0.75V		0.25	0.6	1	ms
$R_{ON(TRACK/SS1_DIS)}$	TRACK/SS1 Pull-Down Resistance at Start-Up					200	Ω
$t_{TRACK/SS1_DIS}$	Soft-Start Discharge Time at Start-Up			65			µs
f_{OSC}	Oscillator Frequency	R_{RT} = 178k	●	1.85	2.25	2.65	MHz
	Internal Default Oscillator Frequency	V_{RT} = SV_{IN}	●	1.8	2.25	2.7	MHz
f_{SYNC}	Synchronization Frequency	t_{LOW} , t_{HIGH} > 30ns		0.4		4	MHz
$V_{MODE/SYNC}$	SYNC Level High Voltage			1.2			V
	SYNC Level Low Voltage					0.3	V
$\varphi_{SW1–SW2}$	Output Phase Shift Between SW1 and SW2	V_{PHASE} < 0.15 • SV_{IN}			0		Deg
		0.35 • SV_{IN} < V_{PHASE} < 0.65 • SV_{IN}			90		Deg
		V_{PHASE} > 0.85 • SV_{IN}			180		Deg

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2), SV_{IN} = PV_{INx} = 3.3V, R_T = 178k, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{MODE} (Note 8)	V_{MODE} High Voltage	Pulse-Skipping Mode		1.0			V
	V_{MODE} Low Voltage	Forced Continuous Mode				0.4	V
PGOOD1	Power Good Voltage Window of V_{DDQ}	TRACK/SS1 = SV_{IN}, Entering Window V_{FB1} Ramping Up V_{FB1} Ramping Down		 2	 –5 5	 –2 	 % %
		TRACK/SS1 = SV_{IN}, Leaving Window V_{FB1} Ramping Up V_{FB1} Ramping Down		 –10.5	 8 –8	 10.5 	 % %
PGOOD2	Power Good Voltage Window of V_{TT}	Entering Window V_{TT} Ramping Up V_{TT} Ramping Down		 2.5	 –5 5	 –2.5 	 % %
		Leaving Window V_{FB2} Ramping Up V_{FB2} Ramping Down		 –10.5	 8 –8	 10.5 	 % %
t_{PGOOD}	Power Good Blanking Time	Entering/Leaving Window		65	105	140	µs
R_{PGOOD}	Power Good Pull-Down On-Resistance	I = 10mA		8	12	30	Ω
V_{RUN}	V_{RUN} Voltage	Input High Input Low	● ●	1 	 	 0.4	V V
	Pull-Down Resistance				4		MΩ

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3618 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3618E is guaranteed to meet performance specifications over the 0°C to 85°C operating junction temperature range. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3618I is guaranteed to meet specifications over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: This parameter is tested in a feedback loop which servos V_{FB1} to the midpoint for the error amplifier (V_{ITH1} = 0.75V).

Note 4: External compensation on ITH pin.

Note 5: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

Note 6: See description of the TRACK/SS pin in the Pin Functions section.

Note 7: When sourcing current, the average output current is defined as flowing out of the SW pin. When sinking current, the average output current is defined as flowing into the SW pin. Sinking mode requires the use of forced continuous mode.

Note 8: See description of the MODE pin in the Pin Functions section.

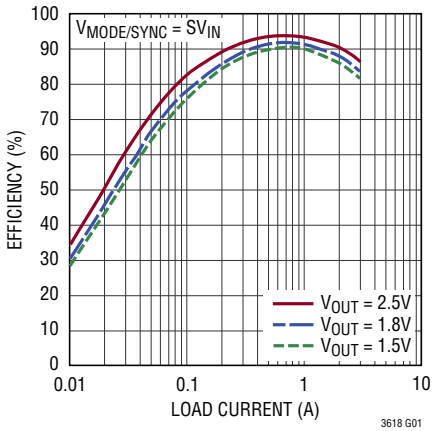
Note 9: Guaranteed by design and correlation to wafer level measurements for QFN packages.

Note 10: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability or permanently damage the device.

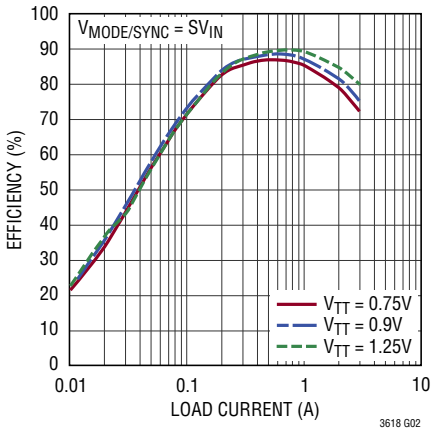
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 3.3V, f = 1MHz, Figure 3 Circuit, unless otherwise noted.

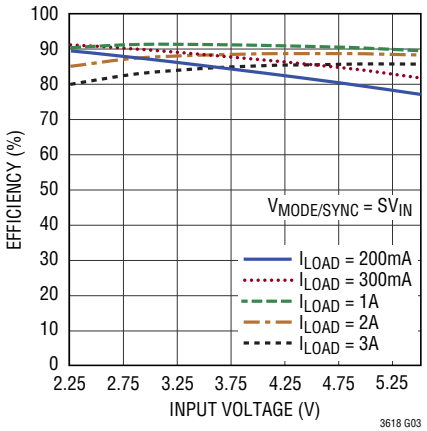
Efficiency vs Load Current



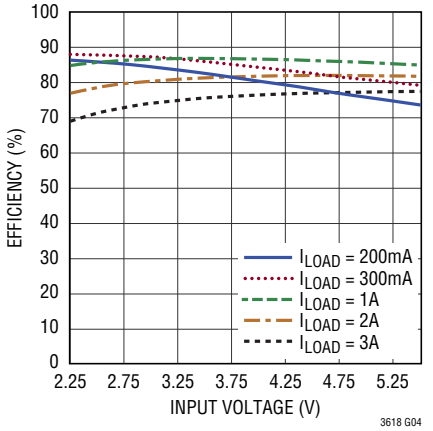
Efficiency vs Load Current



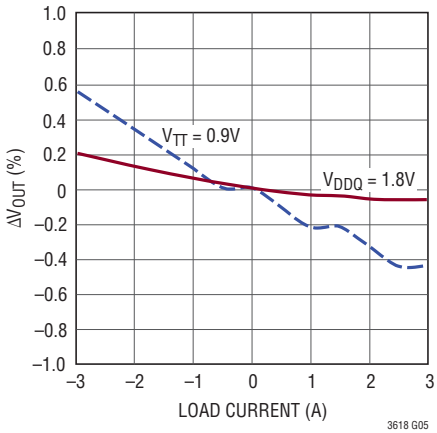
Efficiency vs Input Voltage V_{DDQ} = 1.8V



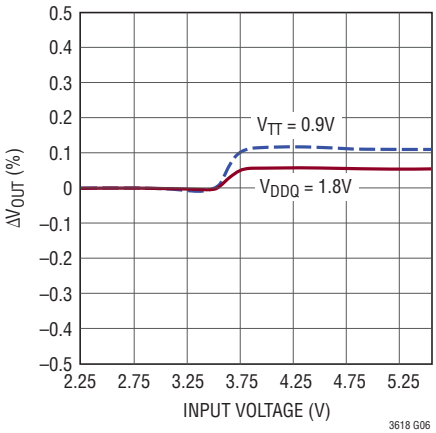
Efficiency vs Input Voltage V_{TT} = 0.9V



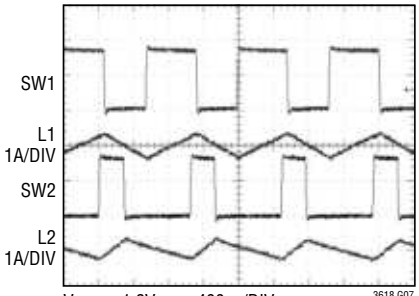
V_{OUT} Load Regulation



Input Voltage Line Regulation

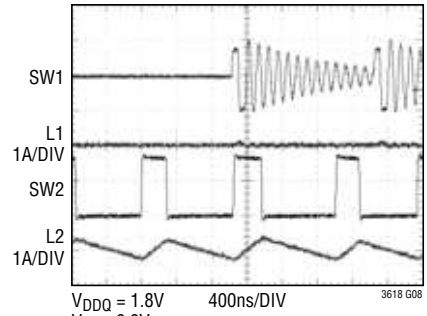


Forced Continuous Mode Operation (FCM)



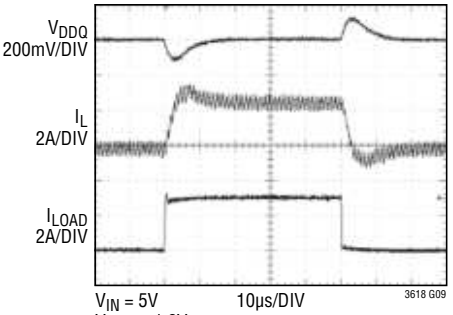
V_{DDQ} = 1.8V 400ns/DIV
V_{TT} = 0.9V
NO LOAD

Pulse-Skipping Mode



V_{DDQ} = 1.8V 400ns/DIV
V_{TT} = 0.9V
NO LOAD
V_{TT} IS ALWAYS IN FORCED CONTINUOUS MODE

Load Step Transient with FCM Internal Compensation

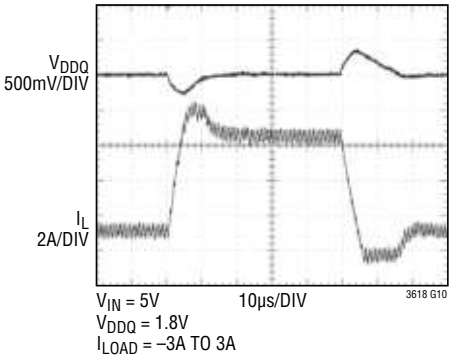


V_{IN} = 5V 10µs/DIV
V_{DDQ} = 1.8V
I_{LOAD} = 0A TO 3A

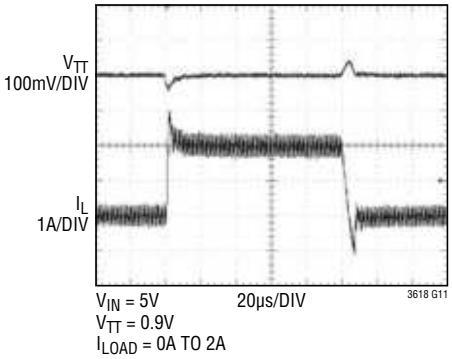
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 3.3V, f = 1MHz, Figure 3 Circuit, unless otherwise noted.

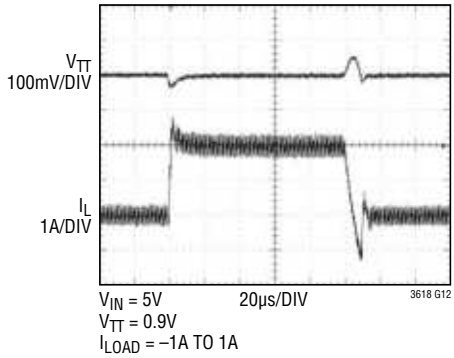
Load Step Transient in Forced Continuous Mode, Internal Compensation



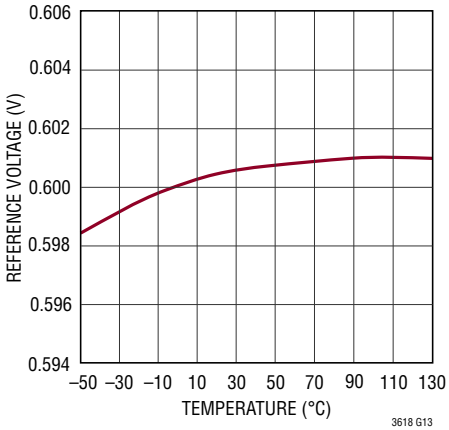
Load Step Transient in Forced Continuous Mode, Internal Compensation



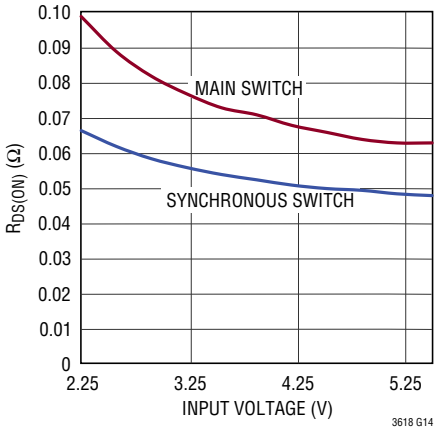
Load Step Transient in Forced Continuous Mode, Internal Compensation



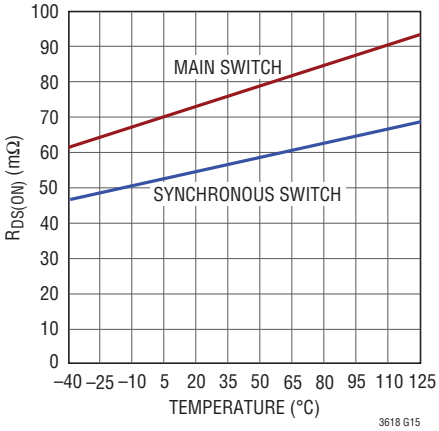
Reference Voltage vs Temperature



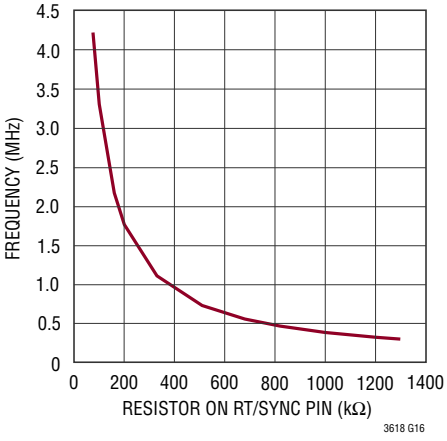
Switch On-Resistance vs Input Voltage



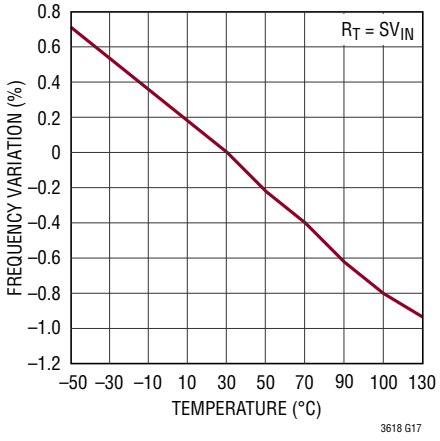
Switch On-Resistance vs Temperature



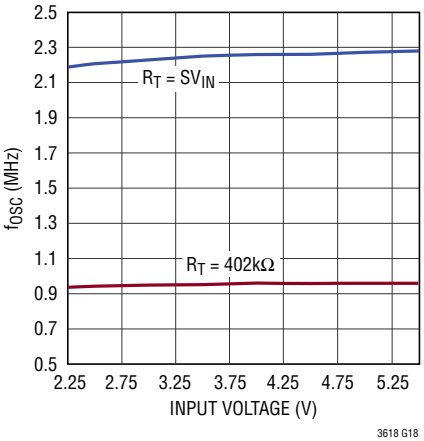
Frequency vs R_T



Frequency vs Temperature



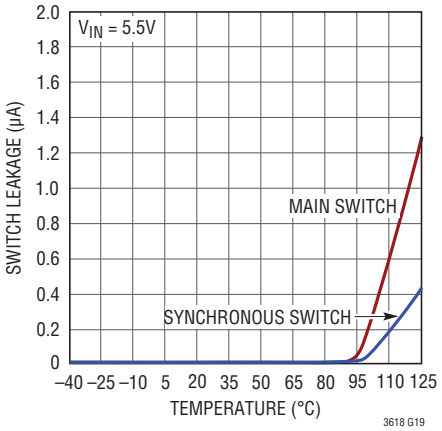
Switching Frequency vs Input Voltage



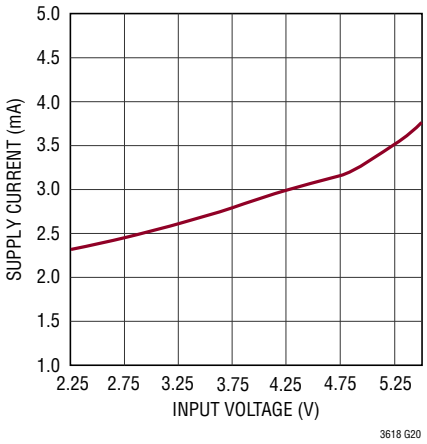
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 3.3V, f = 1MHz, Figure 3 Circuit, unless otherwise noted.

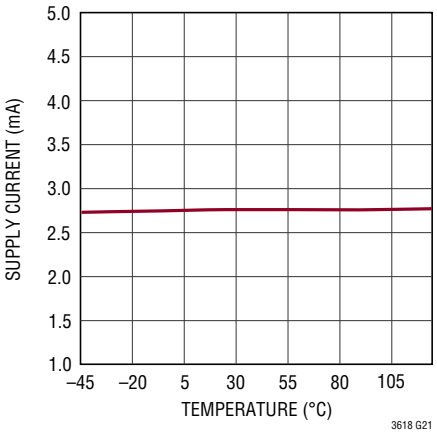
Switch Leakage Current vs Temperature



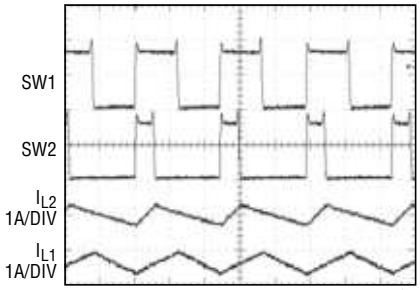
No Load Supply Current vs Input Voltage



No Load Supply Current vs Temperature

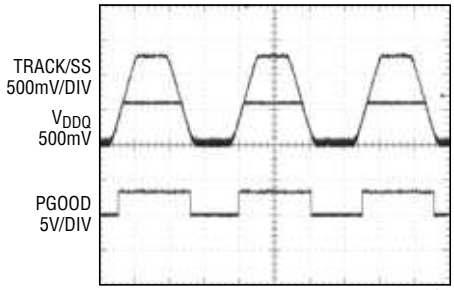


Sinking Current



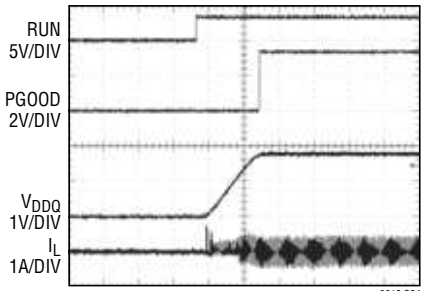
V_{DDQ} = 1.8V 400ns/DIV
V_{TT} = 0.9V
I_{LOAD1}, I_{LOAD2} = –3A

Tracking Up/Down



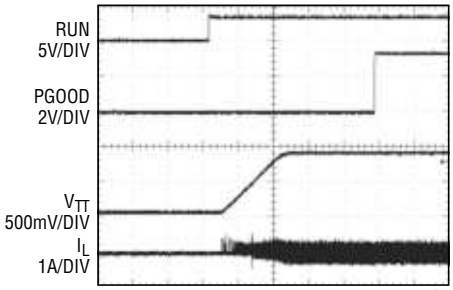
FORCED CONTINUOUS MODE
V_{DDQ} = 0V to 0.6V
I_{LOAD} = 1A

Internal Start-Up V_{DDQ}



V_{DDQ} = 1.8V 1ms/DIV
NO LOAD

Internal Start-Up V_{TT}



V_{TT} = 0.9V 400µs/DIV
NO LOAD

PIN FUNCTIONS (FE/UF)

PHASE (Pin 1/Pin 4): Phase Shift Selection. If pin is tied to SGND, the phase between SW1 and SW2 will be 0°. Tying PHASE to SV_{IN} will select 180° phase shift. With the PHASE pin tied to half of the SV_{IN} voltage, 90° phase shift will be selected.

V_{FB2} (Pin 2/Pin 5): Voltage Feedback Input Pin for V_{TT}. See V_{FB1}.

ITH2 (Pin 3/Pin 6): Error Amplifier Compensation of V_{TT}. See ITH1.

VDDQIN (Pin 4 /Pin 7): External Reference Input. An internal resistor divider to the error amplifier sets the output voltage of V_{TT}. V_{FB2} will regulate to VDDQIN • 0.5.

SGND (Pin 5/Pin 8): Signal Ground. All small-signal and compensation components should connect to this ground pin which, in turn, should be connected to PGND at one point.

PV_{IN2} (Pins 6, 7/Pins 9, 10) V_{TT} Power Supply Input. See PV_{IN1}.

SW2 (Pins 8, 9/Pins 11, 12): V_{TT} Switch Node. See SW1.

RUN2 (Pin 10/Pin 13): Enable Pin for V_{TT}. See RUN1.

RUN1 (Pin 11/Pin 14): Enable Pin for V_{DDQ}. Forcing RUN1 above the input threshold voltage enables the output SW1 of V_{DDQ}. Forcing both RUNx pins to ground shuts down the LTC3618. In shutdown, all functions are disabled and the LTC3618 draws <1µA of supply current.

RT (Pin 12/Pin 15): Oscillator Frequency. This pin provides two modes of setting the switching frequency.

1. Connecting a resistor from RT to ground will set the switching frequency based on the resistor value.
2. Tying this pin to SV_{IN} enables the internal 2.25MHz oscillator frequency.

PGOOD2 (Pin 13/Pin 16): Power Good Output for V_{TT}. See PGOOD1.

VTTR (Pin 14 /Pin 17): Voltage Buffer Output. This pin is the output of an internal voltage buffer whose voltage is equal to VDDQIN • 0.5. Output current capability is ±10mA. Do not exceed 0.1µF capacitance on this pin. This output is enabled/disabled by RUN2.

PGOOD1 (Pin 15/Pin 18): Power Good Output Pin for V_{DDQ}. The open-drain output will be pulled down to ground if the FB1 voltage of the channel is not within the power good voltage window. The PGOOD1 will also be pulled down if the channel is not enabled with the RUN1 pin or an undervoltage at SV_{IN} is detected. The power good window moves in relation to the actual TRACK/SS1 pin voltage.

SW1 (Pins 17, 16/Pins 19, 20): V_{DDQ} Switch Node. Connection to the external inductor. This pin connects to the drains of the internal synchronous power MOSFET switches.

PV_{IN1} (Pins 18, 19/Pins 21, 22): V_{DDQ} Power Supply Inputs. These pins connect to the source of the internal power P-channel MOSFET of V_{DDQ}. P_{VIN1} and P_{VIN2} are independent of each other. They may connect to equal or lower supplies than S_{VIN}.

SV_{IN} (Pin 20/Pin 23) Signal Input Supply. This pin powers the internal control circuitry and is monitored by the undervoltage lockout comparator.

TRACK/SS1 (Pin 21/Pin 24): Internal, External Soft-Start, External Reference Input for V_{DDQ}. The type of start-up behavior for V_{DDQ} is programmable with the TRACK/SS1 pin:

1. Internal soft-start with fixed timing can be programmed by tying TRACK/SS1 to SV_{IN}.
2. External soft-start can be programmed with the timing set by a capacitor to ground and a resistor to SV_{IN}.
3. Tracking the start-up behavior of another supply is programmable (see the Applications Information section).
4. The pin can be used as external reference input.

ITH1 (Pin 23/Pin 2): Error Amplifier Compensation. Connection for external compensation from ITH to SGND. The current comparator's threshold increases with this control voltage. Tying this pin to SV_{IN} enables internal compensation.

V_{FB1} (Pin 22/Pin 1): Voltage Feedback Input Pin for V_{DDQ}. Receives the feedback voltage for V_{DDQ} from the external resistive divider across the output.

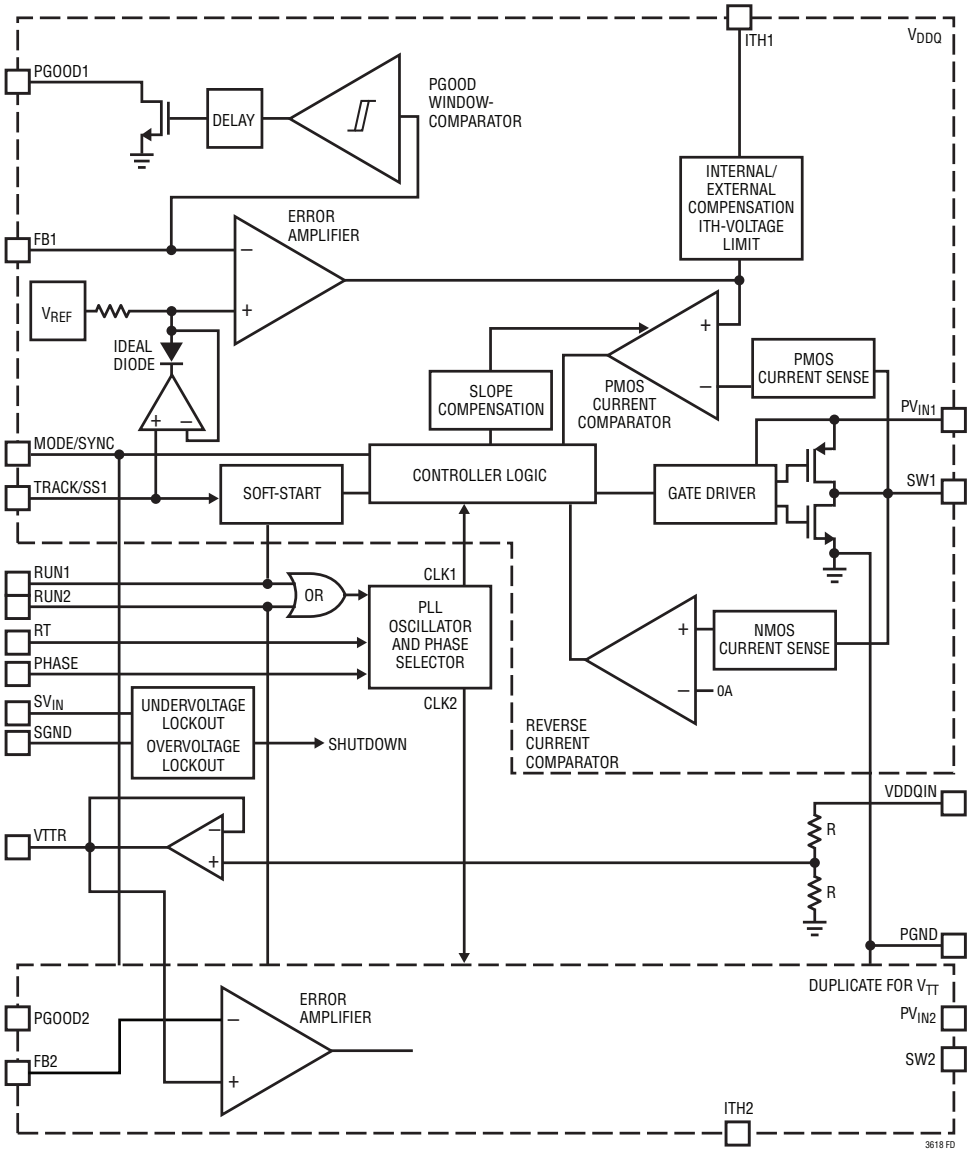
PIN FUNCTIONS (FE/UF)

MODE/SYNC (Pin 24/Pin 3): Mode Selection.

1. Tying the MODE pin to SV_{IN} or SGND enables pulse-skipping mode or forced continuous mode respectively for V_{DDQ} only. The default operation mode for V_{TT} is forced continuous mode. The input to the MODE/SYNC pin should be a digital signal.
2. When a clock signal is applied to this pin, the switching frequency synchronizes to this clock signal and forced continuous mode is selected for V_{DDQ}.

PGND (Exposed Pad Pin 25/ Exposed Pad Pin 25): Power Ground. The exposed pad connects to the sources of the power N-channel MOSFETs. The PGND pin is common for both channels. The exposed pad must be soldered to the PCB for electrical connection and rated thermal performance. Refer to the Operation and Applications Information sections for more information.

FUNCTIONAL BLOCK DIAGRAM



OPERATION

Main Control Loop

The LTC3618 is a dual monolithic step-down DC/DC converter featuring current-mode, constant-frequency operation. The regulated output voltage of the second step-down converter is equal to VDDQIN • 0.5. An additional internal amplifier provides a VTTR output equal to VDDQIN • 0.5, which is capable of driving a ±10mA load.

During normal operation, the internal top power switch (P-channel MOSFET) of each channel is turned on at the beginning of its clock cycle. Current in the inductor increases until the current comparator trips and turns off the top power MOSFET. The peak inductor current at which the current comparator shuts off is controlled by the voltage on the ITH pin. The error amplifier adjusts the voltage on the ITH pin by comparing the feedback signals V_{FBX} (derived from an external resistor divider on the V_{FB1} pin) with a reference (0.6V for V_{DDQ}, VDDQIN • 0.5 for V_{TT}). When the load current increases, it causes a reduction in the feedback voltage relative to the reference. The error amplifier raises the ITH voltage until the average inductor current matches the new load current. Typical voltage range for the ITH pin is from 0.55V to 1.05V with 0.55V corresponding to zero current.

When the top power MOSFET shuts off, the synchronous power switch (N-channel MOSFET) turns on until either the current limit is reached or the next clock cycle begins. The bottom current limit is typically set at –4A for forced continuous mode and 0A for pulse-skipping mode.

The operating frequency defaults to 2.25MHz when RT is connected to SV_{IN}, or can be set by an external resistor connected between the RT pin and ground, or by a clock signal applied to the MODE/SYNC pin. The switching frequency can be set from 400kHz to 4MHz (see the Applications Information section).

Overvoltage and undervoltage comparators pull the PGOOD output low if the output voltage varies more than ±8% (typical) from the set point.

V_{IN} Overvoltage Protection

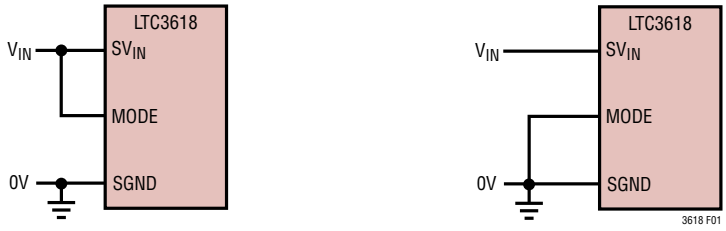
In order to protect the internal power MOSFET devices against transient voltage spikes, the LTC3618 constantly monitors the V_{IN} pin for an overvoltage condition. When V_{IN} rises above 6.5V, the regulator suspends operation by shutting off the MOSFETs. The regulator executes its soft-start when exiting an overvoltage condition.

MODE SELECTION

The MODE/SYNC pin is used to select one of two different operating modes for V_{DDQ}. When the MODE/SYNC pin is tied to SV_{IN}, pulse-skipping mode is selected, when it is tied to ground, forced continuous mode is selected (Figure 1). V_{TT} is always in forced continuous mode.

VTTR Voltage Buffer Output

An internal high accuracy op amp buffer generates a VTTR pin voltage that is equal to VDDQIN • 0.5. VTTR can source and sink up to 10mA and is stable with a 0.1µF capacitor. Short circuit current limit is set around 20mA to prevent damage to the op amp. The VTTR output is also the reference voltage for V_{TT}. Therefore, large transients on this pin will impact the behavior at the V_{TT} output.



1a. Pulse-Skipping Mode **1b. Forced Continuous Mode**

Figure 1. V_{DDQ} Modes of Operation

OPERATION

Pulse-Skipping Mode Operation

Connecting the MODE/SYNC pin to SV_{IN} enables pulse-skipping mode for V_{DDQ} only. As the load current decreases, the peak inductor current will be determined by the voltage on the ITH1 pin until the ITH1 voltage drops below 550mV, corresponding to 0A. At this point switching cycles will be skipped to keep the output voltage in regulation.

Forced Continuous Mode Operation

In forced continuous mode the inductor current is constantly cycled which creates a minimum output voltage ripple at all output current levels.

Connecting the MODE/SYNC pin to ground will select the forced continuous mode operation for V_{DDQ}.

The forced continuous mode must be used if the output is required to sink current.

Dropout Operation

As the input supply voltage approaches the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle, eventually reaching 100% duty cycle. The output voltage will then be determined by the input voltage minus the voltage drop across the internal P-channel MOSFET and the inductor.

Low Supply Operation

The LTC3618 is designed to operate down to an input supply voltage of 2.25V. An important consideration at low input supply voltages is that the $R_{DS(ON)}$ of the P-channel and N-channel power switches increases by 50% compared to 5V. The user should calculate the power dissipation when the LTC3618 is used at 100% duty cycle with low input voltages to ensure that thermal limits are not exceeded.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in current mode constant-frequency architectures by preventing subharmonic oscillations at duty cycles greater than 50%. The LTC3618 implements slope compensation by adding a compensation ramp to the inductor current signal.

Short-Circuit Protection

The peak inductor current at which the current comparator shuts off the top power switch is controlled by the voltage on the ITH pin.

If the output current increases, the error amplifier raises the ITH pin voltage until the average inductor current matches the new load current. In normal operation, the LTC3618 clamps the maximum ITH pin voltage at approximately 1.05V which corresponds to about 5.5A peak inductor current.

When the output is shorted to ground, the inductor current decays very slowly during a single switching cycle. The LTC3618 uses two techniques to prevent current runaway from occurring:

1. If the output voltage drops below 50% of its nominal value, the clamp voltage at the ITH pin is lowered, causing the maximum peak inductor current to lower gradually with the output voltage. When the output voltage reaches 0V, the clamp voltage at the ITH pin drops to 40% of the clamp voltage during normal operation. The short-circuit peak inductor current is determined by the minimum on-time of the LTC3618, the input voltage and the inductor value. This foldback behavior helps in limiting the peak inductor current when the output is shorted to ground. It is disabled during internal or external soft-start and tracking up/down operation (see the Applications Information section).
2. If the inductor current of the bottom MOSFET increases beyond 6A typical, the top power MOSFET will be held off and switching cycles will be skipped until the inductor current reduces.

APPLICATIONS INFORMATION

Operating Frequency

Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values.

Lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

The operating frequency of the LTC3618 is determined by an external resistor that is connected between the RT pin and ground. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator and can be calculated by using the following equation:

$$R_T = \frac{4 \bullet 10^{11} \Omega Hz}{f_{OSC}}$$

Although frequencies as high as 4MHz are possible, the minimum on-time of the LTC3618 imposes a minimum limit on the operating duty cycle. The minimum on-time is typically 80ns, therefore, the minimum duty cycle is equal to 80ns • 100% • f_{OSC}(Hz)

Tying the RT pin to SV_{IN} sets the default internal operating frequency to 2.25MHz.

The minimum on-time also limits the sinking current capability for high switching frequency applications. Figure 2 shows the sinking current vs switching frequency at different input voltages.

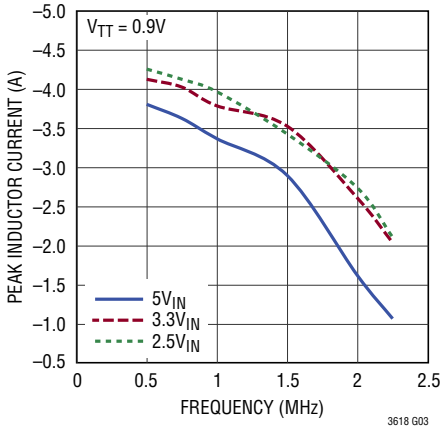


Figure 2. Sinking Current vs Switching Frequency

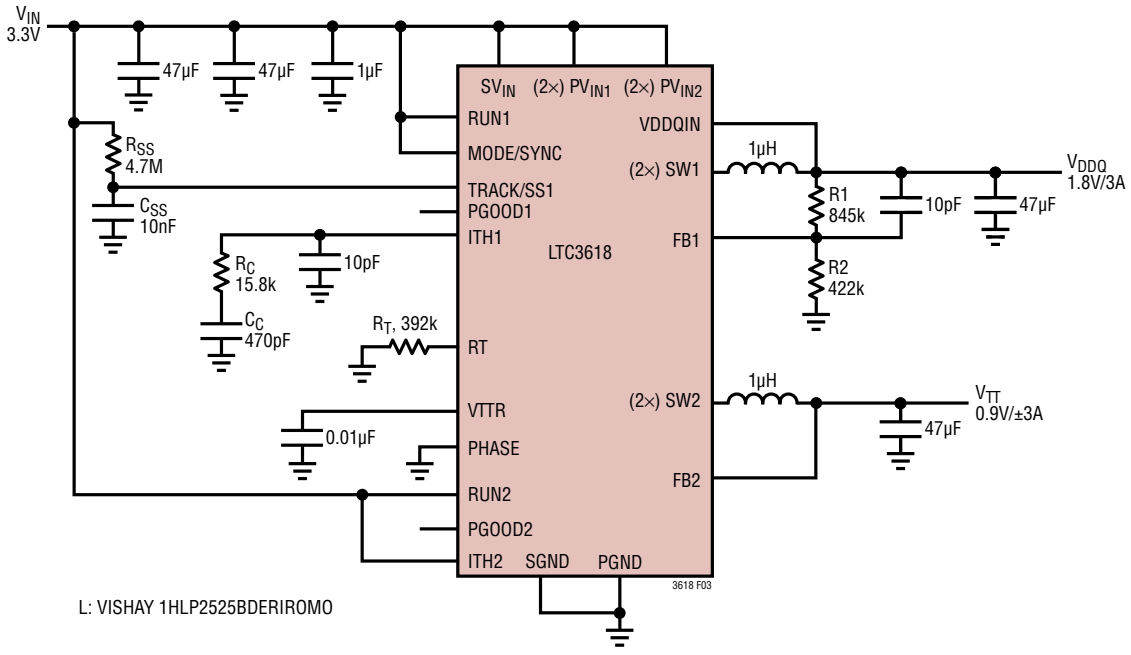


Figure 3. Soft-Start and Compensation for V_{DDQ} Externally Programmed, Compensation for V_{TT} Internally Programmed

APPLICATIONS INFORMATION

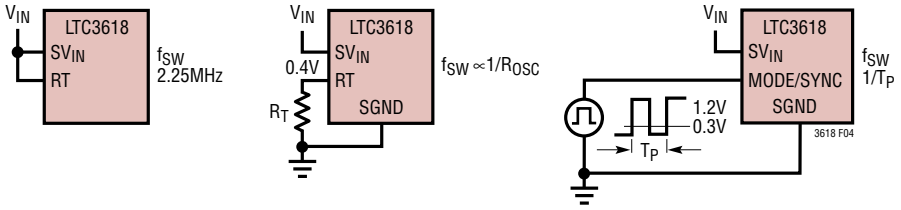


Figure 4. Setting the Switching Frequency

Frequency Synchronization

The LTC3618's internal oscillator can be synchronized to an external frequency by applying a square wave clock signal to the MODE/SYNC pin. During synchronization, the top MOSFET turn-on of V_{DDQ} is locked to the rising edge of the external frequency source. The synchronization frequency range is 400kHz to 4MHz. The internal slope compensation is automatically adapted to the external clock frequency.

In the signal path from the MODE/SYNC clock input to the SW output, the LTC3618 is processing the external clock frequency through an internal PLL.

After detecting an external clock on the first rising edge of MODE/SYNC the PLL starts up with the internal default of 2.25MHz. The internal PLL then requires a certain number of periods to settle until the frequency at SW matches the frequency and phase of MODE/SYNC.

When the external clock signal is removed, the LTC3618 needs approximately 5µs to detect the absence of the external clock. During this time, the PLL will continue to provide clock cycles before it is switched back to the default frequency or selected frequency (set via the external R_T resistor).

In general, any abrupt clock frequency change of the regulator will have an effect on the SW pin timing and may cause equally sudden output voltage changes. This must be taken into account in particular if the external clock frequency is significantly different from the internal default of 2.25MHz.

Phase Selection

V_{TT} will operate in-phase, 180° out-of-phase (anti-phase) or shifted by 90° from V_{DDQ} depending on the state of the PHASE pin—low, midrail or high, respectively. Antiphase generally reduces input voltage and current ripple. Cross-talk between switch nodes SW1, SW2 and components or sensitive lines connected to FBx, ITHx, RT can cause unstable switching waveforms and unexpectedly large input and output voltage ripple.

The situation improves if rising and falling edges of the switch nodes are timed carefully not to coincide. Depending on the duty cycle of the two channels, choose the phase difference between the channels to keep edges as far away from each other as possible.

For a duty cycle of less than 40% for one channel and more than 60% for the other channel, choose a phase shift of 0 or 180° (PHASE = SGND or SV_{IN}). If both channels have a duty cycle of around 50%, select a phase difference of 90° (PHASE = one-half SV_{IN}).

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the inductor ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left(\frac{V_{OUT}}{f_{SW} \bullet L}\right) \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Having a lower ripple current reduces the core losses in the inductor, the ESR losses in the output capacitors and the output voltage ripple. A reasonable starting point for selecting the ripple current is $\Delta I_L = 0.3(I_{OUT(MAX)})$.

APPLICATIONS INFORMATION

The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \left(\frac{V_{OUT}}{f_{SW} \bullet \Delta I_{L(MAX)}}\right) \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for fixed inductor value, but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire, and therefore, copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow a ferrite core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and do not radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. Table 1 shows some typical surface mount inductors that work well in LTC3618 applications.

Table 1. Representative Surface Mount Inductors

INDUCTANCE (µH)	DCR (mΩ)	MAX CURRENT (A)	DIMENSIONS (mm)	HEIGHT (mm)
Vishay IHLP-2020BZ-01				
0.33	7.6	25	5.18 × 5.49	2
0.47	8.9	21	5.18 × 5.49	2
0.68	11.2	15	5.18 × 5.49	2
1	18.9	16	5.18 × 5.49	2
Toko DE3518C Series				
0.22	8	24	4.3 × 4.7	2
Sumida CDMC6D28 Series				
0.3	3.2	15.4	6.7 × 7.25	3
0.47	4.2	13.6	6.7 × 7.25	3
0.68	5.4	11.3	6.7 × 7.25	3
1	8.8	8.8	6.7 × 7.25	3
NEC/Tokin MPLC0730L Series				
0.47	4.5	16.6	6.9 × 7.7	3.0
0.75	7.5	12.2	6.9 × 7.7	3.0
1.0	9.0	10.6	6.9 × 7.7	3.0
Coilcraft DO1813H Series				
0.33	4	10	8.9 × 6.1	5
0.56	10	7.7	8.9 × 6.1	5
Coilcraft SLC7530 Series				
0.27	0.1	14	7.5 × 6.7	3
0.35	0.1	11	7.5 × 6.7	3
0.4	0.1	8	7.5 × 6.7	3

Input Capacitor C_{IN} Selection

In continuous mode, the source current of the top P-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current must be used for C_{IN}.

The maximum RMS capacitor current is given by:

$$I_{RMS} = I_{OUT(MAX)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \sqrt{\left(\frac{V_{IN}}{V_{OUT}} - 1\right)}$$

APPLICATIONS INFORMATION

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

Output Capacitor C_{OUT} Selection

The selection of C_{OUT} is typically driven by the required ESR to minimize voltage ripple and load step transients (low-ESR ceramic capacitors are discussed in the next section). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \le \Delta I_L \bullet \left(ESR + \frac{1}{8 \bullet f_{SW} \bullet C_{OUT}} \right)$$

where f_{SW} = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

In surface mount applications, multiple capacitors may be paralleled to meet the capacitance, ESR or RMS current handling requirement of the application. Aluminum electrolytic, special polymer, ceramic and dry tantalum capacitors are all available in surface mount packages.

Tantalum capacitors have the highest capacitance density, but can have higher ESR and must be surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can often be used in extremely cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability.

Ceramic Input and Output Capacitors

Ceramic capacitors have the lowest ESR and can be cost effective, but also have the lowest capacitance density, high voltage and temperature coefficients, and exhibit audible piezoelectric effects. In addition, the high-Q of ceramic capacitors along with trace inductance can lead to significant ringing.

Ceramic capacitors are tempting for switching regulator use because of their very low ESR. Great care must be taken when using only ceramic input and output capacitors.

Ceramic caps are prone to temperature effects which require the designer to check loop stability over the operating temperature range. To minimize their large temperature and voltage coefficients, only X5R or X7R ceramic capacitors should be used.

When a ceramic capacitor is used at the input, and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the V_{IN} pin. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, the ringing at the input can be large enough to damage the part.

Since the ESR of a ceramic capacitor is so low, the input and output capacitor must instead fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation components and the output capacitor size. Typically, three to four cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop, V_{DROOP}, is usually about two to three times the linear drop of the first cycle. Thus, a good place to start is with the output capacitor size of approximately:

$$C_{OUT} \approx \frac{2.5 \bullet \Delta I_{OUT}}{f_{SW} \bullet V_{DROOP}}$$

More capacitance may be required depending on the duty cycle and load step requirements. In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is very low.

APPLICATIONS INFORMATION

Output Voltage Programming

The output voltage of V_{DDQ} is set by external resistive dividers. For example, V_{DDQ} can be set according to the following equation:

$$V_{DDQ} = 0.6V \bullet \left(1 + \frac{R1}{R2}\right)$$

The resistive divider allows pin V_{FB1} to sense a fraction of the output voltage as shown in Figure 3.

Pulse-Skipping Mode

V_{DDQ} pulse-skipping mode, which is a compromise between low output voltage ripple and efficiency, can be implemented by connecting the MODE/SYNC pin to SV_{IN}. In this condition, the peak inductor current is limited by the minimum on-time of the current comparator. The lowest output voltage ripple is achieved while still operating discontinuously. During very light output loads, pulse-skipping allows only a few switching cycles to skip while maintaining the output voltage in regulation.

Internal and External Compensation

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC load current. When a load step occurs, like the one shown in Figure 5, V_{OUT} shifts by an amount equal to ΔI_{LOAD} • ESR, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. The availability of the ITH pin allows the transient response to be optimized over a wide range of output capacitance.

The ITH1 external components (15.8k and 470pF) shown in Figure 3 will provide an adequate compensation as well as a starting point for most applications. The values can be modified slightly to optimize transient response once the final PCB layout is complete and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system. The external compensation, forced continuous operation circuit in the Typical Applications section uses faster compensation to improve load step response.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. More output capacitance may be required depending on the duty cycle and load step requirements.

If the ITH pin is tied to SV_{IN}, the internal compensation is selected.

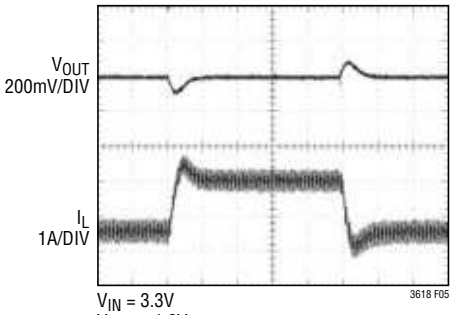


Figure 5. Load Step Transient in FCM with External Compensation

APPLICATIONS INFORMATION

Run and Soft-Start

The RUNx pins provide a means to shut down each channel of the LTC3618. Pulling both pins below 0.3V places the LTC3618 in a low quiescent current shutdown state (I_Q < 1µA).

After enabling the LTC3618 by bringing the RUNx pins above the threshold, the enabled channels enter a soft-start-up state. The type of soft-start behavior of V_{DDQ} is set by the TRACK/SS1 pin. The soft-start cycle begins with an initial discharge pulse pulling down the TRACK/SS1 pin to SGND and discharging the external capacitor C_{SS} (see Figure 3).

The initial discharge is adequate to discharge capacitors up to 33nF. If a larger capacitor is required, connect the external soft-start resistor R_{SS} to the RUN pin to fully discharge the capacitor.

1. Tying this pin to SV_{IN} selects the internal soft-start circuit for V_{DDQ} to the final value within 1ms.
2. If a longer soft-start period is desired, it can be set externally with a resistor and capacitor on the TRACK/SS1 pin as shown in Figure 3. The voltage applied at the TRACK/SS1 pin sets the value of the internal reference at V_{FB1} until TRACK/SS1 is pulled above 0.6V. The external soft-start duration can be calculated by using the following equation:

$$t_{SS1} = R_{SS} \bullet C_{SS} \bullet \ln\left(\frac{SV_{IN}}{SV_{IN} - 0.6V}\right)$$

3. The TRACK/SS1 pin can be used to track the output voltage of another supply.

   The VTTR voltage follows the soft-start behavior of V_{DDQ} at the same rate and ramps up V_{TT} output voltage. If RUN2 is pulled high later than RUN1, VTTR will follow its internal soft-start, and ramps output voltage of V_{TT} at a rate of approximately 850mV/ms.

   Regardless of either the internal or external soft-start state, the MODE/SYNC pin is ignored during start-up and defaults to pulse-skipping mode. In addition, the PGOOD pin is kept low, and the frequency foldback function is disabled.

Output Voltage Tracking Input

In the run state, the TRACK/SS1 pin can be used to track down/up the output voltage of another supply for V_{DDQ}. If $V_{TRACK/SS1}$ again drops below 0.6V, the LTC3618 enters the down-tracking state and V_{DDQ} is referenced to the TRACK/SS1 voltage. If $V_{TRACK/SS1}$ reaches 0.1V value the switching frequency is reduced by 4x to ensure that the minimum duty cycle limit does not prevent the output from following TRACK/SS1 pin. The run state will resume if $V_{TRACK/SS1}$ again exceeds 0.6V and V_{DDQ} is referenced to the internal reference.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as: Efficiency = 100% – (L1 + L2 + L3 + ...) where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: V_{IN} quiescent current and I^2R losses. The V_{IN} quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of little consequence.

1. The V_{IN} quiescent current is due to two components: the DC bias current as given in the Electrical Characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is the current out of V_{IN} due to gate charge, and it is typically larger than the DC bias current. Both the DC bias and gate charge losses are proportional to V_{IN}, thus, their effects will be more pronounced at higher supply voltages.

APPLICATIONS INFORMATION

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW}, and external inductor R_L. In continuous mode the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC), as follows:

$$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. To obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses, including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses, generally account for less than 2% of the total loss.

Thermal Considerations

In most applications, the LTC3618 does not dissipate much heat due to its high efficiency. However, in applications where the LTC3618 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 160°C, all four power switches will be turned off and the SW node will become high impedance.

To prevent the LTC3618 from exceeding the maximum junction temperature, the user will need to do some thermal analysis to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_{RISE} = P_D \bullet \theta_{JA}$$

where P_D is the power dissipated by the regulator, and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature. The junction temperature, T_J, is given by:

$$T_J = T_A + T_{RISE}$$

where T_A is the ambient temperature.

As an example, consider this case: the LTC3618 is in dropout at an input voltage of 3.3V with a load current for each channel of 2A at an ambient temperature of 70°C. Assuming a 20°C rise in junction temperature, to 90°C, results in an $R_{DS(ON)}$ of 0.086Ω (see the graph in the Typical Performance Characteristics section). Therefore, the power dissipated by the part is:

$$P_D = (I_1^2 + I_2^2) \bullet R_{DS(ON)} = 0.69W$$

For the QFN package, the θ_{JA} is 46.9°C/W.

Therefore, the junction temperature of the regulator operating at 70°C ambient temperature is approximately:

$$T_J = 0.69W \bullet 46.9°C/W + 70°C = 102.4°C$$

Note that for very low input voltage, the junction temperature will be higher due to increased switch resistance $R_{DS(ON)}$. It is not recommended to use full load current at high ambient temperature and low input voltage.

To maximize the thermal performance of the LTC3618, the exposed pad should be soldered to a ground plane. See the PC Board Layout Checklist.

Design Example

As a design example, consider using the LTC3618 in an application with the following specifications:

V_{IN} = 3.3V to 5.5V
V_{DDQ} = 1.8V
V_{TT} = 0.9V
$I_{OUT1(MAX)}$ = 3A
$I_{OUT2(MAX)}$ = 3A
$I_{OUT1(MIN)}$ = 200mA
f = 2.25MHz

First, calculate the timing resistor:

$$R_{RT} = \frac{4 \bullet 10^{11}\ \Omega \bullet Hz}{2.25MHz} = 178k$$

APPLICATIONS INFORMATION

Next, calculate the inductor values for approximately 1A ripple current at maximum V_{IN}:

$$L1 = \left(\frac{1.8V}{2.25MHz \bullet 1A}\right) \bullet \left(1 - \frac{1.8V}{5.5V}\right) = 0.54\mu H$$

$$L2 = \left(\frac{0.9V}{2.25MHz \bullet 1A}\right) \bullet \left(1 - \frac{0.9V}{5.5V}\right) = 0.33\mu H$$

Using a standard value of 0.45µH inductor for both channels results in maximum ripple currents of:

$$\Delta I_{L1} = \left(\frac{1.8V}{2.25MHz \bullet 0.45\mu H}\right) \bullet \left(1 - \frac{1.8V}{5.5V}\right) = 1.2A$$

$$\Delta I_{L2} = \left(\frac{0.9V}{2.25MHz \bullet 0.45\mu H}\right) \bullet \left(1 - \frac{0.9V}{5.5V}\right) = 0.71A$$

C_{OUT} will be selected based on the ESR that is required to satisfy the output voltage ripple requirement and the bulk capacitance needed for loop stability. For this design, 47µF ceramic capacitors will be used with X5R or X7R dielectric.

C_{IN} should be sized for a maximum current rating of:

$$I_{RMS(MAX)} = \frac{I_{OUT1}}{2} + \frac{I_{OUT2}}{2} = 2A_{RMS}$$

Decoupling the PV_{IN} with two 47µF X5R or X7R ceramic capacitors is adequate for most applications.

Finally, it is possible to define the soft-start up time choosing the proper value for the capacitor and the resistor connected to TRACK/SS1 pin. If one sets minimum T_{SS} = 5ms and a resistor of 4.7M, the following equation can be solved with the maximum SV_{IN} = 5.5V:

$$C_{SS} = \frac{5ms}{4.7M \bullet \ln\left(\frac{5.5V}{5.5V - 0.6V}\right)} = 9.2nF$$

The standard value of 10nF and 4.7M guarantees the minimum soft-start time of 5ms. In Figure 3, V_{DDQ} shows the schematic for this design example.

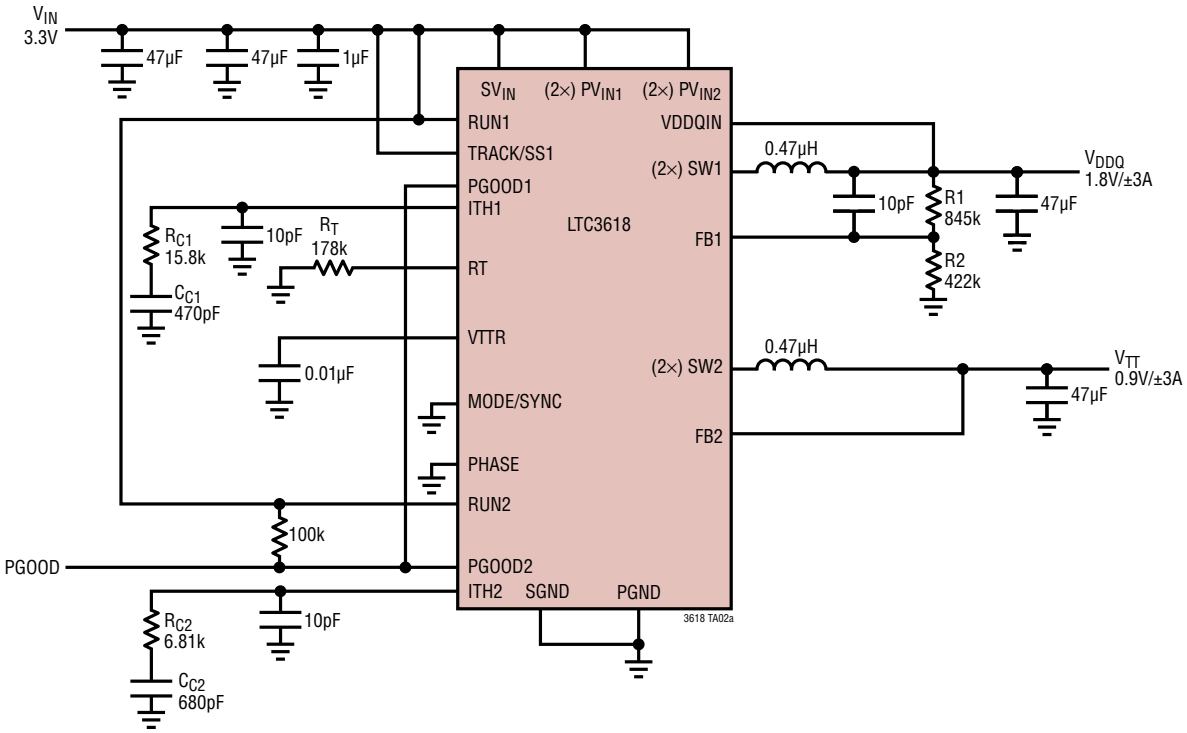
PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3618:

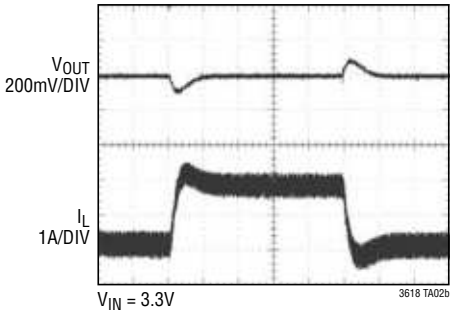
1. A ground plane is recommended. If a ground plane layer is not used, the signal and power grounds should be segregated with all small signal components returning to the SGND pin at one point which is then connected to the PGND node at the exposed pad close to the LTC3618.
2. Connect the (+) terminal of the input capacitors, C_{IN}, as close as possible to the PV_{INx} pins, and the (–) terminal as close as possible to the exposed pad PGND. This capacitor provides the AC current into the internal power MOSFETs.
3. Keep the switching nodes, SWx, away from all sensitive small signal nodes FBx, ITHx, RT.
4. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to PGND (exposed pad) for best performance.
5. Connect the V_{FBx} pins directly to the feedback resistors. The resistor divider must be connected between V_{OUTx} and SGND.

TYPICAL APPLICATIONS

External Compensation, Forced Continuous Operation, In-Phase Switching, Common PGOOD Output

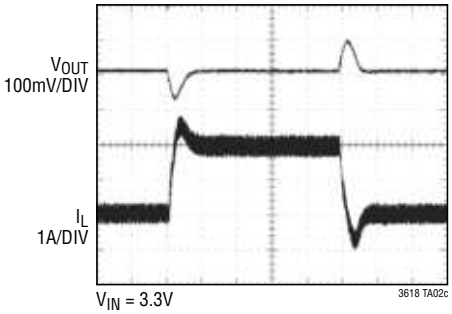


Load Step Transient V_{DDQ}



V_{IN} = 3.3V
V_{OUT} = 1.8V
I_{LOAD} = 200mA TO 2A

Load Step Transient V_{TT}

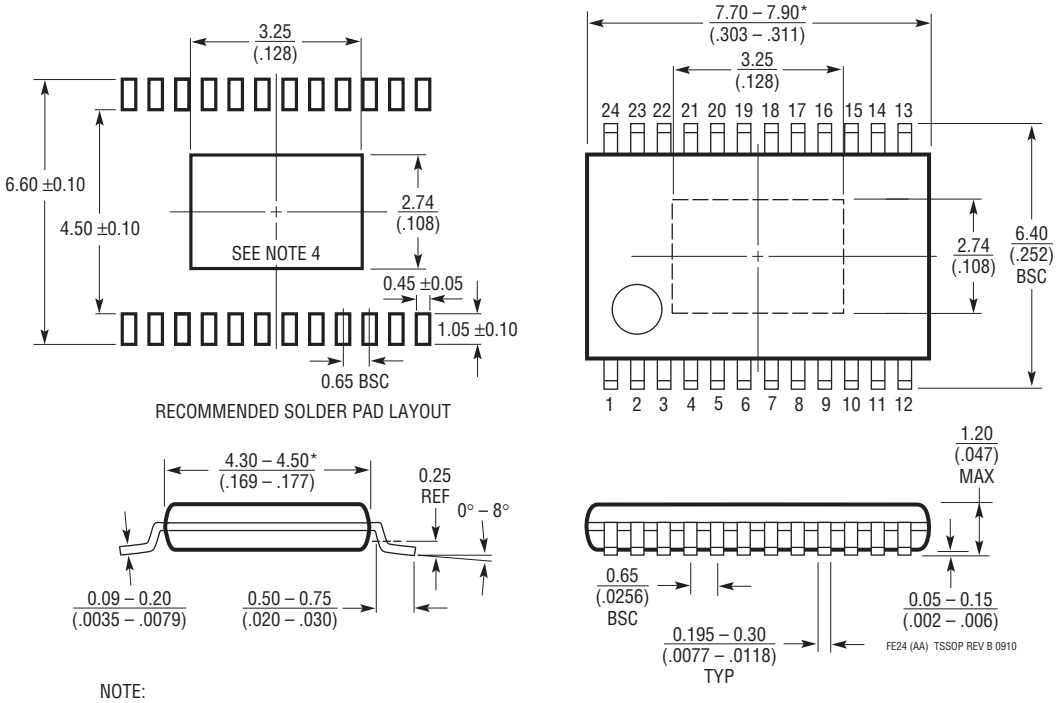


V_{IN} = 3.3V
V_{OUT2} = 0.9V
I_{LOAD} = –1A TO 1A

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

FE Package
24-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1771 Rev B)
Exposed Pad Variation AA

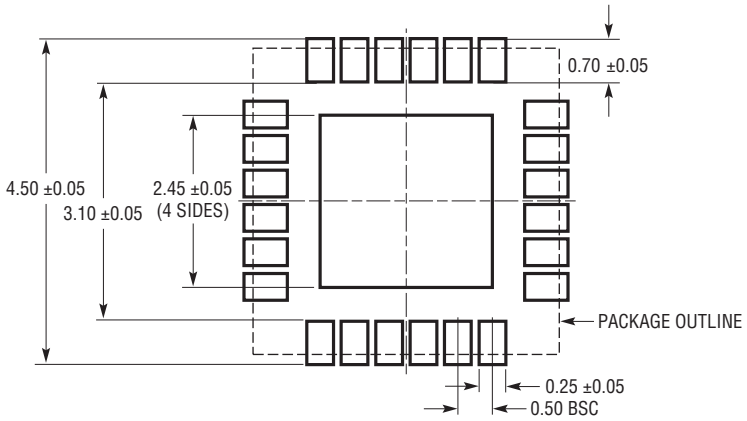


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

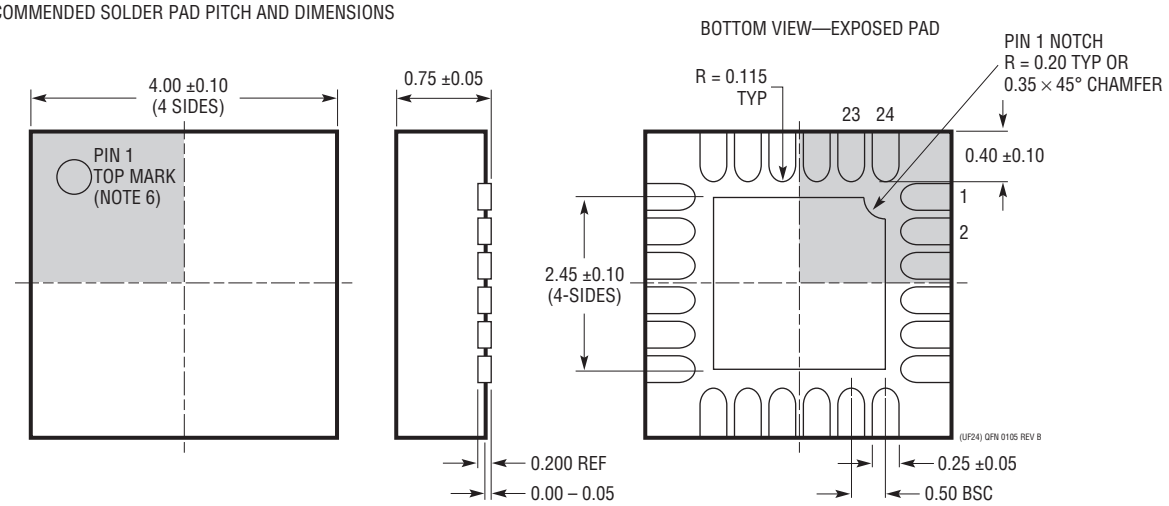
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

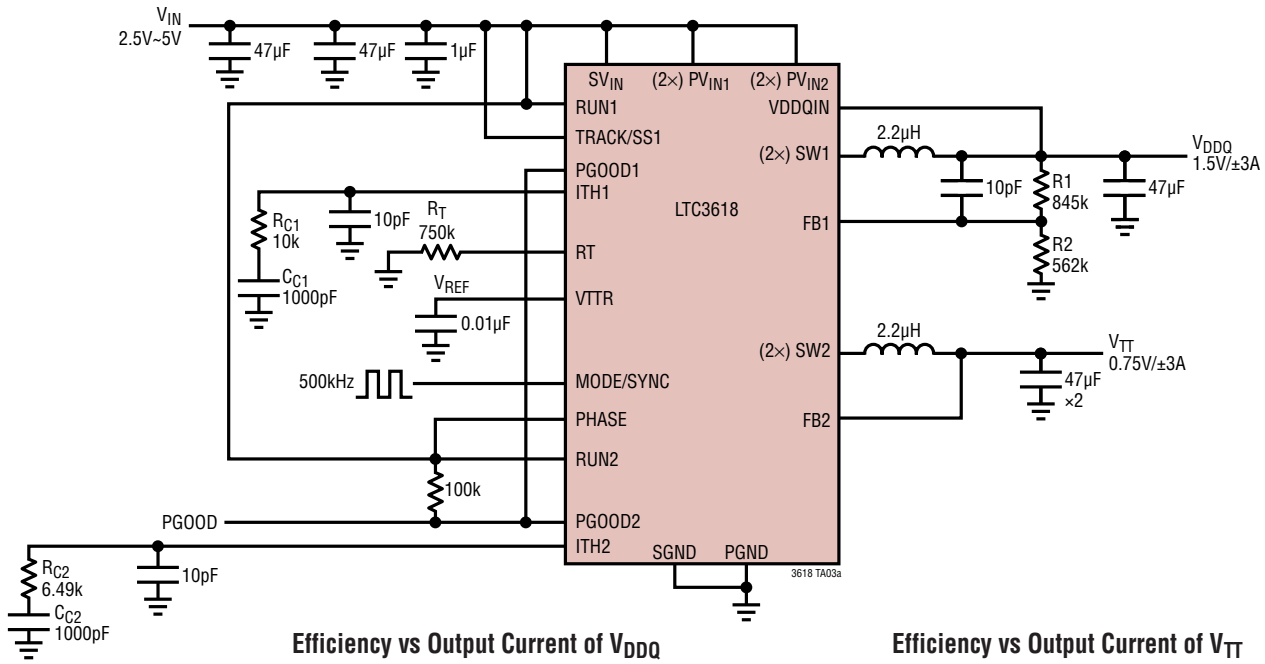
REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/11	Added DDR Power Supply, Termination and Reference to Features	1
		Added conditions to I_{LIMX} specification in Electrical Characteristics	3
		Removed Note 5	4
B	12/11	Inserted RUN1 Absolute Maximum Ratings	2
C	10/13	Modified Thermal Considerations section.	18

LINEAR TECHNOLOGY

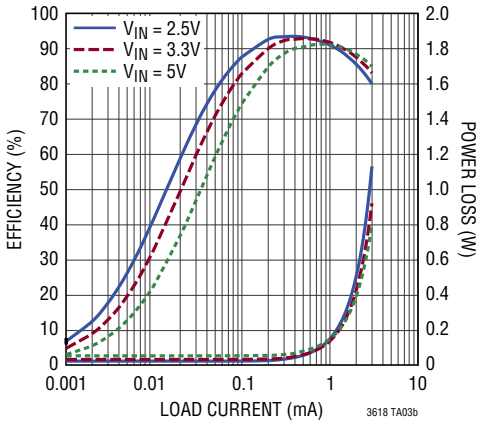
Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

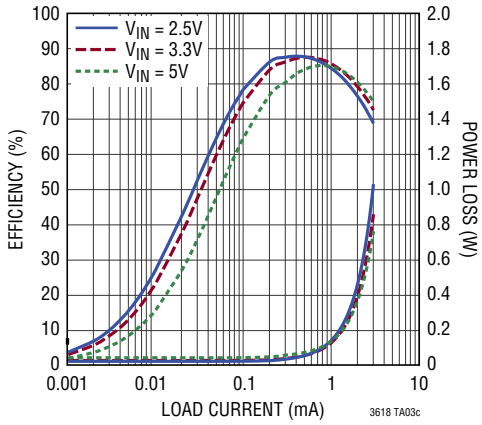
External Compensation, 500kHz Sync 180° Phasing



Efficiency vs Output Current of V_{DDQ}



Efficiency vs Output Current of V_{TT}



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3546	5.5V, Dual 3A/1A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 160µA, I_{SD} < 1µA, 4mm × 5mm QFN-28 Package
LTC3417A-2	5.5V, Dual 1.5A/1A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 125µA, I_{SD} < 1µA, TSSOP-16E and 3mm × 5mm DFN-16 Packages
LTC3612	5.5V, 3A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} < 1µA, 3mm × 4mm QFN-20 and TSSOP-20E Packages
LTC3614	5.5V, 4A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} < 1µA, 3mm × 4mm QFN-20 and TSSOP-20E Packages
LTC3616	5.5V, 6A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} < 1µA, 3mm × 5mm QFN-24 Package
LTC3617	±6A Monolithic Synchronous Buck for DDR Termination	Over 90% Efficiency, V_{IN}: 2.25V to 5.5V, 5k $V_{OUT(MIN)}$ = 0.5V, 3mm × 5mm QFN-24 Package

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