3-Phase, 600kHz, Synchronous Buck Switching Regulator Controller

FEATURES

- **3-Phase Current Mode Controller with Onboard MOSFET Drivers**
- **±5% Output Current Matching Optimizes Thermal Performance and Size of Inductors and MOSFETs**
- **±2% V_{REF} Accuracy Over Temperature Up to 140°C**
- Reduced Power Supply Induced Noise
- ±10% Power Good Output Indicator
- 225kHz to 680kHz Per Phase, PLL, Fixed Frequency
- PWM, Stage Shedding™ or Burst Mode® Operation
- OPTI-LOOP® Compensation Minimizes C_{OUT}
- Adjustable Soft-Start Current Ramping
- Short-Circuit Shutdown Timer with Defeat Option
- Overvoltage Soft Latch
- Adjustable Undervoltage Lockout Threshold
- Selectable Phase Output for Up to 12-Phase Operation
- Available in 36-Pin Narrow (0.209") SSOP and 5mm × 5mm QFN Packages

APPLICATIONS

- Automotive and Industrial Power Supplies
- High Output Current DC/DC Power Supplies

DESCRIPTION

The LTC®3731H is a PolyPhase® synchronous step-down switching regulator controller that drives all N-channel external power MOSFET stages in a phase-lockable fixed frequency architecture. The LTC3731H is rated for operation up to 140°C junction temperature. The 3-phase controller drives its output stages with 120° phase separation at frequencies up to 680kHz per phase to minimize the RMS current losses in both the input and output filter capacitors. The 3-phase technique effectively triples the fundamental frequency, improving transient response while operating each controller at an optimal frequency for efficiency and ease of thermal design. Light load efficiency is optimized by using a choice of output Stage Shedding or Burst Mode operation.

The precision reference supports output voltages from 0.6V to 6V. Current foldback provides protection for the external MOSFETs under short-circuit or overload conditions. Please refer to the LTC3731 data sheet for 0°C to 70°C and –40°C to 85°C rated versions.

LT, LTC, LTM, Linear Technology, the Linear logo, Burst Mode, OPTI-LOOP and PolyPhase are registered trademarks and Stage Shedding is a trademark of Linear Technology Corporation. All other trademarks are the property of their respective owners. Protected by U.S. Patents including 5481178, 5929620, 6177787, 6144194, 6100678, 5408150, 6580258, 6462525, 6304066, 5705919.

TYPICAL APPLICATION

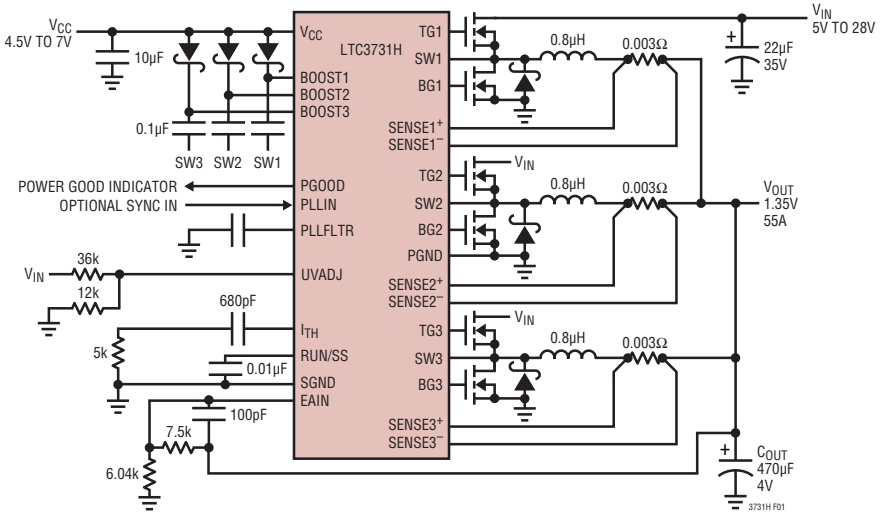
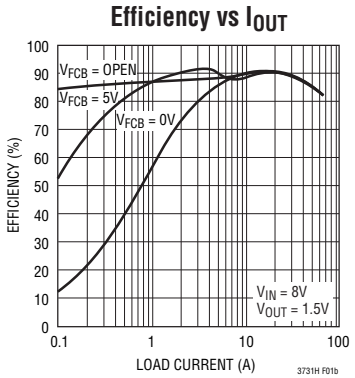


Figure 1. High Current Triple Phase Step-Down Converter



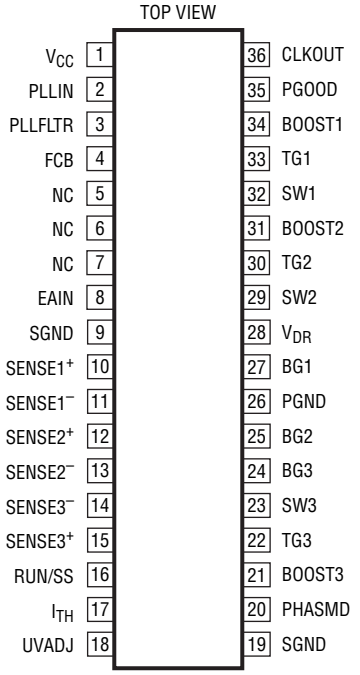
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Topside Driver Voltages ($BOOST_N$) ..... 38V to –0.3V
Switch Voltage (SW_N) ..... 32V to –5V
Boosted Driver Voltage ($BOOST_N$ – SW_N) .... 7V to –0.3V
Peak Output Current <1ms (TG_N, BG_N) 5A
Supply Voltages (V_{CC}, V_{DR}), PGOOD
Pin Voltage ..... 7V to –0.3V
RUN/SS, PLLFLTR, PLLIN, UVADJ,
FCB Voltages ..... V_{CC} to –0.3V

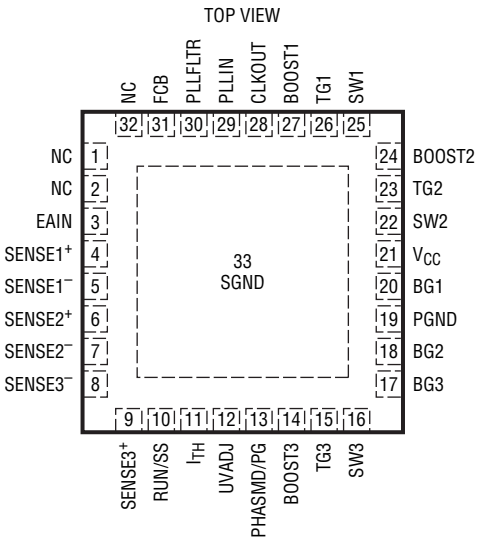
$SENSE^+$, $SENSE^-$ Voltages ..... 5.5V to –0.3V
I_{TH} Voltage ..... 2.4V to –0.3V
Operating Junction
Temperature Range (Note 2) ..... –40°C to 140°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature G Package (Soldering, 10sec) .. 300°C

PIN CONFIGURATION



G PACKAGE
36-LEAD PLASTIC SSOP

T_{JMAX} = 140°C, θ_{JA} = 70°C/W, θ_{JC} = 25°C/W
PINS 5 AND 6 CAN BE GROUNDED OR NC
PIN 7 MUST BE LEFT AS NC



UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W, θ_{JC} = 3°C/W
EXPOSED PAD (PIN 33) IS SGND, MUST BE SOLDERED TO PCB
PINS 1, 2 AND 32 MUST BE LEFT AS NC

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3731HG#PBF	LTC3731HG#TRPBF	LTC3731HG	36-Lead Plastic SSOP	–40°C to 140°C
LTC3731HUH#PBF	LTC3731HUH#TRPBF	3731	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 140°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = $V_{RUN/SS}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
$V_{REGULATED}$	Regulated Voltage at EAIN	V_{ITH} = 1.2V (Note 3)	 ●	0.594 0.590	0.600 0.600	0.606 0.614	V V
$V_{SENSEMAX}$	Maximum Current Sense Threshold	V_{EAIN} = 0.5V, V_{ITH} Open, V_{SENSE1}^-, V_{SENSE2}^-, V_{SENSE3}^- = 0.6V, 1.8V	 ●	65 60	75 75	85 90	mV mV
I_{MATCH}	Maximum Current Threshold Match	Worst-Case Error at $V_{SENSEMAX}$		–5		5	%
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 3) Measured in Servo Loop, ΔI_{TH} Voltage = 1.2V to 0.7V Measured in Servo Loop, ΔI_{TH} Voltage = 1.2V to 2V	 ● ●		 0.1 –0.1	 0.7 –0.7	 % %
$V_{REFLNREG}$	Output Voltage Line Regulation	V_{CC} = 4.5V to 7V			0.03		%/V
g_m	Transconductance Amplifier g_m	I_{TH} = 1.2V, Sink/Source 25µA (Note 3)	●	3	5	7	mmho
g_{mOL}	Transconductance Amplifier GBW	I_{TH} = 1.2V (g_m • Z_L, Z_L = Series 1k – 100kΩ – 1nF)			3		MHz
V_{FCB}	Forced Continuous Threshold		●	0.54	0.60	0.66	V
I_{FCB}	FCB Bias Current	V_{FCB} = 0.65V			0.2	0.7	µA
$V_{BINHIBIT}$	Burst Inhibit Threshold	Measured at FCB Pin		V_{CC} – 1.5	V_{CC} – 0.7	V_{CC} – 0.3	V
UVR	Undervoltage RUN/SS Reset	V_{CC} Lowered Until the RUN/SS Pin is Pulled Low		3.3	3.8	4.5	V
UVADJ	Undervoltage Lockout Threshold			1.13	1.18	1.23	V
I_{UVADJ}	Undervoltage Bias Current	At UVADJ Threshold			0.2	50	nA
I_Q	Input DC Supply Current Normal Mode Shutdown	(Note 4) V_{CC} = 5V $V_{RUN/SS}$ = 0V			 2.3 50	 3.5 100	 mA µA
$I_{RUN/SS}$	Soft-Start Charge Current	$V_{RUN/SS}$ = 1.9V		–0.8	–1.5	–2.5	µA
$V_{RUN/SS}$	RUN/SS Pin ON Threshold	$V_{RUN/SS}$, Ramping Positive		1	1.5	1.9	V
$V_{RUN/SSARM}$	RUN/SS Pin Arming Threshold	$V_{RUN/SS}$, Ramping Positive Until Short-Circuit Latch-Off is Armed			3.8	4.5	V
$V_{RUN/SSLO}$	RUN/SS Pin Latch-Off Threshold	$V_{RUN/SS}$, Ramping Negative			3.2		V
I_{SCL}	RUN/SS Discharge Current	Soft-Short Condition V_{EAIN} = 0.375V, $V_{RUN/SS}$ = 4.5V		–5	–1.5		µA
I_{SDLHO}	Shutdown Latch Disable Current	V_{EAIN} = 0.375V, $V_{RUN/SS}$ = 4.5V			1.5	5	µA
I_{SENSE}	SENSE Pins Source Current	SENSE1+, SENSE1–, SENSE2+, SENSE2–, SENSE3+, SENSE3– All Equal 1.2V; Current at Each Pin			13	20	µA
DF_{MAX}	Maximum Duty Factor	In Dropout, $V_{SENSEMAX}$ ≤ 30mV		95	98.5		%
TG t_R, t_F	Top Gate Rise Time Top Gate Fall Time	C_{LOAD} = 3300pF C_{LOAD} = 3300pF			30 40	90 90	ns ns
BG t_R, t_F	Bottom Gate Rise Time Bottom Gate Fall Time	C_{LOAD} = 3300pF C_{LOAD} = 3300pF			30 20	90 90	ns ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	All Controllers, C_{LOAD} = 3300pF Each Driver			50		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	All Controllers, C_{LOAD} = 3300pF Each Driver			60		ns
$t_{ON(MIN)}$	Minimum On-Time	Tested with a Square Wave (Note 5)			110		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = $V_{RUN/SS}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Good Output Indication							
V_{PGL}	PGOOD Voltage Output Low	I_{PGOOD} = 2mA, G Package I_{PGOOD} = 1.6mA, UH Package			0.1 0.5	0.3 1	V V
I_{PGOOD}	PGOOD Output Leakage	V_{PGOOD} = 5V				1	µA
$V_{PGTHNEG}$ $V_{PGTHPOS}$	PGOOD Trip Thresholds V_{EAIN} Ramping Negative V_{EAIN} Ramping Positive	V_{EAIN} with Respect to Set Output Voltage, PGOOD Goes Low After V_{UVDLY} Delay		 –7 7	 –10 10	 –13 13	 % %
V_{PGDLY}	Power Good Fault Report Delay	After V_{EAIN} is Forced Outside the PGOOD Thresholds			100	150	µs
Oscillator and Phase-Locked Loop							
f_{NOM}	Nominal Frequency	$V_{PLLFLTR}$ = 1.2V		360	400	440	kHz
f_{LOW}	Lowest Frequency	$V_{PLLFLTR}$ = 0V		190	225	260	kHz
f_{HIGH}	Highest Frequency	$V_{PLLFLTR}$ = 2.4V		600	680	750	kHz
V_{PLLTH}	PLLIN Input Threshold	Minimum Pulse Width > 100ns			1		V
R_{PLLIN}	PLLIN Input Resistance				50		kΩ
$I_{PLLFLTR}$	Phase Detector Output Current Sinking Capability Sourcing Capability	 $f_{PLLIN} < f_{OSC}$ $f_{PLLIN} > f_{OSC}$			 20 20		 µA µA
R_{RELPHS}	Controller 2-Controller 1 Phase Controller 3-Controller 1 Phase				120 240		Deg Deg
CLKOUT	Controller 1 TG to CLKOUT Phase	PHASMD = 0V PHASMD = 5V			30 60		Deg Deg

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3731H is guaranteed to meet specifications over the –40°C to 140°C operating junction temperature range. Note that the maximum ambient temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Junction temperature (T_J) is calculated from the ambient temperature T_A and power dissipation PD according to the following formula:

LTC3731HG: $T_J = T_A + (P_D \bullet 70°C/W)$

LTC3731HG: $T_J = T_{CASE} + (P_D \bullet 25°C/W)$

LTC3731HUH: $T_J = T_A + (P_D \bullet 34°C/W)$

High junction temperatures degrade operating lifetimes. Operating lifetime at junction temperatures greater than 125°C is derated to 1000 hours. The LTC3731H is tested under pulsed load conditions such that $T_J \approx T_A$.

Note 3: The IC is tested in a feedback loop that servoes the error amplifier output voltage to its midrange point (V_{ITH} = 1.2V).

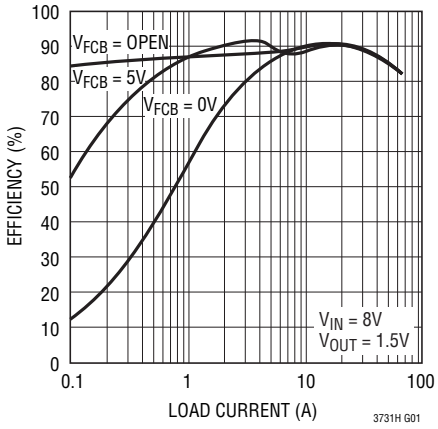
Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

Note 5: The minimum on-time condition corresponds to an inductor peak-to-peak ripple current of ≥40% of I_{MAX} (see minimum on-time considerations in the Applications Information Section).

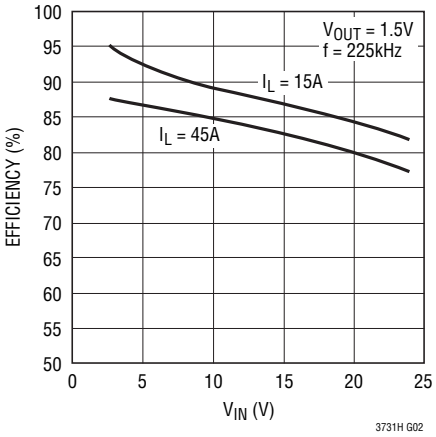
Note 6: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Overtemperature protection becomes active at a junction temperature greater than the maximum operating temperature. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS

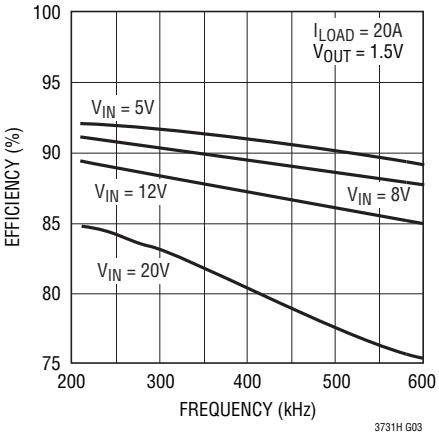
Efficiency vs I_{OUT} (Figure 14)



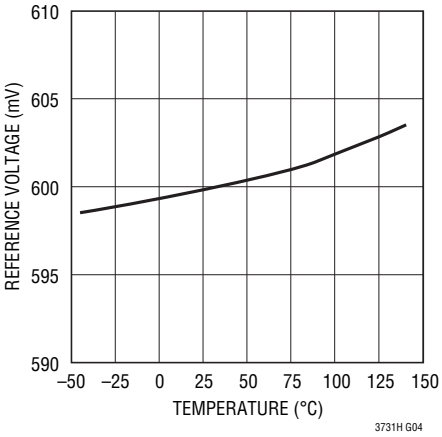
Efficiency vs V_{IN} (Figure 14)



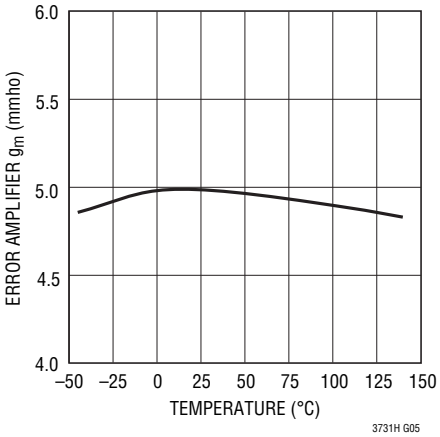
Efficiency vs Frequency (Figure 14)



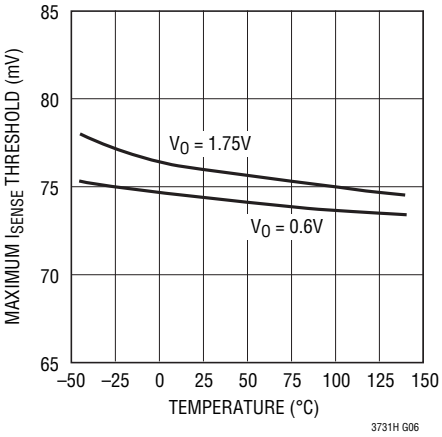
Reference Voltage vs Temperature



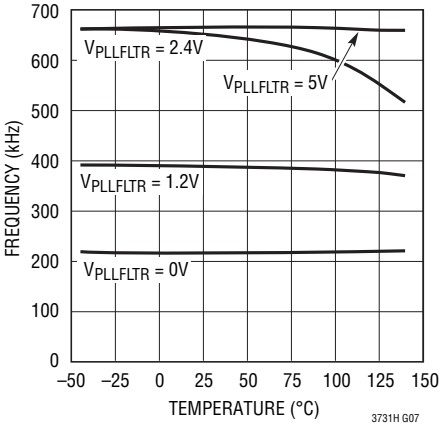
Error Amplifier g_m vs Temperature



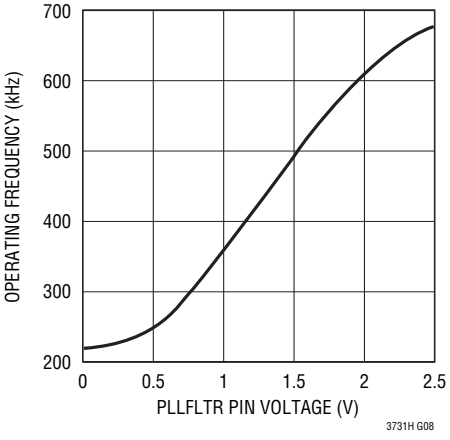
Maximum I_{SENSE} Threshold vs Temperature



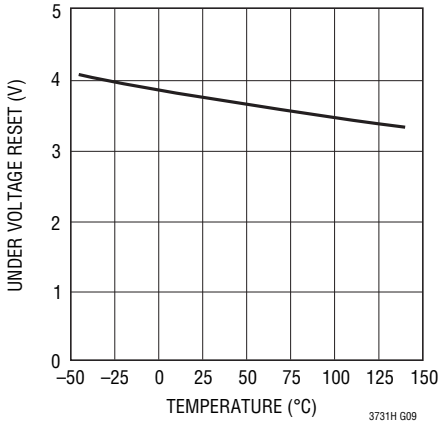
Oscillator Frequency vs Temperature



Operating Frequency vs $V_{PLLFLTR}$

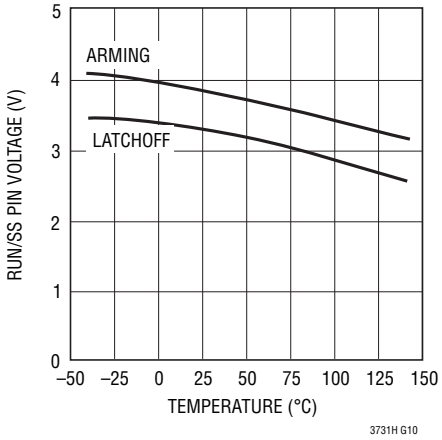


Undervoltage Reset Voltage vs Temperature



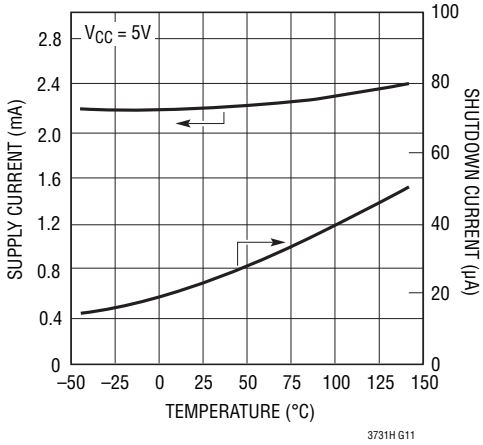
TYPICAL PERFORMANCE CHARACTERISTICS

Short-Circuit Arming and Latchoff vs Temperature



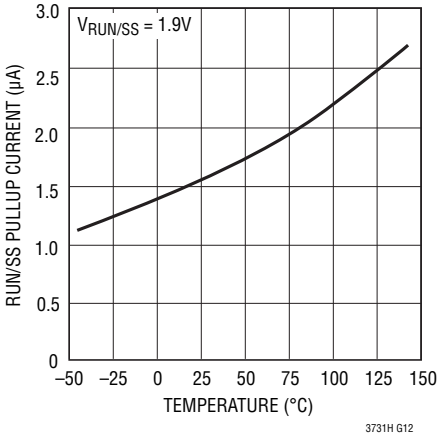
3731H G10

Supply Current vs Temperature



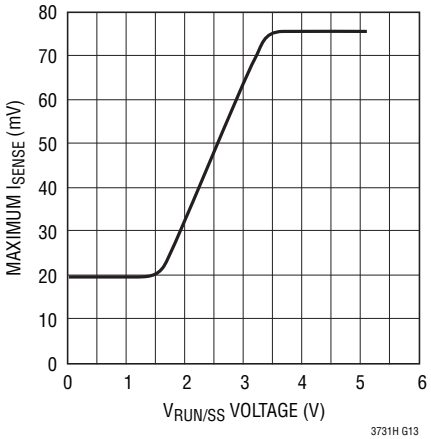
3731H G11

RUN/SS Pull-Up Current vs Temperature



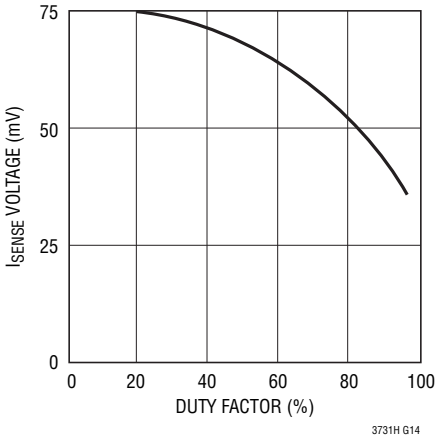
3731H G12

Maximum I_{SENSE} vs $V_{RUN/SS}$



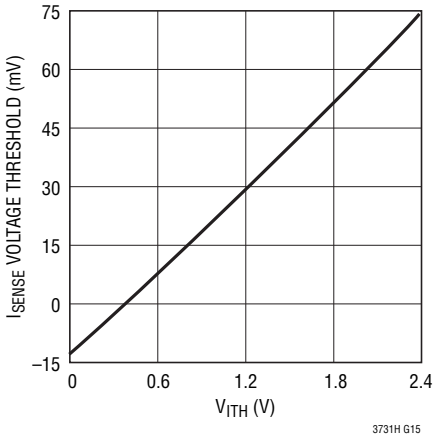
3731H G13

Maximum Current Sense Threshold vs Duty Factor



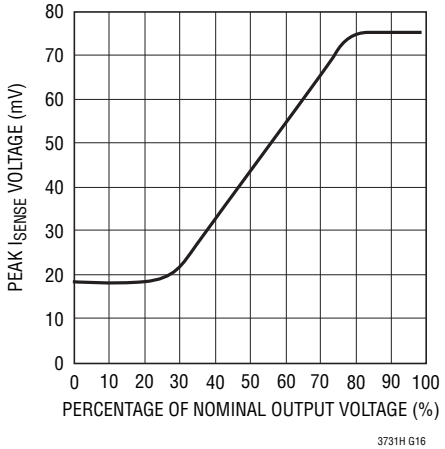
3731H G14

Peak Current Threshold vs V_{ITH}



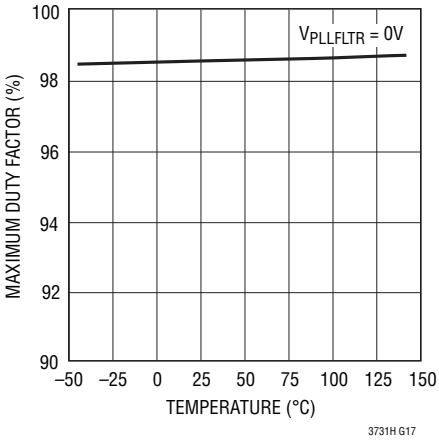
3731H G15

Percentage of Nominal Output vs Peak I_{SENSE} (Foldback)



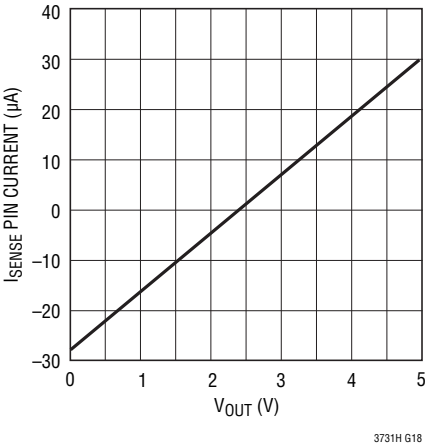
3731H G16

Maximum Duty Factor vs Temperature



3731H G17

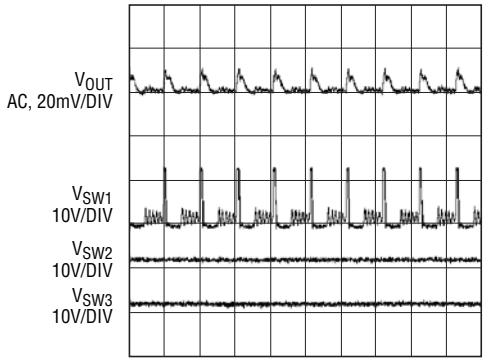
I_{SENSE} Pin Current vs V_{OUT}



3731H G18

TYPICAL PERFORMANCE CHARACTERISTICS

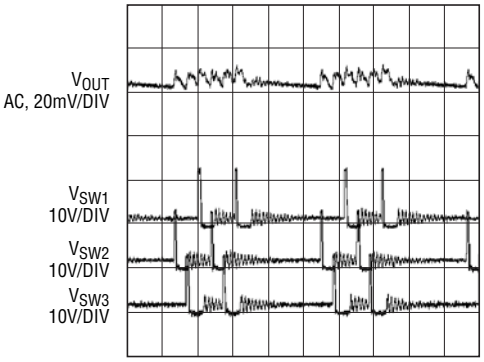
Shed Mode at 1 Amp, Light Load Current (Circuit of Figure 14)



V_{IN} = 12V 4µs/DIV
V_{OUT} = 1.5V
V_{FCB} = V_{CC}
FREQUENCY = 225kHz

3731H G20

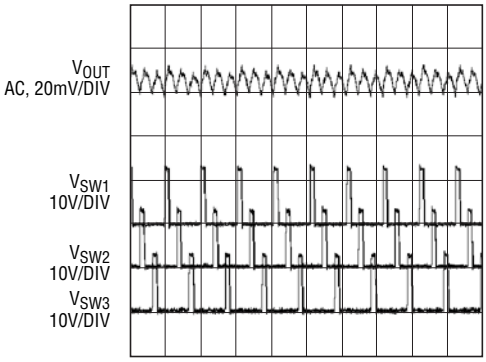
Burst Mode at 1 Amp, Light Load Current (Circuit of Figure 14)



V_{IN} = 12V 4µs/DIV
V_{OUT} = 1.5V
V_{FCB} = OPEN
FREQUENCY = 225kHz

3731H G21

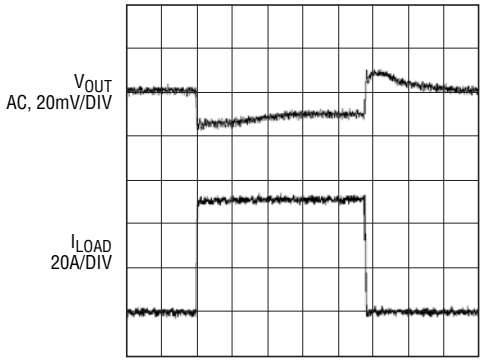
Continuous Mode at 1 Amp, Light Load Current (Circuit of Figure 14)



V_{IN} = 12V 4µs/DIV
V_{OUT} = 1.5V
V_{FCB} = 0V
FREQUENCY = 225kHz

3731H G22

Transient Load Current Response: 0 Amp to 50 Amp (Circuit of Figure 14)



V_{IN} = 12V 20µs/DIV
V_{OUT} = 1.5V
V_{FCB} = V_{CC}
FREQUENCY = 225kHz

3731H G23

PIN FUNCTIONS

BG1 to BG3: High Current Gate Drives for Bottom N-Channel MOSFETs. Voltage swing at these pins is from ground to V_{CC}.

BOOST1 to BOOST3: Positive Supply Pins to the Topside Floating Drivers. Bootstrapped capacitors, charged with external Schottky diodes and a boost voltage source, are connected between the BOOST and SW pins. Voltage swing at the BOOST pins is from boost source voltage (typically V_{CC}) to this boost source voltage + V_{IN} (where V_{IN} is the external MOSFET supply rail).

CLKOUT: Output clock signal available to synchronize other controller ICs for additional MOSFET stages/phases.

EAIN: This is the input to the error amplifier that compares the feedback voltage to the internal 0.6V reference voltage.

FCB: Forced Continuous Control Input. The voltage applied to this pin sets the operating mode of the controller. The forced continuous current mode is active when the applied voltage is less than 0.6V. Burst Mode operation will be active when the pin is allowed to float and a stage shedding mode will be active if the pin is tied to the V_{CC} pin. (Do not apply voltage directly to this pin prior to the application of voltage on the V_{CC} pin.)

PGOOD: This open-drain output is pulled low when the output voltage has been outside the PGOOD tolerance window for the V_{PGDLY} delay of approximately 100µs.

I_{TH}: Error Amplifier Output and Switching Regulator Compensation Point. All three current comparator's thresholds increase with this control voltage.

PGND: Driver Power Ground. This pin connects directly to the sources of the bottom N-channel external MOSFETs and the (–) terminals of C_{IN}.

PHASMD: This pin determines the phase shift between the first controller's rising TG signal and the rising edge of the CLKOUT signal. Logic 0 yields 30 degrees and logic 1 yields 60 degrees.

PLLIN: Synchronization Input to Phase Detector. This pin is internally terminated to SGND with 50kΩ. The phase-locked loop will force the rising top gate signal of controller 1 to be synchronized with the rising edge of the PLLIN signal.

PLLFLTR: The phase-locked loop's lowpass filter is tied to this pin. Alternatively, this pin can be driven with an AC or DC voltage source to vary the frequency of the internal oscillator. (Do not apply voltage directly to this pin prior to the application of voltage on the V_{CC} pin.)

RUN/SS: Combination of Soft-Start, Run Control Input and Short-Circuit Detection Timer. A capacitor to ground at this pin sets the ramp time to full current output as well as the time delay prior to an output voltage short-circuit shutdown. A minimum value of 0.01µF is recommended on this pin.

$SENSE1^+$, $SENSE2^+$, $SENSE3^+$, $SENSE1^-$, $SENSE2^-$, $SENSE3^-$: The Inputs to Each Differential Current Comparator. The I_{TH} pin voltage and built-in offsets between $SENSE^-$ and $SENSE^+$ pins, in conjunction with R_{SENSE}, set the current trip threshold level.

SGND: Signal Ground. This pin must be routed separately under the IC to the PGND pin and then to the main ground plane. The exposed pad in the UH package must be soldered to PCB ground for electrical contact and rated thermal performance.

SW1 to SW3: Switch Node Connections to Inductors. Voltage swing at these pins is from a Schottky diode (external) voltage drop below ground to V_{IN} (where V_{IN} is the external MOSFET supply rail).

TG1 to TG3: High Current Gate Drives for Top N-channel MOSFETs. These are the outputs of floating drivers with a voltage swing equal to the boost voltage source superimposed on the switch node voltage SW.

UVADJ: Input to the Undervoltage Shutdown Comparator. When the applied input voltage is less than 1.2V, this comparator turns off the output MOSFET driver stages and discharges the RUN/SS capacitor.

V_{CC}: Main Supply Pin. Because this pin supplies both the controller circuit power as well as the high power pulses supplied to drive the external MOSFET gates, this pin needs to be very carefully and closely decoupled to the IC's PGND pin.

VDR: Supplies power to the bottom gate drivers only. This pin needs to be very carefully and closely decoupled to the IC's PGND pin.

FUNCTIONAL DIAGRAM

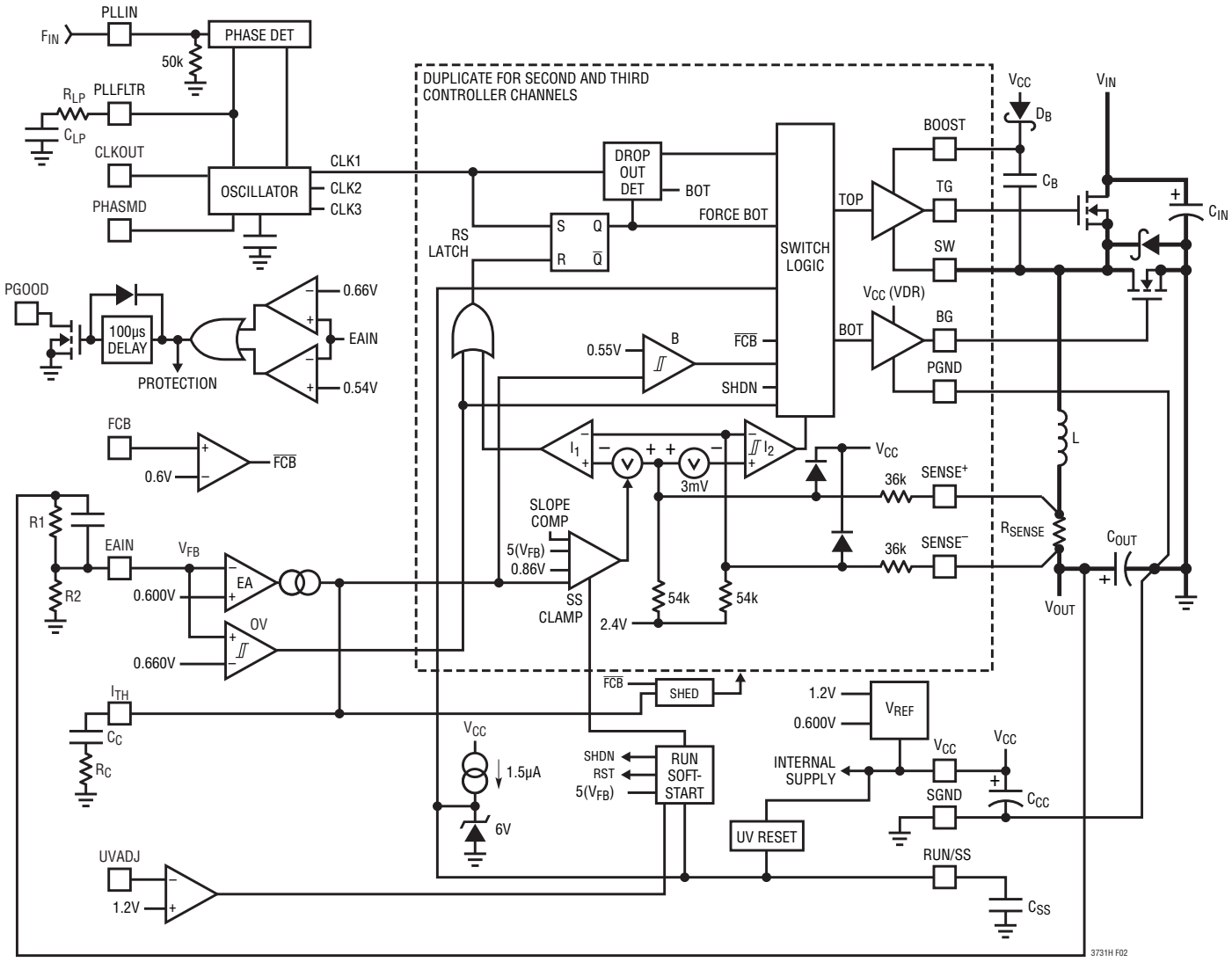


Figure 2

OPERATION (Refer to Functional Diagram)

Main Control Loop

The IC uses a constant frequency, current mode step-down architecture. During normal operation, each top MOSFET is turned on each cycle when the oscillator sets the RS latch, and turned off when the main current comparator, I_1, resets each RS latch. The peak inductor current at which I_1 resets the RS latch is controlled by the voltage on the I_{TH} pin, which is the output of the error amplifier EA. The EAIN pin receives a portion of output voltage feedback signal through the external resistive divider and is compared to the internal reference voltage. When the load current increases, it causes a slight decrease in the EAIN pin voltage relative to the 0.6V reference, which in turn causes the I_{TH} voltage to increase until each inductor's average current matches one third of the new load current (assuming all three current sensing resistors are equal). In Burst Mode operation and stage shedding mode, after each top MOSFET has turned off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by current comparator I_2, or the beginning of the next cycle.

The top MOSFET drivers are biased from floating bootstrap capacitor C_B, which is normally recharged through an external Schottky diode when the top FET is turned off. When V_{IN} decreases to a voltage close to V_{OUT}, however, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector counts the number of oscillator cycles that the bottom MOSFET remains off and periodically forces a brief on period to allow C_B to recharge.

The main control loop is shut down by pulling the RUN/SS pin low. Releasing RUN/SS allows an internal 1.5µA current source to charge soft-start capacitor C_{SS}. When C_{SS} reaches 1.5V, the main control loop is enabled and the internally buffered I_{TH} voltage is clamped but allowed to ramp as the voltage on C_{SS} continues to ramp. This "soft-start" clamping prevents abrupt current from being drawn from the input power source. When the RUN/SS pin is low, all functions are kept in a controlled state. The RUN/SS pin is pulled low when the supply input voltage is below 4V, when the undervoltage lockout pin (UVADJ) is below 1.2V, or when the IC die temperature rises above 160°C.

Low Current Operation

The FCB pin is a logic input to select between three modes of operation.

A) Burst Mode Operation

When the FCB pin voltage is below 0.6V, the controller performs as a continuous, PWM current mode synchronous switching regulator. The top and bottom MOSFETs are alternately turned on to maintain the output voltage independent of direction of inductor current. When the FCB pin is below V_{CC} – 1.5V but greater than 0.6V, the controller performs as a Burst Mode switching regulator. Burst Mode operation sets a minimum output current level before turning off the top switch and turns off the synchronous MOSFET(s) when the inductor current goes negative. This combination of requirements will, at low current, force the I_{TH} pin below a voltage threshold that will temporarily shut off both output MOSFETs until the output voltage drops slightly. There is a burst comparator having 60mV of hysteresis tied to the I_{TH} pin. This hysteresis results in output signals to the MOSFETs that turn them on for several cycles, followed by a variable "sleep" interval depending upon the load current. The resultant output voltage ripple is held to a very small value by having the hysteretic comparator after the error amplifier gain block.

B) Stage Shedding Operation

When the FCB pin is tied to the V_{CC} pin, Burst Mode operation is disabled and the forced minimum inductor current requirement is removed. This provides constant frequency, discontinuous current operation over the widest possible output current range. At approximately 10% of maximum designed load current, the second and third output stages are shut off and the phase 1 controller alone is active in discontinuous current mode. This "stage shedding" optimizes efficiency by eliminating the gate charging losses and switching losses of the other two output stages. Additional cycles will be skipped when the output load current drops below 1% of maximum designed load current in order to maintain the output voltage. This stage shedding operation is not as efficient as Burst Mode operation at very light loads, but does provide lower noise, constant frequency operating mode down to very light load conditions.

OPERATION (Refer to Functional Diagram)

C) Continuous Current Operation

Tying the FCB pin to ground will force continuous current operation. This is the least efficient operating mode, but may be desirable in certain applications. The output can source or sink current in this mode. When sinking current while in forced continuous operation, the controller will cause current to flow back into the input filter capacitor. If large enough, the input capacitor will prevent the input supply from boosting to unacceptably high levels; see C_{IN}/C_{OUT} selection in the Applications Information section.

Frequency Synchronization

The phase-locked loop allows the internal oscillator to be synchronized to an external source using the PLLIN pin. The output of the phase detector at the PLLFLTR pin is also the DC frequency control input of the oscillator, which operates over a 225kHz to 680kHz range corresponding to a voltage input from 0V to 2.4V. When locked, the PLL aligns the turn on of the top MOSFET to the rising edge of the synchronizing signal. When no frequency information is supplied to the PLLIN pin, PLLFLTR goes low, forcing the oscillator to minimum frequency. A DC source can be applied to the PLLFLTR pin to externally set the desired operating frequency. A discharge current of approximately 20µA will be present at the pin with no PLLIN input signal.

Input capacitance ESR requirements and efficiency losses are reduced substantially in a multiphase architecture because the peak current drawn from the input capacitor is effectively divided by the number of phases used and power loss is proportional to the RMS current squared. A 3-stage, single output voltage implementation can reduce input path power loss by 90%.

Power Good

The PGOOD pin is connected to the drain of an internal N-channel MOSFET. The MOSFET is turned on once an internal delay of about 100µs has elapsed and the output voltage has been away from its nominal value by greater than 10%. If the output returns to normal prior to the delay timeout, the timer is reset. There is no delay time for the rising of the PGOOD output once the output voltage is within the ±10% "window."

Phase Mode

The PHASMD pin determines the phase shift between the rising edge of the TG1 output and the rising edge of the CLKOUT signal. Grounding the pin will result in 30 degrees phase shift and tying the pin to V_{CC} will result in 60 degrees. These phase shift values enable extension to 6- and 12-phase systems. The PGOOD function above and the PHASMD function are tied to a common pin in the UH package.

Undervoltage Shutdown Adjust

The voltage applied to the UVADJ pin is compared to the internal 1.2V reference to have an externally programmable undervoltage shutdown. The RUN/SS pin is internally held low until the voltage applied to the UVADJ pin exceeds the 1.2V threshold.

Short-Circuit Detection

The RUN/SS capacitor is used initially to turn on and limit the inrush current from the input power source. Once the controllers have been given time, as determined by the capacitor on the RUN/SS pin, to charge up the output capacitors and provide full load current, the RUN/SS capacitor is then used as a short-circuit timeout circuit. If the output voltage falls to less than 70% of its nominal output voltage, the RUN/SS capacitor begins discharging, assuming that the output is in a severe overcurrent and/or short-circuit condition. If the condition lasts for a long enough period, as determined by the size of the RUN/SS capacitor, the controller will be shut down until the RUN/SS pin voltage is recycled. This built-in latchoff can be overridden by providing >5µA at a compliance of 3.8V to the RUN/SS pin. This additional current shortens the soft-start period but prevents net discharge of the RUN/SS capacitor during a severe overcurrent and/or short-circuit condition. Foldback current limiting is activated when the output voltage falls below 70% of its nominal level whether or not the short-circuit latchoff circuit is enabled. Foldback current limit can be overridden by clamping the EAIN pin such that the voltage is held above the (70%)(0.6V) or 0.42V level even when the actual output voltage is low. Up to 100µA of input current can safely be accommodated by the RUN/SS pin.

OPERATION (Refer to Functional Diagram)

Input Undervoltage Reset

The RUN/SS capacitor will be reset if the input voltage (V_{CC}) is allowed to fall below approximately 4V. The capacitor on the RUN/SS pin will be discharged until the short-circuit arming latch is disarmed. The RUN/SS capacitor will attempt to cycle through a normal soft-start ramp up after the V_{CC} supply rises above 4V. This circuit prevents power supply latchoff in the event of input power switching break-before-make situations. The PGOOD pin is held low during start-up until the RUN/SS capacitor rises above the short-circuit latchoff arming threshold of approximately 3.8V.

APPLICATIONS INFORMATION

The basic application circuit is shown in Figure 1 on the first page of this data sheet. External component selection is driven by the load requirement, and normally begins with the selection of an inductance value based upon the desired operating frequency, inductor current and output voltage ripple requirements. Once the inductors and operating frequency have been chosen, the current sensing resistors can be calculated. Next, the power MOSFETs and Schottky diodes are selected. Finally, C_{IN} and C_{OUT} are selected according to the voltage ripple requirements. The circuit shown in Figure 1 can be configured for operation up to a MOSFET supply voltage of 28V (limited by the external MOSFETs and possibly the minimum on-time).

Operating Frequency

The IC uses a constant frequency, phase-lockable architecture with the frequency determined by an internal capacitor. This capacitor is charged by a fixed current plus an additional current which is proportional to the voltage applied to the PLLFLTR pin. Refer to the Phase-Locked Loop and Frequency Synchronization section for additional information.

A graph for the voltage applied to the PLLFLTR pin versus frequency is given in Figure 3. As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations). The maximum switching frequency is approximately 680kHz.

Inductor Value Calculation and Output Ripple Current

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET gate charge and transition losses. In addition to this basic tradeoff, the effect of inductor value on ripple current and low current operation must also be considered. The PolyPhase approach reduces both input and output ripple currents while optimizing individual output stages to run at a lower fundamental frequency, enhancing efficiency.

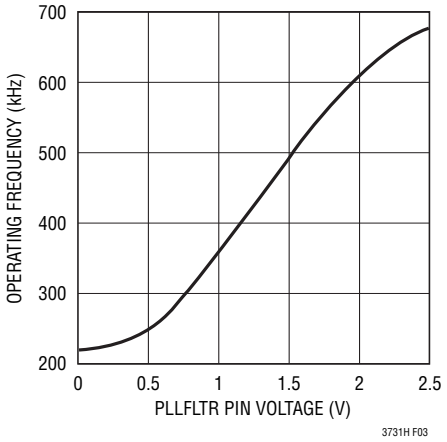


Figure 3. Operating Frequency vs $V_{PLLFLTR}$

The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L per individual section, N, decreases with higher inductance or frequency and increases with higher V_{IN} or V_{OUT}:

$$\Delta I_L = \frac{V_{OUT}}{fL}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

where f is the individual output stage operating frequency.

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In a PolyPhase converter, the net ripple current seen by the output capacitor is much smaller than the individual inductor ripple currents due to the ripple cancellation. The details on how to calculate the net output ripple current can be found in Application Note 77.

Figure 4 shows the net ripple current seen by the output capacitors for the different phase configurations. The output ripple current is plotted for a fixed output voltage as the duty factor is varied between 10% and 90% on the x-axis. The output ripple current is normalized against the inductor ripple current at zero duty factor. The graph can be used in place of tedious calculations. As shown in Figure 4, the zero output ripple current is obtained when:

$$\frac{V_{OUT}}{V_{IN}} = \frac{k}{N} \quad \text{where } k = 1, 2, ..., N-1$$

So the number of phases used can be selected to minimize the output ripple current and therefore the output ripple voltage at the given input and output voltages. In applications having a highly varying input voltage, additional phases will produce the best results.

Accepting larger values of ΔI_L allows the use of low inductances but can result in higher output voltage ripple. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4(I_{OUT})/N$, where N is the number of channels and I_{OUT} is the total load current. Remember, the maximum ΔI_L occurs at the maximum input voltage. The individual inductor ripple currents are constant determined by the input and output voltages, and the inductance.

Inductor Core Selection

Once the value for L1 to L3 is determined, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of ferrite, molypermalloy or Kool Mμ cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

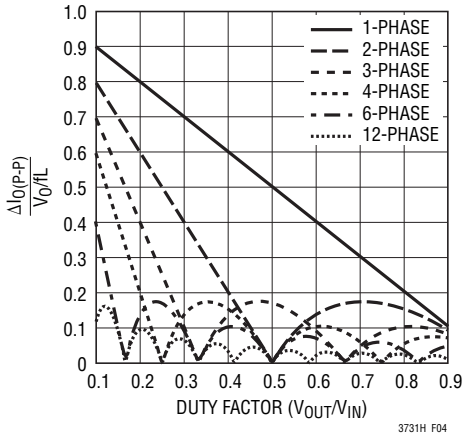


Figure 4. Normalized Peak Output Current vs Duty Factor [$I_{RMS} = 0.3(I_{O(P-P)}$]

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals cancon-centrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ. Toroids are very space efficient, especially when you can use several layers of wire. Because they lack a bobbin, mounting is more difficult. However, designs for surface mount are available which do not increase the height significantly.

Power MOSFET and D1, D2, D3 Selection

At least two external power MOSFETs must be selected for each of the three output sections: One N-channel MOSFET for the top (main) switch and one or more N-channel MOSFET(s) for the bottom (synchronous) switch. The number, type and on-resistance of all MOSFETs selected take into account the voltage step-down ratio as well as the actual position (main or synchronous) in which the MOSFET will be used. A much smaller and much lower input capacitance MOSFET should be used for the top

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MOSFET in applications that have an output voltage that is less than 1/3 of the input voltage. In applications where $V_{IN} >> V_{OUT}$, the top MOSFETs' on-resistance is normally less important for overall efficiency than its input capacitance at operating frequencies above 300kHz. MOSFET manufacturers have designed special purpose devices that provide reasonably low on-resistance with significantly reduced input capacitance for the main switch application in switching regulators.

The peak-to-peak MOSFET gate drive levels are set by the voltage, V_{CC}, requiring the use of logic-level threshold MOSFETs in most applications. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic-level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the on-resistance $R_{DS(ON)}$, input capacitance, input voltage and maximum output current.

MOSFET input capacitance is a combination of several components but can be taken from the typical "gate charge" curve included on most data sheets (Figure 5). The curve is generated by forcing a constant input current into the gate of a common source, current source loaded stage and then plotting the gate voltage versus time. The initial slope is the effect of the gate-to-source and the gate-to-drain capacitance. The flat portion of the curve is the result of the Miller multiplication effect of the drain-to-gate capacitance as the drain drops the voltage across the current source load. The upper sloping line is due to the drain-to-gate accumulation capacitance and the gate-to-source capacitance. The Miller charge (the increase in coulombs on the horizontal axis from a to b while the curve is flat) is specified for a given V_{DS} drain voltage, but can be adjusted for different V_{DS} voltages by multiplying by the ratio of the application V_{DS} to the curve specified V_{DS} values. A way to estimate the C_{MILLER} term is to take the change in gate charge from points a and b on a manufacturers data sheet and divide by the stated V_{DS} voltage specified. C_{MILLER} is the most important selection criteria for determining the transition loss term in the top MOSFET but is not directly specified on MOSFET data sheets. C_{RSS} and C_{OS} are specified sometimes but definitions of these parameters are not included.

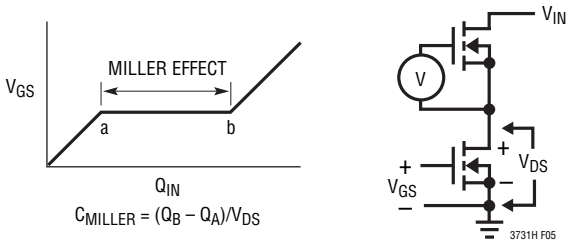


Figure 5. Gate Charge Characteristic

When the controller is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

The power dissipation for the main and synchronous MOSFETs at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}\left(\frac{I_{MAX}}{N}\right)^2(1+\delta)R_{DS(ON)} + V_{IN}{}^2\frac{I_{MAX}}{2N}(R_{DR})(C_{MILLER})\bullet\left[\frac{1}{V_{CC} - V_{TH(IL)}} + \frac{1}{V_{TH(IL)}}\right](f)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}\left(\frac{I_{MAX}}{N}\right)^2(1+\delta)R_{DS(ON)}$$

where N is the number of output stages, δ is the temperature dependency of $R_{DS(ON)}$, R_{DR} is the effective top driver resistance (approximately 2Ω at $V_{GS} = V_{MILLER}$), V_{IN} is the drain potential *and* the change in drain potential in the particular application. $V_{TH(IL)}$ is the data sheet specified typical gate threshold voltage specified in the power MOSFET data sheet at the specified drain current. C_{MILLER} is the calculated capacitance using the gate charge curve from the MOSFET data sheet and the technique described above.

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Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which peak at the highest input voltage. For V_{IN} < 12V, the high current efficiency generally improves with larger MOSFETs, while for V_{IN} > 12V, the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short circuit when the synchronous switch is on close to 100% of the period.

The term (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs.

The Schottky diodes (D1 to D3 in Figure 1) conduct during the dead time between the conduction of the two large power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on, storing charge during the dead time and requiring a reverse recovery period which could cost as much as several percent in efficiency. A 2A to 8A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition loss due to their larger junction capacitance.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of each top N-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. A low ESR input capacitor sized for the maximum RMS current must be used. The details of a close form equation can be found in Application Note 77. Figure 6 shows the input capacitor ripple current for different phase configurations with the output voltage fixed and input voltage varied. The input ripple current is normalized against the DC output current. The graph can be used in place of tedious calculations. The minimum input ripple current can be achieved when the product of phase number and output voltage, $N(V_{OUT})$, is approximately equal to the input voltage V_{IN} or:

$$\frac{V_{OUT}}{V_{IN}} = \frac{k}{N} \text{ where } k = 1, 2, ..., N-1$$

So the phase number can be chosen to minimize the input capacitor size for the given input and output voltages.

In the graph of Figure 4, the local maximum input RMS capacitor currents are reached when:

$$\frac{V_{OUT}}{V_{IN}} = \frac{2k-1}{N} \text{ where } k = 1, 2, ..., N$$

These worst-case conditions are commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the capacitor manufacturer if there is any question.

The Figure 6 graph shows that the peak RMS input current is reduced linearly, inversely proportional to the number N of stages used. It is important to note that the efficiency loss is proportional to the input RMS current squared and therefore a 3-stage implementation results in 90% less power loss when compared to a single phase design. Battery/input protection fuse resistance (if used), PC board trace and connector resistance losses are also reduced by the reduction of the input ripple current in a PolyPhase system. The required amount of input capacitance is further

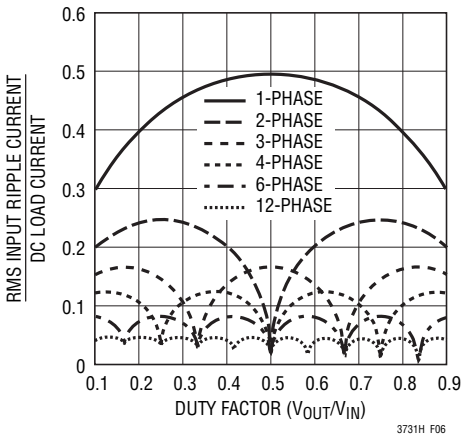


Figure 6. Normalized Input RMS Ripple Current vs Duty Factor for One to Six Output Stages

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reduced by the factor, N, due to the effective increase in the frequency of the current pulses.

Ceramic capacitors are becoming very popular for small designs but several cautions should be observed. "X7R", "X5R" and "Y5V" are examples of a few of the ceramic materials used as the dielectric layer, and these different dielectrics have very different effect on the capacitance value due to the voltage and temperature conditions applied. Physically, if the capacitance value changes due to applied voltage change, there is a concommitant piezo effect which results in radiating sound! A load that draws varying current at an audible rate may cause an attendant varying input voltage on a ceramic capacitor, resulting in an audible signal. A secondary issue relates to the energy flowing back into a ceramic capacitor whose capacitance value is being reduced by the increasing charge. The voltage can increase at a considerably higher rate than the constant current being supplied because the capacitance value is decreasing as the voltage is increasing! Nevertheless, ceramic capacitors, when properly selected and used, can provide the lowest overall loss due to their extremely low ESR.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically once the ESR requirement is satisfied the capacitance is adequate for filtering. The steady-state output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \approx \Delta I_{RIPPLE}\left(ESR + \frac{1}{8NfC_{OUT}}\right)$$

where f = operating frequency of each stage, N is the number of output stages, C_{OUT} = output capacitance and ΔI_L = ripple current in each inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. The output ripple will be less than 50mV at max V_{IN} with $\Delta I_L = 0.4I_{OUT(MAX)}$ assuming:

C_{OUT} required ESR < N • R_{SENSE}

and

$C_{OUT} > 1/(8Nf)(R_{SENSE})$

The emergence of very low ESR capacitors in small, surface mount packages makes very small physical implementations possible. The ability to externally compensate the switching regulator loop using the I_{TH} pin allows a much wider selection of output capacitor types. The impedance characteristics of each capacitor type is significantly different than an ideal capacitor and therefore requires accurate modeling or bench evaluation during design.

Manufacturers such as Nichicon, Nippon Chemi-Con and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo and the Panasonic SP surface mount types have a good (ESR)(size) product. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. Ceramic capacitors from AVX, Taiyo Yuden, Murata and Tokin offer high capacitance value and very low ESR, especially applicable for low output voltage applications.

In surface mount applications, multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. New special polymer surface mount capacitors offer very low ESR also but have much lower capacitive density per unit volume. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. Several excellent choices are the AVX TPS, AVX TPSV, the KEMET T510 series of surface-mount tantalums or the Panasonic SP series of surface mount special polymer capacitors

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available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo POS-CAP, Sanyo OS-CON, Nichicon PL series and Sprague 595D series. Consult the manufacturer for other specific recommendations.

R_{SENSE} Selection for Output Current

Once the frequency and inductor have been chosen, R_{SENSE1}, R_{SENSE2}, R_{SENSE3} are determined based on the required peak inductor current. The current comparator has a typical maximum threshold of 75mV/R_{SENSE} and an input common mode range of SGND to (1.1) • V_{CC}. The current comparator threshold sets the peak inductor current, yielding a maximum average output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current, ΔI_L.

Allowing a margin for variations in the IC and external component values yields:

$$R_{SENSE} = N\frac{50mV}{I_{MAX}}$$

The IC works well with values of R_{SENSE} from 0.002Ω to 0.02Ω.

V_{CC} Decoupling

The V_{CC} and V_{DR} pins supply power to the internal circuits of the controller and to the top and bottom gate drivers. Therefore, they must be bypassed very carefully to ground with ceramic capacitors, type X7R or X5R (depending upon the operating temperature environment) of *at least 1µF immediately next to the IC* and preferably an additional 10µF placed very close to the IC due to the extremely high instantaneous currents involved. The total capacitance, taking into account the voltage coefficient of ceramic capacitors, should be 100 times as large as the total combined gate charge capacitance of ALL of the MOSFETs being driven. Good bypassing close to the IC is necessary to supply the high transient currents required by the MOSFET gate drivers while keeping the 5V supply quiet enough so as not to disturb the very small-signal high bandwidth of the current comparators.

Topside MOSFET Driver Supply (C_B, D_B)

External bootstrap capacitors, C_B, connected to the BOOST pins, supply the gate drive voltages for the topside MOSFETs. Capacitor C_B in the Functional Diagram is charged though diode D_B from V_{CC} when the SW pin is low. When one of the topside MOSFETs turns on, the driver places the C_B voltage across the gate-source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply ($V_{BOOST} = V_{CC} + V_{IN}$). The value of the boost capacitor C_B needs to be 30 to 100 times that of the total gate charge capacitance of the topside MOSFET(s) as specified on the manufacturer's data sheet. The reverse breakdown of D_B must be greater than $V_{IN(MAX)}$.

The output voltage is set by an external resistive divider according to the following formula:

$$V_{OUT} = 0.6V\left(1+\frac{R1}{R2}\right)$$

The resistive divider is connected to the output as shown in Figure 2.

Soft-Start/Run Function

The RUN/SS pin provides three functions: 1) ON/OFF, 2) soft-start and 3) a defeatable short-circuit latch off timer. Soft-start reduces the input power sources' surge currents by gradually increasing the controller's current limit (proportional to an internal buffered and clamped V_{ITH}). The latchoff timer prevents very short, extreme load transients from tripping the overcurrent latch. A small pull-up current (>5µA) supplied to the RUN/SS pin will prevent the overcurrent latch from operating. A maximum pull-up current of 200µA is allowed into the RUN/SS pin even though the voltage at the pin may exceed the absolute maximum rating for the pin. This is a result of the limited current and the internal protection circuit on the pin. The following explanation describes how this function operates.

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An internal 1.5µA current source charges up the C_{SS} capacitor. When the voltage on RUN/SS reaches 1.5V, the controller is permitted to start operating. As the voltage on RUN/SS increases from 1.5V to 3.5V, the internal current limit is increased from 20mV/R_{SENSE} to 75mV/R_{SENSE}. The output current limit ramps up slowly, taking an additional 1s/µF to reach full current. The output current thus ramps up slowly, eliminating the starting surge current required from the input power supply. If RUN/SS has been pulled all the way to ground, there is a delay before starting of approximately:

$$t_{DELAY} = \frac{1.5V}{1.5\mu A} C_{SS} = (1s/\mu F) C_{SS}$$

$$t_{IRAMP} = \frac{3V - 1.5V}{1.5\mu A} C_{SS} = (1s/\mu F) C_{SS}$$

By pulling the RUN/SS controller pin below 0.4V the IC is put into low current shutdown (I_Q < 100µA). The RUN/SS pin can be driven directly from logic as shown in Figure 7. Diode, D1, in Figure 7 reduces the start delay but allows C_{SS} to ramp up slowly, providing the soft-start function. The RUN/SS pin has an internal 6V Zener clamp (see the Functional Diagram).

Fault Conditions: Overcurrent Latchoff

The RUN/SS pins also provide the ability to latch off the controllers when an overcurrent condition is detected. The RUN/SS capacitor is used initially to turn on and limit the inrush current of all three output stages. After the controllers have been started and been given adequate time to charge up the output capacitor and provide full load current, the RUN/SS capacitor is used for a short-circuit timer. If the output voltage falls to less than 70% of its nominal value, the RUN/SS capacitor begins discharging on the assumption that the output is in an overcurrent condition. If the condition lasts for a long enough period, as determined by the size of the RUN/SS capacitor, the discharge current, and the circuit trip point, the controller will be shut down until the RUN/SS pin voltage is recycled. If the overload occurs during start-up, the time can be approximated by:

$$t_{LO1} >> (C_{SS} \bullet 0.6V)/(1.5\mu A) = 4 \bullet 10^5 (C_{SS})$$

If the overload occurs after start-up, the voltage on the RUN/SS capacitor will continue charging and will provide additional time before latching off:

$$t_{LO2} >> (C_{SS} \bullet 3V)/(1.5\mu A) = 2 \bullet 10^6 (C_{SS})$$

This built-in overcurrent latchoff can be overridden by providing a pull-up resistor to the RUN/SS pin from V_{CC} as shown in Figure 7. When V_{CC} is 5V, a 200k resistance will prevent the discharge of the RUN/SS capacitor during an overcurrent condition but also shortens the soft-start period, so a larger RUN/SS capacitor value may be required.

Why should you defeat overcurrent latchoff? During the prototyping stage of a design, there may be a problem with noise pick-up or poor layout causing the protection circuit to latch off the controller. Defeating this feature allows troubleshooting of the circuit and PC layout. The internal foldback current limiting still remains active, thereby protecting the power supply system from failure. A decision can be made after the design is complete whether to rely solely on foldback current limiting or to enable the latchoff feature by removing the pull-up resistor.

The value of the soft-start capacitor C_{SS} may need to be scaled with output current, output capacitance and load current characteristics. The minimum soft-start capacitance is given by:

$$C_{SS} > (C_{OUT})(V_{OUT})\ (10^{-4})\ (R_{SENSE})$$

The minimum recommended soft-start capacitor of C_{SS} = 0.1µF will be sufficient for most applications.

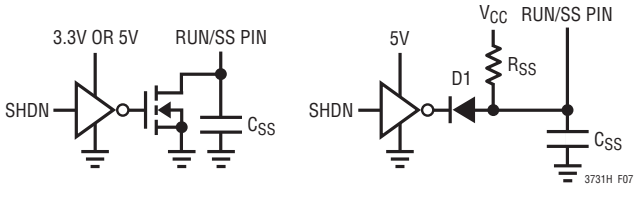


Figure 7. RUN/SS Pin Interfacing

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Current Foldback

In certain applications, it may be desirable to defeat the internal current foldback function. A negative impedance is experienced when powering a switching regulator. That is, the input current is higher at a lower V_{IN} and decreases as V_{IN} is increased. Current foldback is designed to accommodate a normal, resistive load having increasing current draw with increasing voltage. The EAIN pin should be artificially held 70% above its nominal operating level of 0.6V, or 0.42V in order to prevent the IC from "folding back" the peak current level. A suggested circuit is shown in Figure 8.

The emitter of Q1 will hold up the EAIN pin to a voltage in the absence of V_{OUT} that will prevent the internal sensing circuitry from reducing the peak output current. Removing the function in this manner eliminates the external MOSFET's protective feature under short-circuit conditions. This technique will also prevent the short-circuit latchoff function from turning off the part during a short-circuit event and the peak output current will only be limited to $N \bullet 75mV/R_{SENSE}$.

Undervoltage Reset

In the event that the input power source to the IC (V_{CC}) drops below 4V, the RUN/SS capacitor will be discharged to ground. When V_{CC} rises above 4V, the RUN/SS capacitor will be allowed to recharge and initiate another soft-start turn-on attempt. This may be useful in applications that switch between two supplies that are not diode connected, but note that this cannot make up for the resultant interruption of the regulated output.

Phase-Locked Loop and Frequency Synchronization

The IC has a phase-locked loop comprised of an internal voltage controlled oscillator and phase detector. This allows the top MOSFET of output stage 1's turn-on to be locked to the rising edge of an external source. The frequency range of the voltage controlled oscillator is ±50% around the center frequency f_O. A voltage applied to the PLLFLTR pin of 1.2V corresponds to a frequency of approximately 400kHz. The nominal operating frequency range of the IC is 225kHz to 680kHz.

The phase detector used is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector will not lock the internal oscillator to harmonics of the input frequency. The PLL hold-in range, Δf_H, is equal to the capture range, Δf_C:

$$\Delta f_H = \Delta f_C = \pm 0.5\ f_O$$

The output of the phase detector is a complementary pair of current sources charging or discharging the external filter components on the PLLFLTR pin. A simplified block diagram is shown in Figure 9.

If the external frequency (f_{PLLIN}) is greater than the oscillator frequency, f_{OSC}, current is sourced continuously, pulling up the PLLFLTR pin. When the external frequency is less than f_{OSC}, current is sunk continuously, pulling down

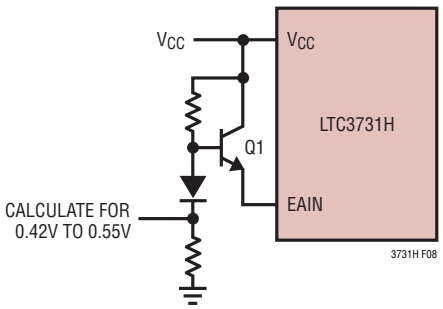


Figure 8. Foldback Current Elimination

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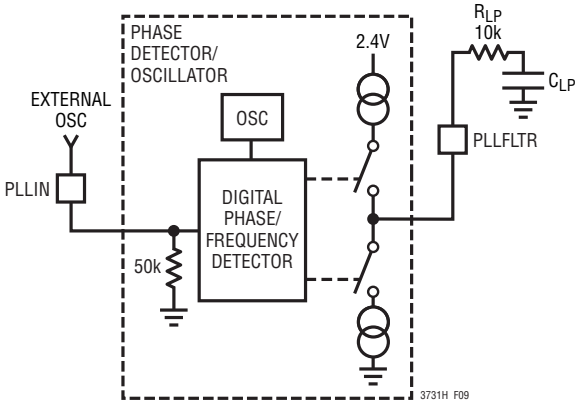


Figure 9. Phase-Locked Loop Block Diagram

the PLLFLTR pin. If the external and internal frequencies are the same, but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. Thus, the voltage on the PLLFLTR pin is adjusted until the phase and frequency of the external and internal oscillators are identical. At this stable operating point, the phase comparator output is open and the filter capacitor C_{LP} holds the voltage. The IC PLLIN pin must be driven from a low impedance source such as a logic gate located close to the pin. When using multiple ICs for a phase-locked system, the PLLFLTR pin of the master oscillator should be biased at a voltage that will guarantee the slave oscillator(s) ability to lock onto the master's frequency. A voltage of 1.7V or below applied to the master oscillator's PLLFLTR pin is recommended in order to meet this requirement. The resultant operating frequency will be approximately 550kHz for 1.7V.

The loop filter components (C_{LP}, R_{LP}) smooth out the current pulses from the phase detector and provide a stable input to the voltage controlled oscillator. The filter components C_{LP} and R_{LP} determine how fast the loop acquires lock. Typically R_{LP} =10k and C_{LP} ranges from 0.01µF to 0.1µF.

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the IC is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge of the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the IC will begin to skip every other cycle, resulting in half-frequency operation. The output voltage will continue to be regulated, but the ripple current and ripple voltage will increase.

The minimum on-time for the IC is generally about 110ns. However, as the peak sense voltage decreases the minimum on-time gradually increases. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

If an application can operate close to the minimum on-time limit, an inductor must be chosen that is low enough in value to provide sufficient ripple amplitude to meet the minimum on-time requirement. *As a general rule, keep the inductor ripple current for each channel equal to or greater than 30% of $I_{OUT(MAX)}$ at $V_{IN(MAX)}$.*

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Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%.

It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%\text{Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \bullet ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. **The availability of the I_{TH} pin not only allows optimization of control loop behavior, but also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response.** Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The I_{TH} external components shown in the Figure 1 circuit will provide an adequate starting point for most applications.

The I_{TH} series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.2 to 5 times their suggested values) to maximize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be decided upon because the various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 80% of full load current having a rise time of <2µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. The initial output voltage step, resulting from the step change in output current, may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the I_{TH} pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C. is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If C_{LOAD} is greater than 2% of C_{OUT}, the switch rise time should be controlled so that the load rise time is limited to approximately $1000 \bullet R_{SENSE} \bullet C_{LOAD}$. Thus a 250µF capacitor and a 2mΩ R_{SENSE} resistor would require a 500µs rise time, limiting the charging current to about 1A.

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Automotive Considerations: Plugging into the Cigarette Lighter

As battery-powered devices go mobile, there is a natural interest in plugging into the cigarette lighter in order to conserve or even recharge battery packs during operation. But before you connect, be advised: you are plugging into the supply from hell. The main battery line in an automobile is the source of a number of nasty potential transients, including load dump, reverse battery and double battery.

Load dump is the result of a loose battery cable. When the cable breaks connection, the field collapse in the alternator can cause a positive spike as high as 60V which takes several hundred milliseconds to decay. Reverse battery is just what it says, while double battery is a consequence of tow-truck operators finding that a 24V jump start cranks cold engines faster than 12V.

The network shown in Figure 10 is the most straightforward approach to protect a DC/DC converter from the ravages of an automotive battery line. The series diode prevents current from flowing during reverse battery, while the transient suppressor clamps the input voltage during load dump. Note that the transient suppressor should not conduct during double-battery operation, but must still clamp the input voltage below breakdown of the converter. Although the IC has a maximum input voltage of 32V on the SW pins, most applications will be limited to 30V by the MOSFET BV_{DSS}.

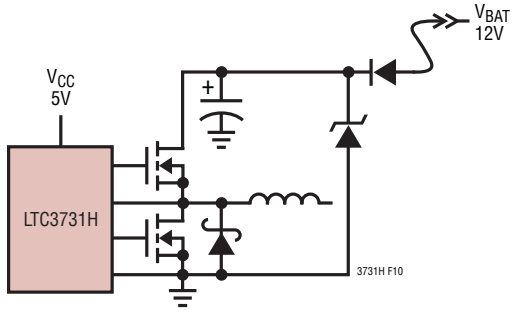


Figure 10. Automotive Application Protection

Design Example

As a design example, assume V_{CC} = 5V, V_{IN} = 12V(nominal), V_{IN} = 20V(max), V_{OUT} = 1.3V, I_{MAX} = 45A and f = 400kHz. The inductance value is chosen first based upon a 30% ripple current assumption. The highest value of ripple current in each output stage occurs at the maximum input voltage.

$$L = \frac{V_{OUT}}{f(\Delta I)}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

$$= \frac{1.3V}{(400kHz)(30\%)(15A)}\left(1-\frac{1.3V}{20V}\right)$$

$$\geq 0.68\mu H$$

Using L = 0.6µH, a commonly available value results in 34% ripple current. The worst-case output ripple for the three stages operating in parallel will be less than 11% of the peak output current.

R_{SENSE1}, R_{SENSE2} and R_{SENSE3} can be calculated by using a conservative maximum sense current threshold of 65mV and taking into account half of the ripple current:

$$R_{SENSE} = \frac{65mV}{15A\left(1+\frac{34\%}{2}\right)} = 0.0037\Omega$$

Use a commonly available 0.003Ω sense resistor.

Next verify the minimum on-time is not violated. The minimum on-time occurs at maximum V_{CC}:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)}(f)} = \frac{1.3V}{20V(400kHz)} = 162ns$$

The output voltage will be set by the resistive divider from the DIFFOUT pin to SGND, R1 and R2 in the Functional Diagram. Set R1 = 13.3k and R2 = 11.3k.

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The power dissipation on the topside MOSFET can be estimated. Using a Fairchild FDS6688 for example, $R_{DS(ON)}$ = 7mΩ, C_{MILLER} = 15nC/15V = 1000pF. At maximum input voltage with T(estimated) = 50°C:

$$P_{MAIN} \approx \frac{1.8V}{20V}(15)^2\left[1+(0.005)(50°C-25°C)\right]$$

$$0.007\Omega+(20)^2\left(\frac{45A}{(2)(3)}\right)(2\Omega)(1000pF)$$

$$\left(\frac{1}{5V-1.8V}+\frac{1}{1.8V}\right)(400kHz)=2.2W$$

The worst-case power dissipation by the synchronous MOSFET under normal operating conditions at elevated ambient temperature and estimated 50°C junction temperature rise is:

$$P_{SYNC}=\frac{20V-1.3V}{20V}(15A)^2(1.25)(0.007\Omega)=1.84W$$

A short circuit to ground will result in a folded back current of:

$$I_{SC} \approx \frac{25mV}{(2+3)m\Omega}+\frac{1}{2}\left(\frac{150ns(20V)}{0.6\mu H}\right)=7.5A$$

with a typical value of $R_{DS(ON)}$ and d = (0.005/°C)(50°C) = 0.25. The resulting power dissipated in the bottom MOSFET is:

$$P_{SYNC} = (7.5A)^2(1.25)(0.007\Omega) \approx 0.5W$$

which is less than one third of the normal, full load conditions. Incidentally, since the load no longer dissipates any power, total system power is decreased by over 90%. Therefore, the system actually cools significantly during a shorted condition!

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 11. Check the following in the PC layout:

1) Are the signal and power ground paths isolated? Keep the SGND at one end of a printed circuit path thus preventing MOSFET currents from traveling under the IC. The IC signal ground pin should be used to hook up all control circuitry on one side of the IC, routing the copper through SGND, under the IC covering the "shadow" of the package, connecting to the PGND pin and then continuing on to the (–) plates of C_{IN} and C_{OUT}. The V_{CC} decoupling capacitor should be placed immediately adjacent to the IC between the V_{CC} pin and PGND. A 1µF ceramic capacitor of the X7R or X5R type is small enough to fit very close to the IC to minimize the ill effects of the large current pulses drawn to drive the bottom MOSFETs. An additional 5µF to 10µF of ceramic, tantalum or other very low ESR capacitance is recommended in order to keep the internal IC supply quiet. The power ground returns to the sources of the bottom N-channel MOSFETs, anodes of the Schottky diodes and (–) plates of C_{IN}, which should have as short lead lengths as possible.

2) Does the V_{FB} pin connect directly to the feedback resistors? The resistive divider R1/R2 must be connected between the (+) plate of C_{OUT} and signal ground.

3) Are the $SENSE^-$ and $SENSE^+$ printed circuit traces for each channel routed together with minimum PC trace spacing? The filter capacitors between $SENSE^+$ and $SENSE^-$ for each channel should be as close as possible to the pins of the IC. Connect the $SENSE^-$ and $SENSE^+$ pins to the pads of the sense resistor as illustrated in Figure 12.

4) Do the (+) plates of C_{PWR} connect to the drains of the topside MOSFETs as closely as possible? This capacitor provides the pulsed current to the MOSFETs.

5) Keep the switching nodes, SWITCH, BOOST and TG away from sensitive small-signal nodes ($SENSE^+$, $SENSE^-$, EAIN). Ideally the SWITCH, BOOST and TG printed circuit traces should be routed away and separated from the IC and especially the "quiet" side of the IC. Separate the high dv/dt traces from sensitive small-signal nodes with ground traces or ground planes.

6) Use a low impedance source such as a logic gate to drive the PLLIN pin and keep the lead as short as possible.

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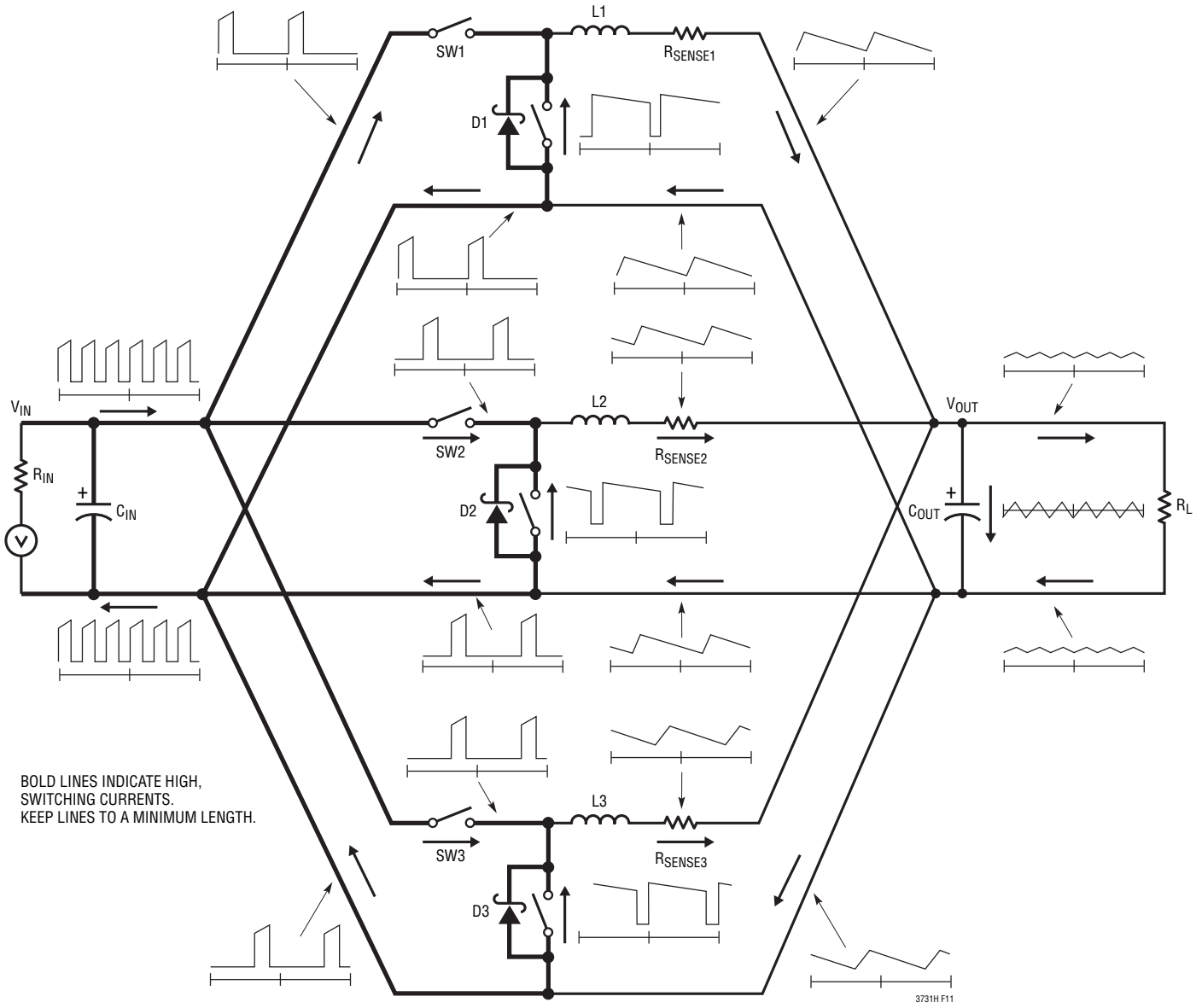


Figure 11. Branch Current Waveforms

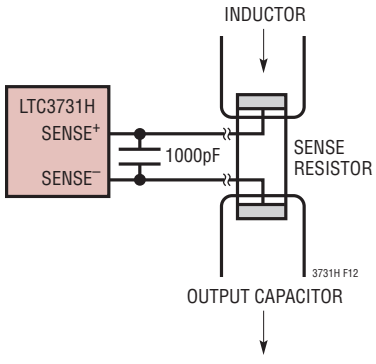


Figure 12. Kelvin Sensing R_{SENSE}

7) The 47pF to 330pF ceramic capacitor between the I_{TH} pin and signal ground should be placed as close as possible to the IC.

Figure 11 illustrates all branch currents in a three-phase switching regulator. It becomes very clear after studying the current waveforms why it is critical to keep the high switching current paths to a small physical size. High electric and magnetic fields will radiate from these "loops" just as radio stations transmit signals. The output capacitor ground should return to the negative terminal

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of the input capacitor and not share a common ground path with any switched current paths. The left half of the circuit gives rise to the "noise" generated by a switching regulator. The ground terminations of the synchronous MOSFETs and Schottky diodes should return to the bottom plate(s) of the input capacitor(s) with a short isolated PC trace since very high switched currents are present. A separate isolated path from the bottom plate(s) of the input and output capacitor(s) should be used to tie in the IC power ground pin (PGND). This technique keeps inherent signals generated by high current pulses taking alternate current paths that have finite impedances during the total period of the switching regulator. External OPTI-LOOP compensation allows overcompensation for PC layouts which are not optimized but this is not the recommended design procedure.

Simplified Visual Explanation of How a 3-Phase Controller Reduces Both Input and Output RMS Ripple Current

The effect of multiphase power supply design significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is divided by, and the effective ripple frequency is multiplied up by the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by, and the effective ripple frequency is increased by the number of phases used. Figure 13 graphically illustrates the principle.

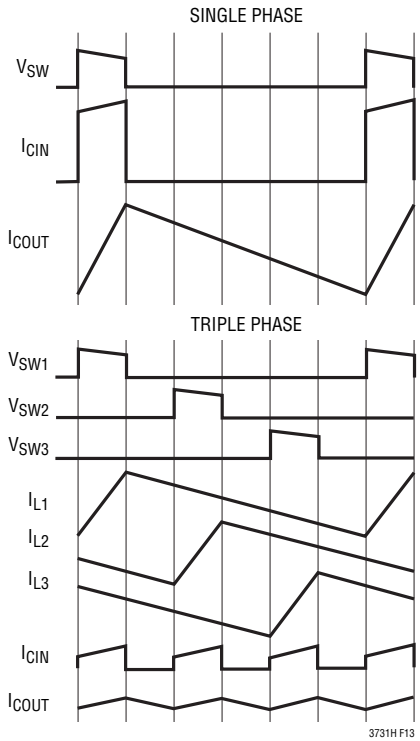


Figure 13. Single and Polyphase Current Waveforms

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The worst-case input RMS ripple current for a single stage design peaks at twice the value of the output voltage. The worst-case input RMS ripple current for a two stage design results in peaks at 1/4 and 3/4 of the input voltage, and the worst-case input RMS ripple current for a three stage design results in peaks at 1/6, 1/2, and 5/6 of the input voltage. The peaks, however, are at ever decreasing levels with the addition of more phases. A higher effective duty factor results because the duty factors "add" as long as the currents in each stage are balanced. Refer to AN19 for a detailed description of how to calculate RMS current for the single stage switching regulator.

Figure 6 illustrates the RMS input current drawn from the input capacitance versus the duty cycle as determined by the ratio of input and output voltage. The peak input RMS current level of the single phase system is reduced by 2/3 in a 3-phase solution due to the current splitting between the three stages.

The output ripple current is reduced significantly when compared to the single phase solution using the same inductance value because the V_{OUT}/L discharge currents term from the stages that has their bottom MOSFETs on subtract current from the $(V_{CC} – V_{OUT})/L$ charging current resulting from the stage which has its top MOSFET on. The output ripple current for a 3-phase design is:

$$I_{P-P} = \frac{V_{OUT}}{(f)(L)}(1-3DC) \quad V_{IN} > 3V_{OUT}$$

The ripple frequency is also increased by three, further reducing the required output capacitance when $V_{CC} < 3V_{OUT}$ as illustrated in Figure 6.

The addition of more phases, by phase locking additional controllers, always results in no net input or output ripple at V_{OUT}/V_{IN} ratios equal to the number of stages implemented. Designing a system with multiple stages close to the V_{OUT}/V_{IN} ratio will significantly reduce the ripple voltage at the input and outputs and thereby improve efficiency, physical size and heat generation of the overall switching power supply. Refer to Application Note 77 for more information on Polyphase circuits.

Efficiency Calculation

To estimate efficiency, the DC loss terms include the input and output capacitor ESR, each MOSFET $R_{DS(ON)}$, inductor resistance R_L, the sense resistance R_{SENSE} and the forward drop of the Schottky rectifier at the operating output current and temperature. Typical values for the design example given previously in this data sheet are:

Main MOSFET $R_{DS(ON)}$ = 7mΩ (9mΩ at 90°C)
Sync MOSFET $R_{DS(ON)}$ = 7mΩ (9mΩ at 90°C)
C_{INESR} = 20mΩ
C_{OUTESR} = 3mΩ
R_L = 2.5mΩ
R_{SENSE} = 3mΩ
$V_{SCHOTTKY}$ = 0.8V at 15A (0.7V at 90°C)
V_{OUT} = 1.3V
V_{IN} = 12V
I_{MAX} = 45A
δ = 0.5%°C (MOSFET temperature coefficient)
N = 3
f = 400kHz

The main MOSFET is on for the duty factor V_{OUT}/V_{IN} and the synchronous MOSFET is on for the rest of the period or simply $(1 – V_{OUT}/V_{IN})$. Assuming the ripple current is small, the AC loss in the inductor can be made small if a good quality inductor is chosen. The average current, I_{OUT}, is used to simplify the calculations. The equation below is not exact but should provide a good technique for the comparison of selected components and give a result that is within 10% to 20% of the final application. Determining the MOSFETs' die temperature may require iterative calculations if one is not familiar with typical performance. A maximum operating junction temperature of 90° to 100°C for the MOSFETs is recommended for high reliability applications.

Common output path DC loss:

$$P_{COMPATH} \approx N\left(\frac{I_{MAX}}{N}\right)^2 (R_L + R_{SENSE}) + C_{OUTESR}\ \text{Loss}$$

This totals 3.7W + C_{OUTESR} loss.

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Total of all three main MOSFETs' DC loss:

$$P_{MAIN} = N\left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{I_{MAX}}{N}\right)^2(1+\delta)R_{DS(ON)} + C_{INESR}\ \text{Loss}$$

This totals 0.87W + C_{INESR} loss (at 90°C).

Total of all three synchronous MOSFETs' DC loss:

$$P_{SYNC} = N\left(1-\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{I_{MAX}}{N}\right)^2(1+\delta)R_{DS(ON)}$$

This totals 7.2W at 90°C.

Total of all three main MOSFETs' AC loss:

$$P_{MAIN} \approx 3(V_{IN})^2\frac{45A}{(2)(3)}(2\Omega)(1000pF)$$

$$\left(\frac{1}{5V-1.8V}+\frac{1}{1.8V}\right)(400kHz) = 6.3W$$

This totals 1W at V_{IN} = 8V, 2.25W at V_{IN} = 12V and 6.25W at V_{IN} = 20V.

Total of all three synchronous MOSFETs' AC gate loss:

$$(3)Q_G\frac{V_{IN}}{V_{DSSPEC}}(f) = (6)(15nC)\frac{V_{IN}}{V_{DSSPEC}}(4E5)$$

This totals 0.08W at V_{IN} = 8V, 0.12W at V_{IN} = 12V and 0.19W at V_{IN} = 20V. The bottom MOSFET does not experience the Miller capacitance dissipation issue that the main switch does because the bottom switch turns on when its drain is close to ground.

The Schottky rectifier loss assuming 50ns nonoverlap time:

2 • 3(0.7V)(15A)(50ns)(4E5)

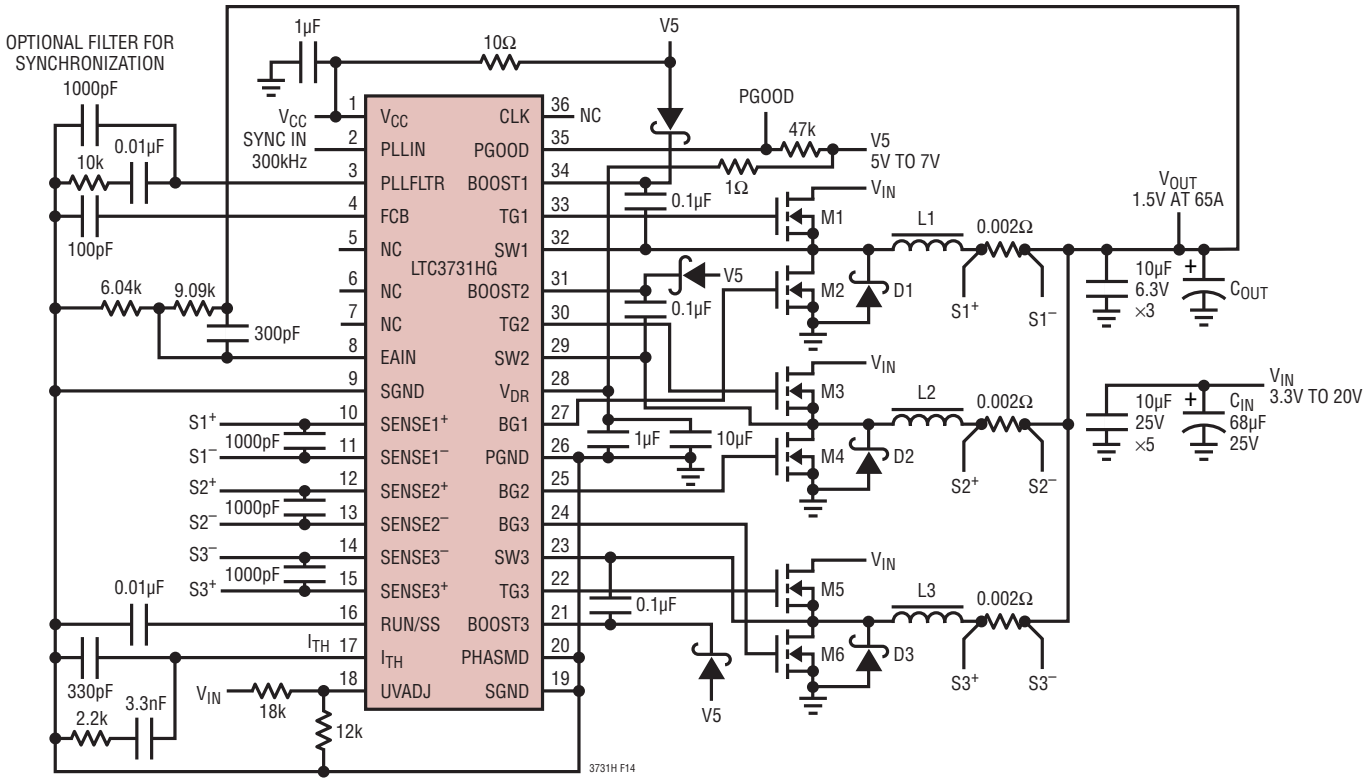
This totals 1.26W.

The total output power is (1.3V)(45A) = 58.5W and the total input power is approximately 60W so the % loss of each component is as follows:

Main switch's AC loss (V_{IN} = 12V)	2.25W	3.75%
Main switch's DC loss	0.87W	1.5%
Synchronous switch AC loss	0.19W	0.3%
Synchronous switch DC loss	7.2W	12%
Power path loss	3.7W	6.1%

The numbers above represent the values at V_{IN} = 12V. It can be seen from this simple example that two things can be done to improve efficiency: 1) Use two MOSFETs on the synchronous side and 2) use a smaller MOSFET for the main switch with smaller C_{MILLER} to better balance the AC loss with the DC loss. A smaller, less expensive MOSFET can actually perform better in the task of the main switch.

TYPICAL APPLICATIONS



V_{IN}: 3.3V TO 20V
V_{OUT}: 1.5V AT 65A
SWITCHING FREQUENCY: 300kHz

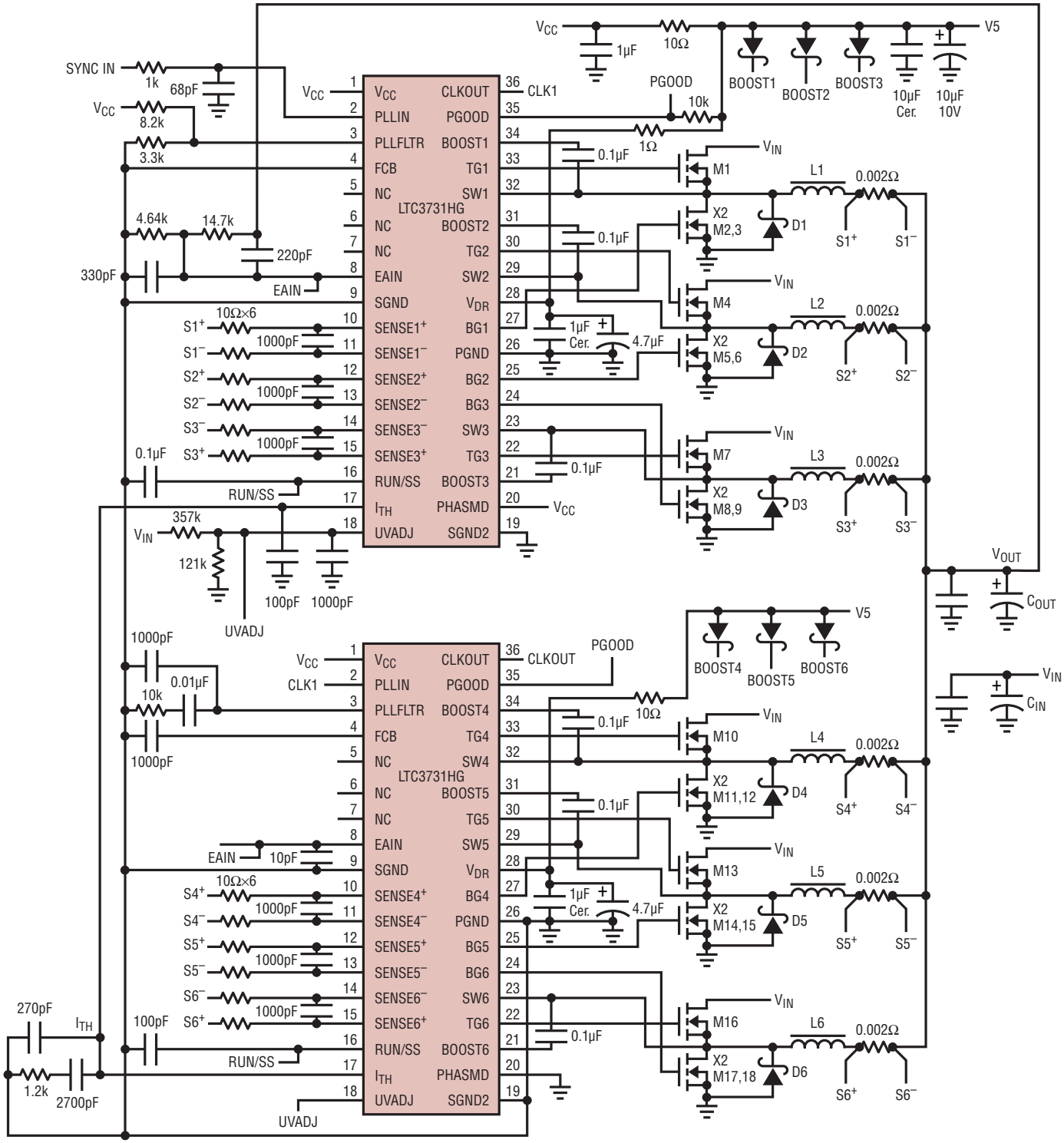
C_{IN}: SANYO OS-CON 25SP68M
C_{OUT}: 270µF/2V ×8 PANASONIC SP EEUE0D271R
OR 470µF/2.5V ×6 SANYO POSCAP 2R5 TPD470M
D1 TO D3: DIODES INC. B340A

L1 TO L3: 0.8µH SUMIDA CEP125-0R8
M1, M3, M5: IRF7821W ×2, Si7860DP
OR HAT2168 ×2
M2, M4, M6: IRF7832 ×2, Si7892DP ×2
OR HAT2165 ×2

Figure 14. 3-Phase 65A Power Supply

TYPICAL APPLICATIONS

2.5V/100A Power Supply



NOTES:
V5: 5V TO 7V
V_{IN}: 10V TO 14V; V_{OUT}: 2.5V/100A
SWITCHING FREQUENCY: 500kHz (V5 = 5V)

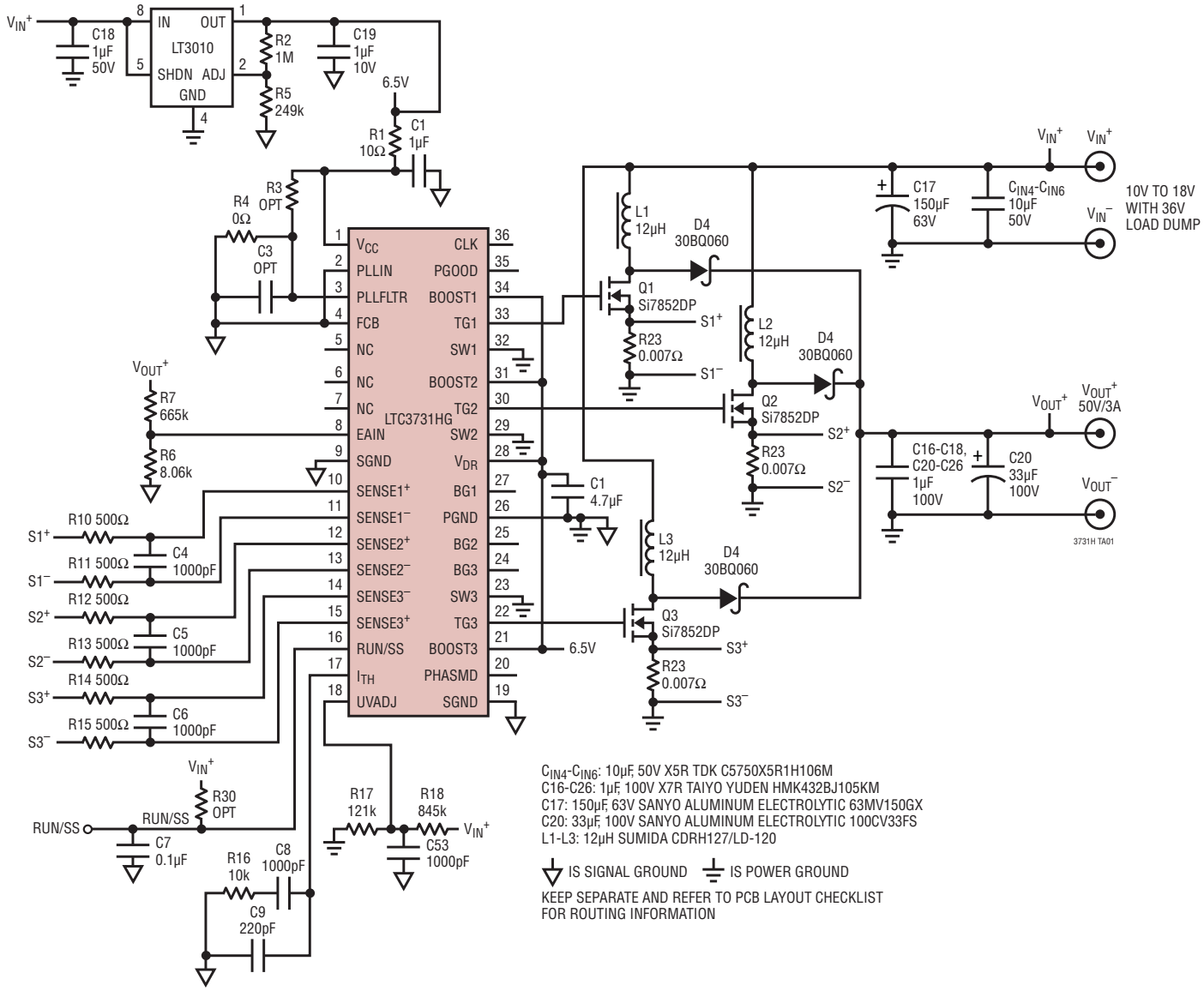
M1, M4, M7, M10, M13, M16:
SILICONIX Si7390DP OR HAT2168
M2, M3, M5, M6, M8, M9, M11, M12, M14, M15, M17, M18: SILICONIX Si7356DP OR HAT2165
D1 TO D6: B320A

L1 TO L6: TOKO FDH1040: 0.56µH
C_{IN}: 10µF/16V CERAMIC × 10 + 270µF/16V SANYO Os-Con
C_{OUT}: 100µF/6.3V/X5R × 10 + 330µF/4V × 8

3731H F15

TYPICAL APPLICATIONS

3-Phase Boost Converter. V_{IN} = 10V to 18V with 36V Load Dump, V_{OUT} = 50V at 3A



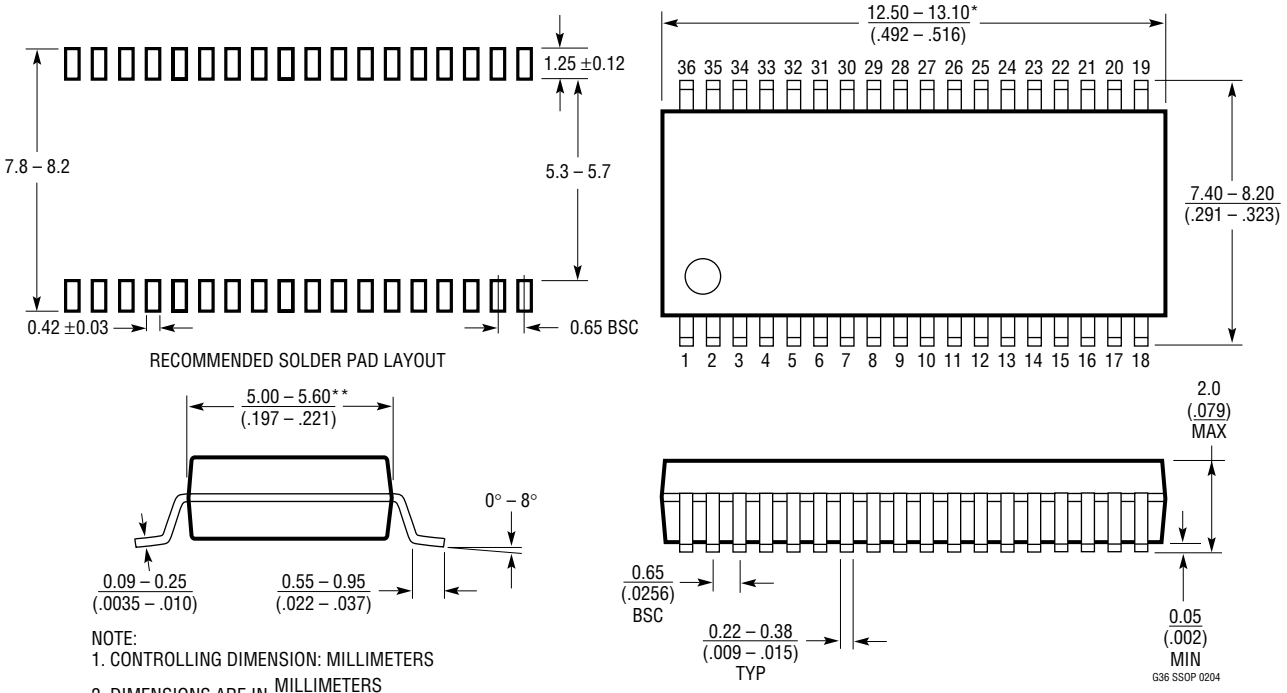
CIN4-CIN6: 10µF, 50V X5R TDK C5750X5R1H106M
C16-C26: 1µF, 100V X7R TAIYO YUDEN HMK432BJ105KM
C17: 150µF, 63V SANYO ALUMINUM ELECTROLYTIC 63MV150GX
C20: 33µF, 100V SANYO ALUMINUM ELECTROLYTIC 100CV33FS
L1-L3: 12µH SUMIDA CDRH127/LD-120

⏚ IS SIGNAL GROUND ⏚ IS POWER GROUND

KEEP SEPARATE AND REFER TO PCB LAYOUT CHECKLIST FOR ROUTING INFORMATION

PACKAGE DESCRIPTION

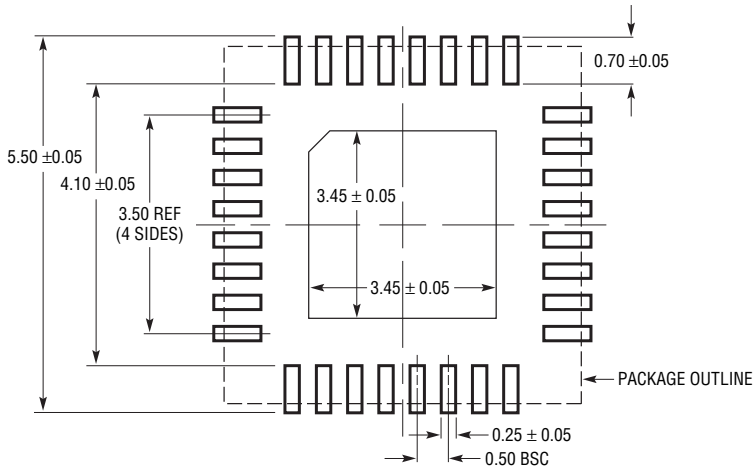
G Package
36-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



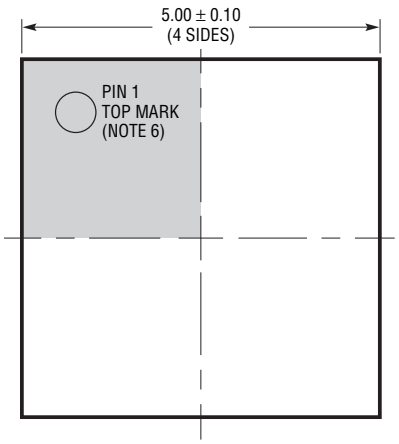
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

PACKAGE DESCRIPTION

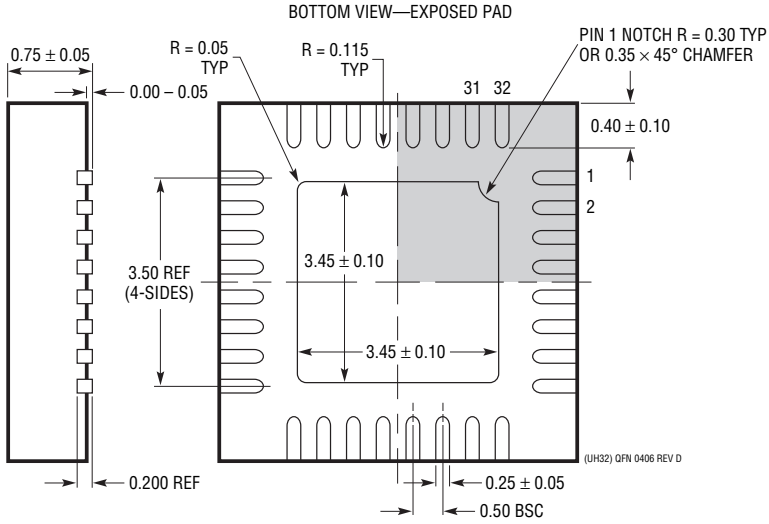
UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693 Rev D)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD



NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

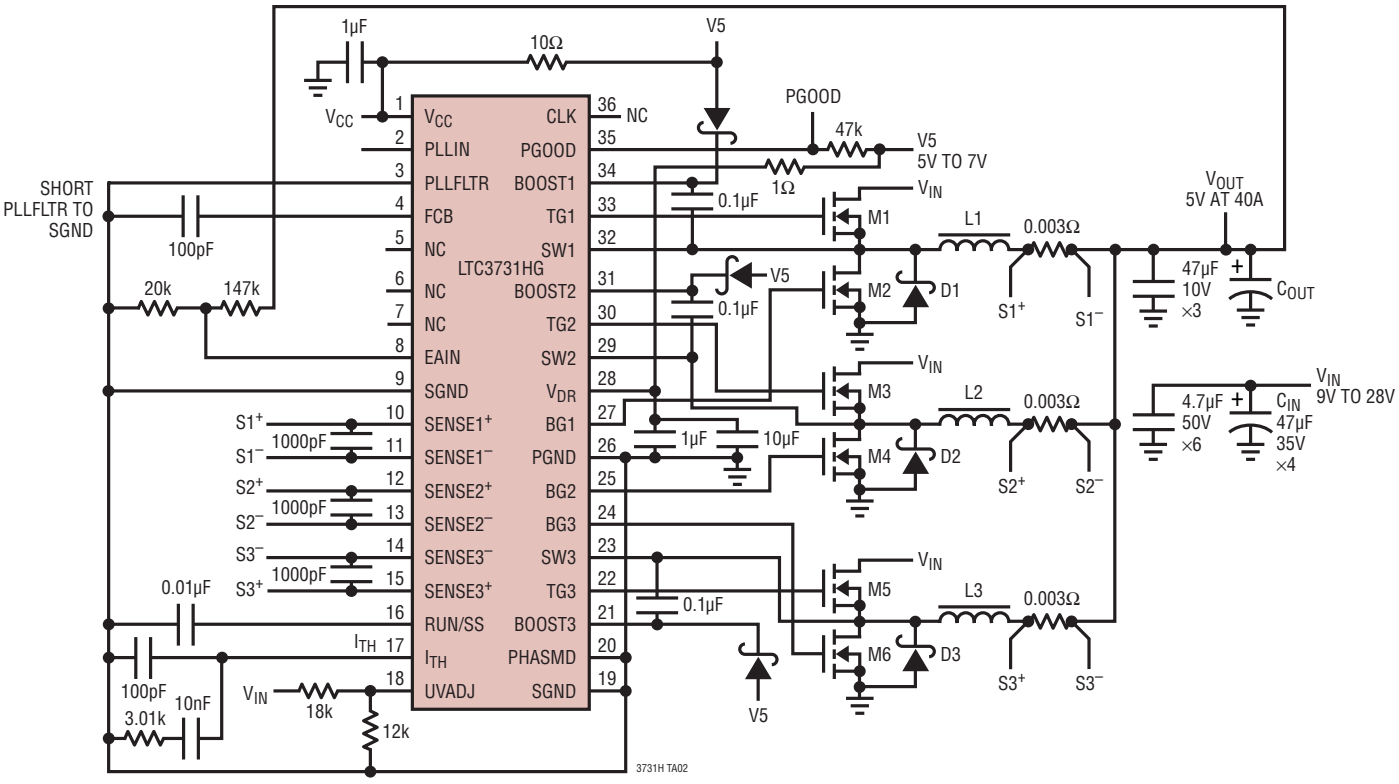
REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	5/10	UH package added. Changes reflected throughout the data sheet	1 - 34

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION



V_{IN}: 9V TO 28V
V_{OUT}: 5V AT 40A
SWITCHING FREQUENCY: 225kHz

C_{IN}: KEMET T521X476M035ATE070 ×4
C_{OUT}: SANYO 6TPE220MI ×3
D1 TO D3: DIODES INC. B340A

L1 TO L3: 2.2µH WURTH 7443320220
M1, M3, M5: RJK0305DPB
M2, M4, M6: RJK0330DPB

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3829	3-Phase, Single Output, Synchronous Step-Down Controller with Differential Amp and DCR Temperature Compensation	4.5V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 5V, Active Voltage Positioning, Stage Shedding
LTC3856	2-Phase, Single Output, Synchronous Step-Down Controller with Differential Amp and DCR Temperature Compensation	4.5V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 5V, Active Voltage Positioning, Stage Shedding
LTC3855	Dual, Multiphase, Synchronous Step-Down DC/DC Controller with Differential Amp and DCR Temperature Compensation	Phase-Lockable Fixed Frequency 250kHz to 770kHz, 4.5V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 12V
LTC3860	Dual, Multiphase, Synchronous Step-Down DC/DC Controller with Differential Amp and Tri-State Output Drive	Operates with Power Blocks, DRMOS Devices or External MOSFETs 3V ≤ V_{IN} ≤ 24V, $t_{ON(MIN)}$ = 20ns
LTC3853	Triple Output, Multiphase Synchronous Step-Down DC/DC Controller, R_{SENSE} or DCR Current Sensing and Tracking	Phase-Lockable Fixed 250kHz to 750kHz Frequency, 4V ≤ V_{IN} ≤ 24V, V_{OUT3} up to 13.5V
LTC3850/ LTC3850-1/ LTC3850-2	Dual 2-Phase, High Efficiency Synchronous Step-Down DC/DC Controller, R_{SENSE} or DCR Current Sensing and Tracking	Phase-Lockable Fixed 250kHz to 780kHz Frequency, 4V ≤ V_{IN} ≤ 30V, 0.8V ≤ V_{OUT} ≤ 5.25V

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