Secondary Side Dual Output Controller with Opto Driver

June 2003

FEATURES

- **Regulates Two Secondary Outputs**
- **Optocoupler Feedback Driver and Second Output Synchronous Driver Controller**
- True Differential Remote Sensing Regulation
- High Switching Frequency: up to 800kHz
- Programmable Current Limit
- Programmable Soft-Start and Power Good
- Automatic Frequency Synchronization
- Available in Thermally Enhanced 28-Lead TSSOP

APPLICATIONS

- 48V Input Isolated DC/DC Converters
- Multiple Output Power Supplies
- Offline Converters
- DC/DC Power Modules

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DESCRIPTION

The LT®3804 is a high efficiency step-down switching regulator with optocoupler feedback control for regulating multiple outputs in single-secondary winding isolated power supplies.

The LT3804 contains an error amplifier and an optocoupler driver to regulate the first (main) output. For the second output regulation, the LT3804 contains a complete PWM controller to drive dual synchronous N-channel MOSFETs. With leading edge modulation, it operates with either current or voltage mode control of the primary side. The LT3804 is synchronized to the falling edge of the transformer secondary winding and can be used in single-ended or double-ended isolated power converter topologies. A user selectable discontinuous conduction mode improves light load efficiency.

True differential Kelvin sensing is used for each output feedback amplifier to achieve high regulation accuracy and design simplicity. Other features include soft start, current limit and power good flags.

TYPICAL APPLICATION

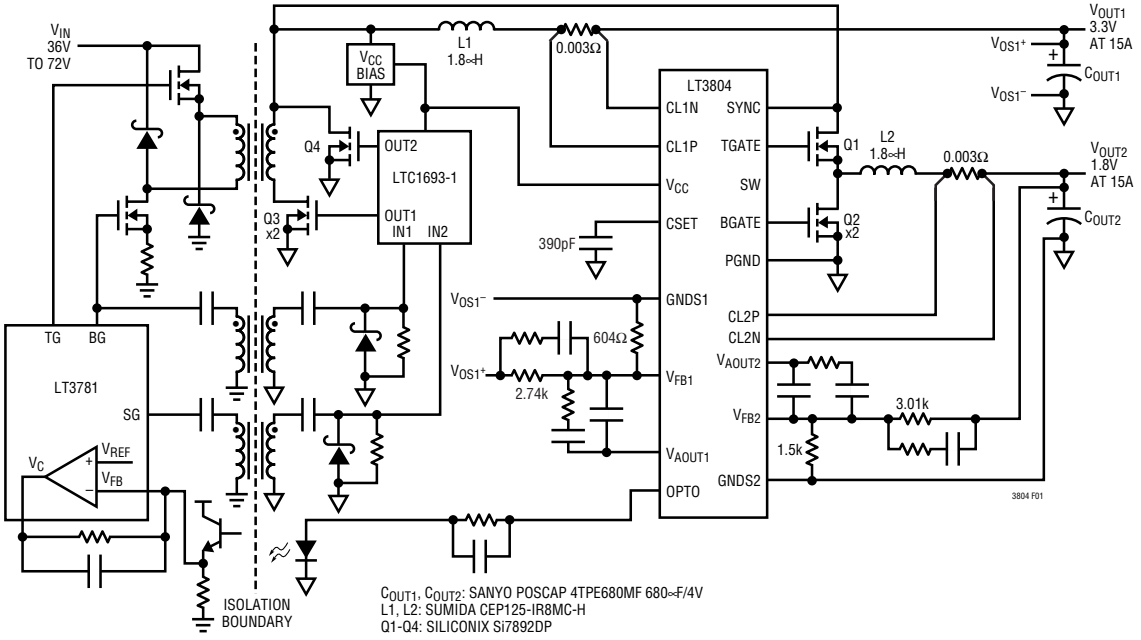


Figure 1. 250kHz, 3.3V and 1.8V Output Isolated DC/DC Converter (Simplified Schematic)

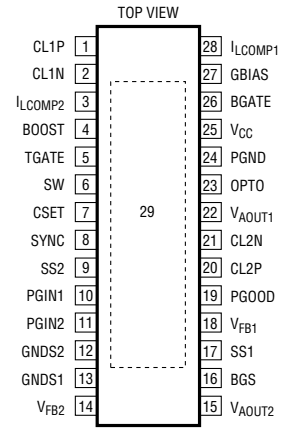
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ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} Supply Voltage 26V
BOOST Pin Voltage with Respect to SW Pin 10V
BOOST Pin Voltage with Respect to GND Pin 35V
SYNC Pin Voltage (Note 2) 30V
GNDS1 Pin Voltage 1V
GNDS2 Pin Voltage 1V
Operating Junction Temperature Range
LT3804E (Note 3) .....–40°C to 125°C
Storage Temperature Range .....–65°C to 150°C
Lead Temperature (Soldering, 10 sec).....300°C

PACKAGE/ORDER INFORMATION



FE PACKAGE
28-LEAD PLASTIC TSSOP

T_{JMAX} = 125°C, θ_{JA} = 38°C/W
EXPOSED PAD IS SGND (PIN 29)
MUST BE CONNECTED TO PCB

ORDER PART NUMBER
LT3804EFE

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 11V, GNDS1=GNDS2=0V, operating maximum V_{CC} = 25V, no load on any outputs, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Overall						
Supply Voltage (V_{CC})		●	8		25	V
Supply Current (I_{VCC})	$V_{AOUT2} \le 1.2V$ (Switching Off)			9	13	mA
BOOST Pin Current	$V_{BOOST} = V_{SW} + 8V$, $0V \le V_{SW} \le 24V$ TGATE High TGATE Low			 2 2	 3 3	 mA mA
Voltage Amplifier V_{A1},V_{A2}						
Reference Voltage (V_{REF1},V_{REF2})	Common Mode: ±20mV (0°C to 125°C) (–40°C to 125°C)	 ●	0.591 0.587	0.6	0.609 0.609	V V
	ΔV_{REF} over Common Mode: ±100mV		–3		3	mV
V_{FB1}, V_{FB2} Pin Input Current	$V_{FB1} = V_{REF1}$, $V_{FB2} = V_{REF2}$			0.2	0.5	µA
Remote Ground Pin (GNDS1,GNDS2) Current	$-100mV \le GNDS1, GNDS2 \le 100mV$	●		–50	–100	µA
V_{AOUT1} High at OA1 Threshold 1.5V	$V_{FB1} = V_{REF1} - 10mV$, $I_{VAOUT1} = -50\mu A$			1.75		V
V_{AOUT1} High at OA1 Threshold 1.25V	$V_{FB1} = V_{REF1} - 10mV$, $I_{VAOUT1} = -50\mu A$			1.45		V
V_{AOUT1} Low	$V_{FB1} = V_{REF1} + 10mV$, $I_{VAOUT1} = 100\mu A$			0.7		V
V_{AOUT2} High	$V_{FB2} = V_{REF2} - 10mV$, $I_{VAOUT2} = -50\mu A$			4.5		V
V_{AOUT2} Low	$V_{FB2} = V_{REF2} + 10mV$, $I_{VAOUT2} = 100\mu A$			0.8		V
V_{AOUT1} Source Current		●	100	230	400	µA
V_{AOUT2} Source Current		●	70	150	250	µA
Open-Loop Gain				100		dB
Gain Bandwidth Product				10		MHz
Soft-Start Current (SS1,SS2)			5	10	24	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 11V, GNDS1=GNDS2=0V, operating maximum V_{CC} = 25V, no load on any outputs, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Opto Driver Amplifier OA1						
OA1 Upper Threshold		●	1.4	1.55	1.65	V
OA1 Threshold Hysteresis				0.25		V
OA1 Voltage Gain (V_{OPTO}/V_{AOUT1})	1.2V < V_{OPTO} < 4V, R_{OPTO} = 1k	●	5.6	6	6.4	V
V_{OPTO} High	V_{AOUT1}= 0.9V, I_{OPTO} = –10mA	●	4.5	5.2	6	V
V_{OPTO} Low	V_{FB1} = V_{REF1} – 10mV, R_{OPTO} = 1k	●	0	0.1	0.25	V
I_{OPTO} Short-Circuit Current Limit	V_{FB1}=V_{REF1} – 10mV, GNDS1 = 0V, V_{OPTO} = 4V	●	–50	–25	–12	mA
Power Good						
Power Good Window Threshold (PGIN1-GNDS1, PGIN2-GNDS2)	–100mV < GNDS1, GNDS2 < 100mV		0.85		1.15	V_{REF}
Input Current (PGIN1,PGIN2)	0V < PGIN1, PGIN2 < 1V			0.2	0.35	µA
Delay Time for Power Bad	25mV Overdrive on PGIN1,PGIN2	●	100	200	300	µs
Output Low (PGOOD)	2mA into the Pin	●		150	300	mV
Current Limit Amplifier CA1, CA2						
Current Limit Threshold (CL1P-CL1N, CL2P-CL2N)	Common Mode Voltage from 0V to V_{CC} – 2.5V V_{AOUT1} = 1.2V, V_{AOUT2} = 2.5V,	●	40	50	60	mV
BGATE Off Threshold at (V_{CL2P}-V_{CL2N}), BGS Pin Float	Commond Mode Voltage from 0V to V_{CC} – 2.5V		0	8	15	mV
Switching Off Threshold at I_{LCOMP2}	$V_{ILCOMP2}$				0.15	V
Input Current (CL1P, CL1N, CL2P, CL2N)	V_{CL2P} = V_{CL1N}, V_{CL2P} = V_{CL2N}			100		µA
Oscillator						
Switching Frequency	C_S = 500pF (NO SYNC)	●	170	200	240	kHz
	C_S = 333pF (NO SYNC)	●	240	280	340	kHz
	C_S = 200pF (NO SYNC)	●	400	470	570	kHz
Synchronization Frequency Range	C_S = 500pF	●	245		400	kHz
	C_S = 333pF	●	345		500	kHz
	C_S = 200pF	●	575		800	kHz
CSET Ramp Valley Voltage	C_S = 1000pF (NO SYNC)		0.90	1.15	1.4	V
CSET Peak-to-Peak Voltage	C_S = 1000pF (NO SYNC)			2.4		V
Synchronization Pulse Threshold on SYNC Pin	Falling Edge V_{SYNC}			2.5		V
Maximum Duty Cycle	V_{FB2} = V_{REF2} – 5mV, C_S > 333pF	●	75	80		%
Gate Drivers (TGATE, BGATE)						
V_{GBIAS}	I_{GBIAS} < 25mA	●	7.5	8	8.5	V
V_{TGATE} High (V_{TGATE} – V_{SW})	I_{TGATE} < 50mA, V_{BOOST} = V_{GBIAS} – 0.5V		5	6	7.5	V
V_{BGATE} High	I_{BGATE} < 50mA	●	5	6	7.5	V
V_{TGATE} Low (V_{TGATE}-V_{SW})	I_{TGATE} < –50mA	●			0.5	V
V_{BGATE} Low	I_{BGATE} < 50mA	●			0.5	V
Peak Gate Drive Current	10nF Load			1		A
Gate Drive Rise and Fall Time	1nF Load			25		ns

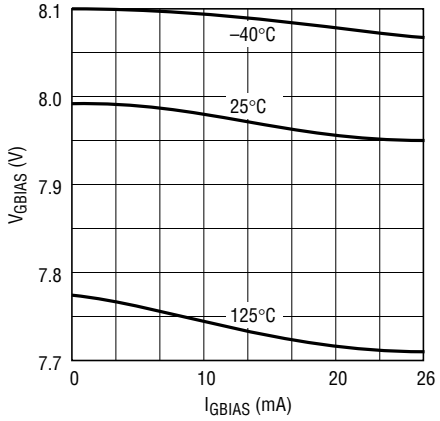
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: If highter than 30V on SYNC pin is needed, add a 10kΩ resistor in series with the pin.

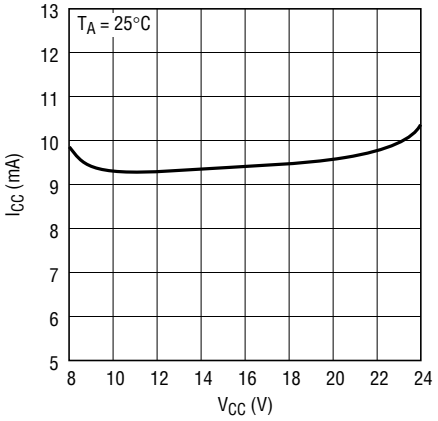
Note 3: The LT3804E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

TYPICAL PERFORMANCE CHARACTERISTICS

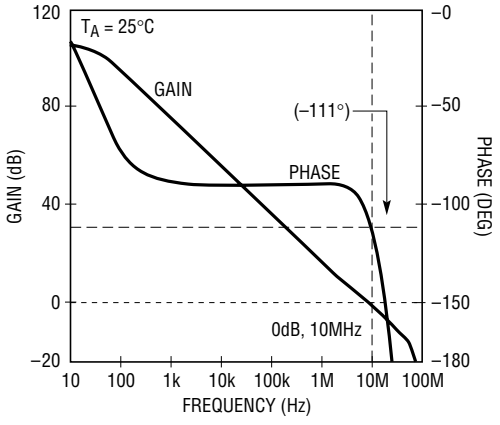
V_{GBIAS} vs I_{GBIAS} Over Junction Temperature



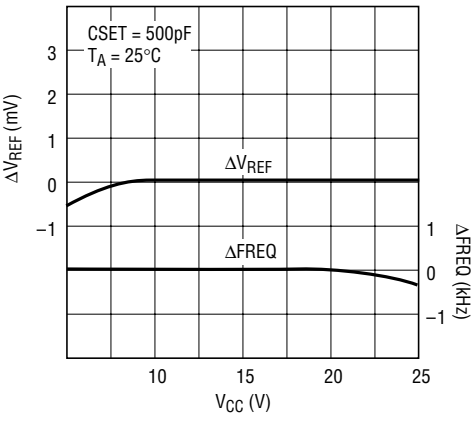
I_{CC} vs V_{CC} (Switching Off)



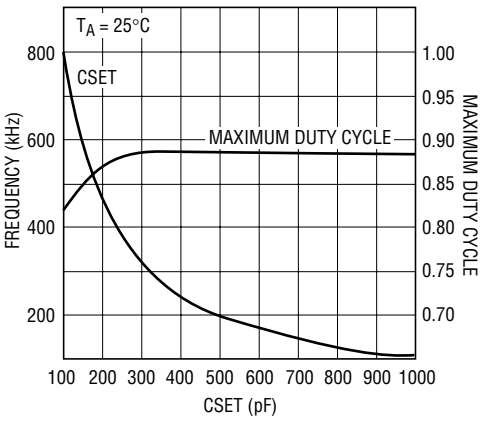
Voltage Amplifier V_{A1}, V_{A2} Gain and Phase



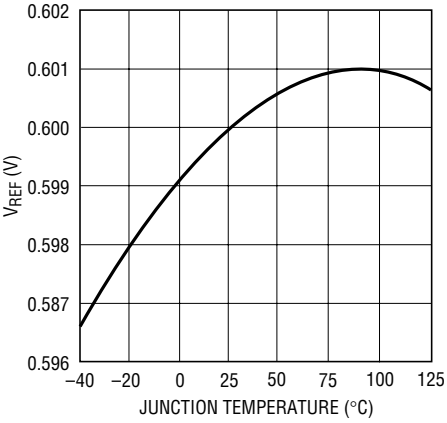
ΔV_{REF} vs V_{CC}, ΔFREQ vs V_{CC}



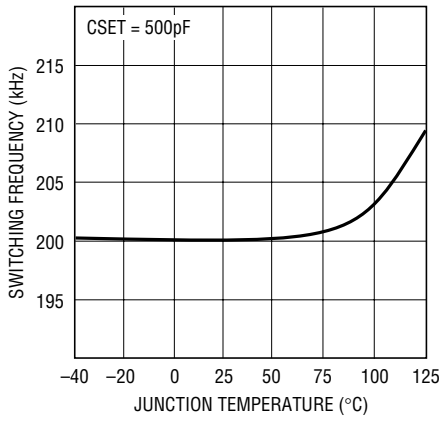
CSET vs Switching Frequency



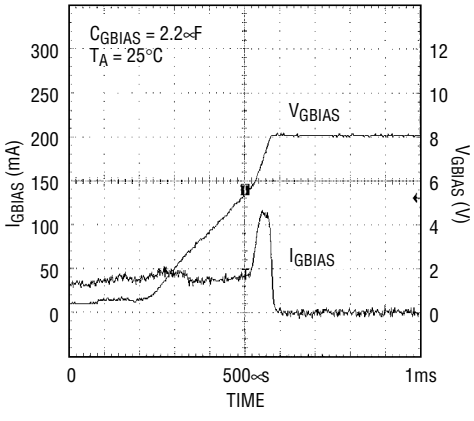
V_{REF} vs Temperature



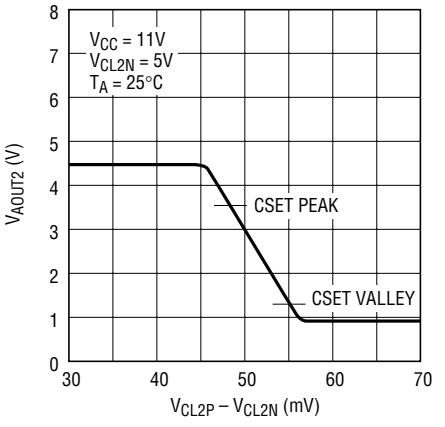
Switching Frequency vs Temperature



G_{BIAS} vs I_{GBIAS} (Charging 2.2µF)



Current Limit Amplifier CA1 Gain at V_{CC} = 11V, V_{CL2N} = 5V



PIN FUNCTIONS

CL1P (Pin 1): Current Limit Amplifier CA1 Positive Input. CA1 drives optocoupler when the first output is in current limit.The threshold is set at 50mV.

CL1N (Pin 2): Current Limit Amplifier CA1 Negative Input. When used, CL1N is connected to the output, and CL1P is connected to the other end of the output current sense resistor.

I_{LCOMP2} (Pin 3): Current Limit Amplifier CA2 Compensation Node. At second output current limit, CA2 pulls down on this pin to regulate output current.

BOOST (Pin 4): Topside (Boosted) Driver Supply.This pin is used to bootstrap and supply the topside power switch gate drive circuitry. In normal operation V_{BOOST} is powered from the internally generated 8V GBIAS; $V_{BOOST} = V_{SW} + 8V$ when TGATE is on.

TGATE (Pin 5): Topside (Boosted) N-Channel MOSFET Driver. When TGATE is on, the voltage is equal to $V_{SW} + 6V$.

SW (Pin 6): Switch Node Connection to Inductor.

CSET (Pin 7): Oscillator Frequency Setting Pin.The capacitor from this pin to ground sets the PWM switching frequency.

SYNC (Pin 8): Synchronization Input. This pin should be connected to the secondary side output of the power transformer with a series resistor. A filtering capacitor of 10pf is recommended.

SS2 (Pin 9): Soft-Start for the Second Output. A capacitor on this pin sets the output ramp-up rate. The typical time for SS2 to reach the programmed level is: (C • 0.6V)/10μA.

PGIN1 (Pin 10): First Output Power Good Input.The voltage setting resistor divider should be connected to GNDS1 if remote sensing is used.

PGIN2 (Pin 11): Second Output Power Good Input. The voltage setting resistor divider should be connected to GNDS2 if remote sensing is used.

GNDS2 (Pin 12): Second Output Remote Ground Sensing.

GNDS1 (Pin 13): First Output Remote Ground Sensing.

V_{FB2} (Pin 14): Voltage Amplifier V_{A2} Inverting Input. A resistor divider to this pin sets the second output voltage. The reference voltage at this pin is V_{REF2} (0.6V referred to remote sensing ground GNDS2).

V_{AOUT2} (Pin 15): Voltage Amplifier V_{A2} Output.

BGS (Pin 16): Bottom Gate Switching Control. CA2 monitors the inductor current and prohibits BGATE from turning on when the inductor current is low (below 8mV across the current sense resistor R_{S2}) allowing discontinous mode operation and avoiding reverse inductor current. Grounding BGS disables this function, so that the PWM is always in continuous mode except during start-up.

SS1 (Pin 17): Soft-Start for the First Output. A capacitor on this pin sets the output ramp-up rate. The typical time for SS1 to reach the programmed level is: (C • 0.6V)/10μA.

V_{FB1} (Pin 18): Voltage Amplifier V_{A1} Inverting Input. A resistor divider to this pin sets the first output voltage. The reference voltage at this pin is V_{REF1} (0.6V referred to remote sensing ground GNDS1).

PGOOD (Pin 19): Power Good. PGOOD goes high to indicate power good only when both PGIN1 and PGIN2 sense power good. A pull up resistor is required on this pin if the power good function is used.

CL2P (Pin 20): Second Output Current Limit Amplifier CA2 Positive Input.The threshold is set at 50mV.

CL2N (Pin 21): Current Limit Amplifier CA2 Negative Input. When used, CL2N is connected to the output capacitor, and CL2P is connected to the other end of the output current sense resistor.

V_{AOUT1} (Pin 22): Voltage Amplifier VA1 Output.

OPTO (Pin 23): Optocoupler Driver. A resistor to the opto diode is required to set the optocoupler bias current. Maximum sourcing current is 10mA at 5V.

PGND (Pin 24): Ground of the Bottom Side N-Channel MOSFET Driver.

V_{CC} (Pin 25): Supply of the Chip. A low ESR capacitor is required to bypass the supply.

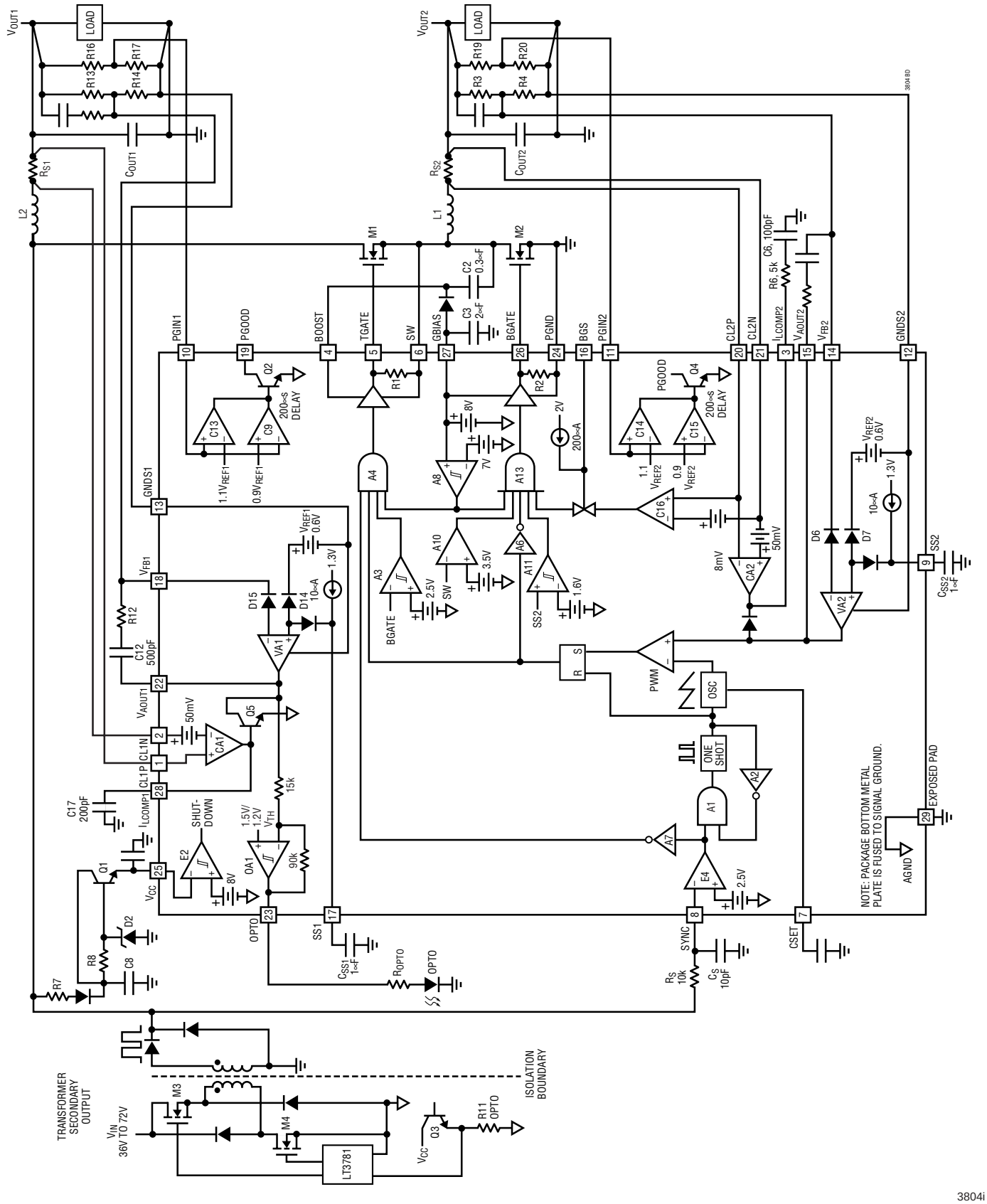
BGATE (Pin 26): Bottom Side N-Channel MOSFET Driver.

GBIAS (Pin 27): 8V Regulator Output for Boostrapping V_{BOOST}. A bypass capacitor of at least 2μF is needed.

I_{LCOMP1} (Pin 28): Current Limit Amplifier CA1 Compensation Node . When the first output is in current limit, CA1 pulls down V_{AOUT1} pin to regulate the first output current.

Exposed Pad (Pin 29): Signal Ground. Must be electrically connected on PCB.

BLOCK DIAGRAM



OPERATION

To generate isolated multiple outputs, most systems use either multiple secondary windings or cascade regulators for each additional output. Multiple secondary windings sacrifice regulation of the auxiliary outputs. Cascaded regulators require a larger inductor for the main output, because all of the power is processed in series. By generating the auxiliary output(s) from the secondary winding of the main output, the LT3804 allows for parallel processing of the output power. This minimizes the main output inductor size and directly regulates the auxiliary output. With synchronous rectification, the system efficiency is greatly improved.

The LT3804 regulates both the main and one auxiliary output, with true remote sensing to achieve high output accuracy. To regulate the first output, the LT3804 contains a high gain error amplifier VA1 and an optocoupler driver OA1 with a unique feature that reduces output overshoot to a minimum. For details see the Applications Information section. The second output includes a voltage amplifier, VA2, (see Block Diagram)a voltage mode PWM with trailing edge synchronization and leading edge modulation, a current limit amplifier, CA2, and high speed synchronous switch drivers.

During normal operation (see Figure 2), a switching cycle begins at the falling edge of the transformer secondary voltage V_S.

The internal oscillator is reset, turning off the top MOSFET, M1, and turning on the bottom MOSFET, M2. During this portion of the cycle, the inductor current is discharged by the output voltage V_{OUT2}. The transformer secondary voltage, V_S, will go high during this portion of the cycle. Since M1 is off, the switch node voltage, V_{SW}, remains zero. The inductor current continues to be discharged by the output voltage V_{OUT2}. This condition lasts until the ramp signal intersects the feedback error amplifier output V_{AOUT2}. The top MOSFET M1 turns on, pulling the switch node voltage to V_S. The inductor current of the LT3804 circuit is then charged by $V_S - V_{OUT2}$. The effective on time of this buck circuit ends when the secondary voltage becomes zero. The next cycle repeats. The ideal equation for duty cycle of the LT3804 is:

$$D2 = V_{OUT2}/V_{SP}$$

where V_{OUT2} is the auxiliary output voltage, V_{SP} is the amplitude of the secondary voltage and D2 is the duty cycle of the switching node voltage V_{SW}, as defined in Figure 2.

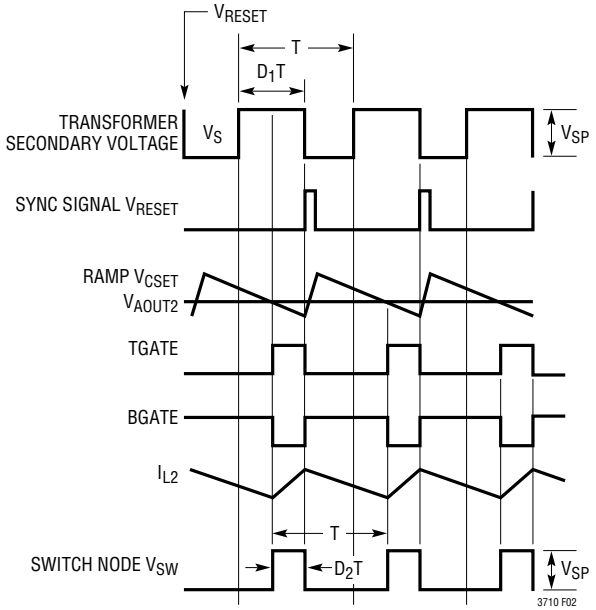


Figure 2. Leading Edge Modulation, Trailing Edge Synchronization

APPLICATIONS INFORMATION

Synchronization and Oscillator Frequency Setting

The switching is synchronized to the secondary winding falling edge and the synchronization threshold is typically 2.5V. The synchronization falling edge triggers an internal inverted ramp (see Figure 2) and starts a new switching cycle for the leading edge voltage mode PWM. The reason for using leading edge modulation is to leave the transformer primary side peak current sensing undisturbed. For proper synchronization, the oscillator frequency should be set lower than the system switching frequency with tolerances taken into account.

$f_{OSC} < (f_{SL} \bullet 0.8)$

f_{SL} is the low limit of the system switching frequency and 0.8 is the tolerance of f_{OSC}.

For example, given a system operating at 200kHz with 15% tolerance, then f_{SL} = 200kHz • 85% = 170kHz; and $f_{OSC} < (170kHz \bullet 0.8)$, so f_{OSC} should be set below 136kHz.

Once f_{OSC} is determined, CSET can be calculated by

$CSET = (103540pF/f_{OSC(kHz)}) – 18pF.$

For f_{OSC} = 200kHz, CSET = 500pF.

Output Voltage Programming

The LT3804 uses true remote sensing (separate ground sensing pins, GNDS1 for the first output and GNDS2 for the second output) to eliminate output error pickup due to parasitic resistance.

The feedback reference voltages V_{REF1} and V_{REF2} are 0.6V referred to GNDS1 and GNDS2 respectively. The output voltage can be easily programmed by a resistor divider, as shown in the Block Diagram:

$V_{OUT1} = 0.6\ (1 + R13/R14)$

$V_{OUT2} = 0.6\ (1 + R3/R4)$

where R14 connects to GNDS1 and R4 connects to GNDS2.

For accurate sensing results, GNDS1 and GNDS2 should stay within –0.1V and 0.1V referred to GND. Note that if either GNDS1 or GNDS2 is not connected, the LT3804 will be shut down.

Power Good

When both outputs reach between 90% and 110% of the programmed level, V_{PGOOD} goes high(a pull-up resistor is required if the function is used) to signal power good. If either output rises above 110% or drops below 90%, V_{PGOOD} goes low after a 200µs delay. PGIN1 senses the first output and PGIN2 senses the second output with a resistor divider. PGIN1 and PGIN2 are compared to the references V_{REF1} and V_{REF2} respectively. Resistor dividers should be connected to GNDS1 and GNDS2 with respect to each output.

Current Limit CA1

The first output current limit is set by the 50mV threshold across CL1P and CL1N, the inputs of the amplifier CA1. By connecting an external resistor R_{S1}(see Block Diagram), the current limit is set for 50mV/R_{S1}. C17 on I_{LCOMP1} stablizes the current limit loop. If current limit is not used, both CL1P and CL1N should be grounded and C17 is not needed.

Current Limit CA2

The second output current limit is set by the 50mV threshold across CL2P and CL2N, the inputs of the amplifier CA2. By connecting an external resistor R_{S2} (see Block Diagram), the current limit is set for 50mV/R_{S2}. R6 and C6 on I_{LCOMP2} stablize the current limit loop. If current limit is not used, both CL2P and CL2N should be grounded and the BGS pin should also be grounded to disable comparator CA2; R6 and C6 are not needed.

APPLICATIONS INFORMATION

Filtering on the SYNC Input

A small RC filter with R_S = 10k and C_S = 10pF is necessary on the SYNC pin to eliminate fast switching glitches caused by coupling from external components and layout parasitics.

Optocoupler Driver

Optocoupler driver OA1 is an amplifier with a fixed gain of 6 and can source up to 10mA into the optocoupler. An external resistor is needed from the OPTO pin to the optocoupler for DC biasing the optocoupler. With a unique 0.3V hysteresis on the threshold V_{TH}, OA1 turns into a comparator when it detects output startup or output short. This comparator action jumpstarts the optocoupler to reduce the output overshoot drastically (see Figure 3).

Soft-Start and Shutdown First Output

During soft-start, V_{SS1} is the reference voltage that controls the output voltage, so the output ramps up following V_{SS1}. The effective range of V_{SS1} is from 0V to V_{REF1}. The typical time for the output to reach the programmed level is:

$t = (CSS1 \bullet 0.6V)/10\mu A$

To shut down the first output, the SS1 pin should be pulled below 50mV by a small signal VN2222 type N-channel MOSFET.

Soft-Start and Shutdown Second Output

During soft-start, V_{SS2} is the reference voltage that controls the output voltage, so the output ramps up following V_{SS2}. The effective range of V_{SS2} is from 0V to V_{REF2}. The typical time for the output to reach the programmed level is:

$t = (CSS2 \bullet 0.6V)/10\mu A$

During start up, BGATE will stay off until V_{SS2} reaches 1.6V. This prevents the bottom MOSFET from turning on if the output is precharged. To shut down the second output, the SS2 pin should be pulled below 50mV by a small signal VN2222 type N-channel MOSFET. Note that during shutdown BGATE will be locked off when V_{SS2} drops below 0.6V. This prevents the bottom MOSFET from discharging the output, which could cause the output to undershoot below ground.

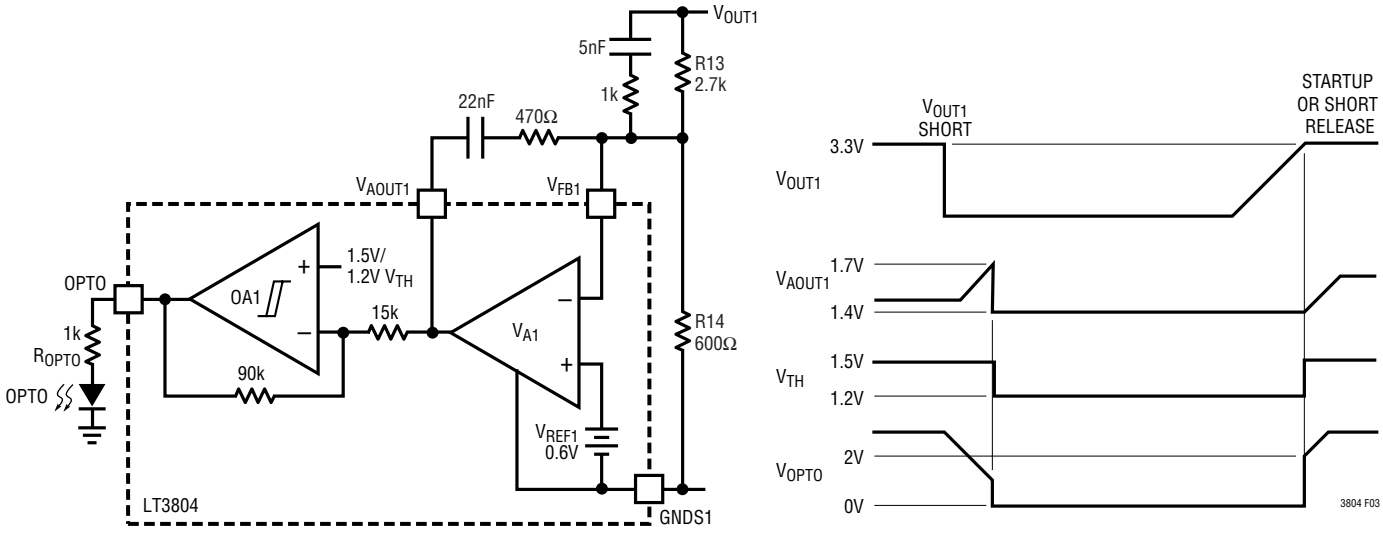


Figure 3. Optocoupler Driver

APPLICATIONS INFORMATION

Output Inductor Selection

The key parameters for choosing the inductor include inductance, RMS and saturation current ratings, and DCR. The inductance must be selected to achieve a reasonable value of ripple current, which is determined by:

$$\Delta I_L = \frac{V_{OUT} \bullet (1 - D)}{f \bullet L}$$

Where V_{OUT} is the output voltage, D is the duty cycle, f is switching frequency and L is the inductance. Typically, the inductor ripple current is designed to be 20% to 40% of the maximum output current.

The RMS current rating must be high enough to deliver the maximum output current. A sufficient saturation current rating should prevent the inductor core from saturating. These two current ratings can be determined by:

$$I_{RMS} \geq \sqrt{I_O^2 + \frac{\Delta I_{LMAX}^2}{12}}$$

$$I_{SAT} \geq I_O + \frac{\Delta I_{LMAX}}{2}$$

where I_O is the maximum DC output current and ΔI_{LMAX} is the maximum peak-to-peak inductor ripple current. To optimize the efficiency, we usually choose the inductor with the minimum DCR if the inductance and current ratings are the same.

Output N-Channel MOSFET Drivers

The LT3804 employs high speed N-channel MOSFET synchronous drivers to achieve high system efficiency. GBIAS is the 8V regulator output to bias and supply the drivers and should be properly bypassed with a low ESR capacitor to the ground plane. A Schottky catch diode is required on the switch node.

Power MOSFET Selection

The LT3804 drives two external N-channel MOSFETs to deliver high currents at high efficiency. The gate drive voltage is typically 6.5V. The key parameters for choosing MOSFETs include drain to source voltage rating V_{DSS} and $R_{DS(ON)}$ at 6.5V gate drive. Note that the transformer secondary voltage waveform will overshoot at its rising edge due to the ringing between transformer leakage inductance and parasitic capacitance. The V_{DSS} of both top and bottom MOSFETs must be sufficiently higher than the maximum overshoot. It is recommended that an RC snubber or voltage clamping circuitry be placed across the transformer secondary winding to limit the V_S overshoot. The $R_{DS(ON)}$ of the MOSFETs should be selected to deliver the required current at the desired efficiency as well as to meet the thermal requirement of the MOSFET package. The conduction power losses of the MOSFETs are:

$$P_{M1} \cong I_O^2 \bullet R_{DS(ON)M1} \bullet D$$

$$P_{M2} \cong I_O^2 \bullet R_{DS(ON)M2} \bullet (1 - D)$$

where I_O is the maximum output current of LT3804 circuit, and $R_{DS(ON)M1}$ and $R_{DS(ON)M2}$ are the on-resistance for the top and bottom MOSFETs, respectively. The $R_{DS(ON)}$ must be determined with 6.5V gate drive at the expected operating temperature. Numerous high performance power MOSFETs are available from Siliconix, International Rectifier and Fairchild. If the V_{DSS} and $R_{DS(ON)}$ ratings are the same, the MOSFETs with the lowest gate charge Q_G should be chosen to minimize the power loss associated with the MOSFET gate drives, the switching transitions, and the controller bias supply.

APPLICATIONS INFORMATION

Light Load Operation of Second Output

If the BGS pin is grounded, the LT3804 stays in continuous mode independent of load condition except during soft-start operation (see the Soft-Start section). If the BGS pin is left open under light load, V_{RS2} will drop below 8mV, BGATE will be turned off(see comparator CA2 of Block Diagram), and the LT3804 will enter discontinous mode operation.

Second Output Capacitor Selection

The selection of the output capacitor is determined by the output ripple and load transient requirements. In low output voltage applications, always choose capacitors with low ESR. The output ripple voltage is approximated by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

where ΔI_L is the inductor peak-to-peak ripple current. A partial list of low ESR high performance capacitor types includes SP capacitors from Panasonic and Cornell Dubilier, POSCAPs and OS-CON capacitors from Sanyo, T510 and T520 surface mount capacitors from Kemet.

Layout Considerations

For maximum efficiency, the switching rise and fall times should be less than 20ns. To prevent radiation, the power MOSFETs, SW pin and input bypass capacitor leads should be kept as short as possible. A ground plane should be used under the switching circuitry to prevent interplane coupling and to act as a thermal spreading path. Note that the bottom metal of the package is the heat sink as well as the IC signal ground, and must be soldered to the ground plane.

Design Example

Figure 4 shows an application example of LT3804. It is a dual output high efficiency isolated DC/DC power supply with 36V to 72V input range, 3.3V/15A and 1.8V/15A outputs. The basic power stage topology is a two-switch forward converter with synchronous rectification. The primary side controller uses an LT3781, a current mode two-switch forward controller with built-in MOSFET drivers. On the secondary side, the LT3804 is used to provide the voltage feedback for the 3.3V output. The output from the built-in optocoupler driver is fed into an optocoupler (MOC207) and then transferred to LT3781 on the primary side to complete the 3.3V regulation. An LTC1693-1 high speed dual N-channel MOSFET driver provides the gate drive for the synchronous MOSFETs at the 3.3V output stage. The LTC1693-1 driver's input signals come from SG and BG outputs of the LT3781 through two small gate drive transformers (T2 and T3).

The LT3804 also precisely regulates the 1.8V output by further reducing and controlling the duty cycle of the switching waveform from the power transformer (T1) secondary winding. In fact, the 1.8V circuit is a special synchronous buck converter whose input is a pulsed waveform instead of a DC voltage.

True differential remote sensing is provided for both outputs to achieve high regulation accuracies. Power good indicator PGOOD will be high only if both outputs are within ±10% of their nominal values.

The LT3804 provides current limit function for both 1.8V and 3.3V outputs. The current limits for 3.3V and 1.8V outputs are estimated to be 50mV/R55 and 50mV/R49, respectively.

APPLICATIONS INFORMATION

A planar transformer PA0191 by Pulse Engineering is employed as the power transformer in this design. This transformer is constructed on a PQ20 core with nine turns of primary windings, two turns of secondary windings and seven turns of auxiliary windings for the LT3781 bias supply. Si7892DP MOSFETs are selected for the secondary side due to their low $R_{DS\ (ON)}$, 30V V_{DSS} rating and compact, thermally enhanced PowerPak SO-8 package.

The switching frequency of the circuit is about 230kHz. 1500V input to output isolation is provided. Additional features of this design include primary side on/off control, input over voltage protection, under voltage lockout, soft start and board over temperature shutdown. The complete design is mounted within a standard half brick PC board with about half inch height.

APPLICATIONS INFORMATION

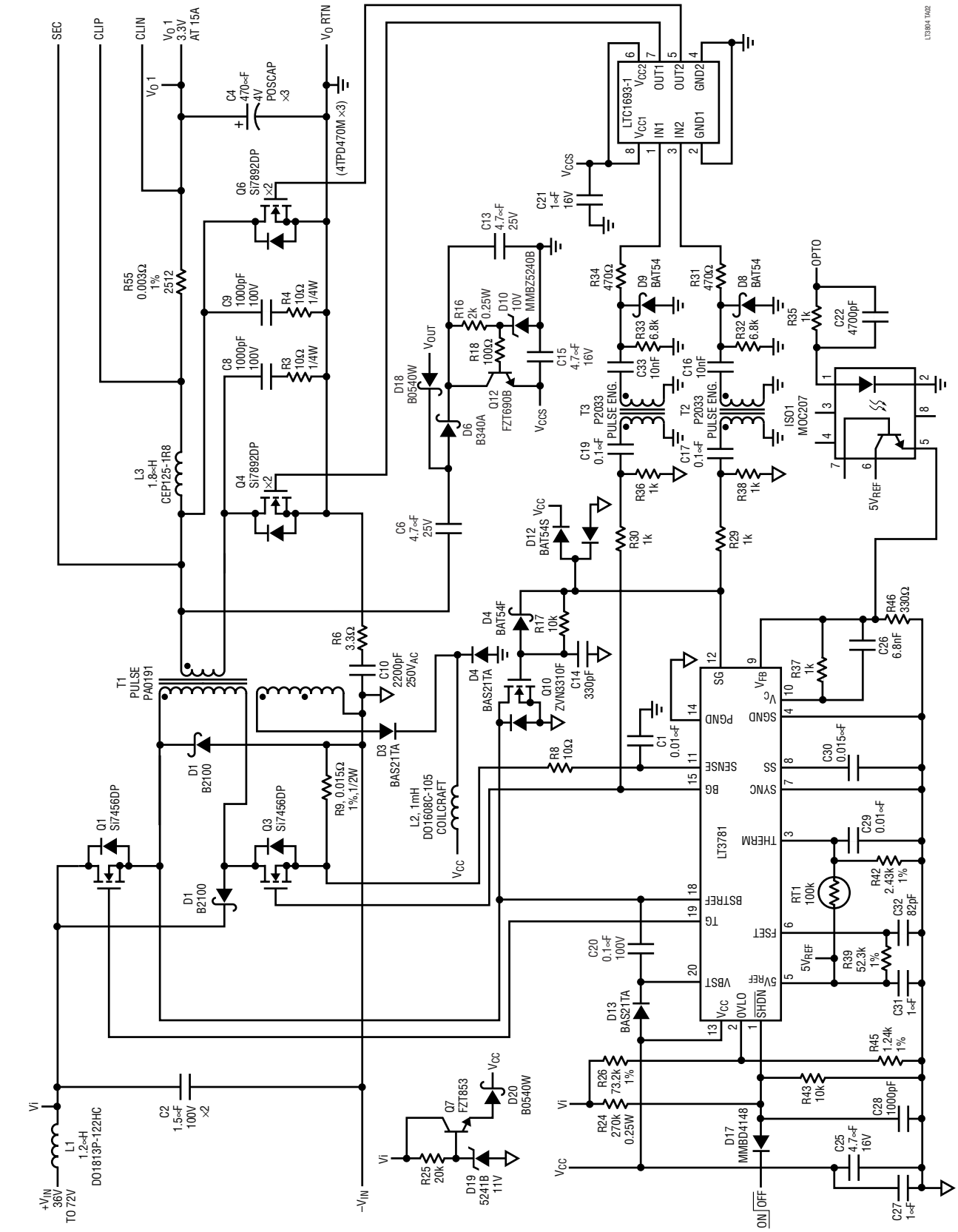


Figure 4. 36V – 72VDC to 3.3V/15A and 1.8V/15A Dual Output Isolated Power Supply (Page 1 of 2)

APPLICATIONS INFORMATION

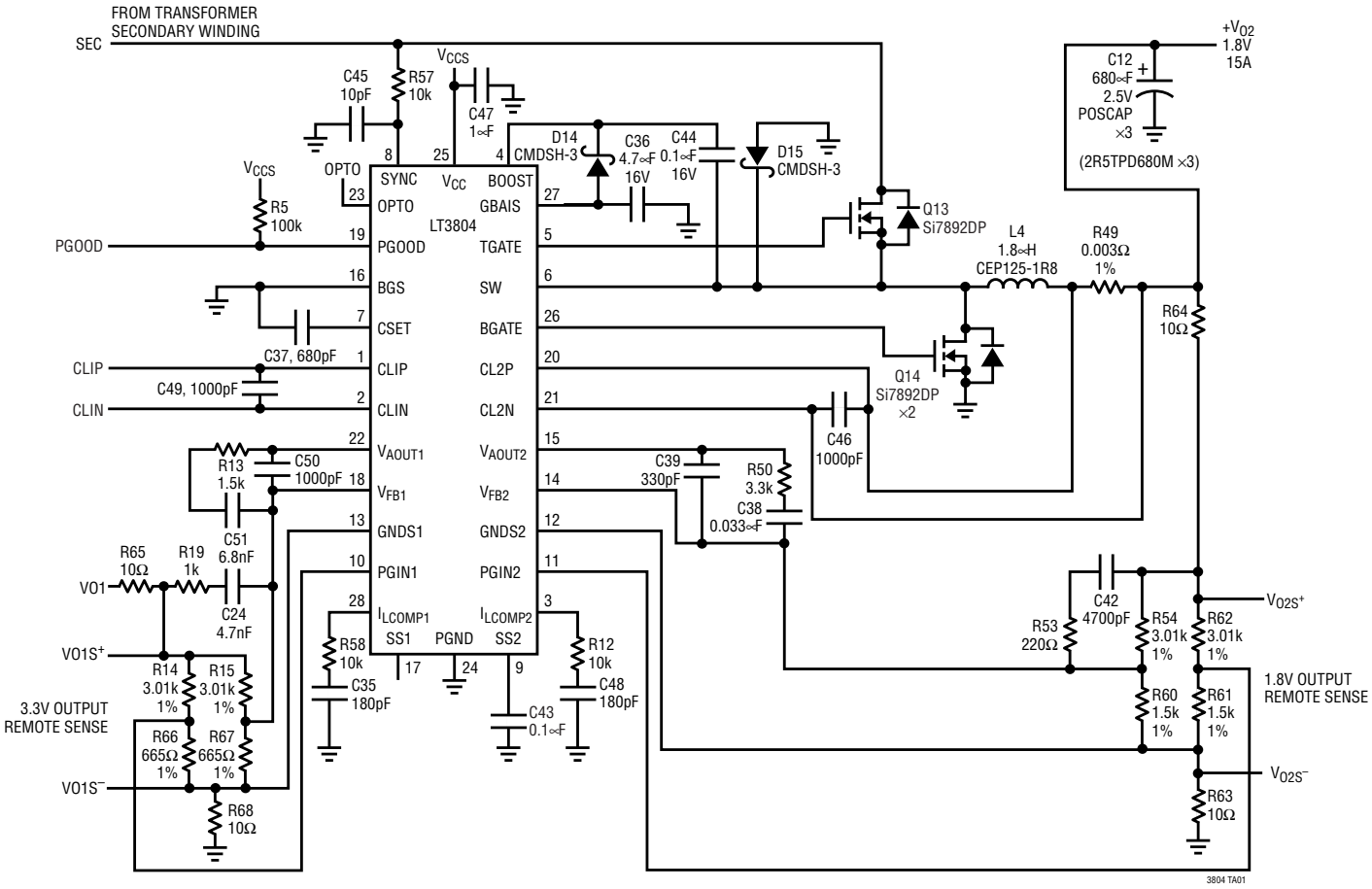
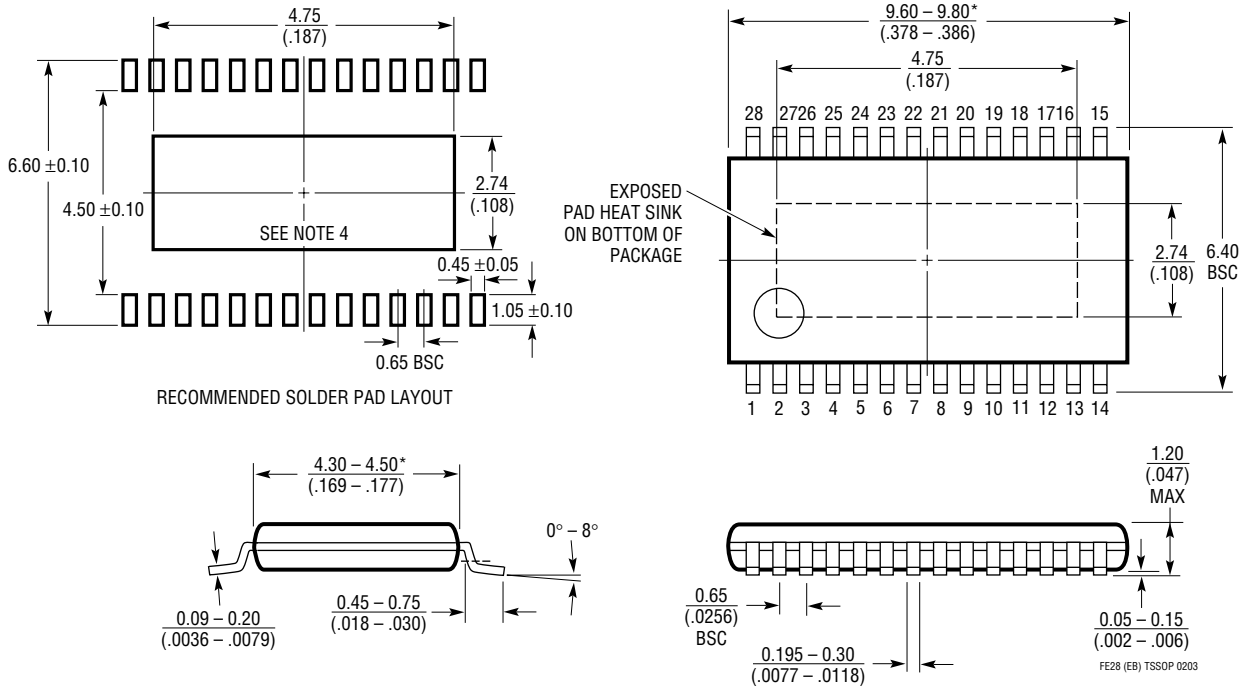


Figure 4. 36V – 72V_{DC} to 3.3V/15A and 1.8V/15A Dual Output Isolated Power Supply (Page 2 of 2)

PACKAGE DESCRIPTION

FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation EB



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1339	High Power Synchronous DC/DC Controller	Operation Up to 60V Maximum
LT1425	Isolated Flyback Switching Regulator	General Purpose with External Application Resistor
LT1431	Programmable Reference	0.4% Initial Voltage Tolerance
LT1680	High Power DC/DC Step-Up Controller	Operation Up to 60V Maximum
LT1725	General Purpose Isolated Flyback Controller	Drives External Power MOSFET with External I_{SENSE} Resistor
LT1737	High Power Isolated Flyback Controller	Sense Output Voltage Directly from Primary-Side Winding
LT1950	PWM Controller for Forward, Flyback, Boost and SEPIC	$3V \leq V_{IN} \leq 25V$, Volt-Second Clamp, Leading-Edge Blanking, Slope Compensation
LT3710	Secondary Side Synchronous Post Regulator	Generates Regulated Auxiliary Output in Isolated DC/DC Converters, Dual N-Channel MOSFET Synchronous Drivers
LTC3722	Synchronous Phase Modulated Full-Bridge Controller	Adaptive or Manual Delay Control for Zero Voltage Switching, Adjustable Maximum ZVS Delay, Current Mode and Voltage Mode.
LT3781	Dual Transistor Synchronous Forward Controller	Operation Up to 72V Maximum

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LT/TP 0603 1K • PRINTED IN USA

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