60V Current Mode Synchronous Switching Regulator Controller

FEATURES

- **High Voltage Operation: Up to 60V**
- **Large 1Ω Gate Drivers**
- **No Current Sense Resistor Required**
- **Dual N-Channel MOSFET Synchronous Drive**
- Extremely Fast Transient Response
- ±0.5% 0.8V Voltage Reference
- Programmable Output Voltage Tracking/Soft-Start
- Generates 5.5V Driver Supply from Input Supply
- Synchronizable to External Clock
- Selectable Pulse Skip Mode Operation
- Power Good Output Voltage Monitor
- Adjustable On-Time/Frequency: $t_{ON(MIN)}$ < 100ns
- Adjustable Cycle-by-Cycle Current Limit
- Programmable Undervoltage Lockout
- Output Overvoltage Protection
- 5mm × 5mm QFN Package

APPLICATIONS

- 48V Telecom and Base Station Power Supplies
- Networking Equipment, Servers
- Automotive and Industrial Control Systems

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DESCRIPTION

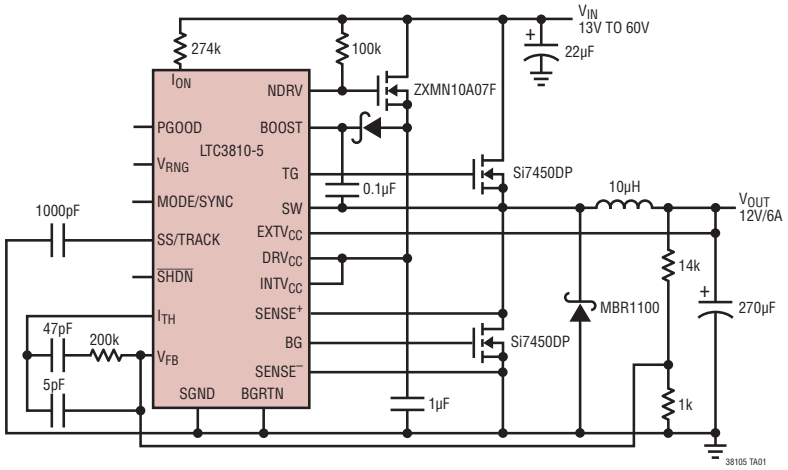
The LTC®3810-5 is a synchronous step-down switching regulator controller that can directly step-down voltages from up to 60V, making it ideal for telecom and automotive applications. The LTC3810-5 uses a constant on-time valley current control architecture to deliver very low duty cycles with accurate cycle-by-cycle current limit, without requiring a sense resistor.

A precise internal reference provides 0.5% DC accuracy. A high bandwidth (25MHz) error amplifier provides very fast line and load transient response. Large 1Ω gate drivers allow the LTC3810-5 to drive multiple MOSFETs for higher current applications. The operating frequency is selected by an external resistor and is compensated for variations in V_{IN} and can also be synchronized to an external clock for switching-noise sensitive applications. A shutdown pin allows the LTC3810-5 to be turned off, reducing the supply current to 240µA.

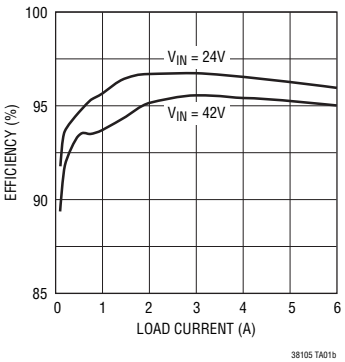
Integrated bias control generates gate drive power from the input supply during start-up or when an output short-circuit occurs, with the addition of a small external SOT23 MOSFET. When in regulation, power is derived from the output for higher efficiency.

TYPICAL APPLICATION

High Efficiency High Voltage Step-Down Converter



Efficiency vs Load Current



ABSOLUTE MAXIMUM RATINGS

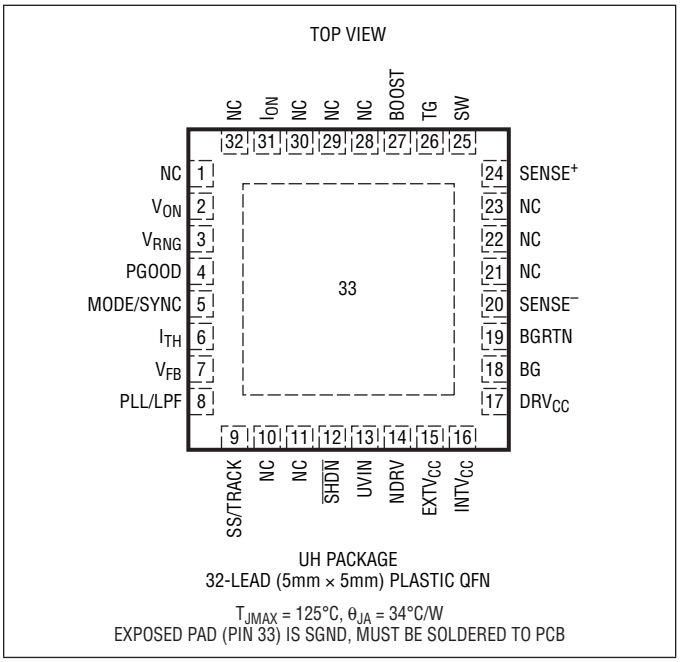
(Note 1)

Supply Voltages
- $INTV_{CC}$, DRV_{CC} ..... –0.3V to 14V
- (DRV_{CC} – BGRTN), (BOOST – SW) ..... –0.3V to 14V
- BOOST (Continuous) ..... –0.3V to 85V
- BOOST (≤400ms) ..... –0.3V to 95V
- BGRTN ..... –5V to 0V
- $EXTV_{CC}$ ..... –0.3V to 15V
- ($EXTV_{CC}$ – $INTV_{CC}$) ..... –12V to 12V

($NDRV – INTV_{CC}$) Voltage ..... –0.3V to 10V
SW, $SENSE^+$ Voltage (Continuous) ..... –1V to 70V
SW, $SENSE^+$ Voltage (400ms) ..... –1V to 80V
I_{ON} Voltage (Continuous) ..... –0.3V to 70V
I_{ON} Voltage (400ms) ..... –0.3V to 80V
SS/TRACK Voltage ..... –0.3V to 5V
PGOOD Voltage ..... –0.3V to 7V
V_{RNG}, V_{ON}, MODE/SYNC, $\overline{SHDN}$, UVIN Voltages ..... –0.3V to 14V
PLL/LPF, FB Voltages ..... –0.3V to 2.7V
TG, BG, $INTV_{CC}$, $EXTV_{CC}$ RMS Currents 50mA
Operating Junction Temperature Range (Notes 2, 3, 7)
- LTC3810E-5 ..... –40°C to 125°C
- LTC3810I-5 ..... –40°C to 125°C
- LTC3810H-5 ..... –40°C to 150°C

Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 33) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3810EUH-5#PBF	LTC3810EUH-5#TRPBF	38105	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3810IUH-5#PBF	LTC3810IUH-5#TRPBF	38105	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING**	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC3810EUH-5	LTC3810EUH-5#TR	38105	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3810IUH-5	LTC3810IUH-5#TR	38105	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3810HUH-5	LTC3810HUH-5#TR	38105	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2), $INTV_{CC}$ = DRV_{CC} = V_{BOOST} = V_{ON} = V_{RNG} = $\overline{SHDN}$ = UV_{IN} = V_{EXTVCC} = V_{NDRV} = 5V, $V_{MODE/SYNC}$ = V_{SENSE^+} = V_{SENSE^-} = V_{BGRTN} = V_{SW} = 0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
$INTV_{CC}$	$INTV_{CC}$ Supply Voltage		●	4.35		14	V
I_Q	$INTV_{CC}$ Supply Current $INTV_{CC}$ Shutdown Current	$\overline{SHDN}$ > 1.5V (Notes 4, 5) $\overline{SHDN}$ = 0V			3 240	6 600	mA µA
I_{BOOST}	BOOST Supply Current	$\overline{SHDN}$ > 1.5V (Note 5) $\overline{SHDN}$ = 0V			270 0	400 5	µA µA
V_{FB}	Feedback Voltage	(Note 4) 0°C to 85°C –40°C to 85°C –40°C to 125°C (I-Grade) –40°C to 150°C (H-Grade)	 ● ● ● ●	0.796 0.794 0.792 0.792 0.792	0.800 0.800 0.800 0.800 0.800	0.804 0.806 0.806 0.808 0.812	V V V V V
$\Delta V_{FB,LINE}$	Feedback Voltage Line Regulation	5V < $INTV_{CC}$ < 14V (Note 4)	●		0.002	0.02	%/V
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	V_{RNG} = 2V, V_{FB} = 0.76V V_{RNG} = 0V, V_{FB} = 0.76V V_{RNG} = $INTV_{CC}$, V_{FB} = 0.76V		256 70 170	320 95 215	384 120 260	mV mV mV
$V_{SENSE(MIN)}$	Minimum Current Sense Threshold	V_{RNG} = 2V, V_{FB} = 0.84V V_{RNG} = 0V, V_{FB} = 0.84V V_{RNG} = $INTV_{CC}$, V_{FB} = 0.84V			–300 –85 –200		mV mV mV
I_{VFB}	Feedback Current	V_{FB} = 0.8V			20	150	nA
A_{VOL}(EA)	Error Amplifier DC Open Loop Gain			65	100		dB
f_U	Error Amp Unity-Gain Crossover Frequency	(Note 6)			25		MHz
$V_{MODE/SYNC}$	MODE/SYNC Threshold	$V_{MODE/SYNC}$ Rising		0.75	0.8	0.85	V
$I_{MODE/SYNC}$	MODE/SYNC Current	MODE/SYNC = 5V			0	1	µA
$V_{\overline{SHDN}}$	Shutdown Threshold			1.2	1.5	2	V
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Input Current				0	1	µA
V_{UVIN}	UVIN Undervoltage Lockout	UVIN Rising UVIN Falling Hysteresis	● ●	0.86 0.78 0.07	0.89 0.80 0.10	0.92 0.82 0.12	V V V
V_{VCCUV}	$INTV_{CC}$ Undervoltage Lockout Linear Regulator Mode External Supply Mode Trickle-Charge Mode	 $INTV_{CC}$ Rising, I_{NDRV} = 100µA $INTV_{CC}$ Rising, NDRV = $INTV_{CC}$ = $EXTV_{CC}$ $INTV_{CC}$ Rising, NDRV = $INTV_{CC}$, $EXTV_{CC}$ = 0 $INTV_{CC}$ Falling	 ● ● ●	 4.05 4.05 8.70	 4.2 4.2 9 3.7	 4.35 4.35 9.30	 V V V V
Oscillator and Phase-Locked Loop							
t_{ON}	On-Time	I_{ON} = 100µA I_{ON} = 300µA		1.55 515	1.85 605	2.15 695	µs ns
$t_{ON(MIN)}$	Minimum On-Time	I_{ON} = 2000µA				100	ns
$t_{OFF(MIN)}$	Minimum Off-Time				250	350	ns
$t_{ON(PLL)}$	t_{ON} Modulation Range by PLL Down Modulation Up Modulation	 I_{ON} = 100µA, $V_{PLL/LPF}$ = 0.6V I_{ON} = 100µA, $V_{PLL/LPF}$ = 1.8V		 2.2 0.6	 3.6 1.2	 5 1.8	 µs µs
$I_{PLL/LPF}$	Phase Detector Output Current Sinking Capability Sourcing Capability	 f_{PLLIN} < f_{SW} f_{PLLIN} > f_{SW}			 15 –25		 µA µA
Driver							
$I_{BG,PEAK}$	BG Driver Peak Source Current	V_{BG} = 0V		0.7	1		A
$R_{BG,SINK}$	BG Driver Pull-Down $R_{DS(ON)}$				1	1.5	Ω
$I_{TG,PEAK}$	TG Driver Peak Source Current	V_{TG} – V_{SW} = 0		0.7	1		A
$R_{TG,SINK}$	TG Driver Pull-Down $R_{DS(ON)}$				1	1.5	Ω

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2), $INTV_{CC}$ = DRV_{CC} = V_{BOOST} = V_{ON} = V_{RNG} = $\overline{SHDN}$ = UV_{IN} = V_{EXTVCC} = V_{NDRV} = 5V, $V_{MODE/SYNC}$ = V_{SENSE^+} = V_{SENSE^-} = V_{BGRTN} = V_{SW} = 0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PGOOD Output							
ΔV_{FBOV}	PGOOD Upper Threshold PGOOD Lower Threshold	V_{FB} Rising V_{FB} Falling		7.5 –7.5	10 –10	12.5 –12.5	% %
$\Delta V_{FB,HYST}$	PGOOD Hysterisis	V_{FB} Returning			1.5	3	%
V_{PGOOD}	PGOOD Low Voltage	I_{PGOOD} = 5mA			0.3	0.6	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V			0	2	µA
PG Delay	PGOOD Delay	V_{FB} Falling			120		µs
Tracking							
$I_{SS/TRACK}$	SS/TRACK Source Current	$V_{SS/TRACK}$ > 0.5V		0.7	1.4	2.5	µA
$V_{FB,TRACK}$	Feedback Voltage at Tracking	V_{TRACK} = 0V, I_{TH} = 1.2V (Note 4) V_{TRACK} = 0.5V, I_{TH} = 1.2V (Note 4)		 0.48	–0.018 0.5	 0.52	V V
V_{CC} Regulators							
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage $EXTV_{CC}$ Rising $EXTV_{CC}$ Hysterisis		●	 4.45 0.1	 4.7 0.25	 0.4	 V V
$V_{INTVCC,1}$	$INTV_{CC}$ Voltage from $EXTV_{CC}$	6V < V_{EXTVCC} < 15V		5.2	5.5	5.8	V
$\Delta V_{EXTVCC,1}$	V_{EXTVCC} - V_{INTVCC} at Dropout	I_{CC} = 20mA, V_{EXTVCC} = 5V			75	150	mV
$\Delta V_{LOADREG,1}$	$INTV_{CC}$ Load Regulation from $EXTV_{CC}$	I_{CC} = 0mA to 20mA, V_{EXTVCC} = 10V			0.01		%
$V_{INTVCC,2}$	$INTV_{CC}$ Voltage from NDRV Regulator	Linear Regulator in Operation		5.2	5.5	5.8	V
$\Delta V_{LOADREG,2}$	$INTV_{CC}$ Load Regulation from NDRV	I_{CC} = 0mA to 20mA, V_{EXTVCC} = 0			0.01		%
I_{NDRV}	Current into NDRV Pin	V_{NDRV} – V_{INTVCC} = 3V		20	40	60	µA
I_{NDRVTO}	Linear Regulator Timeout Enable Threshold			210	270	350	µA
V_{CCSR}	Maximum Supply Voltage	Trickle Charger Shunt Regulator			15		V
I_{CCSR}	Maximum Current into NDRV/$INTV_{CC}$	Trickle Charger Shunt Regulator, $INTV_{CC}$ ≤ 16.7V (Note 8)		10			mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3810-5 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3810E-5 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3810I-5 is guaranteed to meet performance specifications over the full –40°C to 125°C operating junction temperature range. The LTC3810H-5 is guaranteed to meet performance specifications over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

LTC3810-5: $T_J = T_A + (P_D \bullet 34°C/W)$

Note 4: The LTC3810-5 is tested in a feedback loop that servos V_{FB} to the reference voltage with the I_{TH} pin forced to a voltage between 1V and 2V.

Note 5: The dynamic input supply current is higher due to the power MOSFET gate charging being delivered at the switching frequency ($Q_G \bullet f_{OSC}$).

Note 6: Guaranteed by design. Not subject to test.

Note 7: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

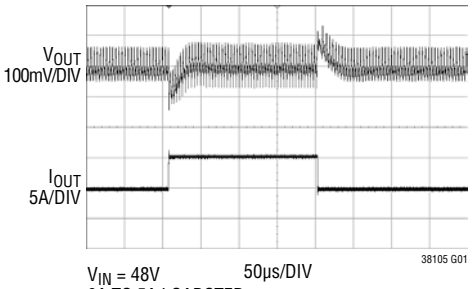
Note 8: I_{CC} is the sum of current into NDRV and $INTV_{CC}$.

Similar Parts Comparison

PARAMETER	LTC3810	LTC3810-5	LTC3812-5
Maximum V_{IN}	100V	60V	60V
MOSFET Gate Drive	6.35V to 14V	4.5V to 14V	4.5V to 14V
$INTV_{CC}$ UV^+	6.2V	4.2V	4.2V
$INTV_{CC}$ UV^-	6V	4V	4V

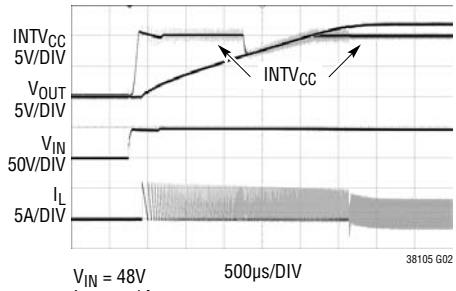
TYPICAL PERFORMANCE CHARACTERISTICS

Load Transient Response



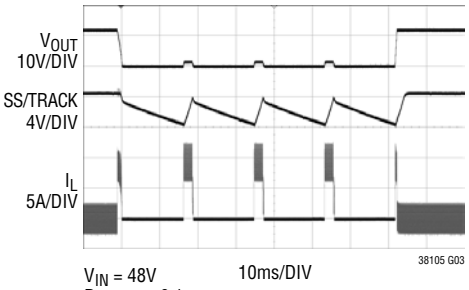
V_{IN} = 48V 50µs/DIV
0A TO 5A LOADSTEP
FRONT PAGE CIRCUIT

Start-Up



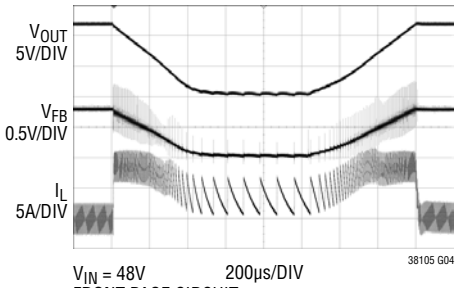
V_{IN} = 48V 500µs/DIV
I_{LOAD} = 1A
MODE/SYNC = 0V
FRONT PAGE CIRCUIT

Short-Circuit/ Fault Timeout Operation



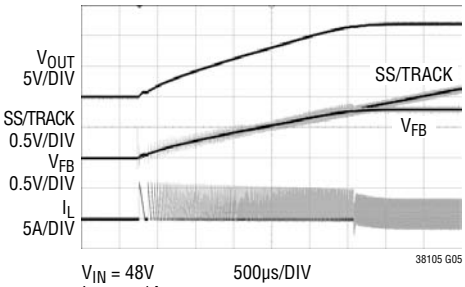
V_{IN} = 48V 10ms/DIV
R_{SHORT} = 0.1Ω
FRONT PAGE CIRCUIT

Short-Circuit/ Foldback Operation



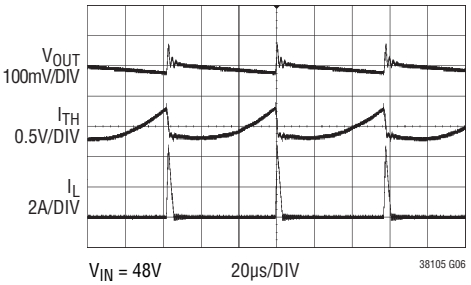
V_{IN} = 48V 200µs/DIV
FRONT PAGE CIRCUIT

Tracking



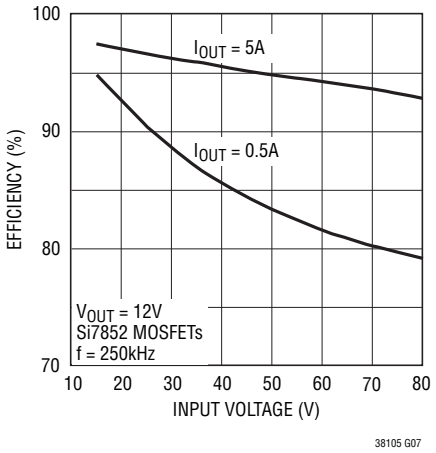
V_{IN} = 48V 500µs/DIV
I_{LOAD} = 1A
MODE/SYNC = 0V
FRONT PAGE CIRCUIT

Pulse Skip Mode Operation

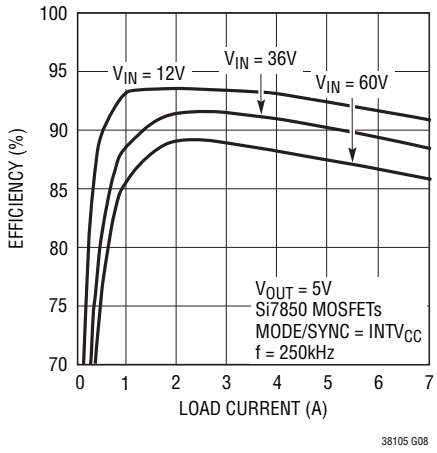


V_{IN} = 48V 20µs/DIV
I_{OUT} = 100mA
MODE/SYNC = $INTV_{CC}$
FRONT PAGE CIRCUIT

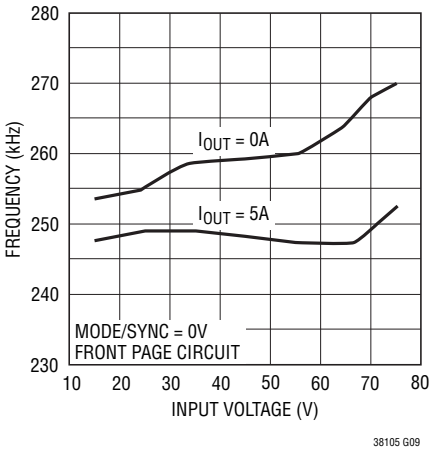
Efficiency vs Input Voltage



Efficiency vs Load Current

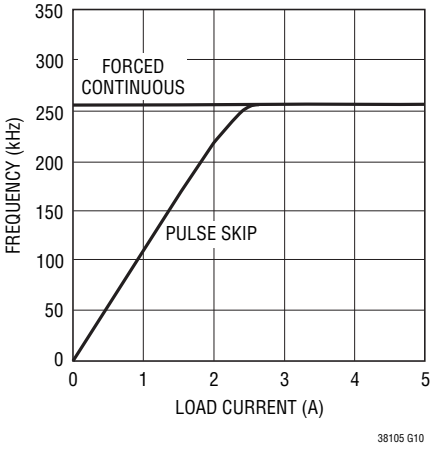


Frequency vs Input Voltage



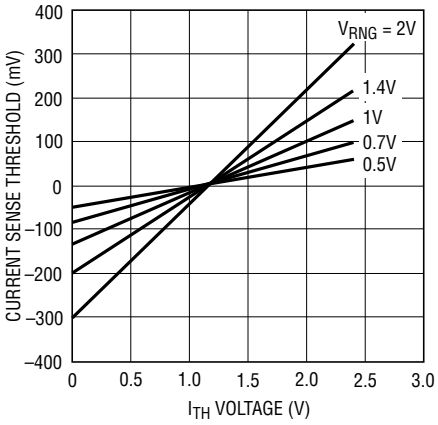
TYPICAL PERFORMANCE CHARACTERISTICS

Frequency vs Load Current



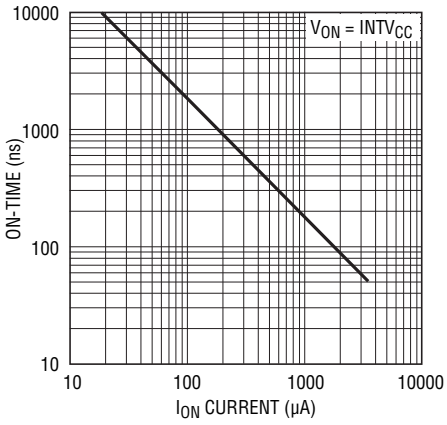
38105 G10

Current Sense Threshold vs I_{TH} Voltage



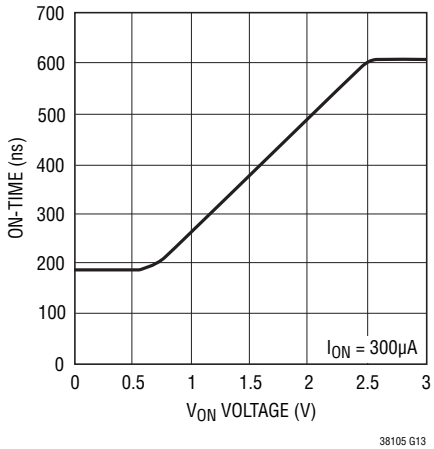
38105 G11

On-Time vs I_{ON} Current



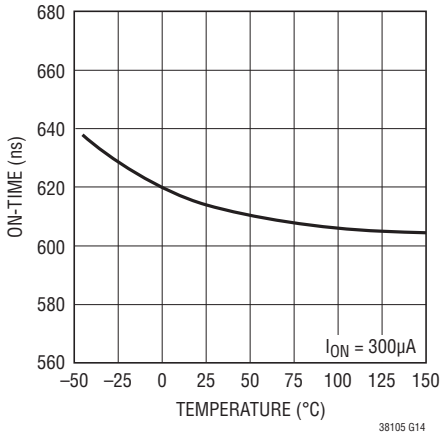
38105 G12

On-Time vs V_{ON} Voltage



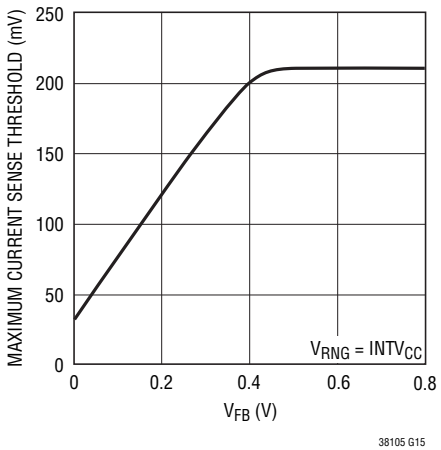
38105 G13

On-Time vs Temperature



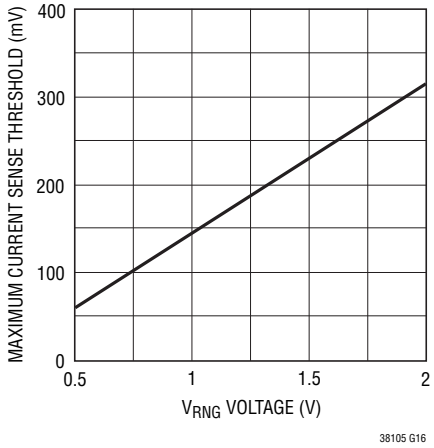
38105 G14

Current Limit Foldback



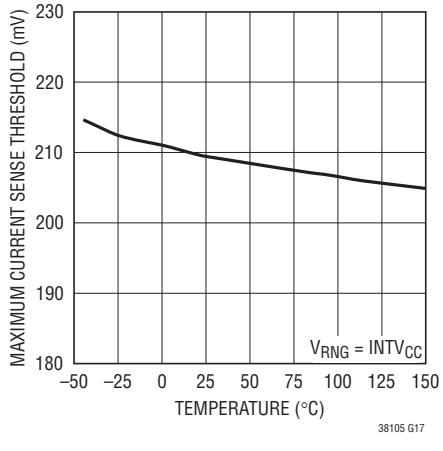
38105 G15

Maximum Current Sense Threshold vs V_{RNG} Voltage



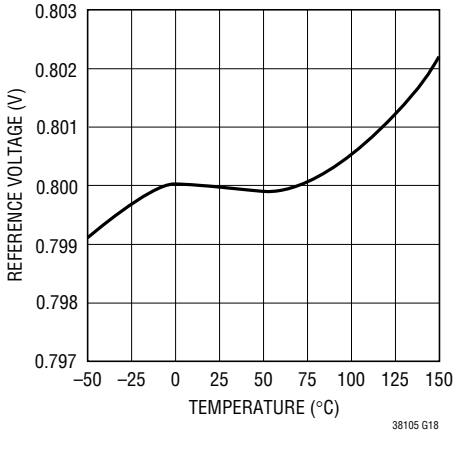
38105 G16

Maximum Current Sense Threshold vs Temperature



38105 G17

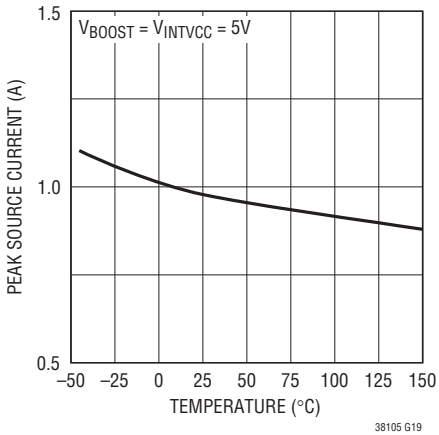
Reference Voltage vs Temperature



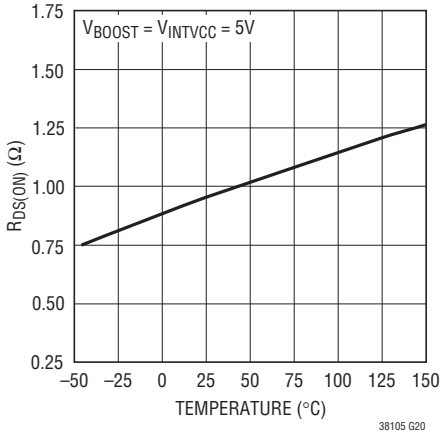
38105 G18

TYPICAL PERFORMANCE CHARACTERISTICS

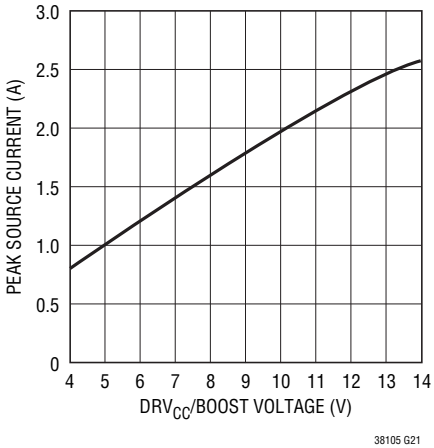
Driver Peak Source Current vs Temperature



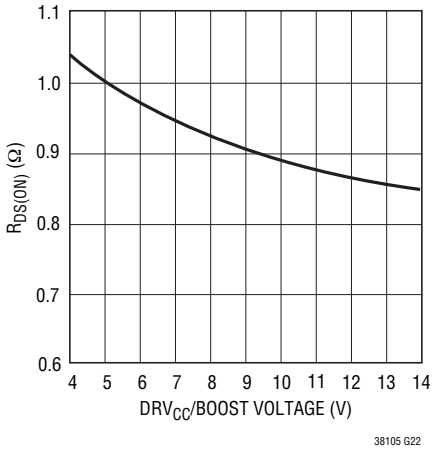
Driver Pull-Down $R_{DS(ON)}$ vs Temperature



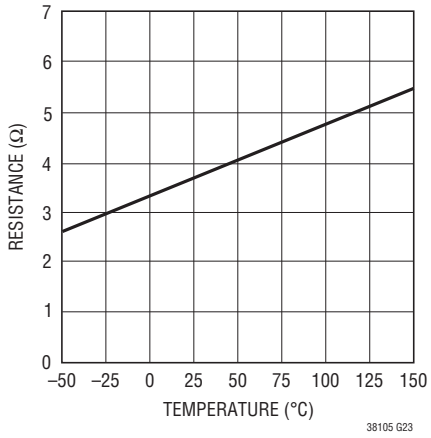
Driver Peak Source Current vs Supply Voltage



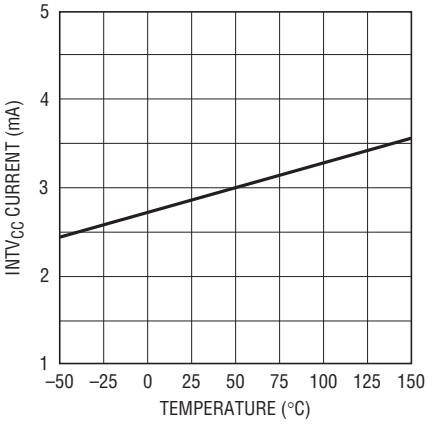
Driver Pull-Down $R_{DS(ON)}$ vs Supply Voltage



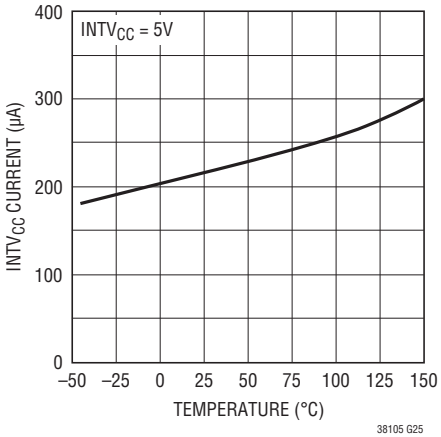
$EXTV_{CC}$ LDO Resistance at Dropout vs Temperature



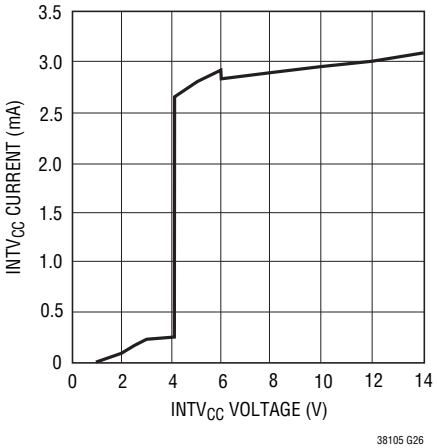
$INTV_{CC}$ Current vs Temperature



$INTV_{CC}$ Shutdown Current vs Temperature

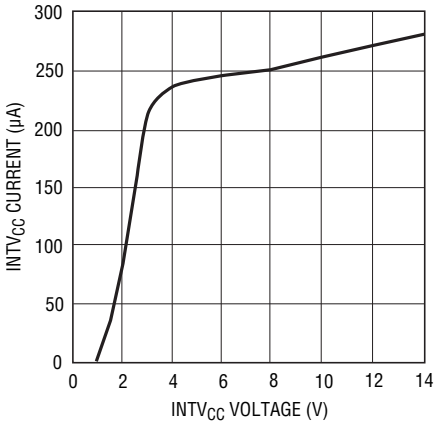


$INTV_{CC}$ Current vs $INTV_{CC}$ Voltage

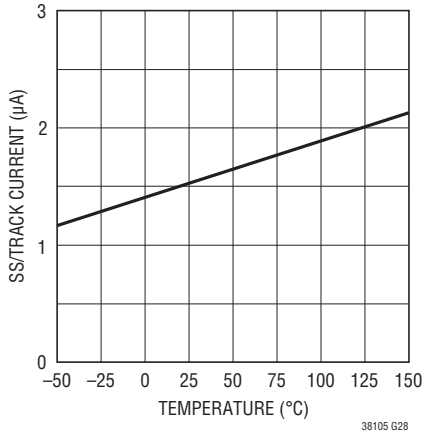


TYPICAL PERFORMANCE CHARACTERISTICS

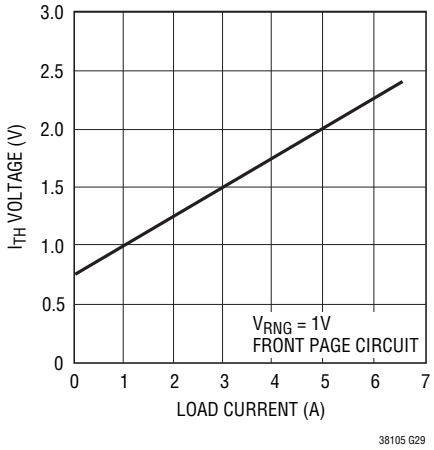
$INTV_{CC}$ Shutdown Current vs $INTV_{CC}$ Voltage



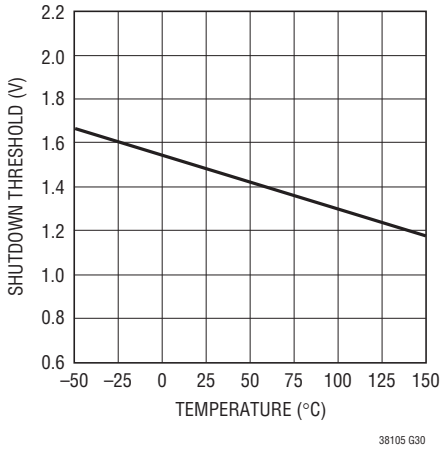
SS/TRACK Pull-Up Current vs Temperature



I_{TH} Voltage vs Load Current



Shutdown Threshold vs Temperature



PIN FUNCTIONS

V_{ON} (Pin 2): On-Time Voltage Input. Voltage trip point for the on-time comparator. Tying this pin to the output voltage or to an external resistive divider from the output makes the on-time proportional to V_{OUT}. The comparator defaults to 0.7V when the pin is grounded and defaults to 2.4V when the pin is connected to $INTV_{CC}$. Tie this pin to $INTV_{CC}$ in high V_{OUT} applications to use a lower R_{ON} value.

V_{RNG} (Pin 3): Sense Voltage Limit Set. The voltage at this pin sets the nominal sense voltage at maximum output current and can be set from 0.5V to 2V by a resistive divider from $INTV_{CC}$. The nominal sense voltage defaults to 95mV when this pin is tied to ground, and 215mV when tied to $INTV_{CC}$.

PGOOD (Pin 4): Power Good Output. Open-drain logic output that is pulled to ground when the output voltage is not between ±10% of the regulation point. The output voltage must be out of regulation for at least 120µs before the power good output is pulled to ground.

MODE/SYNC (Pin 5): Pulse Skip Mode Enable/Sync Pin. This multifunction pin provides pulse skip mode enable/disable control and an external clock input to the phase detector. Pulling this pin below 0.8V or to an external logic-level synchronization signal disables pulse skip mode operation and forces continuous operation. Pulling this pin above 0.8V enables pulse skip mode operation. For a clock input, the phase-locked loop will force the rising top gate signal to be synchronized with the rising edge of the clock signal.This pin can also be connected to a feedback resistor divider from a secondary winding on the inductor to regulate a second output voltage.

I_{TH} (Pin 6): Error Amplifier Compensation Point and Current Control Threshold. The current comparator threshold increases with this control voltage. The voltage ranges from 0V to 2.6V with 1.2V corresponding to zero sense voltage (zero current).

V_{FB} (Pin 7): Feedback Input. Connect V_{FB} through a resistor divider network to V_{OUT} to set the output voltage.

PLL/LPF (Pin 8): The phase-locked loop's lowpass filter is tied to this pin. The voltage at this pin defaults to 1.2V when the IC is not synchronized with an external clock at the MODE/SYNC pin.

SS/TRACK (Pin 9): Soft-Start/Tracking Input. For soft-start, a capacitor to ground at this pin sets the ramp rate of the output voltage (approximately 0.6s/µF). For coincident or ratiometric tracking, connect this pin to a resistive divider between the voltage to be tracked and ground.

$\overline{SHDN}$ (Pin 12): Shutdown Pin. Pulling this pin below 1.5V will shut down the LTC3810-5, turn off both of the external MOSFET switches and reduce the quiescent supply current to 240µA.

UVIN (Pin 13): UVLO Input. This pin is input to the internal UVLO and is compared to an internal 0.8V reference. An external resistor divider is connected to this pin and the input supply to program the undervoltage lockout voltage. When UVIN is less than 0.8V, the LTC3810-5 is shut down.

NDRV (Pin 14): Drive Output for External Pass Device of the Linear Regulator for $INTV_{CC}$. Connect to the gate of an external NMOS pass device and a pull-up resistor to the input voltage V_{IN}.

$EXTV_{CC}$ (Pin 15): External Driver Supply Voltage. When this voltage exceeds 4.7V, an internal switch connects this pin to $INTV_{CC}$ through an LDO and turns off the exter nal MOSFET connected to NDRV, so that controller and gate drive are drawn from $EXTV_{CC}$.

$INTV_{CC}$ (Pin 16): Main Supply Pin. All internal circuits except the output drivers are powered from this pin. $INTV_{CC}$ should be bypassed to ground (Pin 10) with at least a 0.1µF capacitor in close proximity to the LTC3810-5.

DRV_{CC} (Pin 17): Driver Supply Pin. DRV_{CC} supplies power to the BG output driver. This pin is normally connected to $INTV_{CC}$. DRV_{CC} should be bypassed to BGRTN (Pin 20) with a low ESR (X5R or better) 1µF-10µF capacitor in close proximity to the LTC3810-5.

PIN FUNCTIONS

BG (Pin 18): Bottom Gate Drive. The BG pin drives the gate of the bottom N-channel synchronous switch MOSFET. This pin swings from BGRTN to DRV_{CC}.

BGRTN (Pin 19): Bottom Gate Return. This pin connects to the source of the pulldown MOSFET in the BG driver and is normally connected to ground. Connecting a negative supply to this pin allows the synchronous MOSFET's gate to be pulled below ground to help prevent false turn-on during high dV/dt transitions on the SW node. See the Applications Information section for more details.

$SENSE^+$, $SENSE^-$ (Pin 24, Pin 20): Current Sense Comparator Input. The (+) input to the current comparator is normally connected to SW unless using a sense resistor. The (–) input is used to accurately kelvin sense the bottom side of the sense resistor or MOSFET.

SW (Pin 25): Switch Node Connection to Inductor and Bootstrap Capacitor. The voltage swing at this pin is –0.7V (a Schottky diode (external) voltage drop) to V_{IN}.

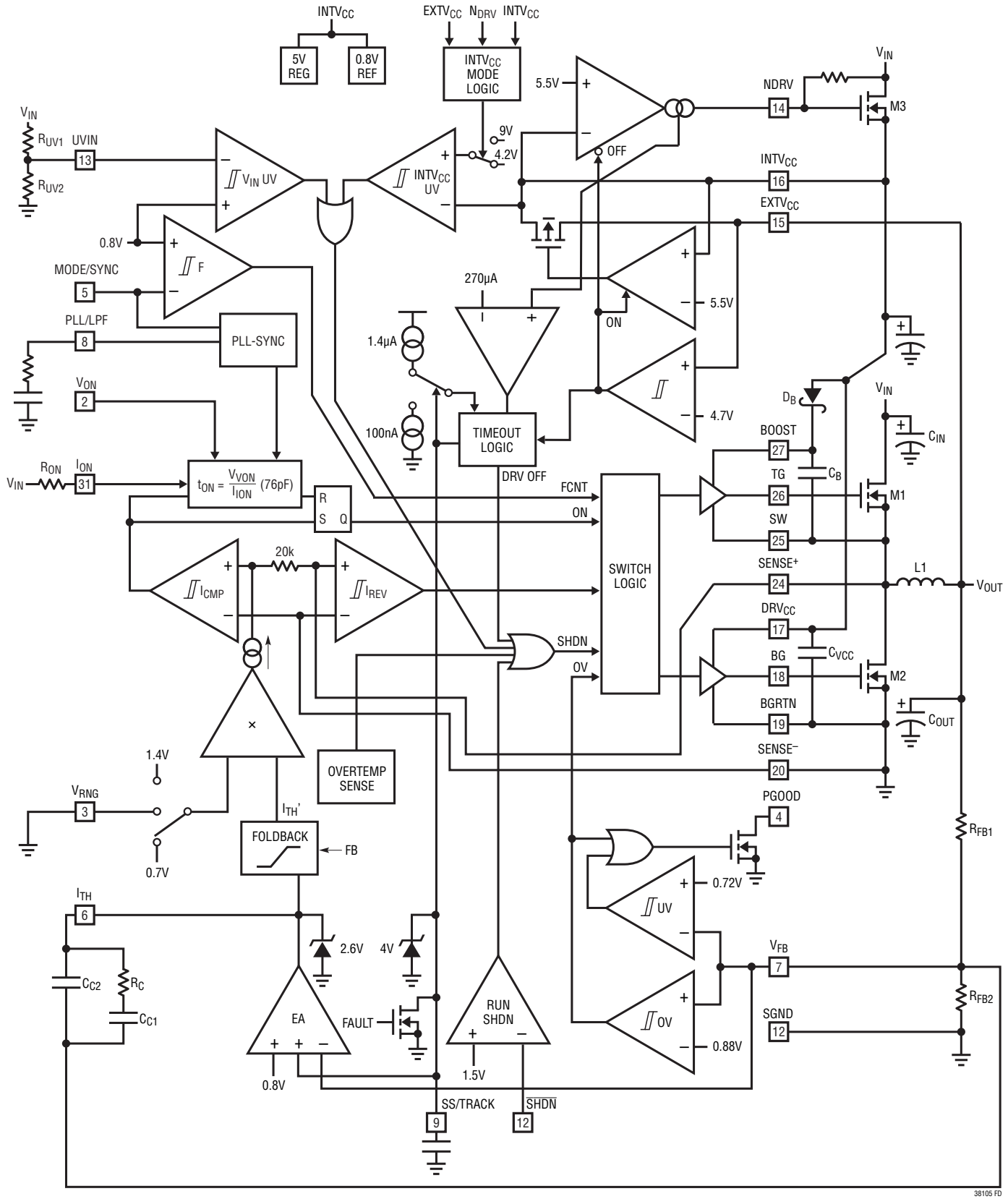
TG (Pin 26): Top Gate Drive. The TG pin drives the gate of the top N-channel synchronous switch MOSFET. The TG driver draws power from the BOOST pin and returns to the SW pin, providing true floating drive to the top MOSFET.

BOOST (Pin 27): Top Gate Driver Supply. The BOOST pin supplies power to the floating TG driver. BOOST should be bypassed to SW with a low ESR (X5R or better) 0.1µF capacitor. An additional fast recovery Schottky diode from DRV_{CC} to the BOOST pin will create a complete floating charge-pumped supply at BOOST.

I_{ON} (Pin 31): On-Time Current Input. Tie a resistor from V_{IN} to this pin to set the one-shot timer current and thereby set the switching frequency.

SGND (Exposed Pad Pin 33): Signal Ground. All small-signal components should connect to this ground and eventually connect to PGND at one point.

FUNCTIONAL DIAGRAM



OPERATION

Main Control Loop

The LTC3810-5 is a current mode controller for DC/DC step-down converters. In normal operation, the top MOSFET is turned on for a fixed interval determined by a one-shot timer (OST). When the top MOSFET is turned off, the bottom MOSFET is turned on until the current comparator I_{CMP} trips, restarting the one-shot timer and initiating the next cycle. Inductor current is determined by sensing the voltage between the $SENSE^-$ and $SENSE^+$ pins using a sense resistor or the bottom MOSFET on-resistance. The voltage on the I_{TH} pin sets the comparator threshold corresponding to the inductor valley current. The fast 25MHz error amplifier EA adjusts this voltage by comparing the feedback signal V_{FB} to the internal 0.8V reference voltage. If the load current increases, it causes a drop in the feedback voltage relative to the reference. The I_{TH} voltage then rises until the average inductor current again matches the load current.

The operating frequency is determined implicitly by the top MOSFET on-time and the duty cycle required to maintain regulation. The one-shot timer generates an on time that is proportional to the ideal duty cycle, thus holding frequency approximately constant with changes in V_{IN}. The nominal frequency can be adjusted with an external resistor R_{ON}.

For applications with stringent constant frequency requirements, the LTC3810-5 can be synchronized with an external clock. By programming the nominal frequency the same as the external clock frequency, the LTC3810-5 behaves as a constant frequency part against the load and supply variations.

Pulling the $\overline{SHDN}$ pin low forces the controller into its shutdown state, turning off both M1 and M2. Forcing a voltage above 1.5V will turn on the device.

Pulse Skip Mode

The LTC3810-5 can operate in one of two modes selectable with the MODE/SYNC pin—pulse skip mode or forced continuous mode (see Figure 1). Pulse skip mode is selected when increased efficiency at light loads is desired (see Figure 2). In this mode, the bottom MOSFET is turned off when inductor current reverses to minimize efficiency loss due to reverse current flow and gate charge switching. At low load currents, I_{TH} will drop below the zero current level (1.2V) shutting off both switches. Both switches will remain off with the output capacitor supplying the load current until the I_{TH} voltage rises above the zero current level to initiate another cycle. In this mode, frequency is proportional to load current at light loads.

Pulse skip mode operation is disabled by comparator F when the MODE/SYNC pin is brought below 0.8V, forcing continuous synchronous operation. Forced continuous mode is less efficient due to resistive losses, but has the advantage of better transient response at low currents, approximately constant frequency operation, and the ability to maintain regulation when sinking current.

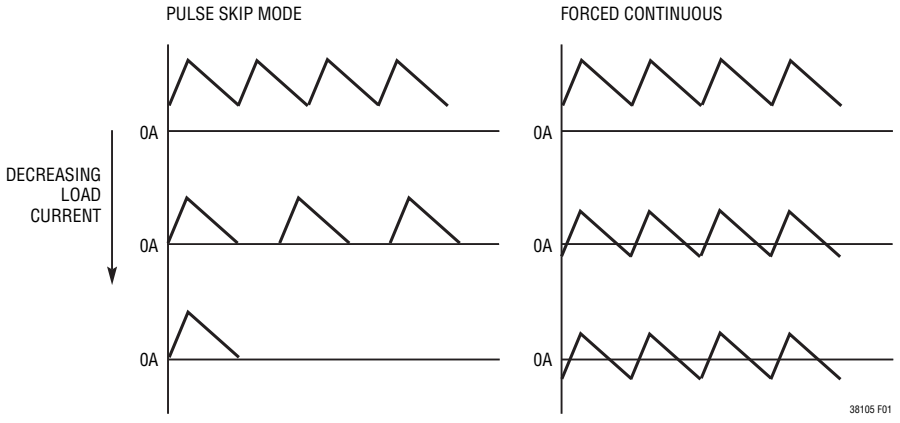


Figure 1. Comparison of Inductor Current Waveforms for Pulse Skip Mode and Forced Continuous Operation

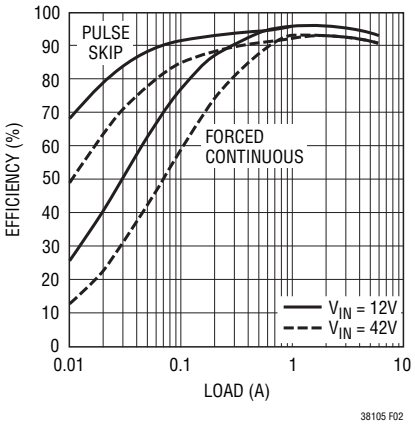


Figure 2. Efficiency in Pulse Skip/ Forced Continuous Modes

OPERATION

Fault Monitoring/Protection

Constant on-time current mode architecture provides accurate cycle-by-cycle current limit protection—a feature that is very important for protecting the high voltage power supply from output short circuits. The cycle-by-cycle current monitor guarantees that the inductor current will never exceed the value programmed on the V_{RNG} pin.

Foldback current limiting provides further protection if the output is shorted to ground. As V_{FB} drops, the buffered current threshold voltage I_{THB} is pulled down and clamped to 1V. This reduces the inductor valley current level to one-sixth of its maximum value as V_{FB} approaches 0V. Foldback current limiting is disabled at start-up.

Overvoltage and undervoltage comparators OV and UV pull the PGOOD output low if the output feedback voltage exits a ±10% window around the regulation point after the internal 120µs power bad mask timer expires. Furthermore, in an overvoltage condition, M1 is turned off and M2 is turned on immediately and held on until the overvoltage condition clears.

The LTC3810-5 provides two undervoltage lockout comparators—one for the $INTV_{CC}/DRV_{CC}$ supply and one for the input supply V_{IN}. The $INTV_{CC}$ UV threshold is 4.2V to guarantee that the MOSFETs have sufficient gate drive voltage before turning on. The V_{IN} UV threshold (UVIN pin) is 0.8V with 10% hysteresis which allows programming the V_{IN} threshold with the appropriate resistor divider connected to V_{IN}. If either comparator inputs are under the UV threshold, the LTC3810-5 is shut down and the drivers are turned off.

Strong Gate Drivers

The LTC3810-5 contains very low impedance drivers capable of supplying amps of current to slew large MOSFET gates quickly. This minimizes transition losses and allows paralleling MOSFETs for higher current applications. A 60V floating high side driver drives the top side MOSFET and a low side driver drives the bottom side MOSFET (see Figure 3). The bottom side driver is supplied directly from the DRV_{CC} pin. The top MOSFET drivers are biased from floating bootstrap capacitor, C_B, which normally is recharged during each off cycle through an external diode from DRV_{CC} when the top MOSFET turns off. In pulse skip mode operation, where it is possible that the bottom MOSFET will be off for an extended period of time, an internal timeout guarantees that the bottom MOSFET is turned on at least once every 25µs for one on-time period to refresh the bootstrap capacitor.

The bottom driver has an additional feature that helps minimize the possibility of external MOSFET shoot-through. When the top MOSFET turns on, the switch node dV/dt pulls up the bottom MOSFET's internal gate through the Miller capacitance, even when the bottom driver is holding the gate terminal at ground. If the gate is pulled up high enough, shoot-through between the top side and bottom side MOSFETs can occur. To prevent this from occurring, the bottom driver return is brought out as a separate pin (BGRTN) so that a negative supply can be used to reduce the effect of the Miller pull-up. For example, if a –2V supply is used on BGRTN, the switch node dV/dt could pull the gate up 2V before the V_{GS} of the bottom MOSFET has more than 0V across it.

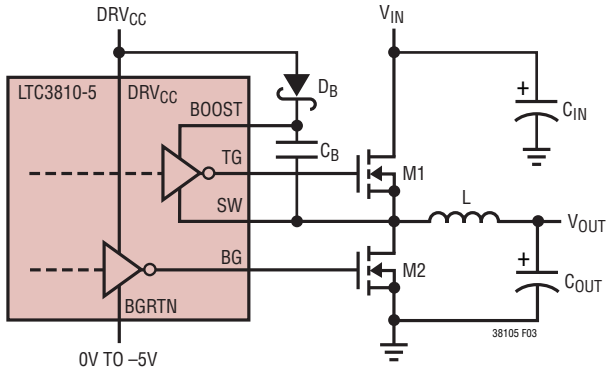


Figure 3. Floating TG Driver Supply and Negative BG Return

IC/Driver Supply Power

The LTC3810-5's internal control circuitry and top and bottom MOSFET drivers operate from a supply voltage ($INTV_{CC}$, DRV_{CC} pins) in the range of 4.5V to 14V. The LTC3810-5 has two integrated linear regulator controllers to easily generate this IC/driver supply from either the high voltage input or from the output voltage. For best efficiency the supply is derived from the input voltage during start-up and then derived from the lower voltage output as soon as the output is higher than 4.7V. Alternatively, the supply can be derived from the input continuously if the output is

OPERATION

<4.7V or an external supply in the appropriate range can be used. The LTC3810-5 will automatically detect which mode is being used and operate properly.

The four possible operating modes for generating this supply are summarized as follows (see Figure 4):

1. LTC3810-5 generates a 5.5V start-up supply from a small external SOT23 N-channel MOSFET acting as linear regulator with drain connected to V_{IN} and gate controlled by the LTC3810-5's internal linear regulator controller through the NDRV pin. As soon as the output voltage reaches 4.7V, the 5.5V IC/driver supply is derived from the output through an internal low-dropout regulator to optimize efficiency. If the output is lost due to a short, the LTC3810-5 goes through repeated low duty cycle soft-start cycles (with the drivers shut off in between) to attempt to bring up the output without burning up the SOT23 MOSFET. This scheme eliminates the long start-up times associated with a conventional trickle charger by using an external MOSFET to quickly charge the IC/driver supply capacitors (C_{INTVCC}, C_{DRVCC}).
2. Similar to (1) except that the external MOSFET is used for continuous IC/driver power instead of just for start-up. The MOSFET is sized for proper dissipation and the driver shutdown/restart for $V_{OUT} < 4.7V$ is disabled. This scheme is less efficient but may be necessary if $V_{OUT} < 4.7V$ and a boost network is not desired.
3. Trickle charge mode provides an even simpler approach by eliminating the external MOSFET. The IC/driver supply capacitors are charged through a single high-valued resistor connected to the input supply. When the $INTV_{CC}$ voltage reaches the turn-on threshold of 9V (automatically raised from 4.7V to provide extra headroom for start-up), the drivers turn on and begin charging up the output capacitor. When the output reaches 4.7V, IC/driver power is derived from the output. In trickle-charge mode, the supply capacitors must have sufficient capacitance such that they are not discharged below the 4V $INTV_{CC}$ UV threshold before the output is high enough to take over or else the power supply will not start.
4. Low voltage supply available. The simplest approach is if a low voltage supply (between 4.5V and 14V) is available and connected directly to the IC/driver supply pins.

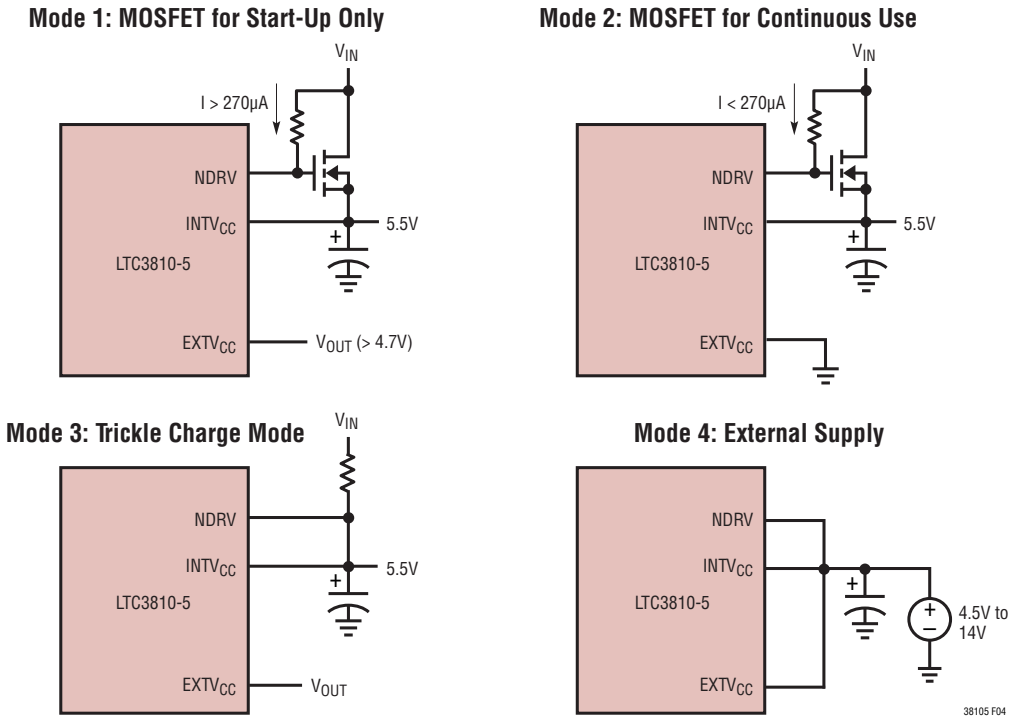


Figure 4. Operating Modes for IC/Driver Supply

APPLICATIONS INFORMATION

The basic LTC3810-5 application circuit is shown on the first page of this data sheet. External component selection is primarily determined by the maximum input voltage and load current and begins with the selection of the sense resistance and power MOSFET switches. The LTC3810-5 uses either a sense resistor or the on-resistance of the synchronous power MOSFET for determining the inductor current. The desired amount of ripple current and operating frequency largely determines the inductor value. Next, C_{IN} is selected for its ability to handle the large RMS current into the converter and C_{OUT} is chosen with low enough ESR to meet the output voltage ripple and transient specification. Finally, loop compensation components are selected to meet the required transient/phase margin specifications.

Maximum Sense Voltage and V_{RNG} Pin

Inductor current is determined by measuring the voltage across a sense resistance that appears between the $SENSE^-$ and $SENSE^+$ pins. The maximum sense voltage is set by the voltage applied to the V_{RNG} pin and is equal to approximately:

$$V_{SENSE(MAX)} = 0.173V_{RNG} – 0.026$$

The current mode control loop will not allow the inductor current valleys to exceed $V_{SENSE(MAX)}/R_{SENSE}$. In practice, one should allow some margin for variations in the LTC3810-5 and external component values and a good guide for selecting the sense resistance is:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{1.3 \bullet I_{OUT(MAX)}}$$

An external resistive divider from $INTV_{CC}$ can be used to set the voltage of the V_{RNG} pin between 0.5V and 2V resulting in nominal sense voltages of 60mV to 320mV. Additionally, the V_{RNG} pin can be tied to SGND or $INTV_{CC}$ in which case the nominal sense voltage defaults to 95mV or 215mV, respectively.

Connecting the $SENSE^+$ and $SENSE^-$ Pins

The LTC3810-5 can be used with or without a sense resistor. When using a sense resistor, place it between the source of the bottom MOSFET, M2 and PGND. Connect the $SENSE^+$ and $SENSE^-$ pins to the top and bottom of the sense resistor. Using a sense resistor provides a well defined current limit, but adds cost and reduces efficiency. Alternatively, one can eliminate the sense resistor and use the bottom MOSFET as the current sense element by simply connecting the $SENSE^+$ pin to the lower MOSFET drain and $SENSE^-$ pin to the MOSFET source. This improves efficiency, but one must carefully choose the MOSFET on-resistance, as discussed below.

Power MOSFET Selection

The LTC3810-5 requires two external N-channel power MOSFETs, one for the top (main) switch and one for the bottom (synchronous) switch. Important parameters for the power MOSFETs are the breakdown voltage BV_{DSS}, threshold voltage $V_{(GS)TH}$, on-resistance $R_{DS(ON)}$, input capacitance and maximum current $I_{DS(MAX)}$.

When the bottom MOSFET is used as the current sense element, particular attention must be paid to its on-resistance. MOSFET on-resistance is typically specified with a maximum value $R_{DS(ON)(MAX)}$ at 25°C. In this case, additional margin is required to accommodate the rise in MOSFET on-resistance with temperature:

$$R_{DS(ON)(MAX)} = \frac{R_{SENSE}}{\rho_T}$$

The ρ_T term is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature (see Figure 5) and typically varies from 0.4%/°C to 1.0%/°C depending on the particular MOSFET used.

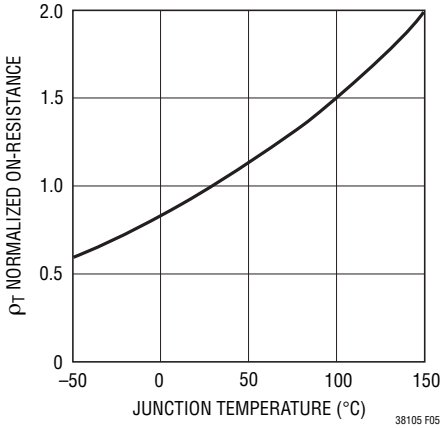


Figure 5. $R_{DS(ON)}$ vs Temperature

APPLICATIONS INFORMATION

The most important parameter in high voltage applications is breakdown voltage BV_{DSS}. Both the top and bottom MOSFETs will see full input voltage plus any additional ringing on the switch node across its drain-to-source during its off-time and must be chosen with the appropriate breakdown specification. The LTC3810-5 is designed to be used with a 4.5V to 14V gate drive supply (DRV_{CC} pin) for driving logic-level MOSFETs ($V_{GS(MIN)} \geq 4.5V$).

For maximum efficiency, on-resistance $R_{DS(ON)}$ and input capacitance should be minimized. Low $R_{DS(ON)}$ minimizes conduction losses and low input capacitance minimizes transition losses. MOSFET input capacitance is a combination of several components but can be taken from the typical "gate charge" curve included on most data sheets (Figure 6).

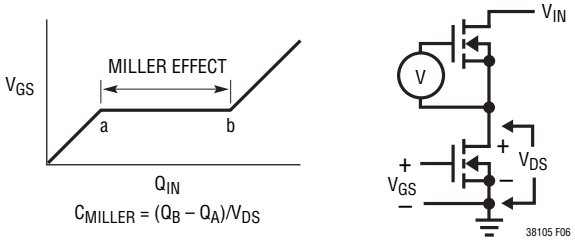


Figure 6. Gate Charge Characteristic

The curve is generated by forcing a constant input current into the gate of a common source, current source loaded stage and then plotting the gate voltage versus time. The initial slope is the effect of the gate-to-source and the gate-to-drain capacitance. The flat portion of the curve is the result of the Miller multiplication effect of the drain-to-gate capacitance as the drain drops the voltage across the current source load. The upper sloping line is due to the drain-to-gate accumulation capacitance and the gate-to-source capacitance. The Miller charge (the increase in coulombs on the horizontal axis from a to b while the curve is flat) is specified for a given V_{DS} drain voltage, but can be adjusted for different V_{DS} voltages by multiplying by the ratio of the application V_{DS} to the curve specified V_{DS} values. A way to estimate the C_{MILLER} term is to take the change in gate charge from points a and b on a manufacturers data sheet and divide by the stated V_{DS} voltage specified. C_{MILLER} is the most important selection criteria for determining the transition loss term in the top MOSFET but is not directly specified on MOSFET data sheets. C_{RSS} and C_{OS} are specified sometimes but definitions of these parameters are not included.

When the controller is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The power dissipation for the main and synchronous MOSFETs at maximum output current are given by:

$$P_{TOP} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(\rho_T)R_{DS(ON)} + V_{IN}{}^2\frac{I_{MAX}}{2}(R_{DR})(C_{MILLER})\bullet\left[\frac{1}{V_{CC} - V_{TH(IL)}} + \frac{1}{V_{TH(IL)}}\right](f)$$

$$P_{BOT} = \frac{V_{IN} - V_{OUT}}{V_{IN}}(I_{MAX})^2(\rho_T)R_{DS(0N)}$$

where ρ_T is the temperature dependency of $R_{DS(ON)}$, R_{DR} is the effective top driver resistance (approximately 2Ω at $V_{GS} = V_{MILLER}$), V_{IN} is the drain potential and the change in drain potential in the particular application. $V_{TH(IL)}$ is the data sheet specified typical gate threshold voltage specified in the power MOSFET data sheet at the specified drain current. C_{MILLER} is the calculated capacitance using the gate charge curve from the MOSFET data sheet and the technique described above.

Both MOSFETs have I^2R losses while the topside N-channel equation incudes an additional term for transition losses, which peak at the highest input voltage. For high input voltage low duty cycle applications that are typical for the LTC3810-5, transition losses are the dominate loss term and therefore using higher $R_{DS(ON)}$ device with lower C_{MILLER} usually provides the highest efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of

APPLICATIONS INFORMATION

the period. Since there is no transition loss term in the synchronous MOSFET, optimal efficiency is obtained by minimizing $R_{DS(ON)}$—by using larger MOSFETs or paralleling multiple MOSFETs.

Multiple MOSFETs can be used in parallel to lower $R_{DS(ON)}$ and meet the current and thermal requirements if desired. The LTC3810-5 contains large low impedance drivers capable of driving large gate capacitances without significantly slowing transition times. In fact, when driving MOSFETs with very low gate charge, it is sometimes helpful to slow down the drivers by adding small gate resistors (10Ω or less) to reduce noise and EMI caused by the fast transitions.

Operating Frequency

The choice of operating frequency is a tradeoff between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses but requires larger inductance and/or capacitance in order to maintain low output ripple voltage.

The operating frequency of LTC3810-5 applications is determined implicitly by the one-shot timer that controls the on-time, t_{ON}, of the top MOSFET switch. The on-time is set by the current out of the I_{ON} pin and the voltage at the V_{ON} pin according to:

$$t_{ON} = \frac{V_{VON}}{I_{ION}}(76pF)$$

Tying a resistor R_{ON} from V_{IN} to the I_{ON} pin yields an on-time inversely proportional to V_{IN}. For a step-down converter, this results in approximately constant frequency operation as the input supply varies:

$$f = \frac{V_{OUT}}{V_{VON} \bullet R_{ON}(76pF)}[H_Z]$$

To hold frequency constant during output voltage changes, tie the V_{ON} pin to V_{OUT} or to a resistive divider from V_{OUT} when $V_{OUT} > 2.4V$. The V_{ON} pin has internal clamps that limit its input to the one-shot timer. If the pin is tied below 0.7V, the input to the one-shot is clamped at 0.7V. Similarly, if the pin is tied above 2.4V, the input is clamped at 2.4V. In high V_{OUT} applications, tie V_{ON} to $INTV_{CC}$. Figures 7a and 7b show how R_{ON} relates to switching frequency for several common output voltages.

Changes in the load current magnitude will cause frequency shift. Parasitic resistance in the MOSFET switches and inductor reduce the effective voltage across the inductance, resulting in increased duty cycle as the load current increases. By lengthening the on-time slightly as current increases, constant frequency operation can be maintained. This is accomplished with a resistive divider from the I_{TH} pin to the V_{ON} pin and V_{OUT}. The values required will depend on the parasitic resistances in the specific application. A good starting point is to feed about 25% of the voltage change at the I_{TH} pin to the V_{ON} pin as shown in Figure 8. Place capacitance on the V_{ON} pin to filter out the I_{TH} variations at the switching frequency.

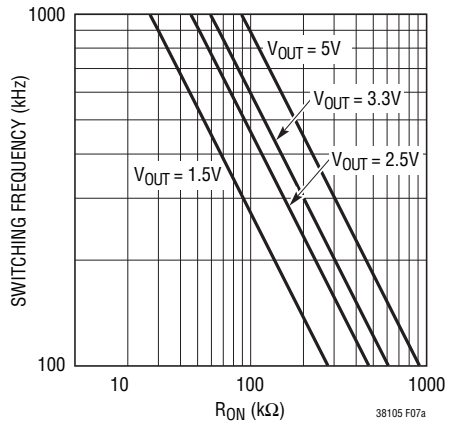


Figure 7a. Switching Frequency vs R_{ON} (V_{ON} = 0V)

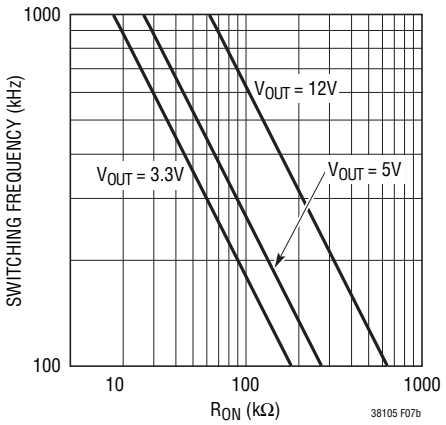


Figure 7b. Switching Frequency vs R_{ON} (V_{ON} = $INTV_{CC}$)

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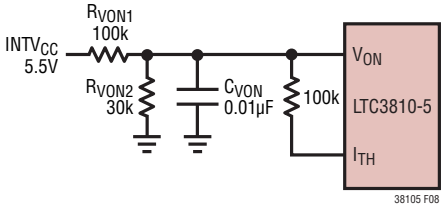


Figure 8. Correcting Frequency Shift with Load Current Changes

Minimum Off-Time and Dropout Operation

The minimum off-time $t_{OFF(MIN)}$ is the smallest amount of time that the LTC3810-5 is capable of turning on the bottom MOSFET, tripping the current comparator and turning the MOSFET back off. This time is generally about 250ns. The minimum off-time limit imposes a maximum duty cycle of $t_{ON}/(t_{ON} + t_{OFF(MIN)})$. If the maximum duty cycle is reached, due to a dropping input voltage for example, then the output will drop out of regulation. The minimum input voltage to avoid dropout is:

$$V_{IN(MIN)} = V_{OUT} \frac{t_{ON} + t_{OFF(MIN)}}{t_{ON}}$$

A plot of maximum duty cycle vs frequency is shown in Figure 9.

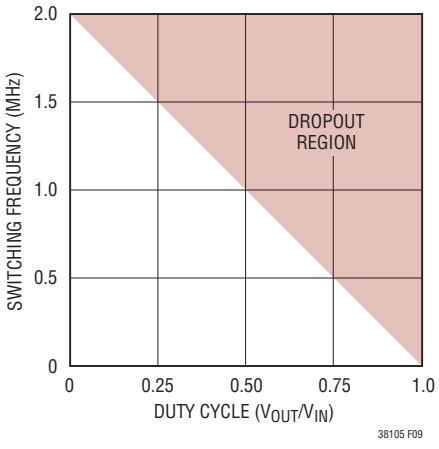


Figure 9. Maximum Switching Frequency vs Duty Cycle

Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \left(\frac{V_{OUT}}{f\,L}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a tradeoff between component size, efficiency and operating frequency.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. The largest ripple current occurs at the highest V_{IN}. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \left(\frac{V_{OUT}}{f\,\Delta I_{L(MAX)}}\right)\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool Mμ® cores. A variety of inductors designed for high current, low voltage applications are available from manufacturers such as Sumida, Panasonic, Coiltronics, Coilcraft and Toko.

Schottky Diode D1 Selection

The Schottky diode D1 shown in the front page schematic conducts during the dead time between the conduction of the power MOSFET switches. It is intended to prevent the body diode of the bottom MOSFET from turning on and storing charge during the dead time, which can cause a modest (about 1%) efficiency loss. The diode can be rated for about one-half to one-fifth of the full load current since it is on for only a fraction of the duty cycle. In order for the diode to be effective, the inductance between it

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and the bottom MOSFET must be as small as possible, mandating that these components be placed adjacently. The diode can be omitted if the efficiency loss is tolerable.

Input Capacitor Selection

In continuous mode, the drain current of the top MOSFET is approximately a square wave of duty cycle V_{OUT}/V_{IN} which must be supplied by the input capacitor. To prevent large input transients, a low ESR input capacitor sized for the maximum RMS current is given by:

$$I_{CIN(RMS)} \cong I_{O(MAX)} \frac{V_{OUT}}{V_{IN}} \left(\frac{V_{IN}}{V_{OUT}} - 1 \right)^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{O(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be placed in parallel to meet size or height requirements in the design.

Because tantalum and OS-CON capacitors are not available in voltages above 30V, ceramics or aluminum electrolytics must be used for regulators with input supplies above 30V. Ceramic capacitors have the advantage of very low ESR and can handle high RMS current, but ceramics with high voltage ratings (> 50V) are not available with more than a few microfarads of capacitance. Furthermore, ceramics have high voltage coefficients which means that the capacitance values decrease even more when used at the rated voltage. X5R and X7R type ceramics are recommended for their lower voltage and temperature coefficients. Another consideration when using ceramics is their high Q which, if not properly damped, may result in excessive voltage stress on the power MOSFETs. Aluminum electrolytics have much higher bulk capacitance, but they have higher ESR and lower RMS current ratings.

A good approach is to use a combination of aluminum electrolytics for bulk capacitance and ceramics for low ESR and RMS current. If the RMS current cannot be handled by the aluminum capacitors alone, when used together, the percentage of RMS current that will be supplied by the aluminum capacitor is reduced to approximately:

$$\%\, I_{RMS,ALUM} \approx \frac{1}{\sqrt{1+(8fCR_{ESR})^2}} \bullet 100\%$$

where R_{ESR} is the ESR of the aluminum capacitor and C is the overall capacitance of the ceramic capacitors. Using an aluminum electrolytic with a ceramic also helps damp the high Q of the ceramic, minimizing ringing.

Output Capacitor Selection

The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple. The output ripple (ΔV_{OUT}) is approximately equal to:

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

Since ΔI_L increases with input voltage, the output ripple is highest at maximum input voltage. ESR also has a significant effect on the load transient response. Fast load transitions at the output will appear as voltage across the ESR of C_{OUT} until the feedback loop in the LTC3810-5 can change the inductor current to match the new load current value. Typically, once the ESR requirement is satisfied the capacitance is adequate for filtering and has the required RMS current rating.

Manufacturers such as Nichicon, Nippon Chemi-Con and Sanyo should be considered for high performance throughhole capacitors. The OS-CON (organic semiconductor dielectric) capacitor available from Sanyo has the lowest product of ESR and size of any aluminum electrolytic at a somewhat higher price. An additional ceramic capacitor in parallel with OS-CON capacitors is recommended to reduce the effect of their lead inductance.

In surface mount applications, multiple capacitors placed in parallel may be required to meet the ESR, RMS current handling and load step requirements. Dry tantalum, special polymer and aluminum electrolytic capacitors are available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density

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than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Several excellent surge-tested choices are the AVX, TPS and TPSV or the KEMET T510 series. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-driven applications providing that consideration is given to ripple current ratings and long term reliability. Other capacitor types include Panasonic SP and Sanyo POSCAPs.

Output Voltage

The LTC3810-5 output voltage is set by a resistor divider according to the following formula:

$$V_{OUT} = 0.8V\left(1+\frac{R_{FB1}}{R_{FB2}}\right)$$

The external resistor divider is connected to the output as shown in the Functional Diagram, allowing remote voltage sensing. The resultant feedback signal is compared with the internal precision 800mV voltage reference by the error amplifier. The internal reference has a guaranteed tolerance of less than ±1%. Tolerance of the feedback resistors will add additional error to the output voltage. 0.1% to 1% resistors are recommended.

Input Voltage Undervoltage Lockout

A resistor divider connected from the input supply to the UVIN pin (see Functional Diagram) is used to program the input supply undervoltage lockout thresholds. When the rising voltage at UVIN reaches 0.88V the LTC3810 turns on, and when the falling voltage at UVIN drops below 0.8V, the LTC3810 is shut down—providing 10% hysterisis. The input voltage UVLO thresholds are set by the resistor divider according to the following formulas:

$$V_{IN,FALLING} = 0.8V\ (1 + R_{UV1}/R_{UV2})$$

and

$$V_{IN,RISING} = 0.88V\ (1 + R_{UV1}/R_{UV2})$$

If input supply undervoltage lockout is not needed, it can be disabled by connecting UVIN to $INTV_{CC}$.

Top MOSFET Driver Supply (C_B, D_B)

An external bootstrap capacitor, C_B, connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. This capacitor is charged through diode D_B from DRV_{CC} when the switch node is low. When the top MOSFET turns on, the switch node rises to V_{IN} and the BOOST pin rises to approximately V_{IN} + $INTV_{CC}$. The boost capacitor needs to store about 100 times the gate charge required by the top MOSFET. In most applications 0.1µF to 0.47µF, X5R or X7R dielectric capacitor is adequate.

The reverse breakdown of the external diode, D_B, must be greater than $V_{IN(MAX)}$. Another important consideration for the external diode is the reverse recovery and reverse leakage, either of which may cause excessive reverse current to flow at full reverse voltage. If the reverse current times reverse voltage exceeds the maximum allowable power dissipation, the diode may be damaged. For best results, use an ultrafast recovery diode such as the MMDL770T1.

Bottom MOSFET Driver Return Supply (BGRTN)

The bottom gate driver, BG, switches from DRV_{CC} to BGRTN where BGRTN can be a voltage between ground and –5V. Why not just keep it simple and always connect BGRTN to ground? In high voltage switching converters, the switch node dV/dt can be many volts/ns, which will pull up on the gate of the bottom MOSFET through its Miller capacitance. If this Miller current, times the internal gate resistance of the MOSFET plus the driver resistance, exceeds the threshold of the FET, shoot-through will occur. By using a negative supply on BGRTN, the BG can be pulled below ground when turning the bottom MOSFET off. This provides a few extra volts of margin before the gate reaches the turn-on threshold of the MOSFET. Be aware that the maximum voltage difference between DRV_{CC} and BGRTN is 14V. If, for example, V_{BGRTN} = –2V, the maximum voltage on DRV_{CC} pin is now 12V instead of 14V.

IC/MOSFET Driver Supplies ($INTV_{CC}$ and DRV_{CC})

The LTC3810-5 drivers are supplied from the DRV_{CC} and BOOST pins (see Figure 2), which have an absolute maximum voltage of 14V. Since the main supply voltage,

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V_{IN} is typically much higher than 14V a separate supply for the IC power ($INTV_{CC}$) and driver power (DRV_{CC}) must be used. The LTC3810-5 has integrated bias supply control circuitry that allows the IC/driver supply to be easily generated from V_{IN} and/or V_{OUT} with minimal external components. There are four ways to do this as shown in the simplified schematics of Figure 3 and explained in the following sections.

Using the Linear Regulator for $INTV_{CC}/DRV_{CC}$ Supply

In Mode 1, a small external SOT23 MOSFET, controlled by the NDRV pin, is used to generate a 5.5V start-up supply from V_{IN}. The small SOT23 package can be used because the NMOS is on continuously only during the brief start-up period. As soon as the output voltage reaches 4.7V, the LTC3810-5 turns off the external NMOS and the LTC3810-5 regulates the 5.5V supply from the $EXTV_{CC}$ pin (connected to V_{OUT} or a V_{OUT} derived boost network) through an internal low dropout regulator. For this mode to work properly, $EXTV_{CC}$ must be in the range $4.7V < EXTV_{CC} < 15V$. If $V_{OUT} < 4.7V$, a charge pump or extra winding can be used to raise $EXTV_{CC}$ to the proper voltage, or alternatively, Mode 2 should be used as explained later in this section. If V_{OUT} is shorted or otherwise goes below the minimum 4.5V threshold, the MOSFET connected to V_{IN} is turned back on to maintain the 5.5V supply. However if the output cannot be brought up within a timeout period, the drivers are turned off to prevent the SOT23 MOSFET from overheating. Soft-start cycles are then attempted at low duty cycle intervals to try to bring the output back up (see Figure 10). This fault timeout operation is enabled by choosing the choosing R_{NDRV} such that the resistor current I_{NDRV} is greater than 270µA by using the following formulas:

$$R_{NDRV} \le \frac{P_{MOSFET(MAX)} / I_{CC} - V_{TH}}{270\mu A}$$

where

$$I_{CC} = (f)\left(Q_{G(TOP)} + Q_{G(BOTTOM)}\right) + 3mA$$

and V_{TH} is the threshold voltage of the MOSFET.

The value of R_{NDRV} also affects the $V_{IN(MIN)}$ as follows:

$$V_{IN(MIN)} = V_{INTVCC(MIN)} + (40\mu A)\ R_{NDRV} + V_T \qquad (1)$$

where $V_{INTVCC(MIN)}$ is normally 4.5V for driving logic-level MOSFETs. If minimum V_{IN} is not low enough, consider reducing R_{NDRV} and/or using a Darlington NPN instead of an NMOS to reduce V_T to ~1.4V.

When using R_{NDRV} equal to the computed value, the LTC3810-5 will enable the low duty cycle soft-start retries only when the desired maximum power dissipation, $P_{MOSFET(MAX)}$, in the MOSFET is exceeded and leave the drivers on continuously otherwise. The shutoff/restart times are a function of the TRACK/SS capacitor value.

The external NMOS for the linear regulator should be a standard 3V threshold type (i.e., not a logic-level threshold). The rate of charge of $INTV_{CC}$ from 0V to 5.5V is controlled by the LTC3810-5 to be approximately 75µs regardless of the size of the capacitor connected to the $INTV_{CC}$ pin. The charging current for this capacitor is approximately:

$$I_C = \left(\frac{5.5V}{75\mu s}\right) C_{INTVCC}$$

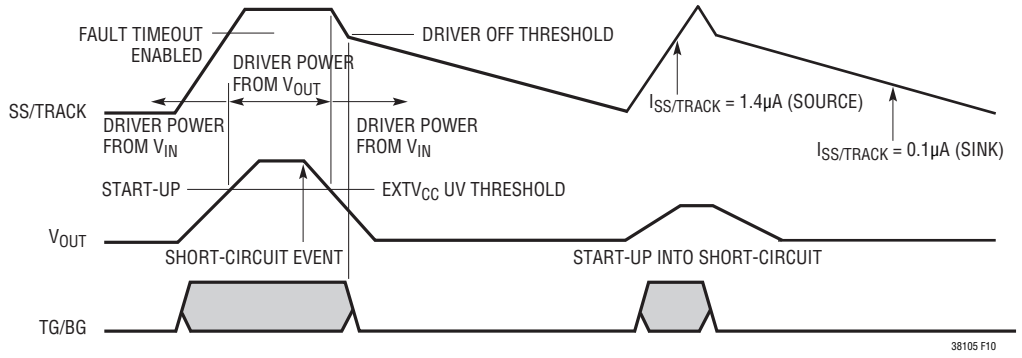


Figure 10. Fault Timeout Operation

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The safe operating area (SOA) for the external NMOS should be chosen so that capacitor charging does not damage the NMOS. Excessive values of capacitor are unnecessary and should be avoided. Typically values in the 1µF to 10µF work well.

One more design requirement for this mode is the minimum soft-start capacitor value. The fault timeout is enabled when SS/TRACK voltage is greater than 4V. This gives the power supply time to bring the output up before it starts the timeout sequence. To prevent timeout sequence from starting prematurely during start-up, a minimum C_{SS} value is necessary to ensure that $V_{SS/TRACK} < 4V$ until $V_{EXTVCC} > 4.7V$. To ensure this, choose:

$$C_{SS} > C_{OUT} \bullet (2.3 \bullet 10^{-6})/I_{OUT(MAX)}$$

Mode 2 should be used if V_{OUT} is outside of the $4.7V < EXTV_{CC} < 15V$ operating range and the extra complexity of a charge pump or extra inductor winding is not wanted to boost this voltage above 4.7V. In this mode, $EXTV_{CC}$ is grounded and the NMOS is chosen to handle the worst-case power dissipation:

$$P_{MOSFET} = \left(V_{IN(MAX)}\right)\left[(f)\left(Q_{G(TOP)} + Q_{G(BOTTOM)}\right) + 3mA\right]$$

To operate properly, the fault timeout operation must be disabled by choosing

$$R_{NDRV} > (V_{IN(MAX)} - 5.5V - V_{TH})/270\mu A$$

If the required R_{NDRV} value results in an unacceptable value for $V_{IN(MIN)}$ (see Equation 1), fault timeout operation can also be disabled by connecting a 500k to 1Meg resistor from SS/TRACK pin to $INTV_{CC}$.

Using Trickle Charge Mode

Trickle charge mode is selected by shorting NDRV and $INTV_{CC}$ and connecting $EXTV_{CC}$ to V_{OUT}. Trickle charge mode has the advantage of not requiring an external MOSFET but takes longer to start up due to slow charge up of C_{INTVCC} and C_{DRVCC} through R_{PULLUP} ($t_{DELAY} = 0.77 \bullet R_{PULLUP} \bullet C_{DRVCC}$) and usually requires larger $INTV_{CC}/DRV_{CC}$ capacitor values to hold up the supply voltage during start-up. Once the $INTV_{CC}/DRV_{CC}$ voltage reaches the trickle charge UV threshold of 9V, the drivers will turn on and start discharging C_{INTVCC}/C_{DRVCC} at a rate determined by the driver current I_G. In order to ensure proper start-up, C_{INTVCC}/C_{DRVCC} must be chosen large enough so that the $EXTV_{CC}$ voltage reaches the switchover threshold of 4.7V before C_{INTVCC}/C_{DRVCC} discharges below the falling UV threshold of 4V. This is ensured if:

$$C_{INTVCC} + C_{DRVCC} > I_G \bullet \left(\text{larger of } \frac{C_{OUT}}{I_{MAX}} \text{ or } \frac{5.5 \bullet 10^5 \bullet C_{SS}}{V_{OUT(REG)}}\right)$$

Where I_G is the gate drive current $= (f)(Q_{G(TOP)} + Q_{G(BOTTOM)})$ and I_{MAX} is the maximum inductor current selected by V_{RNG}.

For R_{PULLUP}, the value should fall in the following range to ensure proper start-up:

$$\text{Min } R_{PULLUP} > (V_{IN(MAX)} - 14V)/I_{CCSR}$$

$$\text{Max } R_{PULLUP} < (V_{IN(MIN)} - 9V)/I_{Q,SHUTDOWN}$$

Using an External Supply Connected to the $INTV_{CC}/DRV_{CC}$ Pins

If an external supply is available between 4.5V and 14V, the supply can be connected directly to the $INTV_{CC}/DRV_{CC}$ pins. In this mode, $INTV_{CC}$, $EXTV_{CC}$ and NDRV must be shorted together.

$INTV_{CC}/DRV_{CC}$ Supply and the $EXTV_{CC}$ Connection

The LTC3810-5 contains an internal low dropout regulator to produce the 5.5V $INTV_{CC}/DRV_{CC}$ supply from the $EXTV_{CC}$ pin voltage. This regulator turns on when the $EXTV_{CC}$ pin is above 4.7V and remains on until $EXTV_{CC}$ drops below 4.45V. This allows the IC/MOSFET power to be derived from the output or an output derived boost network during normal operation and from the external NMOS from V_{IN} during start-up or short-circuit. Using the $EXTV_{CC}$ pin in this way results in significant efficiency gains compared to what would be possible when deriving this power continuously from the typically much higher V_{IN} voltage. The $EXTV_{CC}$ connection also allows the power supply to be configured in trickle charge mode in which it starts up with a high valued "bleed" resistor connected from V_{IN} to $INTV_{CC}$ to charge up the $INTV_{CC}$ capacitor. As soon as the output rises above 4.7V the internal $EXTV_{CC}$ regulator

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takes over before the $INTV_{CC}$ capacitor discharges below the UV threshold. When the $EXTV_{CC}$ regulator is active, the $EXTV_{CC}$ pin can supply up to 50mA RMS. Do not apply more than 15V to the $EXTV_{CC}$ pin. The following list summarizes the possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ grounded. This connection will require $INTV_{CC}$ to be powered continuously from an external NMOS from V_{IN} resulting in an efficiency penalty as high as 10% at high input voltages.
2. $EXTV_{CC}$ connected directly to V_{OUT}. This is the normal connection for 4.7V < V_{OUT} < 15V and provides the highest efficiency. The power supply will start up using an external NMOS or a bleed resistor until the output supply is available.
3. $EXTV_{CC}$ connected to an output-derived boost network. If V_{OUT} < 4.7V. The low voltage output can be boosted using a charge pump or flyback winding to greater than 4.7V.
4. $EXTV_{CC}$ connected to $INTV_{CC}$. This is the required connection for $EXTV_{CC}$ if $INTV_{CC}$ is connected to an external supply where the external supply is 4.5V < V_{EXT} < 15V.

Applications using large MOSFETs with a high input voltage and high frequency of operation may result in a large $EXTV_{CC}$ pin current. Due to the LTC3810-5 thermally enhanced package, maximum junction temperature will rarely be exceeded, however, it is good design practice to verify that the maximum junction temperature rating and RMS current rating are within the maximum limits. Typically, most of the $EXTV_{CC}$ current consists of the MOSFET gates current. In continuous mode operation, this $EXTV_{CC}$ current is:

$$I_{EXTVCC} = f\left(Q_{G(TOP)} + Q_{G(BOTTOM)}\right) + 3mA < 50mA$$

The junction temperature can be estimated from the equations given in Note 2 of the Electrical Characteristics as follows:

$$T_J = T_A + I_{EXTVCC} \bullet (V_{EXTVCC} - V_{INTVCC})(34°C/W)$$

The calculated T_J should be <125°C for E- and I-grade or < 150°C for H-grade. If absolute maximum ratings are exceeded, consider using an external supply connected directly to the $INTV_{CC}$ pin.

FEEDBACK LOOP/COMPENSATION

Feedback Loop Types

In a typical LTC3810-5 circuit, the feedback loop consists of the modulator, the output filter and load, and the feedback amplifier with its compensation network. All of these components affect loop behavior and must be accounted for in the loop compensation. The modulator and output filter consists of the internal current comparator, the output MOSFET drivers and the external MOSFETs, inductor and output capacitor. Current mode control eliminates the effect of the inductor by moving it to the inner loop, reducing it to a first order system. From a feedback loop point of view, it looks like a linear voltage controlled current source from I_{TH} to V_{OUT} and has a gain equal to $(I_{MAX}R_{OUT})/1.2V$. It has fairly benign AC behavior at typical loop compensation frequencies with significant phase shift appearing at half the switching frequency. The external output capacitor and load cause a first order roll off at the output at the $R_{OUT}C_{OUT}$ pole frequency, with the attendant 90° phase shift. This roll off is what filters the PWM waveform, resulting in the desired DC output voltage. The output capacitor also contributes a zero at the $C_{OUT}R_{ESR}$ frequency which adds back the 90° phase and cancels the first order roll off.

So far, the AC response of the loop is pretty well out of the user's control. The modulator is a fundamental piece of the LTC3810-5 design and the external output capacitor is usually chosen based on the regulation and load current requirements without considering the AC loop response. The feedback amplifier, on the other hand, gives us a handle with which to adjust the AC response. The goal is to have 180° phase shift at DC (so the loop regulates), and something less than 360° phase shift (preferably about 300°) at the point that the loop gain falls to 0dB, i.e., the crossover frequency, with as much gain as possible at frequencies below the crossover frequency. Since the modulator/output filter is a first order system with maximum of 90° phase shift (at frequencies below $f_{SW}/4$) and the feedback amplifier adds another 90° of phase shift, some phase boost is required at the crossover frequency to achieve good phase margin. If the ESR zero is below the crossover frequency, this zero may provide enough phase boost to achieve the desired phase margin and the only

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requirement of the compensation will be to guarantee that the gain is below zero at frequencies above $f_{SW}/4$. If the ESR zero is above the crossover frequency, the feedback amplifier will probably be required to provide phase boost. For most LTC3810-5 applications, Type 2 compensation will provide enough phase boost; however some applications where high bandwidth is required with low ESR ceramics and lots of bulk capacitance, Type 3 compensation may be necessary to provide additional phase boost.

The two types of compensation networks, "Type 2" and "Type 3" are shown in Figures 11 and 12. When component values are chosen properly, these networks provide a "phase bump" at the crossover frequency. Type 2 uses a single pole-zero pair to provide up to about 60° of phase boost while Type 3 uses two poles and two zeros to provide up to 150° of phase boost.

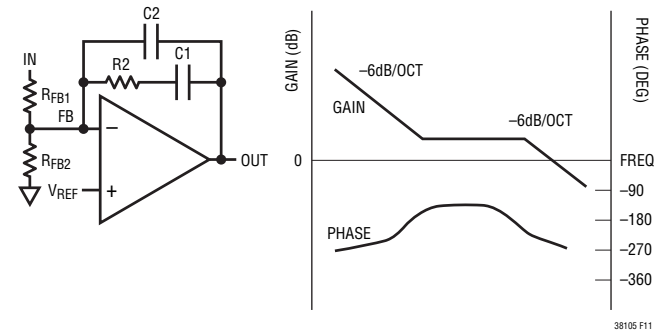


Figure 11. Type 2 Schematic and Transfer Function

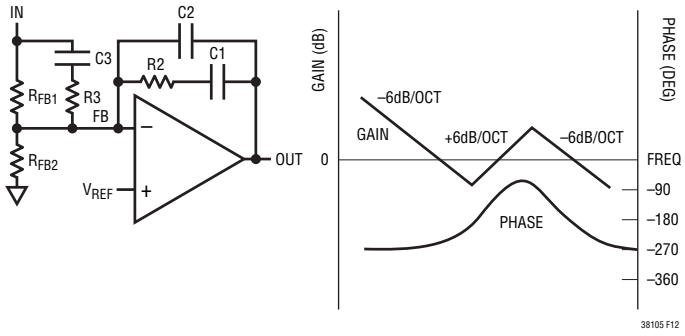


Figure 12. Type 3 Schematic and Transfer Function

Feedback Component Selection

Selecting the R and C values for a typical Type 2 or Type 3 loop is a nontrivial task. The applications shown in this data sheet show typical values, optimized for the power components shown. They should give acceptable performance with similar power components, but can be way off if even one major power component is changed significantly. Applications that require optimized transient response will require recalculation of the compensation values specifically for the circuit in question. The underlying mathematics are complex, but the component values can be calculated in a straightforward manner if we know the gain and phase of the modulator at the crossover frequency.

Modulator gain and phase can be obtained in one of three ways: measured directly from a breadboard, or if the appropriate parasitic values are known, simulated or generated from the modulator transfer function. Measurement will give more accurate results, but simulation or transfer function can often get close enough to give a working system. To measure the modulator gain and phase directly, wire up a breadboard with an LTC3810-5 and the actual MOSFETs, inductor and input and output capacitors that the final design will use. This breadboard should use appropriate construction techniques for high speed analog circuitry: bypass capacitors located close to the LTC3810-5, no long wires connecting components, appropriately sized ground returns, etc. Wire the feedback amplifier with a 0.1µF feedback capacitor from I_{TH} to FB and a 10k to 100k resistor from V_{OUT} to FB. Choose the bias resistor (R_{FB2}) as required to set the desired output voltage. Disconnect R_{FB2} from ground and connect it to a signal generator or to the source output of a network analyzer to inject a test signal into the loop. Measure the gain and phase from the I_{TH} pin to the output node at the positive terminal of the output capacitor. Make sure the analyzer's input is AC coupled so that the DC voltages present at both the I_{TH} and V_{OUT} nodes don't corrupt the measurements or damage the analyzer.

If breadboard measurement is not practical, a SPICE simulation can be used to generate approximate gain/phase curves. Plug the expected capacitor, inductor and MOSFET values into the following SPICE deck and generate an AC plot of V_{OUT}/V_{ITH} with gain in dB and phase in

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degrees. Refer to your SPICE manual for details of how to generate this plot.

```
*3810-5 modulator gain/phase
*2006 Linear Technology
*this file simulates a simplified model of
*the LTC3810-5 for generating a v(out)/
v(ith)
*bode plot

.param rdson=.0135 ;MOSFET rdson
.param Vrng=2    ;use 1.4 for INTVCC and
                    0.7 for ground
.param vsnsmax={0.173*Vrng-0.026}
.param Imax={vsnsmax/rdson}
.param DL=4     ;inductor ripple current

*inductor current
gl out 0 value={(v(ith)-1.2)*Imax/1.2+DL/2}

*output cap
cout out out2 270u ;capacitor value
resr out2 0 0.018 ;capacitor ESR

*load
Rout out 0 2 ; load resistor

vstim ith 0 0 ac 1 ;ac stimulus
.ac dec 100 100 10meg
.probe
.end
```

Mathematical software such as MATHCAD or MATLAB can also be used to generate plots using the following transfer function of the modulator:

$$H(s) = \left(\frac{V_{SENSE(MAX)}}{1.2 \bullet R_{DS(ON)}}\right) \bullet \left(\frac{1 + s \bullet R_{ESR} \bullet C_{OUT}}{1 + s \bullet R_L \bullet C_{OUT}}\right) \bullet R_L \quad (2)$$

$$s = j2\pi f$$

With the gain/phase plot in hand, a loop crossover frequency can be chosen. Usually the curves look something like Figure 13. Choose the crossover frequency about 25% of the switching frequency for maximum bandwidth. Although it may be tempting to go beyond $f_{SW}/4$, remember that significant phase shift occurs at half the switching frequency that isn't modeled in the above H(s) equation and PSPICE code. Note the gain (GAIN, in dB) and phase

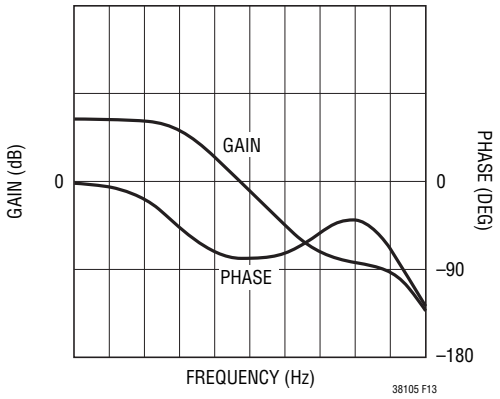


Figure 13. Transfer Function of Buck Modulator

(PHASE, in degrees) at this point. The desired feedback amplifier gain will be –GAIN to make the loop gain at 0dB at this frequency. Now calculate the needed phase boost, assuming 60° as a target phase margin:

BOOST = – (PHASE + 30°)

If the required BOOST is less than 60°, a Type 2 loop can be used successfully, saving two external components. BOOST values greater than 60° usually require Type 3 loops for satisfactory performance.

Finally, choose a convenient resistor value for R_{FB1} (10k is usually a good value). Now calculate the remaining values:

(K is a constant used in the calculations)

f = chosen crossover frequency

G = $10^{(GAIN/20)}$ (this converts GAIN in dB to G in absolute gain)

TYPE 2 Loop:

$$K = \tan\left(\frac{BOOST}{2} + 45°\right)$$

$$C2 = \frac{1}{2\pi \bullet f \bullet G \bullet K \bullet R_{FB1}}$$

$$C1 = C2\left(K^2 - 1\right)$$

$$R2 = \frac{K}{2\pi \bullet f \bullet C1}$$

$$R_{FB2} = \frac{V_{REF}(R_{FB1})}{V_{OUT} - V_{REF}}$$

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TYPE 3 Loop:

$$K = \tan^2\left(\frac{BOOST}{4} + 45^\circ\right)$$

$$C2 = \frac{1}{2\pi \bullet f \bullet G \bullet R_{FB1}}$$

$$C1 = C2(K-1)$$

$$R2 = \frac{\sqrt{K}}{2\pi \bullet f \bullet C1}$$

$$R3 = \frac{R_{FB1}}{K-1}$$

$$C3 = \frac{1}{2\pi f\sqrt{K} \bullet R3}$$

$$R_{FB2} = \frac{V_{REF}(R_{FB1})}{V_{OUT} - V_{REF}}$$

SPICE or mathematical software can be used to generate the gain/phase plots for the compensated power supply to do a sanity check on the component values before trying them out on the actual hardware. For software, use the following transfer function:

T(s) = A(s)H(s)

where H(s) was given in Equation 2 and A(s) depends on compensation circuit used:

Type 2:

$$A(s) = \frac{1 + s \bullet R2 \bullet C1}{s \bullet R_{FB1} \bullet (C1 + C2) \bullet \left(1 + s \bullet R2 \bullet \frac{C1 \bullet C2}{C1 + C2}\right)}$$

Type 3:

$$A(s) = \frac{1}{s \bullet R_{FB1} \bullet (C1 + C2)} \bullet \frac{\left(1 + s \bullet (R_{FB1} + R3) \bullet C3\right) \bullet (1 + s \bullet R2 \bullet C1)}{(1 + s \bullet R3 \bullet C3) \bullet \left(1 + s \bullet R2 \bullet \frac{C1 \bullet C2}{C1 + C2}\right)}$$

For SPICE, replace VSTIM line in the previous PSPICE code with following code and generate a gain/phase plot of V(out)/V(outin):

```
rfb1 outin vfb 52.5k
rfb2 vfb 0 10k
eithx ithx 0 laplace {0.8-v(vfb)} =
            {1/(1+s/1000)}
eith ith 0 value={limit(1e6*v(ithx),0,2.4)}
cc1 ith vfb 4p
cc2 ith x1 8p
rc x1 vfb 210k
rf outin x2 11k ;delete this line for Type 2
cf x2 vfb 120p ;delete this line for Type 2
vstim out outin dc=0 ac=1m
```

Pulse Skip Mode Operation and MODE/SYNC Pin

The MODE/SYNC pin determines whether the bottom MOSFET remains on when current reverses in the inductor. Tying this pin above its 0.8V threshold enables pulse skip mode operation where the bottom MOSFET turns off when inductor current reverses. The load current at which current reverses and discontinuous operation begins depends on the amplitude of the inductor ripple current and will vary with changes in V_{IN}. Tying the MODE/SYNC pin below the 0.8V threshold forces continuous synchronous operation, allowing current to reverse at light loads and maintaining high frequency operation. To prevent forcing current back into the main power supply, potentially boosting the input supply to a dangerous voltage level, forced continuous mode of operation is disabled when the TRACK/SS voltage is below the reference voltage during soft-start or tracking. During these two periods, the PGOOD signal is forced low.

Table 1

MODE/SYNC PIN	CONDITION
DC Voltage: 0V to 0.75V	Forced Continuous Current Reversal Enabled
DC Voltage: ≥ 0.85V	Pulse Skip Mode Operation No Current Reversal
Feedback Resistors	Regulating a Secondary Winding
Ext. Clock 0V to ≥ 2V	Forced Continuous Current Reversal Enabled

APPLICATIONS INFORMATION

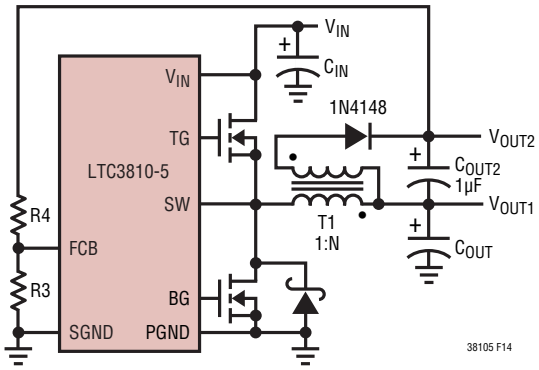


Figure 14. Secondary Output Loop

In addition to providing a logic input to force continuous operation, the MODE/SYNC pin provides a mean to maintain a flyback winding output when the primary is operating in pulse skip mode. The secondary output V_{OUT2} is normally set as shown in Figure 14 by the turns ratio N of the transformer. However, if the controller goes into pulse skip mode and halts switching due to a light primary load current, then V_{OUT2} will droop. An external resistor divider from V_{OUT2} to the MODE/SYNC pin sets a minimum voltage $V_{OUT2(MIN)}$ below which continuous operation is forced until V_{OUT2} has risen above its minimum.

$$V_{OUT2(MIN)} = 0.8V\left(1+\frac{R4}{R3}\right)$$

Fault Conditions: Current Limit and Foldback

The maximum inductor current is inherently limited in a current mode controller by the maximum sense voltage. In the LTC3810-5, the maximum sense voltage is controlled by the voltage on the V_{RNG} pin. With valley current control, the maximum sense voltage and the sense resistance determine the maximum allowed inductor valley current. The corresponding output current limit is:

$$I_{LIMIT} = \frac{V_{SNS(MAX)}}{R_{DS(ON)}\ \rho_T} + \frac{1}{2}\Delta I_L$$

The current limit value should be checked to ensure that $I_{LIMIT(MIN)} > I_{OUT(MAX)}$. The minimum value of current limit generally occurs with the largest V_{IN} at the highest ambient temperature, conditions that cause the largest power loss in the converter. Note that it is important to check for self-consistency between the assumed MOSFET junction temperature and the resulting value of I_{LIMIT} which heats the MOSFET switches.

Caution should be used when setting the current limit based upon the $R_{DS(ON)}$ of the MOSFETs. The maximum current limit is determined by the minimum MOSFET on-resistance. Data sheets typically specify nominal and maximum values for $R_{DS(ON)}$, but not a minimum. A reasonable assumption is that the minimum $R_{DS(ON)}$ lies the same percentage below the typical value as the maximum lies above it. Consult the MOSFET manufacturer for further guidelines.

To further limit current in the event of a short-circuit to ground, the LTC3810-5 includes foldback current limiting. If the output falls by more than 50%, then the maximum sense voltage is progressively lowered to about one-tenth of its full value.

Be aware also that when the fault timeout is enabled for the external NMOS regulator, an over current limit may cause the output to fall below the minimum 4.5V UV threshold. This condition will cause a linear regulator timeout/restart sequence as described in the Linear Regulator Timeout section if this condition persists.

Soft-Start and Tracking

The LTC3810-5 has the ability to either soft-start by itself with a capacitor or track the output of another supply. When the device is configured to soft-start by itself, a capacitor should be connected to the TRACK/SS pin. The LTC3810-5 is put in a low quiescent current shutdown state (I_Q ~240µA) if the $\overline{SHDN}$ pin voltage is below 1.5V. The TRACK/SS pin is actively pulled to ground in this shutdown state. Once the $\overline{SHDN}$ pin voltage is above 1.5V, the LTC3810-5 is powered up. A soft-start current of 1.4µA then starts to charge the soft-start capacitor C_{SS}. Note that soft-start is achieved not by limiting the maximum output current of the controller but by controlling the ramp rate of the output voltage. Current foldback is disabled during this soft-start phase. During the soft-start phase, the LTC3810-5 is ramping the reference voltage until it reaches 0.8V. The force continuous mode is also

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disabled and PGOOD signal is forced low during this phase. The total soft-start time can be calculated as:

$$t_{SOFTSTART} = 0.8 \bullet C_{SS}/1.4\mu A$$

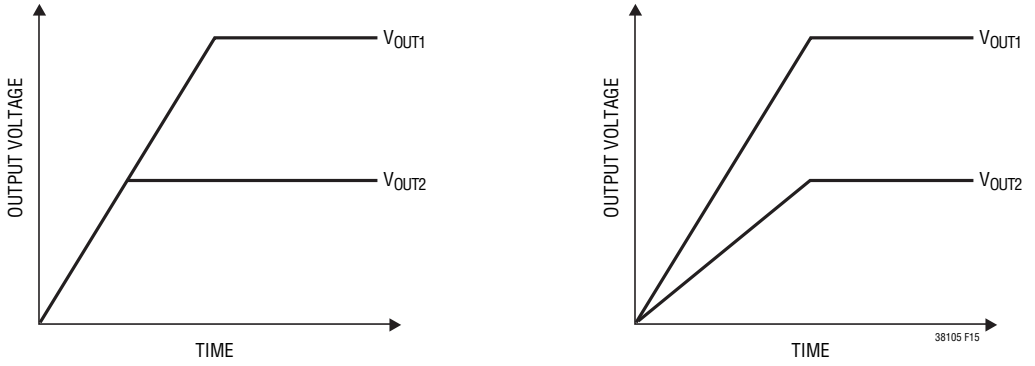
When the device is configured to track another supply, the feedback voltage of the other supply is duplicated by a resistor divider and applied to the TRACK/SS pin. Therefore, the voltage ramp rate on this pin is determined by the ramp rate of the other supply output voltage.

Output Voltage Tracking

The LTC3810-5 allows the user to program how its output ramps up by means of the TRACK/SS pin. Through this pin, the output can be set up to either coincidentally or ratiometrically track with another supply's output, as shown in Figure 15. In the following discussions, V_{OUT1} refers to the master LTC3810-5's output and V_{OUT2} refers to the slave LTC3810-5's output.

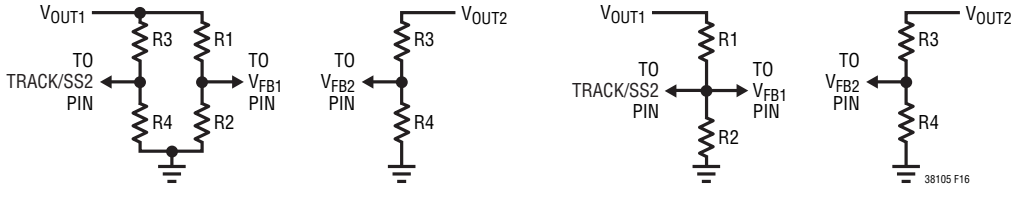
To implement the coincident tracking in Figure 15a, connect an additional resistive divider to V_{OUT1} and connect its midpoint to the TRACK/SS pin of the slave IC. The ratio of this divider should be selected the same as that of the slave IC's feedback divider shown in Figure 16. In this tracking mode, V_{OUT1} must be set higher than V_{OUT2}. To implement the ratiometric tracking, the ratio of the divider should be exactly the same as the master IC's feedback divider. Note that the internal soft-start current will introduce a small error on the tracking voltage depending on the absolute values of the tracking resistive divider.

By selecting different resistors, the LTC3810-5 can achieve different modes of tracking including the two in Figure 15. So which mode should be programmed? While either mode in Figure 15 satisfies most practical applications, there do exist some tradeoffs. The ratiometric mode saves a pair of resistors, but the coincident mode offers better output regulation. This can be better understood with the



(15a) Coincident Tracking **(15b) Ratiometric Tracking**

Figure 15. Two Different Modes of Output Voltage Tracking



(16a) Coincident Tracking Setup **(16b) Ratiometric Tracking Setup**

Figure 16. Setup for Coincident and Ratiometric Tracking

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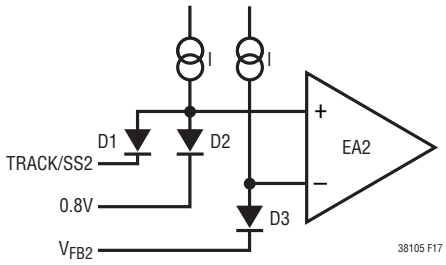


Figure 17. Equivalent Input Circuit of Error Amplifier

help of Figure 17. At the input stage of the slave IC's error amplifier, two common anode diodes are used to clamp the equivalent reference voltage and an additional diode is used to match the shifted common mode voltage. The top two current sources are of the same amplitude. In the coincident mode, the TRACK/SS voltage is substantially higher than 0.8V at steady state and effectively turns off D1. D2 and D3 will therefore conduct the same current and offer tight matching between V_{FB2} and the internal precision 0.8V reference. In the ratiometric mode, however, TRACK/SS equals 0.8V at steady state. D1 will divert part of the bias current to make V_{FB2} slightly lower than 0.8V. Although this error is minimized by the exponential I-V characteristic of the diode, it does impose a finite amount of output voltage deviation. Furthermore, when the master IC's output experiences dynamic excursion (under load transient, for example), the slave IC output will be affected as well. *For better output regulation, use the coincident tracking mode instead of ratiometric.*

Phase-Locked Loop and Frequency Synchronization

The LTC3810-5 has a phase-locked loop comprised of an internal voltage controlled oscillator and phase detector. This allows the top MOSFET turn-on to be locked to the rising edge of an external source. The frequency range of the voltage controlled oscillator is ±30% around the center frequency f_O. The center frequency is the operating frequency discussed in the Operating Frequency section. The LTC3810-5 incorporates a pulse detection circuit that will detect a clock on the MODE/SYNC pin. In turn, it will turn on the phase-locked loop function. The pulse width of the clock has to be greater than 400ns and the amplitude of the clock should be greater than 2V.

The internal oscillator locks to the external clock after the second clock transition is received. When external synchronization is detected, LTC3810-5 will operate in forced continuous mode. If an external clock transition is not detected for three successive periods, the internal oscillator will revert to the frequency programmed by the R_{ON} resistor.

During the start-up phase, phase-locked loop function is disabled. When LTC3810-5 is not in synchronization mode, PLL/LPF pin voltage is set to around 1.215V. Frequency synchronization is accomplished by changing the internal on-time current according to the voltage on the PLL/LPF pin.

The phase detector used is an edge sensitive digital type which provides zero degrees phase shift between the external and internal pulses. This type of phase detector will not lock up on input frequencies close to the harmonics of the V_{CO} center frequency. The PLL hold-in range, Δf_H, is equal to the capture range, Δf_C:

$$\Delta f_H = \Delta f_C = \pm 0.3\ f_O$$

The output of the phase detector is a complementary pair of current sources charging or discharging the external filter network on the PLL/LPF pin. A simplified block diagram is shown in Figure 18.

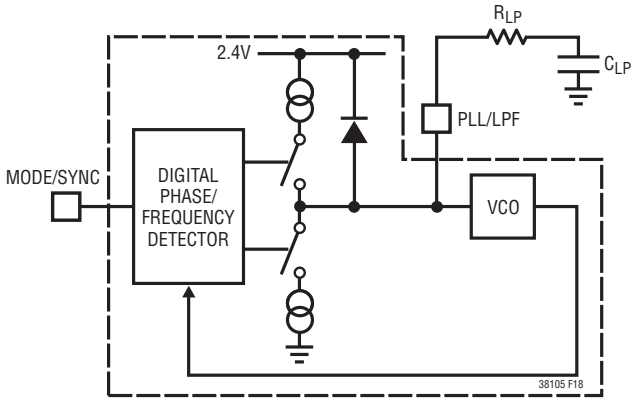


Figure 18. Phase-Locked Loop Block Diagram

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If the external frequency (f_{MODE}) is greater than the oscillator frequency f_O, current is sourced continuously, pulling up the PLL/LPF pin. When the external frequency is less than f_O, current is sunk continuously, pulling down the PLL/LPF pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. Thus the voltage on the PLL/LPF pin is adjusted until the phase and frequency of the external and internal oscillators are identical. At this stable operating point the phase comparator output is open and the filter capacitor C_{LP} holds the voltage. The LTC3810-5 MODE/SYNC pin must be driven from a low impedance source such as a logic gate located close to the pin.

The loop filter components (C_{LP}, R_{LP}) smooth out the current pulses from the phase detector and provide a stable input to the voltage controlled oscillator. The filter components C_{LP} and R_{LP} determine how fast the loop acquires lock. Typically R_{LP} = 10kΩ and C_{LP} is 0.01µF to 0.1µF.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in the circuit produce losses, four main sources account for most of the losses in LTC3810-5 circuits:

1. DC I^2R losses. These arise from the resistances of the MOSFETs, inductor and PC board traces and cause the efficiency to drop at high output currents. In continuous mode the average output current flows through L, but is chopped between the top and bottom MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and the board traces to obtain the DC I^2R loss. For example, if $R_{DS(ON)}$ = 0.01Ω and R_L = 0.005Ω, the loss will range from 15mW to 1.5W as the output current varies from 1A to 10A.
2. Transition loss. This loss arises from the brief amount of time the top MOSFET spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors. The loss is significant at input voltages above 20V and can be estimated from the second term of the P_{MAIN} equation found in the Power MOSFET Selection section. When transition losses are significant, efficiency can be improved by lowering the frequency and/or using a top MOSFET(s) with lower C_{RSS} at the expense of higher $R_{DS(ON)}$.
3. $INTV_{CC}/DRV_{CC}$ current. This is the sum of the MOSFET driver and control currents. Control current is typically about 3mA and driver current can be calculated by: $I_{GATE} = f(Q_{G(TOP)} + Q_{G(BOT)})$, where $Q_{G(TOP)}$ and $Q_{G(BOT)}$ are the gate charges of the top and bottom MOSFETs. This loss is proportional to the supply voltage that $INTV_{CC}/DRV_{CC}$ is derived from, i.e., V_{IN} for the external NMOS linear regulator, V_{OUT} for the internal $EXTV_{CC}$ regulator, or V_{EXT} when an external supply is connected to $INTV_{CC}/DRV_{CC}$.
4. C_{IN} loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator. It must have a very low ESR to minimize the AC I^2R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.

Other losses, including C_{OUT} ESR loss, Schottky diode D1 conduction loss during dead time and inductor core loss generally account for less than 2% additional loss. When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If you make a change and the input current decreases, then the efficiency has increased. If there is no change in input current, then there is no change in efficiency.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current.

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When load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

Design Example

As a design example, take a supply with the following specifications: V_{IN} = 12V to 60V, V_{OUT} = 5V ±5%, $I_{OUT(MAX)}$ = 6A, f = 250kHz. First, calculate the timing resistor:

$$R_{ON} = \frac{5V}{2.4V \bullet 250kHz \bullet 76pF} = 110k$$

and choose the inductor for about 40% ripple current at the maximum V_{IN}:

$$L = \frac{5V}{250kHz \bullet 0.4 \bullet 6A}\left(1 - \frac{5V}{60V}\right) = 7.6\mu H$$

With a 7.7µH inductor, ripple current will vary from 1.5A to 2.4A (25% to 40%) over the input supply range.

Next, choose the bottom MOSFET switch. Since the drain of the MOSFET will see the full supply voltage 60V (max) plus any ringing, choose an 60V MOSFET. The Si7850DP has:

BV_{DSS} = 60V
$R_{DS(ON)}$ = 31mΩ (max)/25mΩ (nom),
δ = 0.007/°C,
C_{MILLER} = (8.3nC – 2.8nC)/30V = 183pF,
$V_{GS(MILLER)}$ = 3.8V,
θ_{JA} = 22°C/W.

This yields a nominal sense voltage of:

$$V_{SNS(NOM)} = 6A \bullet 1.3 \bullet 0.025\Omega = 195mV$$

To guarantee proper current limit at worst-case conditions, increase nominal V_{SNS} by at least 50% to 320mV (by tying V_{RNG} to 2V). To check if the current limit is acceptable at V_{SNS} = 320mV, assume a junction temperature of about 55°C above a 70°C ambient ($\rho_{125°C}$ = 1.7):

$$I_{LIMIT} \geq \frac{320mV}{1.7 \bullet 0.031\Omega} + \frac{1}{2} \bullet 2.4A = 7.3A$$

and double-check the assumed T_J in the MOSFET:

$$P_{BOT} = \frac{60V - 5V}{60V} \bullet 7.3A^2 \bullet 1.7 \bullet 0.031\Omega = 2.6W$$

T_J = 70°C + 2.6W • 22°C/W = 127°C

Verify that the Si7850DP is also a good choice for the top MOSFET by checking its power dissipation at current limit and maximum input voltage, assuming a junction temperature of 30°C above a 70°C ambient ($\rho_{100°C}$ = 1.5):

$$P_{MAIN} = \frac{5V}{60V} \bullet 7.3A^2 (1.5 \bullet 0.031\Omega) + 60V^2 \bullet \frac{7.3A}{2} \bullet 2\Omega \bullet 183pF \bullet \left(\frac{1}{5V - 3.8V} + \frac{1}{3.8V}\right) \bullet 250kHz = 0.206W + 1.32W = 1.53W$$

T_J = 70°C + 1.53W • 22°C/W = 104°C

The junction temperature will be significantly less at nominal current, but this analysis shows that careful attention to heat sinking on the board will be necessary in this circuit.

Since V_{OUT} > 4.7V, the $INTV_{CC}$ voltage can be generated from V_{OUT} with the internal LDO by connecting V_{OUT} to the $EXTV_{CC}$ pin. A small SOT23 MOSFET such as the ZXMN10A07F can be used for the pass device if fault timeout is enabled. Choose R_{NDRV} to guarantee that fault timeout is enabled when power dissipation of M3 exceeds 0.4W (max for 70°C ambient):

$$I_{CC} = 250kHz \bullet 2 \bullet 18nC + 3mA = 12mA$$

$$R_{NDRV} \leq \frac{0.4W / 0.012A - 3V}{270\mu A} = 112k$$

So, choose R_{NDRV} = 100k.

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C_{IN} is chosen for an RMS current rating of about 3A at 85°C. The output capacitors are chosen for a low ESR of 0.018Ω to minimize output voltage changes due to inductor ripple current and load steps. The ripple voltage will be only:

$$\Delta V_{OUT(RIPPLE)} = \Delta I_{L(MAX)} \bullet ESR = 2.4A \bullet 0.018\Omega = 43mV$$

However, a 0A to 6A load step will cause an output change of up to:

$$\Delta V_{OUT(STEP)} = \Delta I_{LOAD} \bullet ESR = 6A \bullet 0.018\Omega = 108mV$$

An optional 10µF ceramic output capacitor is included to minimize the effect of ESL in the output ripple. The complete circuit is shown in Figure 19.

PC Board Layout Checklist

When laying out a PC board follow one of two suggested approaches. The simple PC board layout requires a dedicated ground plane layer. Also, for higher currents, it is recommended to use a multilayer board to help with heat sinking power components.

- The ground plane layer should not have any traces and it should be as close as possible to the layer with power MOSFETs.
- Place C_{IN}, C_{OUT}, MOSFETs, D1 and inductor all in one compact area. It may help to have some components on the bottom side of the board.
- Use an immediate via to connect the components to ground plane including SGND and PGND of LTC3810-5. Use several bigger vias for power components.

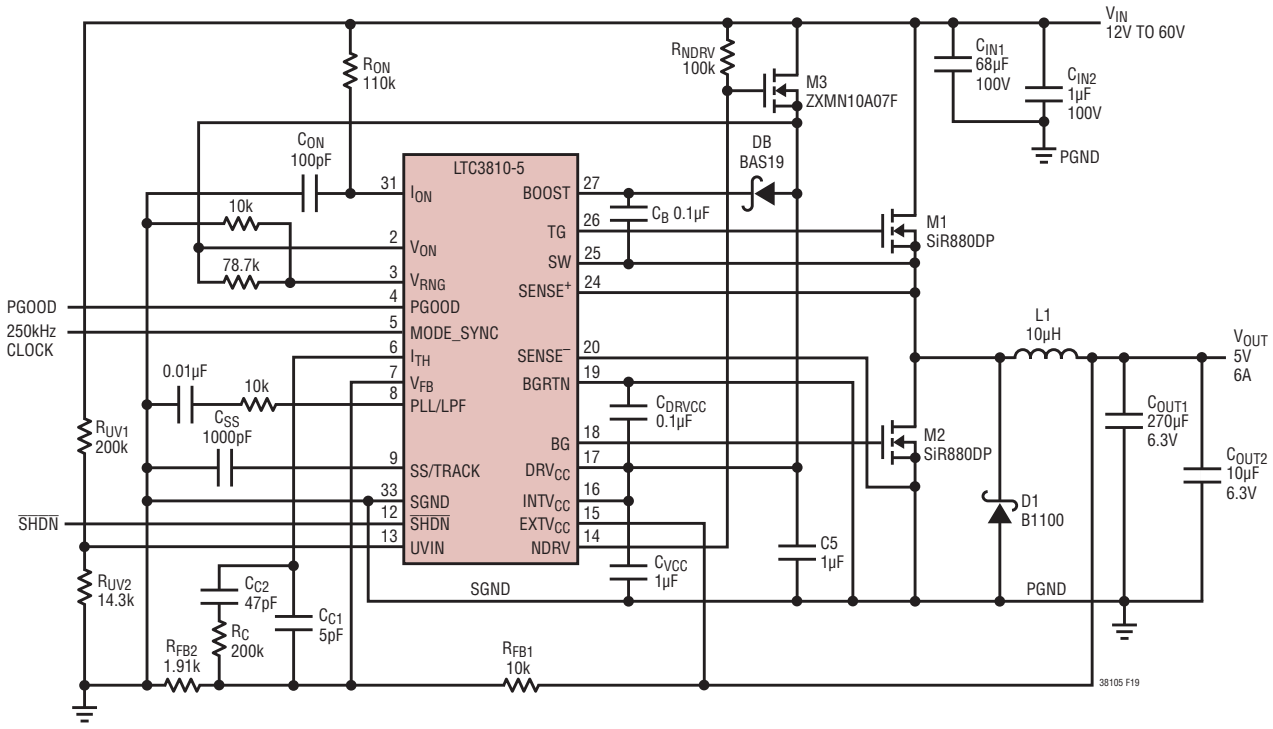


Figure 19. 12V to 60V Input Voltage to 5V/6A Synchronized at 250kHz

APPLICATIONS INFORMATION

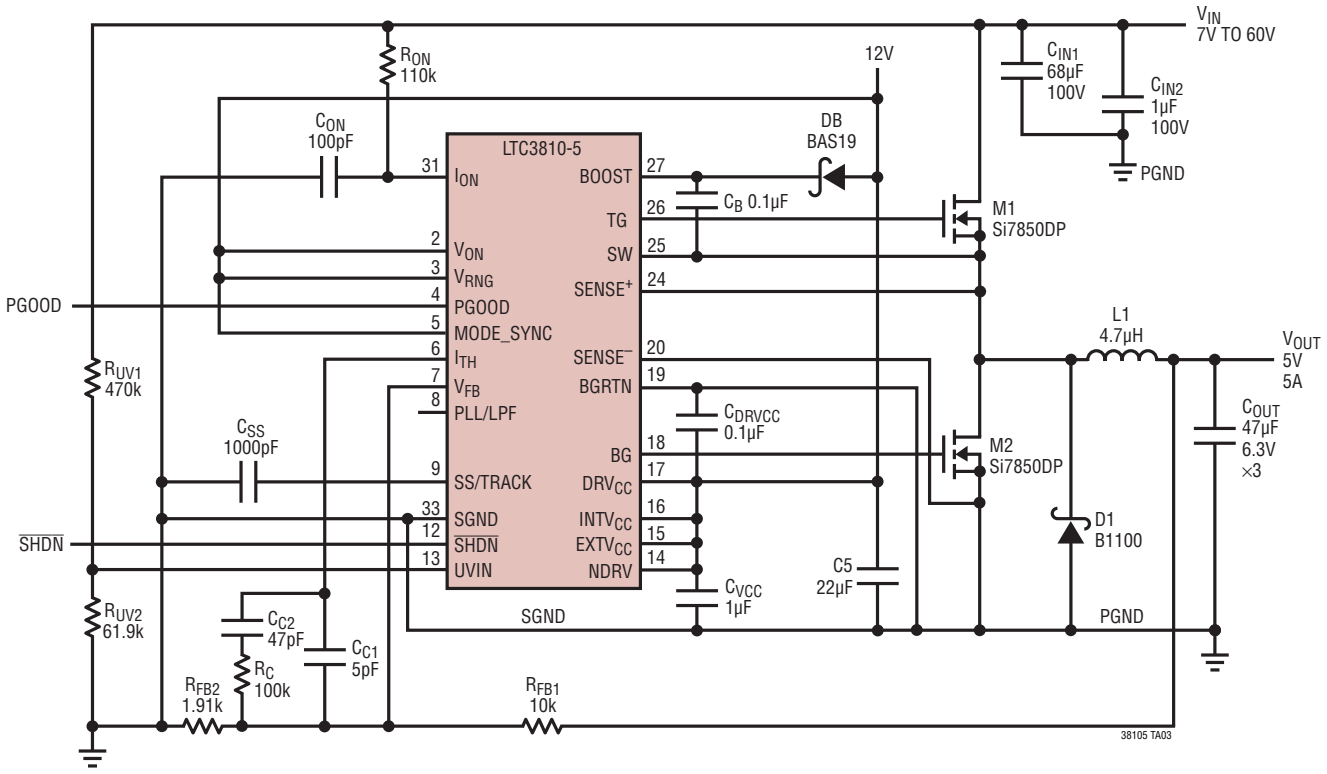
- Use compact plane for switch node (SW) to improve cooling of the MOSFETs and to keep EMI down.
- Use planes for V_{IN} and V_{OUT} to maintain good voltage filtering and to keep power losses low.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power component. You can connect the copper areas to any DC net (V_{IN}, V_{OUT}, GND or to any other DC rail in your system).

When laying out a printed circuit board, without a ground plane, use the following checklist to ensure proper operation of the controller.

- Segregate the signal and power grounds. All small signal components should return to the SGND pin at one point which is then tied to the PGND pin close to the source of M2.
- Place M2 as close to the controller as possible, keeping the PGND, BG and SW traces short.
- Connect the input capacitor(s) C_{IN} close to the power MOSFETs. This capacitor carries the MOSFET AC current.
- Keep the high dV/dt SW, BOOST and TG nodes away from sensitive small-signal nodes.
- Connect the $INTV_{CC}$ decoupling capacitor C_{VCC} closely to the $INTV_{CC}$ and SGND pins.
- Connect the top driver boost capacitor C_B closely to the BOOST and SW pins.
- Connect the bottom driver decoupling capacitor C_{DRVCC} closely to the DRV_{CC} and BGRTN pins.

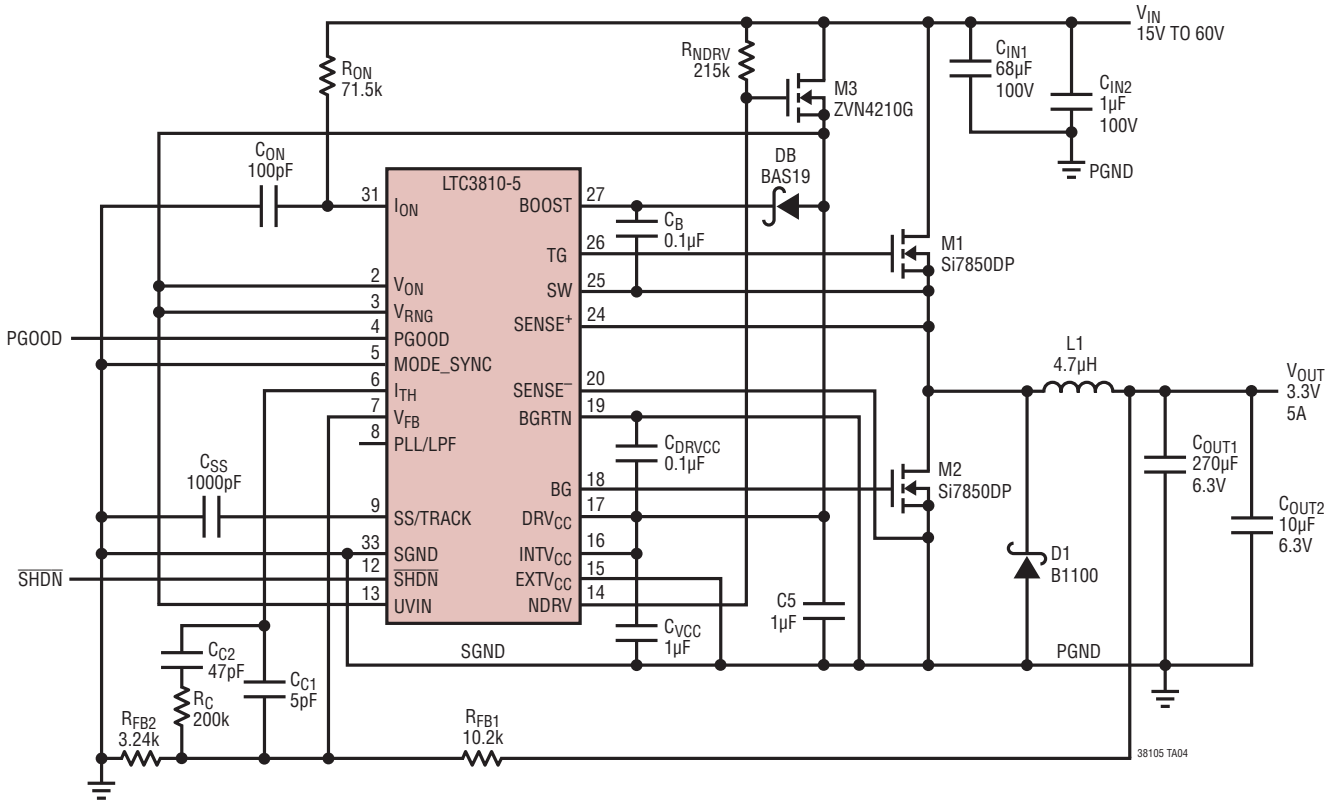
TYPICAL APPLICATIONS

7V to 60V Input Voltage to 5V/5A with IC Power from 12V Supply and All Ceramic Output Capacitors



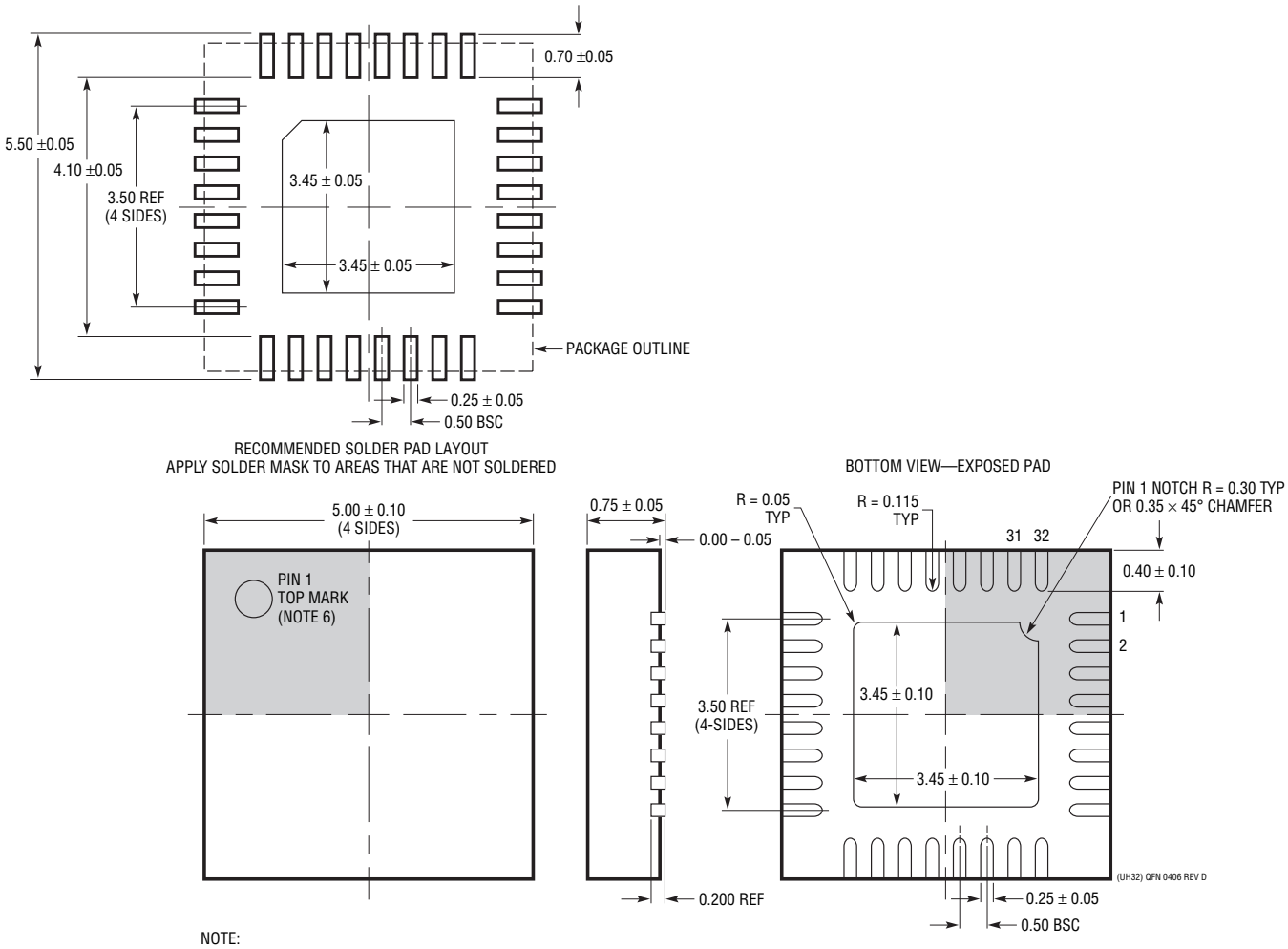
TYPICAL APPLICATIONS

15V to 60V Input Voltage to 3.3V/5A with Fault Timeout, Pulse Skip and V_{IN} UV Disabled



PACKAGE DESCRIPTION

UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693 Rev D)



NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev D)

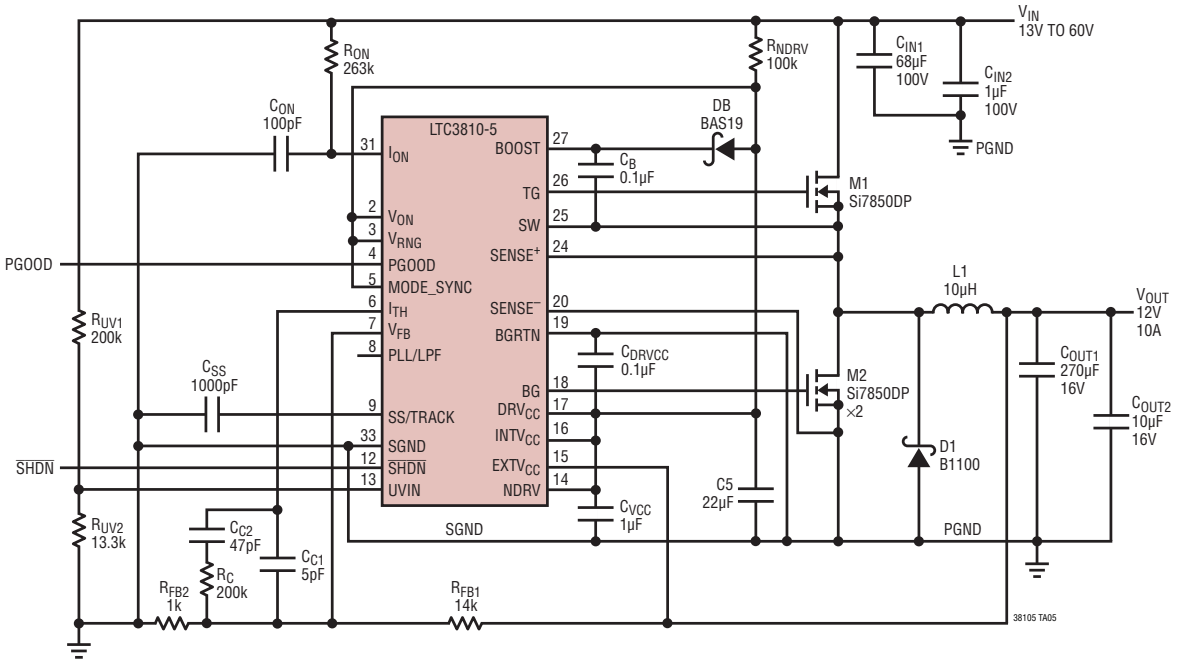
REV	DATE	DESCRIPTION	PAGE NUMBER
D	12/10	Change to Operating Temperature Range	2
		Updated Order Information table	2
		Change made to Feedback Voltage (V_{FB})	3
		Change to Note 2 and Note 7	4
		Addition of 150°C to graphs G14, G17, G18, G19, G20, G23, G24, G25, G28 and G30	6, 7, 8
		Formula change: Type 2 and Type 3	26
		Updated Related Parts table	38

LINEAR TECHNOLOGY

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TYPICAL APPLICATION

13V to 60V Input Voltage to 12V/10A with Trickle Charger Start-Up



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3891	60V, Low I_Q, Synchronous Step-Down DC/DC Controller	PLL Fixed Frequency 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 24V, TSSOP-20E, 3mm × 4mm QFN-20
LTC3890	60V, Low I_Q, Dual Output 2-Phase Synchronous Step-Down DC/DC Controller	PLL Fixed Frequency 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 24V, 5mm × 5mm QFN-32
LTC3810	100V Synchronous Step-Down DC/DC Controller	Constant On-time Valley Current Mode, 4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 0.93V_{IN}, SSOP-28
LTC3812-5	60V Synchronous Step-Down DC/DC Controller	Constant On-time Valley Current Mode, 4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 0.93V_{IN}, TSSOP-16E
LTC3703	100V Synchronous Step-Down DC/DC Controller	PLL Fixed Frequency 100kHz to 600kHz, 4V ≤ V_{IN} ≤ 100V, 0.8V ≤ V_{OUT} ≤ 0.93V_{IN}, SSOP-16, SSOP-28
LT3845A	60V, Low I_Q, Single Output Synchronous Step-Down DC/DC Controller	Adjustable Fixed Frequency 100kHz to 500kHz, 4V≤ V_{IN} ≤ 60V, 1.23V ≤ V_{OUT} ≤ 36V, TSSOP-16E
LT3824	60V, Low I_Q, Step-Down DC/DC Controller, 100% Duty Cycle	Selectable Fixed Frequency 200kHz to 600kHz, 4V≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ V_{IN}, I_Q = 40µA, MSOP-10E

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