High Voltage, Current Mode Switching Regulator Controller with Programmable Operating Frequency

FEATURES

- **High Voltage Operation: Up to 60V**
- **Output Voltages Up to 36V (Step Down)**
- **Programmable Constant Frequency: 100kHz to 500kHz**
- Synchronizable up to 600kHz
- Burst Mode® Operation: 120µA Supply Current
- 10µA Shutdown Supply Current
- ±1.3% Reference Accuracy
- Drives N-Channel MOSFET
- Programmable Soft-Start
- Programmable Undervoltage Lockout
- Internal High Voltage Regulator for Gate Drive
- Thermal Shutdown
- Current Limit Unaffected by Duty Cycle
- 16-Pin Thermally Enhanced TSSOP Package

APPLICATIONS

- Industrial Power Distribution
- 12V and 42V Automotive and Heavy Equipment
- High Voltage Single Board Systems
- Distributed Power Systems
- Avionics
- Telecom Power

DESCRIPTION

The LT®3844 is a DC/DC controller used for medium power, low part count, high efficiency supplies. It offers a wide 4V to 60V input range (7.5V minimum start-up voltage) and can implement step-down, step-up, inverting and SEPIC topologies.

The LT3844 includes Burst Mode operation, which reduces quiescent current below 120µA and maintains high efficiency at light loads. An internal high voltage bias regulator allows for simple biasing.

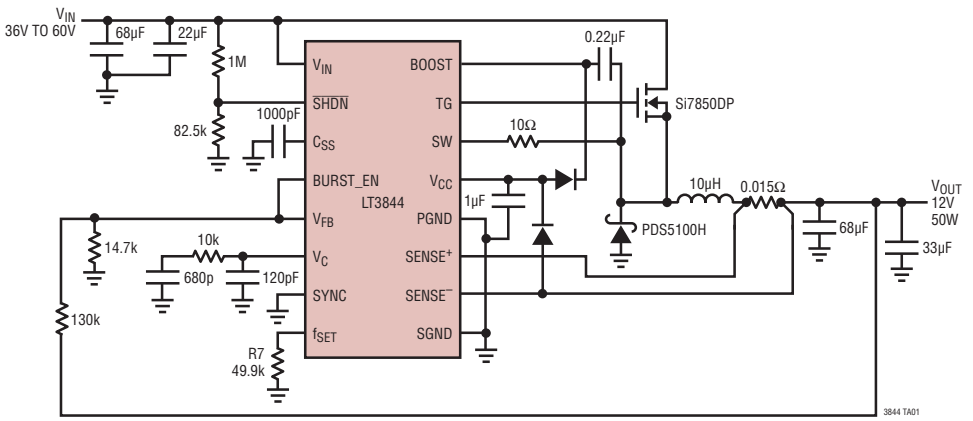
Additional features include current mode control for fast line and load transient response; programmable fixed operating frequency that can be synchronized to an external clock for noise sensitive applications; a gate driver capable of driving large N-channel MOSFETs; a precision undervoltage lockout function; 10µA shutdown current; short-circuit protection and a programmable soft-start function.

The LT3844 is available in a 16-lead thermally enhanced TSSOP package.

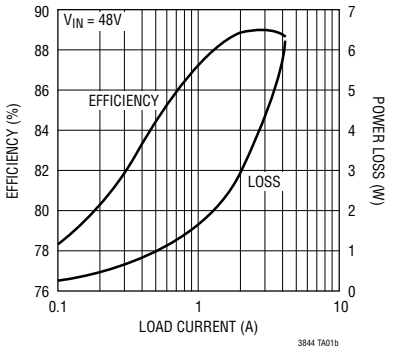
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TYPICAL APPLICATION

High Voltage Step-Down Regulator 48V to 12V, 50W



Efficiency and Power Loss vs Load Current

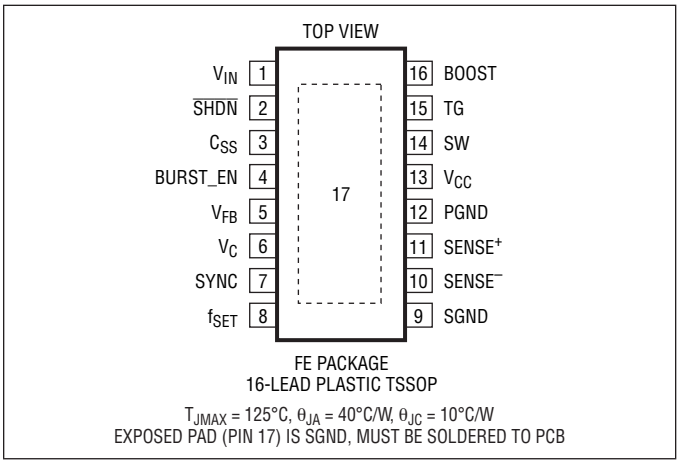


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{IN}) ..... 65V to –0.3V
Boosted Supply Voltage (BOOST) ..... 80V to –0.3V
Switch Voltage (SW) (Note 8) ..... 65V to –1V
Differential Boost Voltage
  BOOST to SW ..... 24V to –0.3V
Bias Supply Voltage (V_{CC}) ..... 24V to –0.3V
SENSE+ and SENSE– Voltages ..... 40V to –0.3V
Differential Sense Voltage
  SENSE+ to SENSE– ..... 1V to –1V
BURST_EN Voltage ..... 24V to –0.3V
SYNC, V_C, V_{FB}, C_{SS} and $\overline{SHDN}$ Voltages ..... 5V to –0.3V
$\overline{SHDN}$ Pin Currents 1mA
Operating Junction Temperature Range (Note 2)
  LT3844E (Note 3) ..... –40°C to 125°C
  LT3844I ..... –40°C to 125°C
Storage Temperature ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



FE PACKAGE
16-LEAD PLASTIC TSSOP

T_{JMAX} = 125°C, θ_{JA} = 40°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LT3844#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3844EFE#PBF	LT3844EFE#TRPBF	3844EFE	16-Lead Plastic TSSOP	–40°C to 125°C
LT3844IFE#PBF	LT3844IFE#TRPBF	3844IFE	16-Lead Plastic TSSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 20V, V_{CC} = BOOST = BURST_EN = 10V, $\overline{SHDN}$ = 2V, R_{SET} = 49.9k, SENSE– = SENSE+ = 10V, SGND = PGND = SW = SYNC = 0V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Operating Voltage Range (Note 4)		●	4		60	V
V_{IN} Minimum Start Voltage		●			7.5	V
V_{IN} UVLO Threshold (Falling)		●	3.6	3.8	4	V
V_{IN} UVLO Threshold Hysteresis				670		mV
V_{IN} Supply Current	V_{CC} > 9V			20		µA
V_{IN} Burst Mode Current	V_{BURST_EN} = 0V, V_{FB} = 1.35V			20		µA
V_{IN} Shutdown Current	$V_{\overline{SHDN}}$ = 0V			10	15	µA
BOOST Operating Voltage Range		●			75	V
BOOST Operating Voltage Range (Note 5)	$V_{BOOST} – V_{SW}$	●			20	V
BOOST UVLO Threshold (Rising)	$V_{BOOST} – V_{SW}$			5		V
BOOST UVLO Threshold Hysteresis	$V_{BOOST} – V_{SW}$			400		mV
BOOST Supply Current (Note 6)				1.4		mA
BOOST Burst Mode Current	V_{BURST_EN} = 0V			0.1		µA
BOOST Shutdown Current	$V_{\overline{SHDN}}$ = 0V			0.1		µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 20V, V_{CC} = BOOST = BURST_EN = 10V, $\overline{SHDN}$ = 2V, R_{SET} = 49.9k, $SENSE^-$ = $SENSE^+$ = 10V, SGND = PGND = SW = SYNC = 0V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} Operating Voltage Range (Note 5)		●			20	V
V_{CC} Output Voltage	Over Full Line and Load Range	●		8	8.3	V
V_{CC} UVLO Threshold (Rising)				6.25		V
V_{CC} UVLO Threshold Hysteresis				500		mV
V_{CC} Supply Current (Note 6)		●		1.7	2.1	mA
V_{CC} Burst Mode Current	V_{BURST_EN} = 0V			95		µA
V_{CC} Shutdown Current	$V_{\overline{SHDN}}$ = 0V			20		µA
V_{CC} Current Limit		●	–40	–120		mA
Error Amp Reference Voltage	Measured at V_{FB} Pin		1.224	1.231	1.238	V
		●	1.215		1.245	V
V_{FB} Pin Input Current	V_{FB} = 1.231V			25		nA
$\overline{SHDN}$ Enable Threshold (Rising)		●	1.3	1.35	1.4	V
$\overline{SHDN}$ Threshold Hysteresis				120		mV
Sense Pins Common Mode Range		●	0		36	V
Current Limit Sense Voltage	$V_{SENSE}^+ - V_{SENSE}^-$	●	90	100	115	mV
Input Current ($I_{SENSE}^+ + I_{SENSE}^-$)	$V_{SENSE(CM)}$ = 0V			350		µA
	$V_{SENSE(CM)}$ = 2V			–25		µA
	$V_{SENSE(CM)}$ > 4V			–170		µA
Operating Frequency			290	300	310	kHz
		●	270		330	kHz
Minimum Programmable Frequency		●			100	kHz
Maximum Programmable Frequency		●	500			kHz
External Sync Frequency Range		●	100		600	kHz
SYNC Input Resistance				40		kΩ
SYNC Voltage Threshold		●		1.4	2	V
Soft-Start Capacitor Control Current				2		µA
Error Amp Transconductance		●	270	340	410	µS
Error Amp DC Voltage Gain				62		dB
Error Amp Sink/Source Current				±30		µA
TG Drive On Voltage (Note 7)	C_{LOAD} = 2200pF			9.8		V
TG Drive Off Voltage	C_{LOAD} = 2200pF			0.1		V
TG Drive Rise/Fall Time	10% to 90% or 90% to 10%, C_{LOAD} = 2200pF			40		ns
Minimum TG Off Time		●		350	500	ns
Minimum TG On Time		●		250	350	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3844 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3: The LT3844E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3844I is guaranteed over the full –40°C to 125°C operating junction temperature range.

Note 4: V_{IN} voltages below the start-up threshold (7.5V) are only supported when the V_{CC} is externally driven above 6.5V.

Note 5: Operating range is dictated by MOSFET absolute maximum VGS.

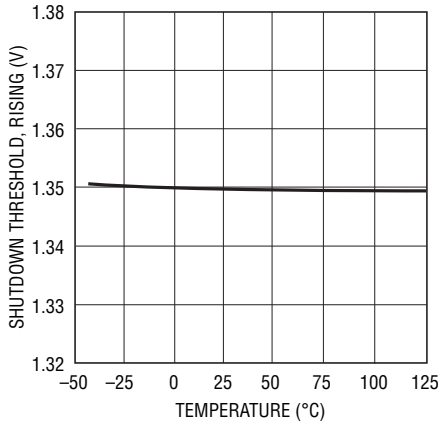
Note 6: Supply current specification does not include switch drive currents. Actual supply currents will be higher.

Note 7: DC measurement of gate drive output "ON" voltage is typically 8.6V. Internal dynamic bootstrap operation yields typical gate "ON" voltages of 9.8V during standard switching operation. Standard operation gate "ON" voltage is not tested but guaranteed by design.

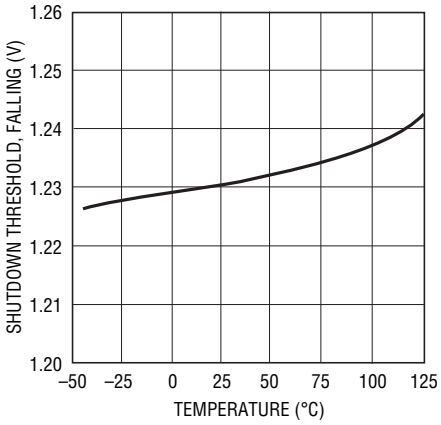
Note 8: The –1V absolute maximum on the SW pin is a transient condition. It is guaranteed by design and not subject to test.

TYPICAL PERFORMANCE CHARACTERISTICS

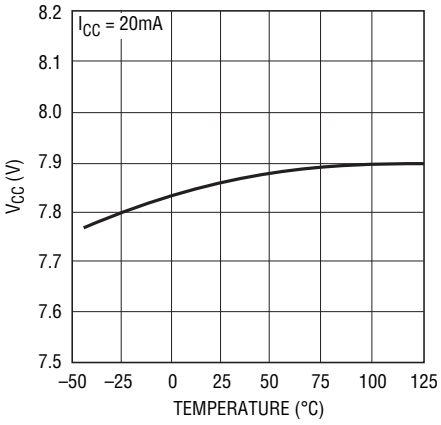
Shutdown Threshold (Rising) vs Temperature



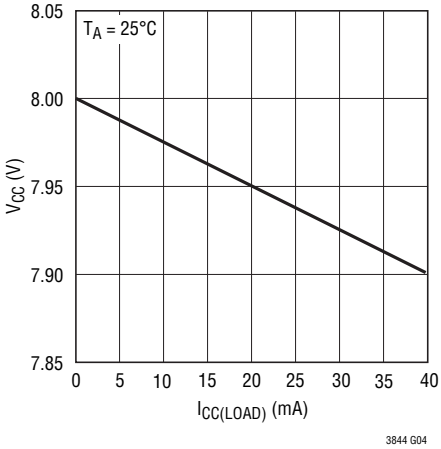
Shutdown Threshold (Falling) vs Temperature



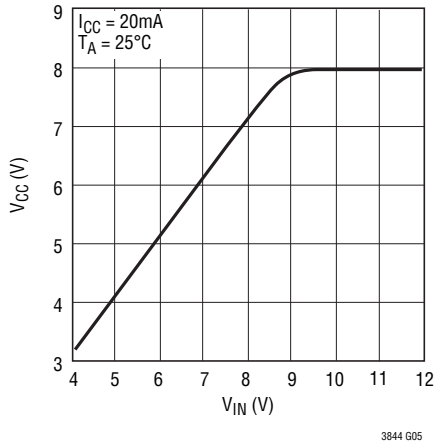
V_{CC} vs Temperature



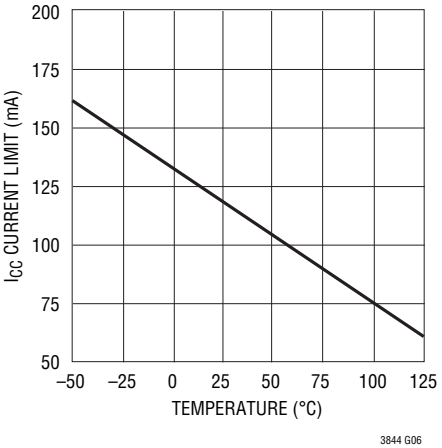
V_{CC} vs $I_{CC(LOAD)}$



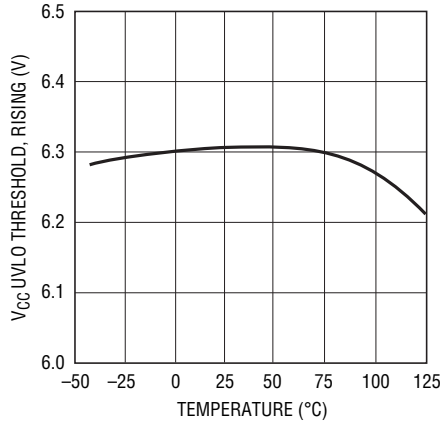
V_{CC} vs V_{IN}



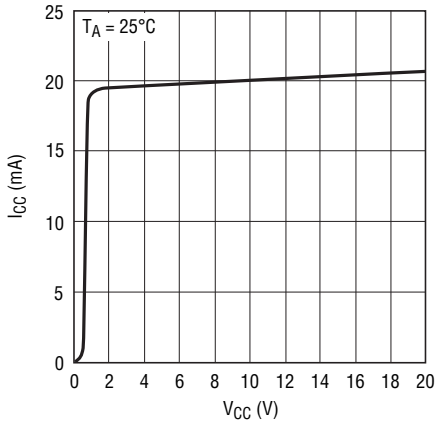
I_{CC} Current Limit vs Temperature



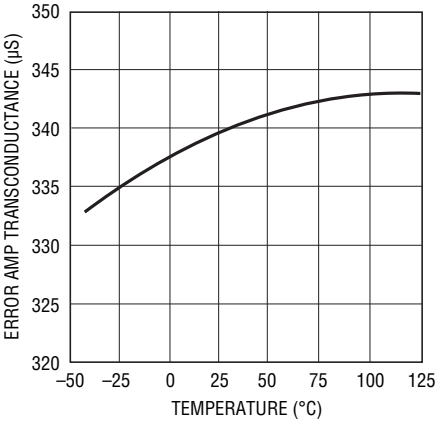
V_{CC} UVLO Threshold (Rising) vs Temperature



I_{CC} vs V_{CC} ($\overline{SHDN}$ = 0V)

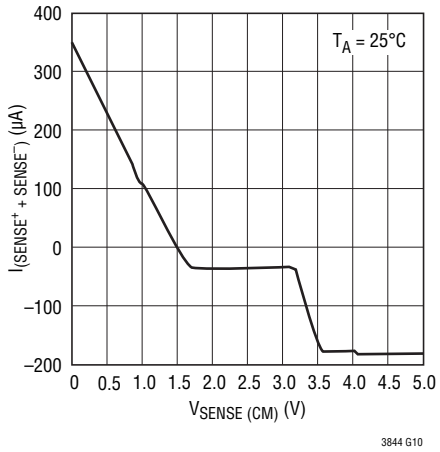


Error Amp Transconductance vs Temperature

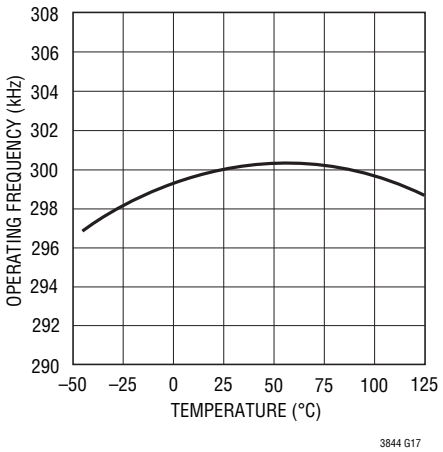


TYPICAL PERFORMANCE CHARACTERISTICS

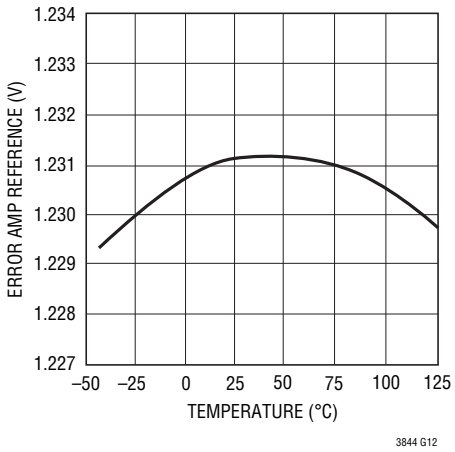
$I_{(SENSE^+ + SENSE^-)}$ vs $V_{SENSE(CM)}$



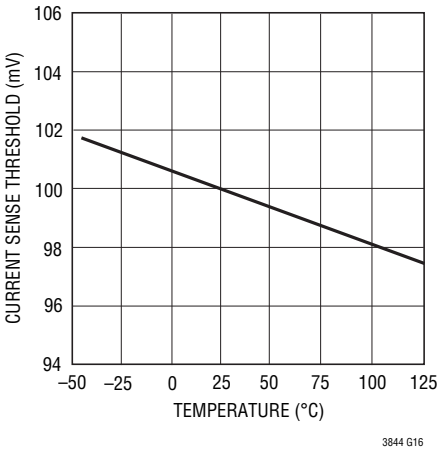
Operating Frequency vs Temperature



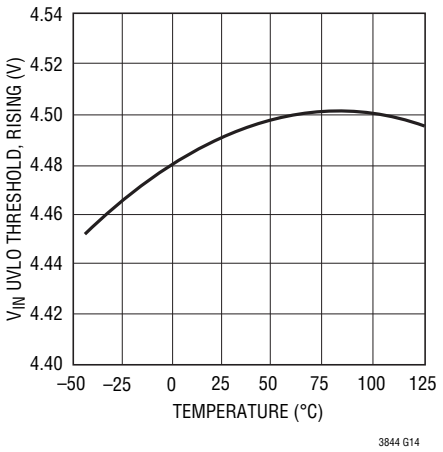
Error Amp Reference vs Temperature



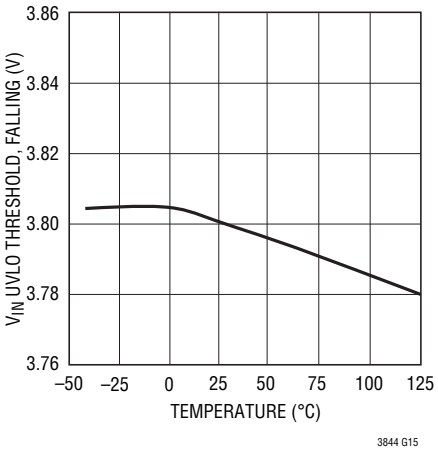
Maximum Current Sense Threshold vs Temperature



V_{IN} UVLO Threshold (Rising) vs Temperature



V_{IN} UVLO Threshold (Falling) vs Temperature



PIN FUNCTIONS

V_{IN} (Pin 1): The V_{IN} pin is the main supply pin and should be decoupled to SGND with a low ESR capacitor located close to the pin.

$\overline{SHDN}$ (Pin 2): The $\overline{SHDN}$ pin has a precision IC enable threshold of 1.35V (rising) with 120mV of hysteresis. It is used to implement an undervoltage lockout (UVLO) circuit. See Applications Information section for implementing a UVLO function. When the $\overline{SHDN}$ pin is pulled below a transistor V_{BE} (0.7V), a low current shutdown mode is entered, all internal circuitry is disabled and the V_{IN} supply current is reduced to approximately 9µA. Typical pin input bias current is <10µA and the pin is internally clamped to 6V.

C_{SS} (Pin 3): The soft-start pin is used to program the supply soft-start function. Use the following formula to calculate C_{SS} for a given output voltage slew rate:

$$C_{SS} = 2\mu A(t_{SS}/1.231V)$$

The pin should be left unconnected when not using the soft-start function.

BURST_EN (Pin 4): The BURST_EN pin is used to enable or disable Burst Mode operation. Connect the BURST_EN pin to ground to enable the burst mode function. Connect the pin to V_{FB} or V_{CC} to disable the Burst Mode function.

V_{FB} (Pin 5): The output voltage feedback pin, V_{FB}, is externally connected to the supply output voltage via a resistive divider. The V_{FB} pin is internally connected to the inverting input of the error amplifier. In regulation, V_{FB} is 1.231V.

V_C (Pin 6): The V_C pin is the output of the error amplifier whose voltage corresponds to the maximum (peak) switch current per oscillator cycle. The error amplifier is typically configured as an integrator circuit by connecting an RC network from the V_C pin to SGND. This circuit creates the dominant pole for the converter regulation control loop. Specific integrator characteristics can be configured to optimize transient response. When Burst Mode operation is enabled (see Pin 4 description), an internal low impedance clamp on the V_C pin is set at 100mV below the burst threshold, which limits the negative excursion of the pin voltage. Therefore, this pin cannot be pulled low with a low impedance source. If the V_C pin must be externally manipulated, do so through a 1k series resistance.

SYNC (Pin 7): The SYNC pin provides an external clock input for synchronization of the internal oscillator. R_{SET} is set such that the internal oscillator frequency is 10% to 25% below the external clock frequency. If unused the SYNC pin is connected to SGND. For more information see "Oscillator Sync" in the Applications Information section of this data sheet.

f_{SET} (Pin 8): The f_{SET} pin programs the oscillator frequency with an external resistor, R_{SET}. The resistor is required even when supplying external sync clock signal. See the Applications Information section for resistor value selection details.

SGND (Pin 9, 17): The SGND pin is the low noise ground reference. It should be connected to the $-V_{OUT}$ side of the output capacitors. Careful layout of the PCB is necessary to keep high currents away from this SGND connection. See the Applications Information section for helpful hints on PCB layout of grounds.

$SENSE^-$ (Pin 10): The $SENSE^-$ pin is the negative input for the current sense amplifier and is connected to the V_{OUT} side of the sense resistor for step-down applications. The sensed inductor current limit is set to 100mV across the SENSE inputs.

$SENSE^+$ (Pin 11): The $SENSE^+$ pin is the positive input for the current sense amplifier and is connected to the inductor side of the sense resistor for step-down applications. The sensed inductor current limit is set to 100mV across the SENSE inputs.

PGND (Pin 12): The PGND pin is the high current ground reference for internal low side switch and the V_{CC} regulator circuit. Connect the pin directly to the negative terminal of the V_{CC} decoupling capacitor. See the Applications Information section for helpful hints on PCB layout of grounds.

PIN FUNCTIONS

V_{CC} (Pin 13): The V_{CC} pin is the internal bias supply decoupling node. Use a low ESR 1µF or greater ceramic capacitor to decouple this node to PGND. Most internal IC functions are powered from this bias supply. An external diode connected from V_{CC} to the BOOST pin charges the bootstrapped capacitor during the off-time of the main power switch. Back driving the V_{CC} pin from an external DC voltage source, such as the V_{OUT} output of the regulator supply, increases overall efficiency and reduces power dissipation in the IC. In shutdown mode this pin sinks 20µA until the pin voltage is discharged to 0V.

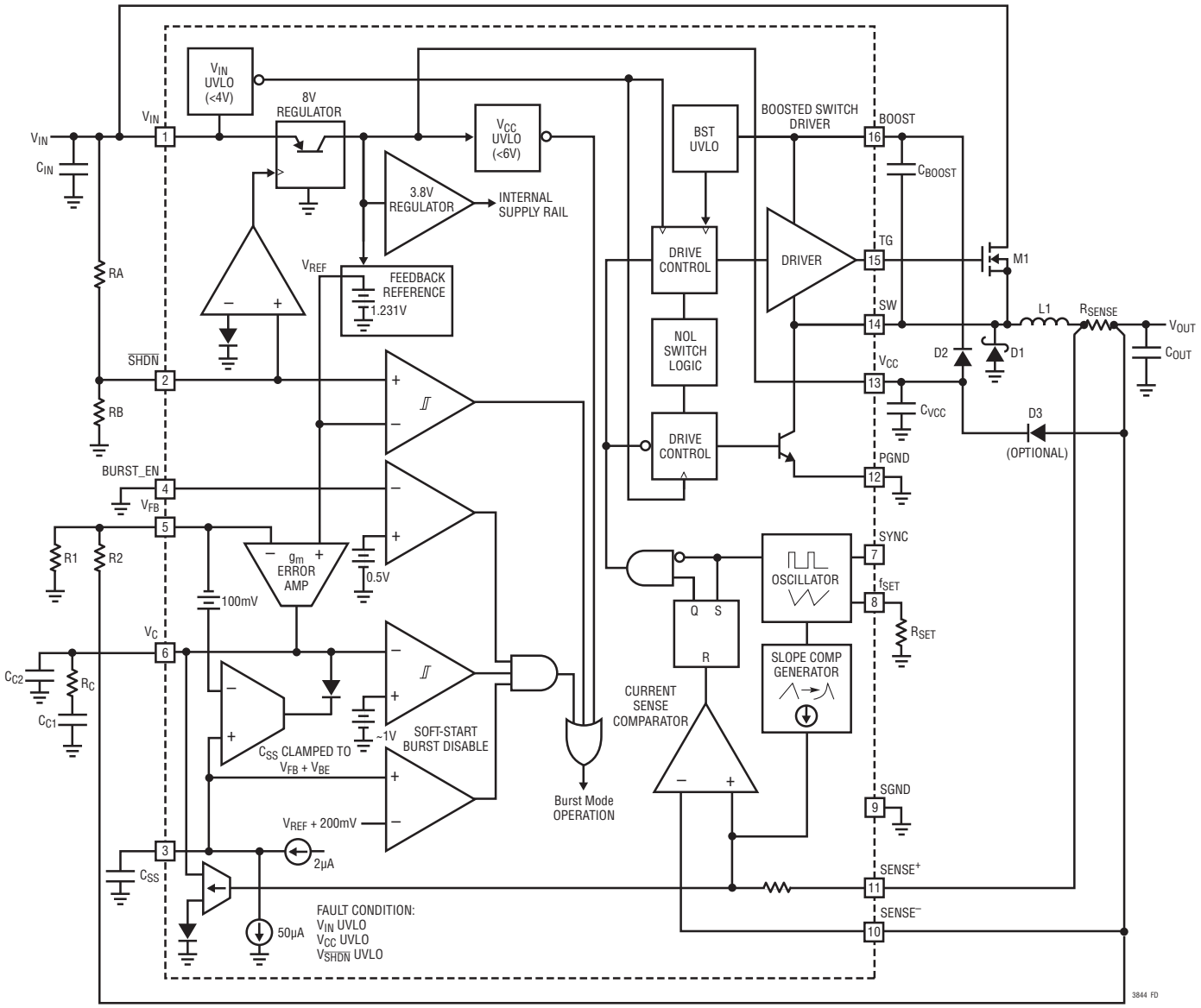
SW (Pin 14): In step-down applications the SW pin is connected to the cathode of an external clamping Schottky diode, the drain of the power MOSFET and the inductor. The SW node voltage swing is from V_{IN} during the on-time of the power MOSFET, to a Schottky voltage drop below ground during the off-time of the power MOSFET. In start-up and in operating modes where there is insufficient inductor current to freewheel the Schottky diode, an internal switch is turned on to pull the SW pin to ground so that the BOOST pin capacitor can be charged. Give careful consideration in choosing the Schottky diode to limit the negative voltage swing on the SW pin.

TG (Pin 15): The TG pin is the bootstrapped gate drive for the top N-Channel MOSFET. Since very fast high currents are driven from this pin, connect it to the gate of the power MOSFET with a short and wide, typically 0.02" width, PCB trace to minimize inductance.

BOOST (Pin 16): The BOOST pin is the supply for the bootstrapped gate drive and is externally connected to a low ESR ceramic boost capacitor referenced to SW pin. The recommended value of the BOOST capacitor, C_{BOOST}, is 50 times greater than the total input capacitance of the topside MOSFET. In most applications 0.1µF is adequate. The maximum voltage that this pin sees is $V_{IN} + V_{CC}$, ground referred.

Exposed Pad (Pin 17): SGND. The exposed leadframe is internally connected to the SGND pin. Solder the exposed pad to the PCB ground for electrical contact and optimal thermal performance.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

The LT3844 is a PWM controller with a constant frequency, current mode control architecture. It is designed for low to medium power, switching regulator applications. Its high operating voltage capability allows it to step up or down input voltages up to 60V without the need for a transformer. The LT3844 is used in nonsynchronous applications, meaning that a freewheeling rectifier diode (D1 of Function Diagram) is used instead of a bottom side MOSFET. For circuit operation, please refer to the Functional Diagram of the IC and Typical Application on the front page of the data sheet. The LT3800 is a similar part that uses synchronous rectification, replacing the diode with a MOSFET in a step-down application.

Main Control Loop

During normal operation, the external N-channel MOSFET switch is turned on at the beginning of each cycle. The switch stays on until the current in the inductor exceeds a current threshold set by the DC control voltage, V_C, which is the output of the voltage control loop. The voltage control loop monitors the output voltage, via the V_{FB} pin voltage, and compares it to an internal 1.231V reference. It increases the current threshold when the V_{FB} voltage is below the reference voltage and decreases the current threshold when the V_{FB} voltage is above the reference voltage. For instance, when an increase in the load current occurs, the output voltage drops causing the V_{FB} voltage to drop relative to the 1.231V reference. The voltage control loop senses the drop and increases the current threshold. The peak inductor current is increased until the average inductor current equals the new load current and the output voltage returns to regulation.

Current Limit/Short-Circuit

The inductor current is measured with a series sense resistor (see the Typical Application on the front page). When the voltage across the sense resistor reaches the maximum current sense threshold, typically 100mV, the TG MOSFET driver is disabled for the remainder of that cycle. If the maximum current sense threshold is still exceeded at the beginning of the next cycle, the entire cycle is skipped. Cycle skipping keeps the inductor currents to a reasonable value during a short-circuit, particularly when V_{IN} is high. Setting the sense resistor value is discussed in the "Application Information" section.

V_{CC}/Boosted Supply

An internal V_{CC} regulator provides V_{IN} derived gate-drive power for start-up under all operating conditions with MOSFET gate charge loads up to 90nC. The regulator can operate continuously in applications with V_{IN} voltages up to 60V, provided the power dissipation of the regulator does not exceed 250mW. The power dissipation is calculated as follows:

$$P_{d(REG)} = (V_{IN} - 8V) \bullet f_{SW} \bullet Q_G$$

where Q_G is the MOSFET gate charge.

In applications where these conditions are exceeded, V_{CC} must be derived from an external source after start-up. Maximum continuous regulator power dissipation may be exceeded for short duration V_{IN} transients.

For higher converter efficiency and less power dissipation in the IC, V_{CC} can also be supplied from an external supply such as the converter output. When an external supply back drives the internal V_{CC} regulator through an external diode and the V_{CC} voltage is pulled to a diode above its regulation voltage, the internal regulator is disabled and goes into a low current mode. V_{CC} is the bias supply for most of the internal IC functions and is also used to charge the bootstrapped capacitor (C_{BOOST}) via an external diode. The external MOSFET switch is biased from the bootstrapped capacitor. While the external MOSFET switch is off, an internal BJT switch, whose collector is connected to the SW pin and emitter is connected to the PGND pin, is turned on to pull the SW node to PGND and recharge the bootstrap capacitor. The switch stays on until either the start of the next cycle or until the bootstrapped capacitor is fully charged.

MOSFET Driver

The LT3844 contains a high speed boosted driver to turn on and off an external N-channel MOSFET switch. The MOSFET driver derives its power from the boost capacitor which is referenced to the SW pin and the source of the MOSFET. The driver provides a large pulse of current to turn on the MOSFET fast to minimize transition times. Multiple MOSFETs can be paralleled for higher current operation.

OPERATION (Refer to Functional Diagram)

To eliminate the possibility of shoot through between the MOSFET and the internal SW pull-down switch, an adaptive nonoverlap circuit ensures that the internal pull-down switch does not turn on until the gate of the MOSFET is below its turn on threshold.

Low Current Operation (Burst Mode Operation)

To increase low current load efficiency, the LT3844 is capable of operating in Linear Technology's proprietary Burst Mode operation where the external MOSFET operates intermittently based on load current demand. The Burst Mode function is disabled by connecting the BURST_EN pin to V_{CC} or V_{FB} and enabled by connecting the pin to SGND.

When the required switch current, sensed via the V_C pin voltage, is below 15% of maximum, Burst Mode operation is employed and that level of sense current is latched onto the IC control path. If the output load requires less than this latched current level, the converter will overdrive the output slightly during each switch cycle. This overdrive condition is sensed internally and forces the voltage on the V_C pin to continue to drop. When the voltage on V_C drops 150mV below the 15% load level, switching is disabled, and the LT3844 shuts down most of its internal circuitry, reducing total quiescent current to 120µA. When the converter output begins to fall, the V_C pin voltage begins to climb. When the voltage on the V_C pin climbs back to the 15% load level, the IC returns to normal operation and switching resumes. An internal clamp on the V_C pin is set at 100mV below the output disable threshold, which limits the negative excursion of the pin voltage, minimizing the converter output ripple during Burst Mode operation.

During Burst Mode operation, the V_{IN} pin current is 20µA and the V_{CC} current is reduced to 100µA. If no external drive is provided for V_{CC}, all V_{CC} bias currents originate from the V_{IN} pin, giving a total V_{IN} current of 120µA. Burst current can be reduced further when V_{CC} is driven using an output derived source, as the V_{CC} component of V_{IN} current is then reduced by the converter duty cycle ratio.

Start-Up

The following section describes the start-up of the supply and operation down to 4V once the step-down supply is up and running. For the protection of the LT3844 and the switching supply, there are internal undervoltage lockout (UVLO) circuits with hysteresis on V_{IN}, V_{CC} and V_{BOOST}, as shown in the Electrical Characteristics table. Start-up and continuous operation require that all three of these undervoltage lockout conditions be satisfied because the TG MOSFET driver is disabled during any UVLO fault condition. In start-up, for most applications, V_{CC} is powered from V_{IN} through the high voltage linear regulator of the LT3844. This requires V_{IN} to be high enough to drive the V_{CC} voltage above its undervoltage lockout threshold. V_{CC}, in turn, has to be high enough to charge the BOOST capacitor through an external diode so that the BOOST voltage is above its undervoltage lockout threshold. There is an NPN switch that pulls the SW node to ground each cycle during the TG power MOSFET off-time, ensuring the BOOST capacitor is kept fully charged. Once the supply is up and running, the output voltage of the supply can backdrive V_{CC} through an external diode. Internal circuitry disables the high voltage regulator to conserve V_{IN} supply current. Output voltages that are too low or too high to backdrive V_{CC} require additional circuitry such as a voltage doubler or linear regulator. Once V_{CC} is backdriven from a supply other than V_{IN}, V_{IN} can be reduced to 4V with normal operation maintained.

Soft-Start

The soft-start function controls the slew rate of the power supply output voltage during start-up. A controlled output voltage ramp minimizes output voltage overshoot, reduces inrush current from the V_{IN} supply, and facilitates supply sequencing. A capacitor, C_{SS}, connected from the C_{SS} pin to SGND, programs the slew rate. The capacitor is charged from an internal 2µA current source producing a ramped voltage. The capacitor voltage overrides the internal reference to the error amplifier. If the V_{FB} pin voltage exceeds

OPERATION (Refer to Functional Diagram)

the C_{SS} pin voltage then the current threshold set by the DC control voltage, V_C, is decreased and the inductor current is lowered. This in turn decreases the output voltage slew rate allowing the C_{SS} pin voltage ramp to catch up to the V_{FB} pin voltage. An internal 100mV offset is added to the V_{FB} pin voltage relative to the to C_{SS} pin voltage so that at start-up the soft-start circuit will discharge the V_C pin voltage below the DC control voltage equivalent to zero inductor current. This will reduce the input supply inrush current. The soft-start circuit is disabled once the C_{SS} pin voltage has been charged to 200mV above the internal reference of 1.231V.

During a V_{IN} UVLO, V_{CC} UVLO or $\overline{SHDN}$ UVLO event, the C_{SS} pin voltage is discharged with a 50µA current source. In normal operation the C_{SS} pin voltage is clamped to a diode above the V_{FB} pin voltage. Therefore, the value of the C_{SS} capacitor is relevant in how long of a fault event will retrigger a soft-start. In other words, if any of the above UVLO conditions occur, the C_{SS} pin voltage will be discharged with a 50µA current source. There is a diode worth of voltage headroom to ride through the fault before the C_{SS} pin voltage enters its active region and the soft-start function is enabled.

Also, since the C_{SS} pin voltage is clamped to a diode above the V_{FB} pin voltage, during a short circuit the C_{SS} pin voltage is pulled low because the V_{FB} pin voltage is low. Once the short has been removed the V_{FB} pin voltage starts to recover. The soft-start circuit takes control of the output voltage slew rate once the V_{FB} pin voltage has exceeded the slowly ramping C_{SS} pin voltage, reducing the output voltage overshoot during a short-circuit recovery.

Slope/Antislope Compensation

The IC incorporates slope compensation to eliminate potential subharmonic oscillations in the current control loop. The IC's slope compensation circuit imposes an artificial ramp on the sensed current to increase the rising slope as duty cycle increases.

Typically, this additional ramp affects the sensed current value, thereby reducing the achievable current limit value by the same amount as the added ramp represents. As such, the current limit is typically reduced as the duty cycle increases. The LT3844, however, contains antislope compensation circuitry to eliminate the current limit reduction associated with slope compensation. As the slope compensation ramp is added to the sensed current, a similar ramp is added to the current limit threshold. The end result is that the current limit is not compromised so the LT3844 can provide full power regardless of required duty cycle.

Shutdown

The LT3844 includes a shutdown mode where all the internal IC functions are disabled and the V_{IN} current is reduced to less than 10µA. The shutdown pin can be used for undervoltage lockout with hysteresis, micropower shutdown or as a general purpose on/off control of the converter output. The shutdown function has two thresholds. The first threshold, a precision 1.23V threshold with 120mV of hysteresis, disables the converter from switching. The second threshold, approximately a 0.7V referenced to SGND, completely disables all internal circuitry and reduces the V_{IN} current to less than 10µA. See the Application Information section for more information.

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The basic LT3844 step-down (buck) application, shown in the Typical Application on the front page, converts a larger positive input voltage to a lower positive or negative output voltage. This Application Information section assists selection of external components for the requirements of the power supply.

R_{SENSE} Selection

The current sense resistor, RS_{ENSE}, monitors the inductor current of the supply (See Typical Application on front page). Its value is chosen based on the maximum required output load current. The LT3844 current sense amplifier has a maximum voltage threshold of, typically,

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100mV. Therefore, the peak inductor current is 100mV/R_{SENSE}. The maximum output load current, $I_{OUT(MAX)}$, is the peak inductor current minus half the peak-to-peak ripple current, ΔI_L.

Allowing adequate margin for ripple current and external component tolerances, R_{SENSE} can be calculated as follows:

$$R_{SENSE} = \frac{70mV}{I_{OUT(MAX)}}$$

Typical values for R_{SENSE} are in the range of 0.005Ω to 0.05Ω.

Operating Frequency

The choice of operating frequency and inductor value is a trade off between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses and gate charge losses. However, lower frequency operation requires more inductance for a given amount of ripple current, resulting in a larger inductor size and higher cost. If the ripple current is allowed to increase, larger output capacitors may be required to maintain the same output ripple. For converters with high step-down V_{IN}-to-V_{OUT} ratios, another consideration is the minimum on-time of the LT3844 (see the Minimum On-time Considerations section). A final consideration for operating frequency is that in noise-sensitive communications systems, it is often desirable to keep the switching noise out of a sensitive frequency band. The LT3844 uses a constant frequency architecture that can be programmed over a 100kHz to 500kHz range with a single resistor from the f_{SET} pin to ground, as shown in Figure 1. The nominal voltage on the f_{SET} pin is 1V and the current that flows from this pin is used to charge an internal oscillator capacitor. The value of R_{SET} for a given operating frequency can be chosen from Figure 4 or from the following equation:

$$R_{SET}(k\Omega) = 8.4 \bullet 10^4 \bullet f_{SW}^{(-1.31)}$$

Table 1 lists typical resistor values for common operating frequencies:

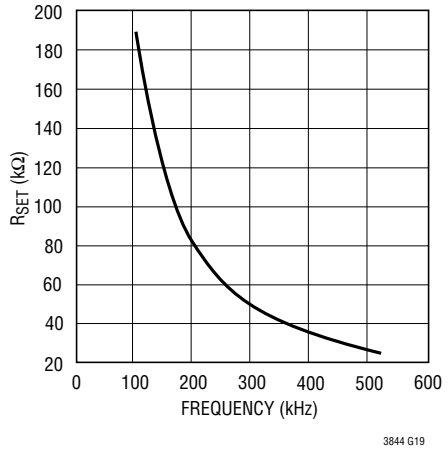


Figure 1. Timing Resistor (R_{SET}) Value

Table 1. Recommended 1% Standard Values

R_{SET}	f_{SW}
191kΩ	100kHz
118kΩ	150kHz
80.6kΩ	200kHz
63.4kΩ	250kHz
49.9kΩ	300kHz
40.2kΩ	350kHz
33.2kΩ	400kHz
27.4kΩ	450kHz
23.2kΩ	500kHz

Step-Down Converter: Inductor Selection

The critical parameters for selection of an inductor are minimum inductance value, volt-second product, saturation current and/or RMS current.

For a given ΔI, The minimum inductance value is calculated as follows:

$$L \geq V_{OUT} \bullet \frac{V_{IN(MAX)} - V_{OUT}}{f_{SW} \bullet V_{IN(MAX)} \bullet \Delta I_L}$$

f_{SW} is the switch frequency.

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The typical range of values for ΔI_L is (0.2 • $I_{OUT(MAX)}$) to (0.5 • $I_{OUT(MAX)}$), where $I_{OUT(MAX)}$ is the maximum load current of the supply. Using ΔI_L = 0.3 • $I_{OUT(MAX)}$ yields a good design compromise between inductor performance versus inductor size and cost. A value of ΔI_L = 0.3 • $I_{OUT(MAX)}$ produces a ±15% of $I_{OUT(MAX)}$ ripple current around the DC output current of the supply. Lower values of ΔI_L require larger and more costly magnetics. Higher values of ΔI_L will increase the peak currents, requiring more filtering on the input and output of the supply. If ΔI_L is too high, the slope compensation circuit is ineffective and current mode instability may occur at duty cycles greater than 50%. To satisfy slope compensation requirements the minimum inductance is calculated as follows:

$$L > V_{OUT} \bullet \frac{2DC_{MAX} - 1}{DC_{MAX}} \bullet \frac{R_{SENSE} \bullet 8.33}{f_{SW}}$$

Some magnetics vendors specify a volt-second product in their data sheet. If they do not, consult the magnetics vendor to make sure the specification is not being exceeded by your design. The volt-second product is calculated as follows:

$$\text{Volt-second } (\mu s) = \frac{(V_{IN(MAX)} - V_{OUT}) \bullet V_{OUT}}{V_{IN(MAX)} \bullet f_{SW}}$$

The magnetics vendors specify either the saturation current, the RMS current or both. When selecting an inductor based on inductor saturation current, use the peak current through the inductor, $I_{OUT(MAX)} + \Delta I_L/2$. The inductor saturation current specification is the current at which the inductance, measured at zero current, decreases by a specified amount, typically 30%.

When selecting an inductor based on RMS current rating, use the average current through the inductor, $I_{OUT(MAX)}$. The RMS current specification is the RMS current at which the part has a specific temperature rise, typically 40°C, above 25°C ambient.

After calculating the minimum inductance value, the volt-second product, the saturation current and the RMS current for your design, select an off-the-shelf inductor. Contact the Application group at Linear Technology for further support.

For more detailed information on selecting an inductor, please see the "Inductor Selection" section of Linear Technology Application Note 44.

Step-Down Converter: MOSFET Selection

The selection criteria of the external N-channel standard level power MOSFET include on resistance($R_{DS(ON)}$), reverse transfer capacitance (C_{RSS}), maximum drain source voltage (V_{DSS}), total gate charge (Q_G) and maximum continuous drain current.

For maximum efficiency, minimize $R_{DS(ON)}$ and C_{RSS}. Low $R_{DS(ON)}$ minimizes conduction losses while low C_{RSS} minimizes transition losses. The problem is that $R_{DS(ON)}$ is inversely related to C_{RSS}. Balancing the transition losses with the conduction losses is a good idea in sizing the MOSFET. Select the MOSFET to balance the two losses.

Calculate the maximum conduction losses of the MOSFET:

$$P_{COND} = (I_{OUT(MAX)})^2 \left(\frac{V_{OUT}}{V_{IN}}\right)(R_{DS(ON)})$$

Note that $R_{DS(ON)}$ has a large positive temperature dependence. The MOSFET manufacturer's data sheet contains a curve, $R_{DS(ON)}$ vs Temperature.

Calculate the maximum transition losses:

$$P_{TRAN} = (k)(V_{IN})^2 (I_{OUT(MAX)})(C_{RSS})(f_{SW})$$

where k is a constant inversely related to the gate driver current, approximated by k = 2 for LT3844 applications.

The total maximum power dissipation of the MOSFET is the sum of these two loss terms:

$$P_{FET(TOTAL)} = P_{COND} + P_{TRAN}$$

To achieve high supply efficiency, keep the $P_{FET(TOTAL)}$ to less than 3% of the total output power. Also, complete a thermal analysis to ensure that the MOSFET junction temperature is not exceeded.

$$T_J = T_A + P_{FET(TOTAL)} \bullet \theta_{JA}$$

where θ_{JA} is the package thermal resistance and T_A is the ambient temperature. Keep the calculated T_J below the maximum specified junction temperature, typically 150°C.

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Note that when V_{IN} is high and f_{SW} is high, the transition losses may dominate. A MOSFET with higher $R_{DS(ON)}$ and lower C_{RSS} may provide higher efficiency. MOSFETs with higher voltage V_{DSS} specification usually have higher $R_{DS(ON)}$ and lower C_{RSS}.

Choose the MOSFET V_{DSS} specification to exceed the maximum voltage across the drain to the source of the MOSFET, which is $V_{IN(MAX)}$ plus any additional ringing on the switch node. Ringing on the switch node can be greatly reduced with good PCB layout and, if necessary, an RC snubber.

The internal V_{CC} regulator is capable of sourcing up to 40mA which limits the maximum total MOSFET gate charge, Q_G, to 40mA/f_{SW}. The Q_G vs V_{GS} specification is typically provided in the MOSFET data sheet. Use Q_G at V_{GS} of 8V. If V_{CC} is back driven from an external supply, the MOSFET drive current is not sourced from the internal regulator of the LT3844 and the Q_G of the MOSFET is not limited by the IC. However, note that the MOSFET drive current is supplied by the internal regulator when the external supply back driving V_{CC} is not available such as during start-up or short-circuit.

The manufacturer's maximum continuous drain current specification should exceed the peak switch current, $I_{OUT(MAX)} + \Delta I_L/2$.

During the supply start-up, the gate drive levels are set by the V_{CC} voltage regulator, which is approximately 8V. Once the supply is up and running, the V_{CC} can be back driven by an auxiliary supply such as V_{OUT}. It is important not to exceed the manufacturer's maximum V_{GS} specification. A standard level threshold MOSFET typically has a V_{GS} maximum of 20V.

Step-Down Converter: Rectifier Selection

The rectifier diode (D1 on the Functional Diagram) in a buck converter generates a current path for the inductor current when the main power switch is turned off. The rectifier is selected based upon the forward voltage, reverse voltage and maximum current. A Schottky diode is recommended. Its low forward voltage yields the lowest power loss and highest efficiency. The maximum reverse voltage that the diode will see is $V_{IN(MAX)}$.

In continuous mode operation, the average diode current is calculated at maximum output load current and maximum V_{IN}:

$$I_{DIODE(AVG)} = I_{OUT(MAX)} \frac{V_{IN(MAX)} - V_{OUT}}{V_{IN(MAX)}}$$

To improve efficiency and to provide adequate margin for short-circuit operation, a diode rated at 1.5 to 2 times the maximum average diode current, $I_{DIODE(AVG)}$, is recommended.

Step-Down Converter: Input Capacitor Selection

A local input bypass capacitor is required for buck converters because the input current is pulsed with fast rise and fall times. The input capacitor selection criteria are based on the bulk capacitance and RMS current capability. The bulk capacitance will determine the supply input ripple voltage. The RMS current capability is used to keep from overheating the capacitor.

The bulk capacitance is calculated based on maximum input ripple, ΔV_{IN}:

$$C_{IN(BULK)} = \frac{I_{OUT(MAX)} \bullet V_{OUT}}{\Delta V_{IN} \bullet f_{SW} \bullet V_{IN(MIN)}}$$

ΔV_{IN} is typically chosen at a level acceptable to the user. 100mV to 200mV is a good starting point. Aluminum electrolytic capacitors are a good choice for high voltage, bulk capacitance due to their high capacitance per unit area.

The capacitor's RMS current is:

$$I_{CIN(RMS)} = I_{OUT} \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{(V_{IN})^2}}$$

If applicable, calculate it at the worst-case condition, $V_{IN} = 2V_{OUT}$. The RMS current rating of the capacitor is specified by the manufacturer and should exceed the calculated $I_{CIN(RMS)}$. Due to their low ESR (equivalent series resistance), ceramic capacitors are a good choice for high voltage, high RMS current handling. Note that the ripple current ratings from aluminum electrolytic capacitor manufacturers are based on 2000 hours of life. This makes

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it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required.

The combination of aluminum electrolytic capacitors and ceramic capacitors is an economical approach to meeting the input capacitor requirements. The capacitor voltage rating must be rated greater than $V_{IN(MAX)}$. Multiple capacitors may also be paralleled to meet size or height requirements in the design. Locate the capacitor very close to the MOSFET switch and use short, wide PCB traces to minimize parasitic inductance.

Step-Down Converter: Output Capacitor Selection

The output capacitance, C_{OUT}, selection is based on the design's output voltage ripple, ΔV_{OUT} and transient load requirements. ΔV_{OUT} is a function of ΔI_L and the C_{OUT} ESR. It is calculated by:

$$\Delta V_{OUT} = \Delta I_L \bullet \left(ESR + \frac{1}{(8 \bullet f_{SW} \bullet C_{OUT})} \right)$$

The maximum ESR required to meet a ΔV_{OUT} design requirement can be calculated by:

$$ESR(MAX) = \frac{(\Delta V_{OUT})(L)(f_{SW})}{V_{OUT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)}$$

Worst-case ΔV_{OUT} occurs at highest input voltage. Use paralleled multiple capacitors to meet the ESR requirements. Increasing the inductance is an option to lower the ESR requirements. For extremely low ΔV_{OUT}, an additional LC filter stage can be added to the output of the supply. Application Note 44 has some good tips on sizing an additional output filter.

Output Voltage Programming

A resistive divider sets the DC output voltage according to the following formula:

$$R2 = R1\left(\frac{V_{OUT}}{1.231V} - 1\right)$$

The external resistor divider is connected to the output of the converter as shown in Figure 2. Tolerance of the feedback resistors will add additional error to the output voltage.

Example: V_{OUT} = 12V; R1 = 10k

$$R2 = 10k\left(\frac{12V}{1.231V} - 1\right) = 87.48k - \text{use } 86.6k\ 1\%$$

The V_{FB} pin input bias current is typically 25nA, so use of extremely high value feedback resistors could cause a converter output that is slightly higher than expected. Bias current error at the output can be estimated as:

$$\Delta V_{OUT(BIAS)} = 25nA \bullet R2$$

Supply UVLO and Shutdown

The $\overline{SHDN}$ pin has a precision voltage threshold with hysteresis which can be used as an undervoltage lockout threshold (UVLO) for the power supply. Undervoltage lockout keeps the LT3844 in shutdown until the supply input voltage is above a certain voltage programmed by the user. The hysteresis voltage prevents noise from falsely tripping UVLO.

Resistors are chosen by first selecting R_B. Then:

$$R_A = R_B \bullet \left(\frac{V_{SUPPLY(ON)}}{1.35V} - 1\right)$$

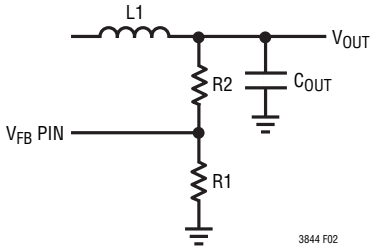


Figure 2. Output Voltage Feedback Divider

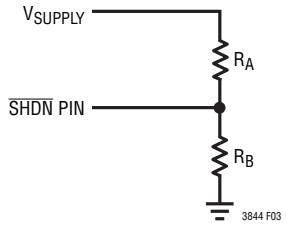


Figure 3. Undervoltage Lockout Circuit

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$V_{SUPPLY(ON)}$ is the input voltage at which the undervoltage lockout is disabled and the supply turns on.

Example: Select $R_B = 49.9k\Omega$, $V_{SUPPLY(ON)} = 14.5V$ (based on a 15V minimum input voltage)

$$R_A = 49.9k \bullet \left(\frac{14.5V}{1.35V} - 1\right)$$

$$= 486.1k \text{ (499k resistor is selected)}$$

If low supply current in standby mode is required, select a higher value of R_B.

The supply turn off voltage is 9% below turn on. In the example the $V_{SUPPLY(OFF)}$ would be 13.2V.

If additional hysteresis is desired for the enable function, an external positive feedback resistor can be used from the LT3844 regulator output.

The shutdown function can be disabled by connecting the $\overline{SHDN}$ pin to the V_{IN} through a large value pull-up resistor. This pin contains a low impedance clamp at 6V, so the $\overline{SHDN}$ pin will sink current from the pull-up resistor(R_{PU}):

$$I_{\overline{SHDN}} = \frac{V_{IN} - 6V}{R_{PU}}$$

Because this arrangement will clamp the $\overline{SHDN}$ pin to the 6V, it will violate the 5V absolute maximum voltage rating of the pin. This is permitted, however, as long as the absolute maximum input current rating of 1mA is not exceeded. Input $\overline{SHDN}$ pin currents of <100µA are recommended: a 1M or greater pull-up resistor is typically used for this configuration.

Soft-Start

The desired soft-start time (t_{SS}) is programmed via the C_{SS} capacitor as follows:

$$C_{SS} = \frac{2\mu A \bullet t_{SS}}{1.231V}$$

The amount of time in which the power supply can withstand a V_{IN}, V_{CC} or $V_{\overline{SHDN}}$ UVLO fault condition (t_{FAULT}) before the C_{SS} pin voltage enters its active region is approximated by the following formula:

$$t_{FAULT} = \frac{C_{SS} \bullet 0.65V}{50\mu A}$$

Oscillator SYNC

The oscillator can be synchronized to an external clock. Set the R_{SET} resistor at least 10% below the desired sync frequency.

It is recommended that the SYNC pin be driven with a square wave that has amplitude greater than 2V, pulse width greater than 1ms and rise time less than 500ns. The rising edge of the sync wave form triggers the discharge of the internal oscillator capacitor.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. Express percent efficiency as:

% Efficiency = 100% - (L1 + L2 + L3 + ...)

where L1, L2, etc. are individual loss terms as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main contributors usually account for most of the losses in LT3844 circuits:

1. LT3844 V_{IN} and V_{CC} current loss
2. I^2R conduction losses
3. MOSFET transition loss
4. Schottky diode conduction loss

1. The V_{IN} and V_{CC} currents are the sum of the quiescent currents of the LT3844 and the MOSFET drive currents. The quiescent currents are in the LT3844 Electrical Characteristics table. The MOSFET drive current is a result of charging the gate capacitance of the power MOSFET each cycle with a packet of charge, Q_G. Q_G is found in the MOSFET data sheet. The average charging current is calculated as $Q_G \bullet f_{SW}$. The power loss term due to these currents can be reduced by backdriving V_{CC} with a lower voltage than V_{IN} such as V_{OUT}.

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2. I^2R losses are calculated from the DC resistances of the MOSFET, the inductor, the sense resistor and the input and output capacitors. In continuous conduction mode the average output current flows through the inductor and R_{SENSE} but is chopped between the MOSFET and the Schottky diode. The resistances of the MOSFET ($R_{DS(ON)}$) and the R_{SENSE} multiplied by the duty cycle can be summed with the resistances of the inductor and R_{SENSE} to obtain the total series resistance of the circuit. The total conduction power loss is proportional to this resistance and usually accounts for between 2% to 5% loss in efficiency.
3. Transition losses of the MOSFET can be substantial with input voltages greater than 20V. See MOSFET Selection section.
4. The Schottky diode can be a major contributor of power loss especially at high input to output voltage ratios (low duty cycles) where the diode conducts for the majority of the switch period. Lower V_f reduces the losses. Note that oversizing the diode does not always help because as the diode heats up the V_f is reduced and the diode loss term is decreased.

   I^2R losses and the Schottky diode loss dominate at high load currents. Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% total additional loss in efficiency.

PCB Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation. These items are illustrated graphically in the layout diagram of Figure 3.

1. Keep the signal and power grounds separate. The signal ground consists of the LT3844 SGND pin, the Exposed Pad on the backside of the LT3844 IC and the (–) terminal of V_{OUT}. The signal ground is the quiet ground and does not contain any high, fast currents. The power ground consists of the Schottky diode anode, the (–) terminal of the input capacitor and the ground return of the V_{CC} capacitor. This ground has very fast high currents and is considered the noisy ground. The two grounds are connected to each other only at the (–) terminal of V_{OUT}.
2. Use short wide traces in the loop formed by the MOSFET, the Schottky diode and the input capacitor to minimize high frequency noise and voltage stress from parasitic inductance. Surface mount components are preferred.
3. Connect the V_{FB} pin directly to the feedback resistors independent of any other nodes, such as the $SENSE^-$ pin. Connect the feedback resistors between the (+) and (–) terminals of C_{OUT}. Locate the feedback resistors in close proximity to the LT3844 to keep the high impedance node, V_{FB}, as short as possible.
4. Route the $SENSE^-$ and $SENSE^+$ traces together and keep as short as possible.
5. Locate the V_{CC} and BOOST capacitors in close proximity to the IC. These capacitors carry the MOSFET driver's high peak currents. Place the small-signal components away from high frequency switching nodes (BOOST, SW and TG). In the layout shown in Figure 3, place all the small-signal components on one side of the IC and all the power components on the other. This helps to keep the signal and power grounds separate.
6. A small decoupling capacitor (100pF) is sometimes useful for filtering high frequency noise on the feedback and sense nodes. If used, locate as close to the IC as possible.
7. The LT3844 packaging will efficiently remove heat from the IC through the Exposed Pad on the backside of the part. The Exposed Pad is soldered to a copper footprint on the PCB. Make this footprint as large as possible to improve the thermal resistance of the IC case to ambient air. This helps to keep the LT3844 at a lower temperature.
8. Make the trace connecting the gate of MOSFET M1 to the TG pin of the LT3844 short and wide.

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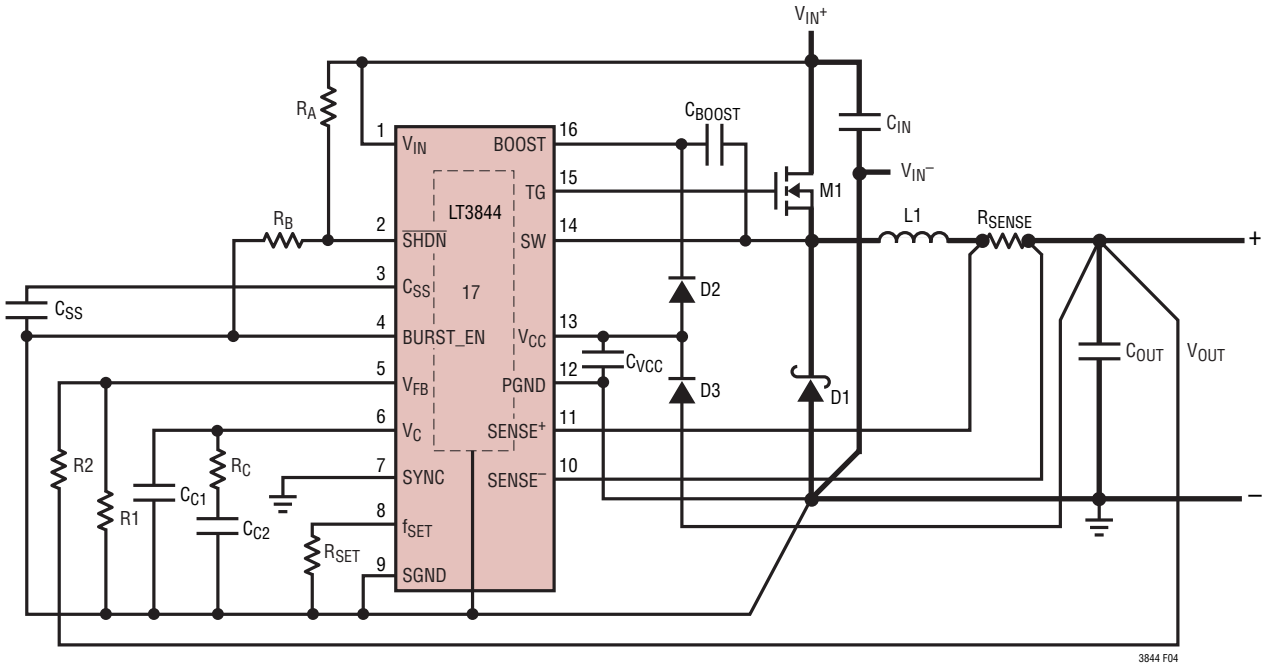


Figure 4. LT3844 Layout Diagram (See PCB Layout Checklist)

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Minimum On-Time Considerations (Buck Mode)

Minimum on-time, $t_{ON(MIN)}$, is the smallest amount of time that the LT3844 is capable of turning the top MOSFET on and off again. It is determined by internal timing delays and the amount of gate charge required turning on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \bullet f_{SW}} > t_{ON(MIN)}$$

where $t_{ON(MIN)}$ is typically 350ns worst case.

If the duty cycle falls below what can be accommodated by the minimum on-time, the LT3844 will begin to skip cycles. The output will be regulated, but the ripple current and ripple voltage will increase. If lower frequency operation is acceptable, the on-time can be increased above $t_{ON(MIN)}$ for the same step-down ratio.

Boost Converter Design

The LT3844 can be used to configure a boost converter to step-up voltages to as high as hundreds of volts. An example of a boost converter circuit schematic is shown in the Typical Applications section. The following sections are a guide to designing a boost converter:

The maximum duty cycle of the main switch is:

$$DC_{MAX} = \frac{V_{OUT} - V_{IN(MIN)}}{V_{OUT}}$$

Boost Converter: Inductor Selection

The critical parameters for selection of an inductor are minimum inductance value and saturation current. The minimum inductance value is calculated as follows:

$$L_{MIN} = \frac{V_{IN(MIN)}}{\Delta I_L \bullet f_{SW}} \bullet DC_{MAX}$$

f_{SW} is the switch frequency.

Similar to the buck converter, the typical range of values for ΔI_L is $(0.2 \bullet I_{L(MAX)})$ to $(0.5 \bullet I_{L(MAX)})$, where $I_{L(MAX)}$ is the maximum average inductor current.

$$I_{L(MAX)} = I_{OUT(MAX)} \bullet \frac{V_{OUT}}{V_{IN(MIN)}}$$

Using $\Delta I_L = 0.3 \bullet I_{L(MAX)}$ yields a good design compromise between inductor performance versus inductor size and cost.

The inductor must not saturate at the peak operating current, $I_{L(MAX)} + \Delta I_L/2$. The inductor saturation current specification is the current at which the inductance, measured at zero current, decreases by a specified amount, typically 30%.

One drawback of boost regulators is that they cannot be current limited for output shorts because the current steering diode makes a direct connection between input and output. Therefore, the inductor current during an output short circuit is only limited by the available current of the input supply.

After calculating the minimum inductance value and the saturation current for your design, select an off-the-shelf inductor. For more detailed information on selecting an inductor, please see the “Inductor Selection” section of Linear Technology Application Note 19.

Boost Converter: MOSFET Selection

The selection criteria of the external N-channel standard level power MOSFET include on resistance ($R_{DS(ON)}$), reverse transfer capacitance (C_{RSS}), maximum drain source voltage (V_{DSS}), total gate charge (Q_G) and maximum continuous drain current.

For maximum efficiency, minimize $R_{DS(ON)}$ and C_{RSS}. Low $R_{DS(ON)}$ minimizes conduction losses while low C_{RSS} minimizes transition losses. The problem is that $R_{DS(ON)}$ is inversely related to C_{RSS}. Balancing the transition losses with the conduction losses is a good idea in sizing the

APPLICATIONS INFORMATION

MOSFET. Select the MOSFET to balance the two losses. Calculate the maximum conduction losses of the MOSFET:

$$P_{COND} = DC_{MAX}\left(\frac{I_{OUT(MAX)}}{1-DC_{MAX}}\right)\bullet R_{DS(ON)}$$

Note that $R_{DS(ON)}$ has large positive temperature dependence. The MOSFET manufacturer's data sheet contains a curve, $R_{DS(ON)}$ vs Temperature. Calculate the maximum transition losses:

$$P_{TRAN} = \frac{(k)(V_{OUT})^2(I_{OUT(MAX)})(C_{RSS})(f_{SW})}{(1-DC_{MAX})}$$

where k is a constant inversely related to the gate driver current, approximated by k = 2 for LT3844 applications. The total maximum power dissipation of the MOSFET is the sum of these two loss terms:

$$P_{FET(TOTAL)} = P_{COND} + P_{TRAN}$$

To achieve high supply efficiency, keep the $P_{FET(TOTAL)}$ to less than 3% of the total output power. Also, complete a thermal analysis to ensure that the MOSFET junction temperature is not exceeded.

$$T_J = T_A + P_{FET(TOTAL)} \bullet \theta_{JA}$$

where θ_{JA} is the package thermal resistance and T_A is the ambient temperature. Keep the calculated T_J below the maximum specified junction temperature, typically 150°C. Note that when V_{OUT} is high (>20V), the transition losses may dominate. A MOSFET with higher $R_{DS(ON)}$ and lower C_{RSS} may provide higher efficiency. MOSFETs with higher voltage V_{DSS} specification usually have higher $R_{DS(ON)}$ and lower C_{RSS}.

Choose the MOSFET V_{DSS} specification to exceed the maximum voltage across the drain to the source of the MOSFET, which is V_{OUT} plus the forward voltage of the rectifier, typically less than 1V.

The internal V_{CC} regulator is capable of sourcing up to 40mA which limits the maximum total MOSFET gate charge, Q_G, to 40mA / f_{SW}. The Q_G vs V_{GS} specification is typically provided in the MOSFET data sheet. Use Q_G at V_{GS} of 8V. If V_{CC} is back driven from an external supply, the MOSFET drive current is not sourced from the internal regulator of the LT3844 and the Q_G of the MOSFET is not limited by the IC. However, note that the MOSFET drive current is supplied by the internal regulator when the external supply back driving V_{CC} is not available such as during start-up or short-circuit.

The manufacturer's maximum continuous drain current specification should exceed the peak switch current which is the same as the inductor peak current, $I_{L(MAX)} + \Delta I_L/2$.

During the supply start-up, the gate drive levels are set by the V_{CC} voltage regulator, which is approximately 8V. Once the supply is up and running, the V_{CC} can be back driven by an auxiliary supply such as V_{OUT}. It is important not to exceed the manufacturer's maximum V_{GS} specification. A standard level threshold MOSFET typically has a V_{GS} maximum of 20V.

Boost Converter: Rectifier Selection

The rectifier is selected based upon the forward voltage, reverse voltage and maximum current. A Schottky diode is recommended for its low forward voltage and yields the lowest power loss and highest efficiency. The maximum reverse voltage that the diode will see is V_{OUT}. The average diode current is equal to the maximum output load current, $I_{OUT(MAX)}$. A diode rated at 1.5 to 2 times the maximum average diode current is recommended. Remember boost converters are not short-circuit protected.

Boost Converter: Output Capacitor Selection

In boost mode, the output capacitor requirements are more demanding due to the fact that the current waveform is pulsed instead of continuous as in a buck converter. The choice of component(s) is driven by the acceptable ripple voltage which is affected by the ESR, ESL and bulk capacitance. The total output ripple voltage is:

$$\Delta V_{OUT} = I_{OUT(MAX)}\left(\frac{1}{f_{SW}\bullet C_{OUT}} + \frac{ESR}{1-DC_{MAX}}\right)$$

where the first term is due to the bulk capacitance and the second term due to the ESR.

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The choice of output capacitor is also driven by the RMS ripple current requirement. The RMS ripple current is:

$$I_{RMS(COUT)} = I_{OUT(MAX)} \bullet \sqrt{\frac{V_{OUT} - V_{IN(MIN)}}{V_{IN(MIN)}}}$$

At lower output voltages (<30V) it may be possible to satisfy both the output ripple voltage and RMS requirements with one or more capacitors of a single type. However, at output voltages above 30V where capacitors with both low ESR and high bulk capacitance are hard to find, the best approach is to use a combination of aluminum electrolytic and ceramic capacitors. The low ESR ceramic capacitor will minimize the ESR while the Aluminum Electrolytic capacitor will supply the required bulk capacitance.

Boost Converter: Input Capacitor Selection

The input capacitor of a boost converter is less critical than the output capacitor, due to the fact that the inductor is in series with the input and the input current waveform is continuous. The input voltage source impedance determines the size of the input capacitor, which is typically in the range of 10µF to 100µF. A low ESR capacitor is recommended though not as critical as with the output capacitor. The RMS input capacitor ripple current for a boost converter is:

$$I_{RMS(CIN)} = 0.3 \bullet \frac{V_{IN(MIN)}}{L \bullet f_{SW}} \bullet DC_{MAX}$$

Please note that the input capacitor can see a very high surge current when a battery is suddenly connected to the input of the converter and solid tantalum capacitors can fail catastrophically under these conditions. Be sure to specify surge-tested capacitors.

Boost Converter: R_{SENSE} Selection

The boost application in the Typical Applications section has the location of the current sense resistor in series with the inductor with one side referenced to V_{IN}. This location was chosen for two reasons. Firstly, the circulating current is always monitored so in the case of an output overvoltage or input overcurrent condition the main switch will skip cycles to protect the circuitry. Secondly, the V_{IN} node can be considered low noise since it is heavily filtered and the input current is not pulsed but continuous.

In the case where the input voltage exceeds the voltage limits on the LT3844 Sense pins, the sense resistor can be moved to the source of the MOSFET. In both cases the resistor value is the calculated using the same formula.

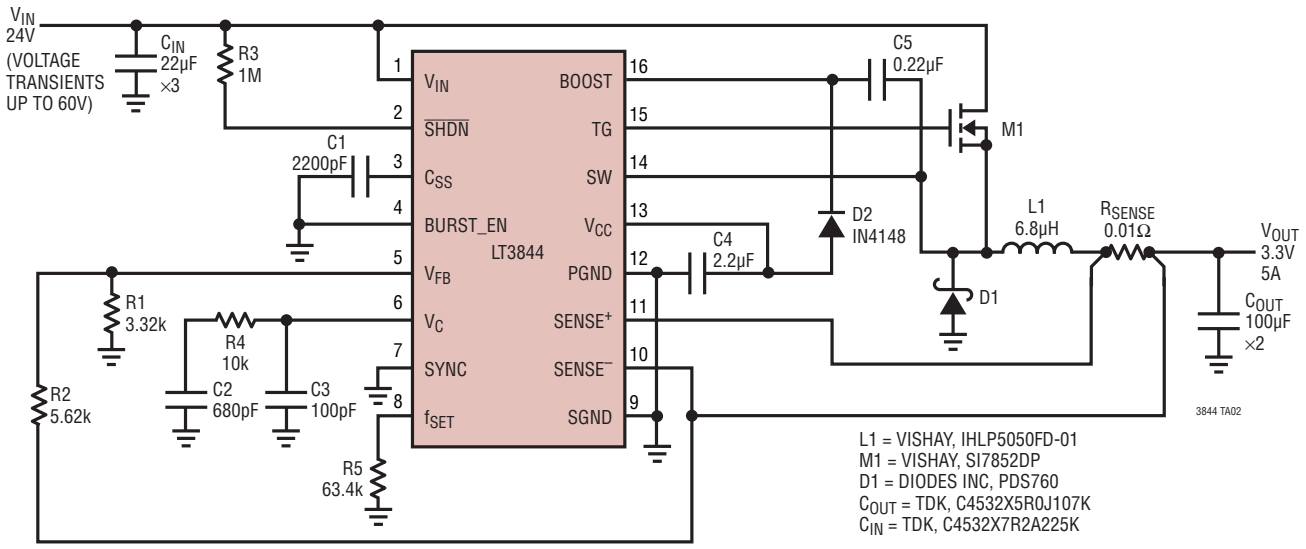
The LT3844 current comparator has a maximum threshold of 100mV/R_{SENSE}. The current comparator threshold sets the peak of the inductor current. Allowing adequate margin for ripple current and external component tolerances, R_{SENSE} can be calculated as follows:

$$R_{SENSE} = \frac{70mV}{I_{L(MAX)}}$$

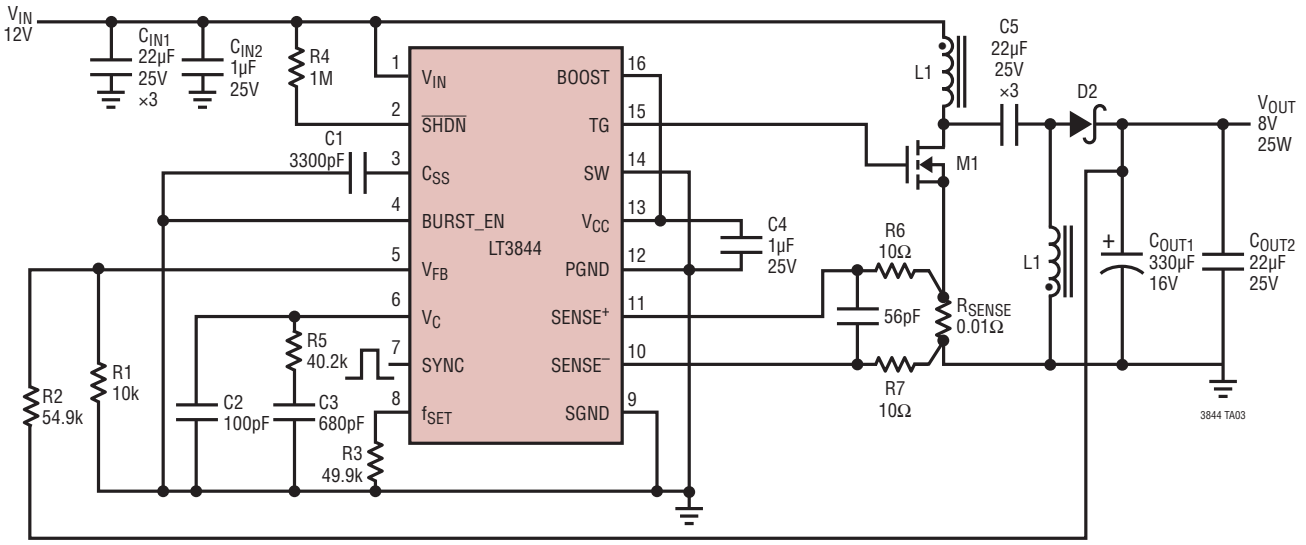
Where $I_{L(MAX)}$ is the maximum average inductor current as calculated in the Boost Converter: Inductor Selection section.

TYPICAL APPLICATIONS

All Ceramic Capacitor Application, 24V to 3.3V at 5A, f_{SW} = 250kHz



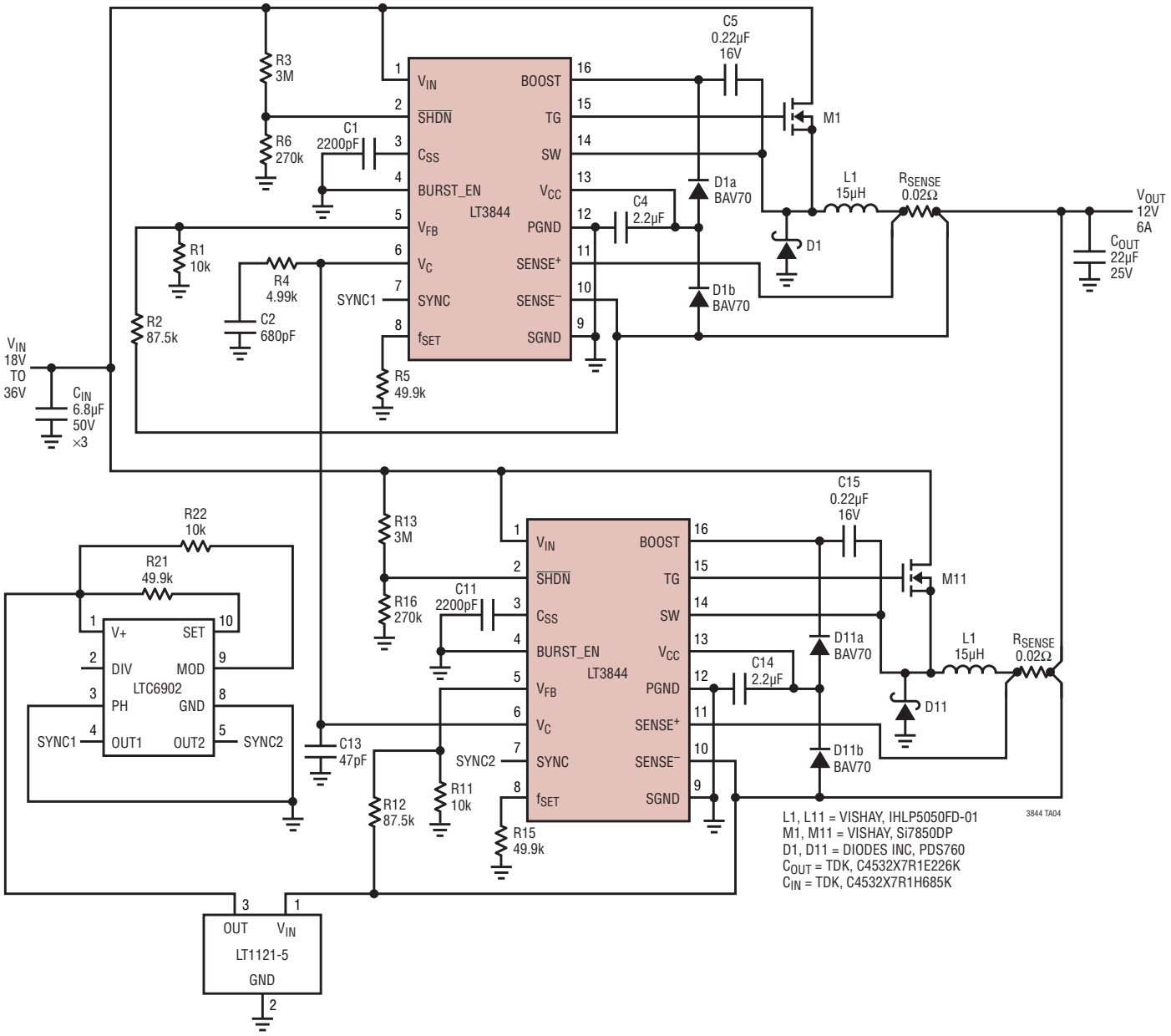
8V to 20V to 8V, 25W SEPIC Application



L1 = COILTRONICS, VERSAPAC VP5-0083
C_{IN}, C5, C_{OUT2} = TDK, C4532X7R1E226M
D2 = ONSEMI, MBRD660
C_{OUT} = SANYO OS-CON, 16SVP330M
C_{IN} = VISHAY, Si7852DP

TYPICAL APPLICATIONS

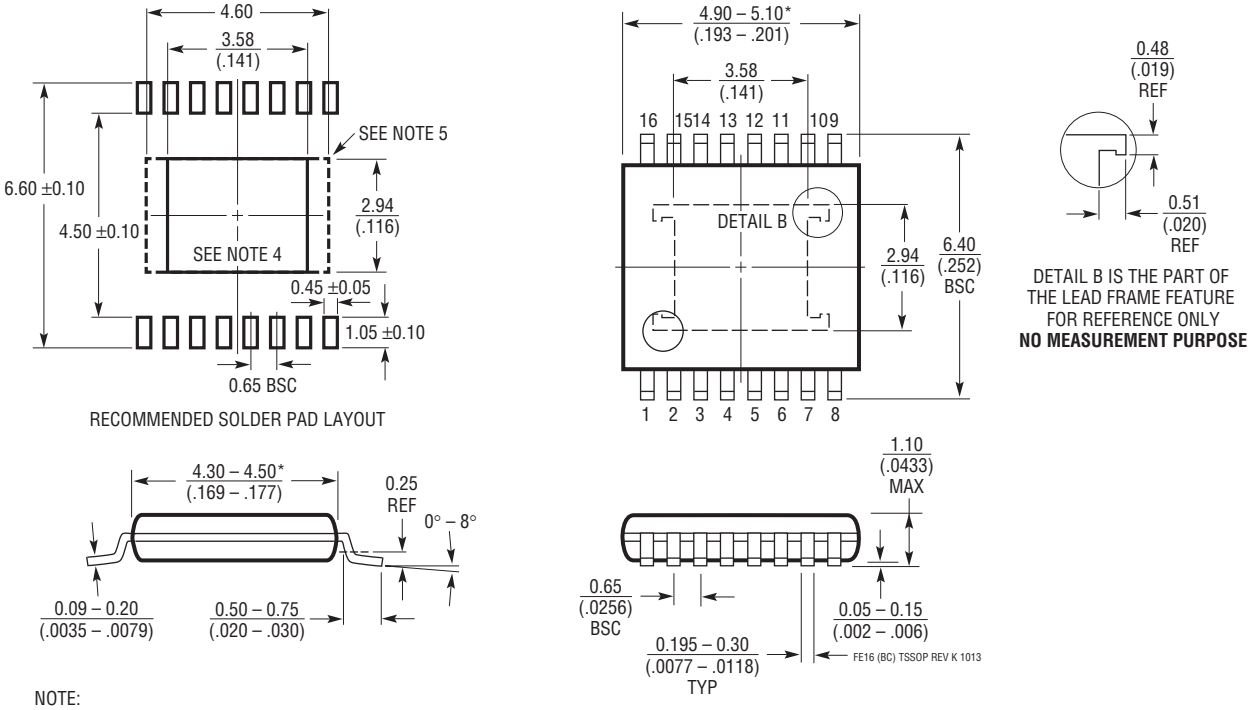
Two Phase Spread Spectrum 24V Input to 12V, 6A Output



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT3844#packaging for the most recent package drawings.

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev K)
Exposed Pad Variation BC



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
5. BOTTOM EXPOSED PADDLE MAY HAVE METAL PROTRUSION IN THIS AREA. THIS REGION MUST BE FREE OF ANY EXPOSED TRACES OR VIAS ON PCB LAYOUT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

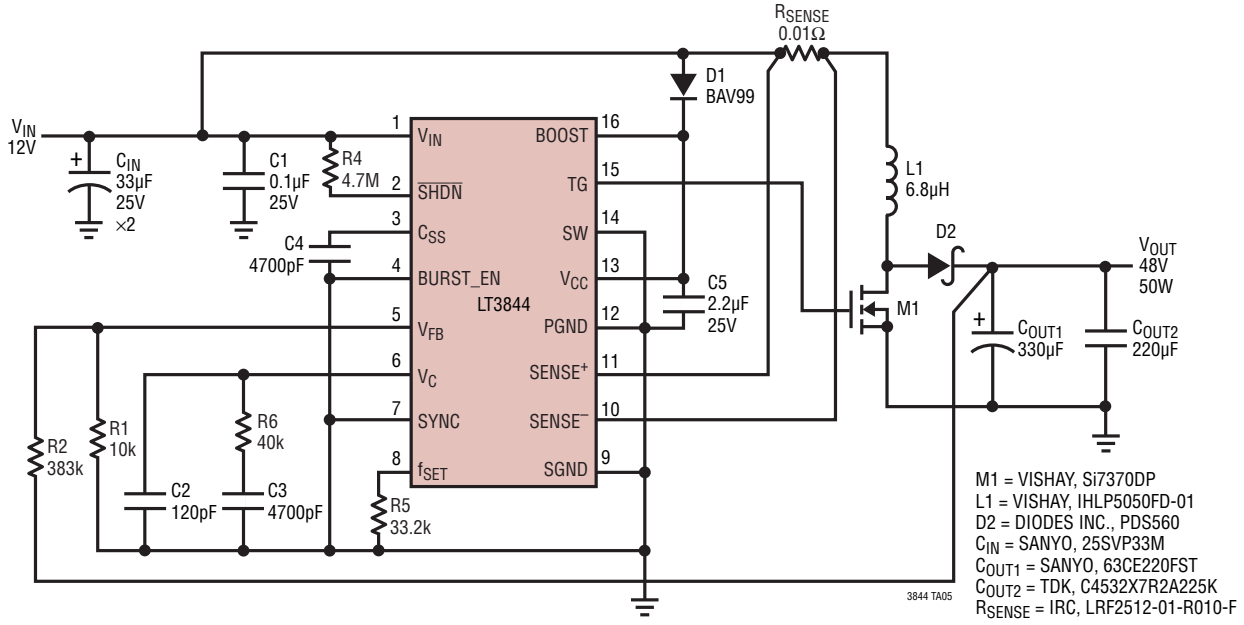
REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	04/16	Modified the Block Diagram	8
		Changed lower schematic C5 value	22

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

12V to 48V 50W Step-Up Converter with 400kHz Switching Frequency



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3840	Wide Input Range Synchronous Regulator Controller with Integrated Buck-Boost Bias Voltage requlator	Synchronizable Fixed Frequency 100kHz to 600kHz, 2.5V ≤ V_{IN} ≤ 60V, 1.23V ≤ V_{OUT} ≤ 60V, I_Q = 75µA, TSSOP-28, 4mm × 6mm QFN-38
LT3845A	60V, Low I_Q, Single Output Synchronous Step-Down DC/DC Controller	Synchronizable Fixed Frequency 100kHz to 600kHz, 4V ≤ V_{IN} ≤ 60V, 1.23V ≤ V_{OUT} ≤ 36V, I_Q = 120µA, TSSOP-16
LT3800	60V, Low I_Q, Single Output Synchronous Step-Down DC/DC Controller	Fixed 200kHz Frequency, 4V≤ V_{IN} ≤ 60V, 1.23V ≤ V_{OUT} ≤ 36V, I_Q = 120µA, TSSOP-16
LTC®3891	60V, Low I_Q, Synchronous Step-Down DC/DC Controller	Phase-Lockable Fixed Frequency, 50kHz to 900kHz 4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA
LTC3864	60V, Low I_Q, Step-Down DC/DC Controller 100% Duty Cycle Capability	Selectable Fixed Frequency, 200kHz to 600kHz 3.5V≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ V_{IN}, I_Q = 40µA, MSOP-10E
LTC3892	60V, Low I_Q, Dual 2-Phase Synchronous Step-Down DC/DC Controller with Adjustable Gate Drive Voltage	Phase-Lockable Fixed Frequency, 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 0.99V_{IN}, I_Q = 29µA
LT8709	Negative Input Synchronous Multi-Topology DC/DC Control	–80V ≤ V_{IN} ≤ –4.5V, Up to 400kHz Programmable Operating Frequency, TSSOP-20
LT8710	Synchronous SEPIC/Inverting/Boost Controller with Output Current Control	4.5V ≤ V_{IN} ≤ 80V, 100kHz to 1MHz Programmable Operating Frequency, TSSOP-20
LT8705	80V V_{IN} and V_{OUT} Synchronous 4-Switch Buck- Boost DC/DC Controller	2.8V ≤ V_{IN} ≤ 80V, 100kHz to 400kHz Programmable Operating Frequency, 5mm × 7mm QFN-38 and TSSOP-38

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LT 0416 REV C • PRINTED IN USA
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