PIC16(L)F184XX

Full-Featured, Low Pin Count Microcontrollers with XLP Product Brief

Description

PIC16(L)F184XX microcontrollers feature Intelligent Analog, Core Independent Peripherals (CIPs) and communication peripherals combined with eXtreme Low-Power (XLP) for a wide range of general purpose and low-power applications. Features such as a 12-bit Analog-to-Digital Converter with Computation (ADC^2), Memory Access Partitioning (MAP), the Device Information Area (DIA), Power-saving operating modes, and Peripheral Pin Select (PPS), offer flexible solutions for a wide variety of custom applications.

Core Features

- C Compiler Optimized RISC Architecture
- Only 48 instructions
- Operating Speed:
  - DC – 32 MHz clock input
  - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Timers:
  - Up to two 24-bit timers
  - Up to four 8-bit timers
  - Up to four 16-bit timers
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRTE)
- Brown-out Reset (BOR)
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
  - Variable prescaler selection
  - Variable window size selection
  - Configurable in hardware (Configuration Words) and/or software
- Programmable Code Protection

Memory

- Up to 28 KB Program Flash Memory
- Up to 2 KB Data SRAM Memory
- 256B Data EEPROM

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- Direct, Indirect and Relative Addressing modes
- Memory Access Partition (MAP):
  - Write-protect
  - Customizable partition
- Device Information Area (DIA)
- Device Configuration Information (DCI)

Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF184XX)
  - 2.3V to 5.5V (PIC16F184XX)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

Power-Saving Operation Modes

- Doze: CPU and Peripherals Running at Different Cycle Rates (typically CPU is lower)
- Idle: CPU Halted While Peripherals Operate
- Sleep: Lowest Power Consumption
- Peripheral Module Disable (PMD):
  - Ability to selectively disable hardware module to minimize active power consumption of unused peripherals

eXtreme Low-Power (XLP) Features

- Sleep mode: 50 nA @ 1.8, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 uA @ 32 kHz, 1.8V, typical
  - 32 uA/MHz @ 1.8V, typical

Digital Peripherals

- Configurable Logic Cell (CLC):
  - 4 CLCs
  - Integrated combinational and sequential logic
- Complementary Waveform Generator (CWG):
  - Up to 3 CWGs
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Multiple signal sources
- Capture/Compare/PWM (CCP) modules:

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  - Up to 5 CCPs
  - 16-bit resolution for Capture/Compare modes
  - 10-bit resolution for PWM mode
- Pulse-Width Modulators (PWM):
  - 2 10-bit PWMs
- Numerically Controlled Oscillator (NCO):
  - Precision linear frequency generator (@50% duty cycle) with 0.0001% step size of source input clock
  - Input Clock: 0 Hz < f_{NCO} < 32 MHz
  - Resolution: $f_{NCO}/2^{20}$
- Peripheral Pin Select (PPS):
  - I/O pin remapping of digital peripherals
- Serial Communications:
  - EUSART
    - Up to 2 EUSARTs
    - RS-232, RS-485, LIN compatible
    - Auto-Baud Detect, Auto-wake-up on Start.
  - Master Synchronous Serial Port (MSSP)
    - Up to 2 MSSPs
    - SPI
    - I^2C, SMBus and PMBus™ compatible
- Data Signal Modulator (DSM)
  - Modulates a carrier signal with digital data to create custom carrier synchronized output waveforms
- Up to 26 I/O Pins:
  - Individually programmable pull-ups
  - Slew rate control
  - Interrupt-on-change with edge-select
  - Input level selection control (ST or TTL)
  - Digital open-drain enable
- Timer modules:
  - Timer0:
    - 8/16-bit timer/counter
    - Synchronous or asynchronous operation
    - Programmable prescaler/postscaler
    - Time base for capture/compare function
  - Timer1/3/5 with gate control:
    - 16-bit timer/counter
    - Programmable internal or external clock sources
    - Multiple gate sources
    - Multiple gate modes
    - Time base for capture/compare function
  - Timer2/4/6 with Hardware Limit Timer:
    - 8-bit timers

        - Programmable prescaler/postscaler
        - Time base for PWM function
        - Hardware Limit (HLT) and one-shot extensions
        - Selectable clock sources
    - Signal Measurement Timer (SMT)
        - Up to 2 SMTs
        - 24-bit timer/counter with programmable prescaler

Analog Peripherals

- Analog-to-Digital Converter (ADC):
    - 12-bit with up to 24 external channels
    - Conversion available during Sleep
    - Automated post-processing
    - Automated math functions on input signals:
        - Averaging, filter calculations, oversampling and threshold comparison
    - Integrated charge pump for low-voltage operation
    - CVD support
- Zero-Cross Detect (ZCD):
    - AC high voltage zero-crossing detection for simplifying TRIAC control
    - Synchronized switching control and timing
- Temperature Sensor Circuit
- Comparator:
    - 2 Comparators
    - Fixed Voltage Reference at (non)inverting input(s)
    - Comparator outputs externally accessible
- Digital-to-Analog Converter (DAC):
    - 5-bit resolution, rail-to-rail
    - Positive Reference Selection
    - Unbuffered I/O pin output
    - Internal connections to ADCs and comparators
- Fixed Voltage Reference (FVR) module:
    - 1.024V, 2.048V and 4.096V output levels

Flexible Oscillator Structure

- High-Precision Internal Oscillator:
    - Software-selectable frequency range up to 32 MHz
    - ±2% at calibration (nominal)
- 4x PLL for use with external sources
    - up to 32 MHz (4-8 MHz input)
- 2x PLL for use with the HFINTOSC
    - up to 32 MHz
- Low-Power Internal 31 kHz Oscillator (LFINTOSC)
- External 32.768 kHz Crystal Oscillator (SOCS)

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- External Oscillator Block with:
  - Three crystal/resonator modes up to 20 MHz
  - Three external clock modes up to 32 MHz
  - Fail-Safe Clock Monitor
    - Detects clock source failure
  - Oscillator Start-up Timer (OST)
    - Ensures stability of crystal oscillator sources

Family Types

Table 1. PIC16(L)F184XX Family Types

Device	Program Flash Memory (Words)	Program Flash Memory (Kbytes)	Data Memory (EEPROM) (bytes)	Data SRAM (bytes)	I/O's(2)	12-bit ADC (ch)	5-bit DAC	Comparators	CWG	Clock Ref	Timers (8/16-bit)	CCP	PWM	NCO	EUSART	MSSP (I^2C/SPI)	CLC	DSM	PPS	XLP	PMD	Windowed Watchdog Timer	Memory Access Partition	Device Information Area	Debug(1)
PIC16(L)F18424	4096	7	256	512	12	11	1	2	2	1	4/4	4	2	1	1	1	4	1	Y	Y	Y	Y	Y	Y	I
PIC16(L)F18425	8192	14	256	1024	12	11	1	2	2	1	4/4	4	2	1	1	2	4	1	Y	Y	Y	Y	Y	Y	I
PIC16(L)F18426	16384	28	256	2048	12	11	1	2	2	1	4/4	4	2	1	1	2	4	1	Y	Y	Y	Y	Y	Y	I
PIC16(L)F18444	4096	7	256	512	12	17	1	2	2	1	4/4	4	2	1	1	1	4	1	Y	Y	Y	Y	Y	Y	I
PIC16(L)F18445	8192	14	256	1024	12	17	1	2	2	1	4/4	4	2	1	1	2	4	1	Y	Y	Y	Y	Y	Y	I
PIC16(L)F18446	16384	28	256	2048	12	17	1	2	2	1	4/4	4	2	1	1	2	4	1	Y	Y	Y	Y	Y	Y	I
PIC16(L)F18455	8192	14	256	1024	26	24	1	2	3	1	4/4	5	2	1	2	2	4	1	Y	Y	Y	Y	Y	Y	I
PIC16(L)F18456	16384	28	256	2048	26	24	1	2	3	1	4/4	5	2	1	2	2	4	1	Y	Y	Y	Y	Y	Y	I

Note:

1. I - Debugging integrated on chip.
2. One pin is input-only.

Packages

Packages	PDIP	SOIC	SSOP	TSSOP	UQFN (4x4)
PIC16(L)F18424	●	●		●	●
PIC16(L)F18425	●	●		●	●
PIC16(L)F18426	●	●		●	●
PIC16(L)F18444	●	●	●		●

Packages	PDIP	SOIC	SSOP	TSSOP	UQFN (4x4)
PIC16(L)F18445	•	•	•		•
PIC16(L)F18446	•	•	•		•
PIC16(L)F18455	•	•	•		•
PIC16(L)F18456	•	•	•		•

Note: Pin details are subject to change.

Important: For other small form-factor package availability and marking information, visit www.microchip.com/ packaging or contact your local sales office.

Pin Diagrams

1 14/16-Pin Diagrams

Figure 1. 14-Pin PDIP, SOIC, TSSOP

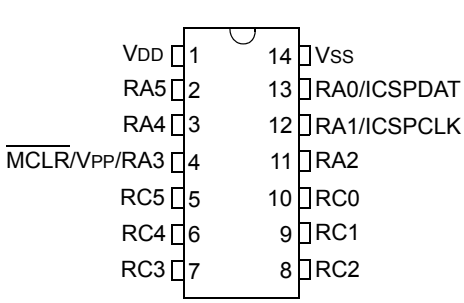
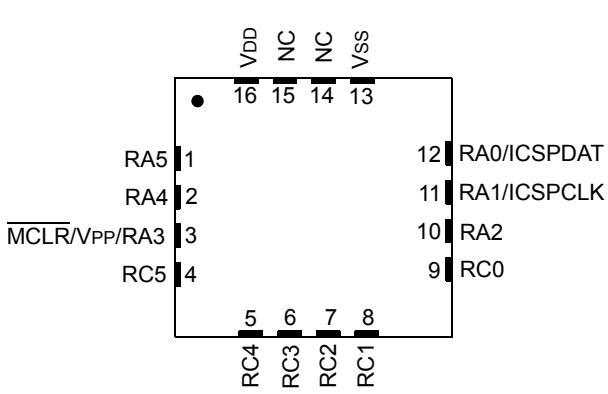


Figure 2. 16-Pin UQFN (4x4)



Note: It is recommended that the exposed bottom pad be connected to V_{SS}.

Related Links

14/16-Pin Allocation Table

2 20-Pin Diagrams

Figure 3. 20-Pin PDIP, SOIC, TSSOP

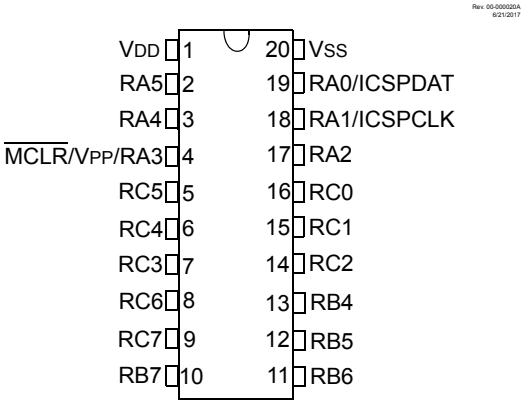
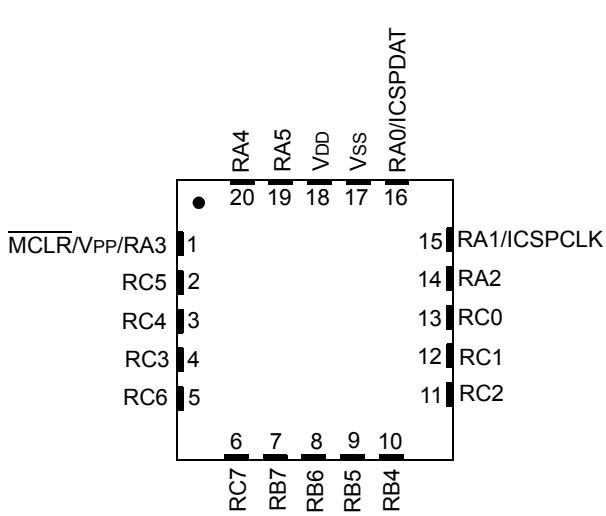


Figure 4. 20-Pin UQFN (4x4)



Note: It is recommended that the exposed bottom pad be connected to V_{SS}.

Related Links

20-Pin Allocation Table

3 28-Pin Diagrams

Figure 5. 28-pin SPDIP, SSOP, SOIC

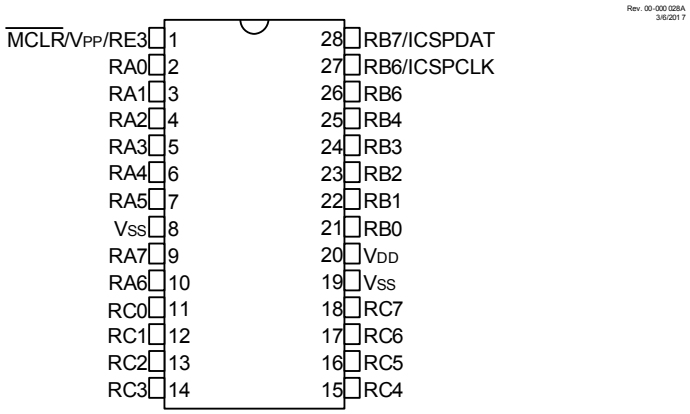
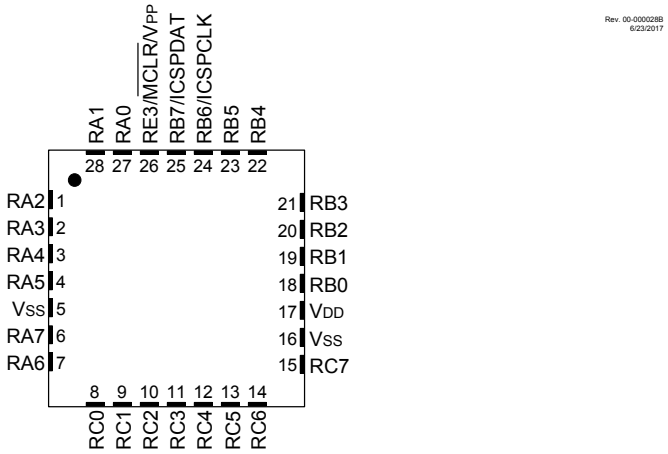


Figure 6. 28-pin UQFN



Note: It is recommended that the exposed bottom pad be connected to V_{SS}.

Related Links

28-Pin Allocation Table

Pin Allocation Tables

1 14/16-Pin Allocation Table

I/O	14-pin PDIP/SOIC/TSSOP	16-pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC	CLKR	Interrupts	Pull-up	Basic
RA0	13	12	ANA0	—	C1IN0+	—	DAC1OUT1	MDSRC(1)	—	—	—	—	$\overline{SS2}$(1)	—	—	—	—	IOCA0	Y	ICDDAT ICSPDAT
RA1	12	11	ANA1	ADCVREF+	C1IN0 C2IN0-	—	DAC1VREF+	—	—	—	—	—	—	—	—	—	—	IOCA1	Y	ICDCLK ICSPCLK
RA2	11	10	ANA2	ADCVREF-	—	—	DAC1VREF-	—	T0CKI(1)	CCP3IN(1)	—	CWG1IN(1) CWG2IN(1)	—	ZCD1	—	—	—	IOCA2	Y	INT0(1)
RA3	4	3	—	—	—	—	—	—	T6IN(1)	—	—	—	—	—	—	—	—	IOCA3	Y	$\overline{MCLR}$ V_{PP}
RA4	3	2	ANA4	—	—	—	—	—	T1G(1) SMT1WIN(1)	—	—	—	—	—	—	—	—	IOCA4	Y	CLKOUT SOSCO OSC2
RA5	2	1	ANA5	—	—	—	—	—	T1CKI(1) T2IN(1) SMT1SIG(1)	—	—	—	—	—	—	CLCIN3(1)	—	IOCA5	Y	CLKIN SOSCI OSC1
RC0	10	9	ANC0	—	C2IN0+	—	—	—	T5CKI(1)	—	—	—	SCK1(1) SCL1(1,3,4)	—	—	—	—	IOCC0	Y	—
RC1	9	8	ANC1	—	C1IN1- C2IN1-	—	—	—	T4IN(1)	CCP4IN(1)	—	—	SDI1(1) SDA1(1,3,4)	—	—	CLCIN2(1)	—	IOCC1	Y	—
RC2	8	7	ANC2 ADACT(1)	—	C1IN2- C2IN2-	—	—	MDCARL(1)	—	—	—	—	—	—	—	—	—	IOCC2	Y	—
RC3	7	6	ANC3	—	C1IN3- C2IN3-	—	—	—	T5G(1)	CCP2IN(1)	—	—	$\overline{SS1}$(1)	—	—	CLCIN0(1)	—	IOCC3	Y	—
RC4	6	5	ANC4	—	—	—	—	—	T3G(1)	—	—	—	SCK2(1,5) SCL2(1,3,4,5)	—	CK1(1,3)	CLCIN1(1)	—	IOCC4	Y	—
RC5	5	4	ANC5	—	—	—	—	MDCARH(1)	T3CKI(1)	CCP1IN(1)	—	—	SDI2(1,5) SDA2(1,3,4,5)	—	RX1(1) DT1(1,3)	—	—	IOCC5	Y	—
V_{DD}	1	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD}
V_{SS}	14	13	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}
OUT(2)	—	—	ADCGRDA	—	C1OUT	NCO1OUT	—	DSM1OUT	TMR0OUT	CCP1OUT	PWM6OUT	CWG1A CWG2A	SDO1 SDO2	—	DT1(3)	CLC1OUT	CLKR	—	—	—

I/O	14-pin PDIP/SOIC/TSSOP	16-pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC	CLKR	Interrupts	Pull-up	Basic
	—	—	ADCGRDB	—	C2OUT	—	—	—	—	CCP2OUT	PWM7OUT	CWG1B CWG2B	SCK1 SCK2	—	CK1(3)	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP3OUT	—	CWG1C CWG2C	SCL1(3) SCL2(3)	—	TX1	CLC3OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP4OUT	—	CWG1D CWG2D	SDA1(3) SDA2(3)	—	—	CLC4OUT	—	—	—	—

Note:

1. This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2. All digital output signals shown in these rows are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options.
3. This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4. These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I^2C specific or SMBUS input buffer thresholds.
5. MSSP2 is not available on the PIC16(L)F18424 or PIC16(L)F18444 devices.

2 20-Pin Allocation Table

I/O	20-pin PDIP/SOIC/TSSOP	20-pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC	CLKR	Interrupts	Pull-up	Basic
RA0	19	16	ANA0	—	C1IN0+	—	DAC1OUT1	—	—	—	—	—	—	—	—	—	—	IOCA0	Y	ICDDAT/ ICSPDAT
RA1	18	15	ANA1	ADCVREF+	C1IN0- C2IN0-	—	DAC1VREF+	MDSRC(1)	—	—	—	—	$\overline{SS2}$(1)	—	—	—	—	IOCA1	Y	ICDCLK/ ICSPCLK
RA2	17	14	ANA2	ADCVREF-	—	—	DAC1VREF-	—	T0CKI(1)	—	—	CWG1IN(1) CWG2IN(1)	—	ZCD1	—	CLCIN0(1)	—	IOCA2	Y	INT0(1)
RA3	4	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA3	Y	$\overline{MCLR}$ V_{PP}
RA4	3	20	ANA4	—	—	—	—	—	T1G(1)	CCP4IN(1)	—	—	—	—	—	—	—	IOCA4	Y	CLKOUT

I/O	20-pin PDIP/SOIC/TSSOP	20-pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC	CLKR	Interrupts	Pull-up	Basic
									SMT1WIN(1)											SOSCO OSC2
RA5	2	19	ANA5	—	—	—	—	—	T1CKI(1) T2IN(1) SMT1SIG(1)	—	—	—	—	—	—	—	—	IOCA5	Y	CLKIN SOSCI OSC1
RB4	13	10	ANB4	—	—	—	—	—	T5G(1)	—	—	—	SDI1(1) SDA1(1,3,4)	—	—	CLCIN2(1)	—	IOCB4	Y	—
RB5	12	9	ANB5	—	—	—	—	—	—	CCP3IN(1)	—	—	SCK2(1,5) SCL2(1,3,4,5)	—	RX1(1) DT1(1,3)	CLCIN3(1)	—	IOCB5	Y	—
RB6	11	8	ANB6	—	—	—	—	—	—	—	—	—	SCK1(1) SCL1(1,3,4)	—	—	—	—	IOCB6	Y	—
RB7	10	7	ANB7	—	—	—	—	—	T6IN(1)	—	—	—	SDI2(1,5) SDA2(1,3,4,5)	—	CK1(1,3)	—	—	IOCB7	Y	—
RC0	16	13	ANC0	—	C2IN0+	—	—	—	T3CKI(1) T3G(1)	—	—	—	—	—	—	—	—	IOCC0	Y	—
RC1	15	12	ANC1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	—	—	—	—	IOCC1	Y	—
RC2	14	11	ANC2 ADACT(1)	—	C1IN2- C2IN2-	—	—	MDCARL(1)	T5CKI(1)	—	—	—	—	—	—	—	—	IOCC2	Y	—
RC3	7	4	ANC3	—	C1IN3- C2IN3-	—	—	—	—	CCP2IN(1)	—	—	—	—	—	CLCIN1(1)	—	IOCC3	Y	—
RC4	6	3	ANC4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCC4	Y	—
RC5	5	2	ANC5	—	—	—	—	MDCARH(1)	T4IN(1)	CCP1IN(1)	—	—	—	—	—	—	—	IOCC5	Y	—
RC6	8	5	ANC6	—	—	—	—	—	—	—	—	—	$\overline{SS1}$(1)	—	—	—	—	IOCC6	Y	—
RC7	9	6	ANC7	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCC7	Y	—
V_{DD}	1	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD}
V_{SS}	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}
OUT(2)	—	—	ADCGRDA	—	C1OUT	NCO1OUT	—	DSM1OUT	TMR0OUT	CCP1OUT	PWM6OUT	CWG1A CWG2A	SDO1 SDO2	—	DT1(3)	CLC1OUT	CLKR	—	—	—
	—	—	ADCGRDB	—	C2OUT	—	—	—	—	CCP2OUT	PWM7OUT	CWG1B CWG2B	SCK1 SCK2	—	CK1(3)	CLC2OUT	—	—	—	—

I/O	20-pin PDIP/SOIC/TSSOP	20-pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC	CLKR	Interrupts	Pull-up	Basic
	—	—	—	—	—	—	—	—	—	CCP3OUT	—	CWG1C CWG2C	SCL1(3) SCL2(3)	—	TX1	CLC3OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP4OUT	—	CWG1D CWG2D	SDA1(3) SDA2(3)	—	—	CLC4OUT	—	—	—	—

Note:

1. This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2. All digital output signals shown in these rows are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options.
3. This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
4. These pins are configured for I^2C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I^2C specific or SMBUS input buffer thresholds.
5. MSSP2 is not available on the PIC16(L)F18424 or PIC16(L)F18444 devices.

3 28-Pin Allocation Table

I/O	28-pin PDIP/SOIC/TSSOP	28-pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC	CLKR	Interrupts	Pull-up	Basic
RA0	2	27	ANA0	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	—	—	CLCIN0(1)	—	IOCA0	Y	—
RA1	3	28	ANA1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	—	—	CLCIN1(1)	—	IOCA1	Y	—
RA2	4	1	ANA2	ADCVREF-	C1IN0+ C2IN0+	—	DAC1VREF- DAC1OUT1	—	—	—	—	—	—	—	—	—	—	IOCA2	Y	—
RA3	5	2	ANA3	ADCVREF+	C1IN1+	—	DAC1VREF+	MDCARL(1)	—	—	—	—	—	—	—	—	—	IOCA3	Y	—
RA4	6	3	ANA4	—	—	—	—	MDCARH(1)	T0CKI(1)	CCP5IN(1)	—	—	—	—	—	—	—	IOCA4	Y	—
RA5	7	4	ANA5	—	—	—	—	MDSRC(1)	—	—	—	—	$\overline{SS1}$(1)	—	—	—	—	IOCA5	Y	—
RA6	10	7	ANA6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA6	Y	OSC2 CLKOUT
RA7	9	6	ANA7	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA7	Y	OSC1 CLKIN
RB0	21	18	ANB0	—	C2IN1+	—	—	—	—	CCP4IN(1)	—	CWG1IN(1)	—	ZCD1	—	—	—	IOCB0	Y	INT0(1)

I/O	28-pin PDIP/SOIC/TSSOP	28-pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC	CLKR	Interrupts	Pull-up	Basic
RB1	22	19	ANB1	—	C1IN3- C2IN3-	—	—	—	—	—	—	CWG2IN(1)	SCK2(1) SCL2(1,3)	—	—	—	—	IOCB1	Y	—
RB2	23	20	ANB2	—	—	—	—	—	—	—	—	CWG3IN(1)	SDI2(1) SDA2(1,3)SS2(1)	—	—	—	—	IOCB2	Y	—
RB3	24	21	ANB3	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—	—	—	IOCB3	Y	—
RB4	25	22	ANB4 ADACT(1)	—	—	—	—	—	T5G(1) SMT2WIN(1)	—	—	—	—	—	—	—	—	—	IOCB4	Y	—
RB5	26	23	ANB5	—	—	—	—	—	T1G(1) SMT2SIG(1)	CCP3IN(1)	—	—	—	—	—	—	—	—	IOCB5	Y	—
RB6	27	24	ANB6	—	—	—	—	—	—	—	—	—	—	—	CK2(1,3)	CLCIN2(1)	—	IOCB6	Y	ICSPCLK ICDCLK
RB7	28	25	ANB7	—	—	—	DAC1OUT2	—	T6IN(1)	—	—	—	—	—	RX2(1) DT2(1,3)	—	—	IOCB7	Y	ICSPDAT ICDDAT
RC0	11	8	ANC0	—	—	—	—	—	T1CKI(1) T3CKI(1) T3G(1) SMT1WIN(1)	—	—	—	—	—	—	—	—	IOCC0	Y	SOSCO
RC1	12	9	ANC1	—	—	—	—	—	SMT1SIG(1)	CCP2IN(1)	—	—	—	—	—	—	—	IOCC1	Y	SOSCI
RC2	13	10	ANC2	—	—	—	—	—	T5CKI(1)	CCP1IN(1)	—	—	—	—	—	—	—	IOCC2	Y	—
RC3	14	11	ANC3	—	—	—	—	—	T2IN(1)	—	—	—	SCK1(1) SCL1(1,3)	—	—	—	—	IOCC3	Y	—
RC4	15	12	ANC4	—	—	—	—	—	—	—	—	—	SDI1(1) SDA1(1,3)	—	—	—	—	IOCC4	Y	—
RC5	16	13	ANC5	—	—	—	—	—	T4IN(1)	—	—	—	—	—	—	—	—	IOCC5	Y	—
RC6	17	14	ANC6	—	—	—	—	—	—	—	—	—	—	—	—	CK1(1,3)	—	IOCC6	Y	—
RC7	18	15	ANC7	—	—	—	—	—	—	—	—	—	—	—	—	RX1(1) DT1(1,3)	—	IOCC7	Y	—
RE3	1	26	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCE3	Y	MCLR VPP
VDD	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	8	5	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
VSS	19	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT(2)	—	—	ADCGRDA	—	C1OUT	NCO1OUT	—	DSM1OUT	TMR0OUT	CCP1OUT	PWM6OUT	CWG1A CWG2A CWG3A	SDO1 SDO2	—	DT1(3) DT2(3)	CLC1OUT	CLKR	—	—	—

I/O	28-pin PDIP/SOIC/TSSOP	28-pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	ZCD	EUSART	CLC	CLKR	Interrupts	Pull-up	Basic
	—	—	ADCGRDB	—	C2OUT	—	—	—	—	CCP2OUT	PWM7OUT	CWG1B CWG2B CWG3B	SCK1 SCK2	—	CK1(3) CK2(3)	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP3OUT	—	CWG1C CWG2C CWG3C	SCL1(3) SCL2(3)	—	TX1 TX2	CLC3OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP4OUT	—	CWG1D CWG2D CWG3D	SDA1(3) SDA2(3)	—	—	CLC4OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP5OUT	—	—	—	—	—	—	—		—	—

Note:

1. This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2. All digital output signals shown in these rows are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options.
3. This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

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