HCS361

KEELOQ® Code Hopping Encoder

FEATURES

Security

- Programmable 28/32-bit serial number
- Programmable 64-bit encryption key
- Each transmission is unique
- 67-bit transmission code length
- 32-bit hopping code
- 35-bit fixed code (28/32-bit serial number, 4/0-bit function code, 1-bit status, 2-bit CRC)
- Encryption keys are read protected

Operating

- 2.0-6.6V operation
- Four button inputs
  - 15 functions available
- Selectable baud rate
- Automatic code word completion
- Battery low signal transmitted to receiver
- Nonvolatile synchronization data
- PWM and VPWM modulation

Other

- Easy to use programming interface
- On-chip EEPROM
- On-chip oscillator and timing components
- Button inputs have internal pull-down resistors
- Current limiting on $\overline{\text{LED}}$ output
- Minimum component count

Enhanced Features Over HCS300

- 48-bit seed vs. 32-bit seed
- 2-bit CRC for error detection
- 28/32-bit serial number select
- Two seed transmission methods
- PWM and VPWM modulation
- Wake-up signal in VPWM mode
- IR Modulation mode

Typical Applications

The HCS361 is ideal for Remote Keyless Entry (RKE) applications. These applications include:

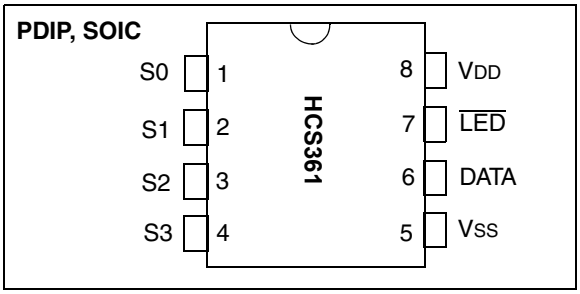
- Automotive RKE systems
- Automotive alarm systems
- Automotive immobilizers
- Gate and garage door openers
- Identity tokens
- Burglar alarm systems

DESCRIPTION

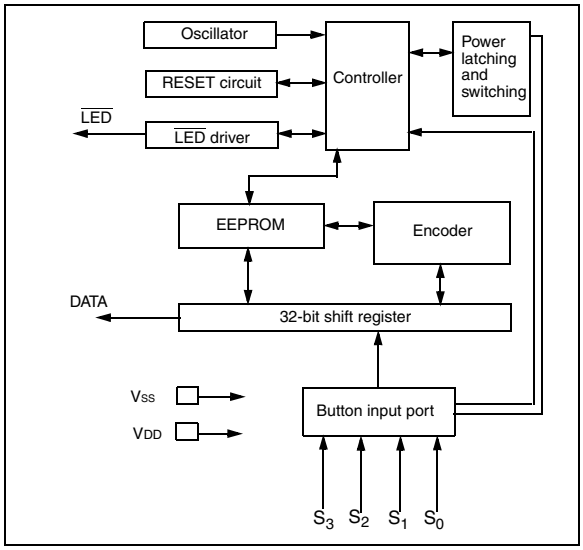
The HCS361 is a code hopping encoder designed for secure Remote Keyless Entry (RKE) systems. The HCS361 utilizes the KEELOQ® code hopping technology, which incorporates high security, a small package outline and low cost, to make this device a perfect solution for unidirectional remote keyless entry systems and access control systems.

PACKAGE TYPES

PDIP, SOIC



HCS361 BLOCK DIAGRAM



DESCRIPTION

The HCS361 combines a 32-bit hopping code generated by a nonlinear encryption algorithm, with a 28/32-bit serial number and 7/3 status bits to create a 67-bit transmission stream.

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The crypt key, serial number and configuration data are stored in an EEPROM array which is not accessible via any external connection. The EEPROM data is programmable but read protected. The data can be verified only after an automatic erase and programming operation. This protects against attempts to gain access to keys or manipulate synchronization values. The HCS361 provides an easy-to-use serial interface for programming the necessary keys, system parameters and configuration data.

1.0 SYSTEM OVERVIEW

Key Terms

The following is a list of key terms used throughout this data sheet. For additional information on KEELOQ and Code Hopping, refer to Technical Brief 3 (TB003).

- **RKE** - Remote Keyless Entry
- **Button Status** - Indicates what button input(s) activated the transmission. Encompasses the 4 button status bits S3, S2, S1 and S0 (Figure 3-2).
- **Code Hopping** - A method by which a code, viewed externally to the system, appears to change unpredictably each time it is transmitted.
- **Code word** - A block of data that is repeatedly transmitted upon button activation (Figure 3-2).
- **Transmission** - A data stream consisting of repeating code words (Figure 9-1).
- **Crypt key** - A unique and secret 64-bit number used to encrypt and decrypt data. In a symmetrical block cipher such as the KEELOQ algorithm, the encryption and decryption keys are equal and will therefore be referred to generally as the crypt key.
- **Encoder** - A device that generates and encodes data.
- **Encryption Algorithm** - A recipe whereby data is scrambled using a crypt key. The data can only be interpreted by the respective decryption algorithm using the same crypt key.
- **Decoder** - A device that decodes data received from an encoder.
- **Decryption algorithm** - A recipe whereby data scrambled by an encryption algorithm can be unscrambled using the same crypt key.
- **Learn** – Learning involves the receiver calculating the transmitter's appropriate crypt key, decrypting the received hopping code and storing the serial number, synchronization counter value and crypt key in EEPROM. The KEELOQ product family facilitates several learning strategies to be implemented on the decoder. The following are examples of what can be done.
  - **Simple Learning**
    The receiver uses a fixed crypt key, common to all components of all systems by the same manufacturer, to decrypt the received code word's encrypted portion.
  - **Normal Learning**
    The receiver uses information transmitted during normal operation to derive the crypt key and decrypt the received code word's encrypted portion.
  - **Secure Learn**
    The transmitter is activated through a special button combination to transmit a stored 60-bit seed value used to generate the transmitter's crypt key. The receiver uses this seed value to derive the same crypt key and decrypt the received code word's encrypted portion.
- **Manufacturer's code** – A unique and secret 64-bit number used to generate unique encoder crypt keys. Each encoder is programmed with a crypt key that is a function of the manufacturer's code. Each decoder is programmed with the manufacturer code itself.

The HCS361 code hopping encoder is designed specifically for keyless entry systems; primarily vehicles and home garage door openers. The encoder portion of a keyless entry system is integrated into a transmitter, carried by the user and operated to gain access to a vehicle or restricted area. The HCS361 is meant to be a cost-effective yet secure solution to such systems, requiring very few external components (Figure 2-1).

Most low-end keyless entry transmitters are given a fixed identification code that is transmitted every time a button is pushed. The number of unique identification codes in a low-end system is usually a relatively small number. These shortcomings provide an opportunity for a sophisticated thief to create a device that 'grabs' a transmission and retransmits it later, or a device that quickly 'scans' all possible identification codes until the correct one is found.

The HCS361, on the other hand, employs the KEELOQ code hopping technology coupled with a transmission length of 66 bits to virtually eliminate the use of code 'grabbing' or code 'scanning'. The high security level of the HCS361 is based on the patented KEELOQ technology. A block cipher based on a block length of 32 bits and a key length of 64 bits is used. The algorithm obscures the information in such a way that even if the transmission information (before coding) differs by only one bit from that of the previous transmission, the next

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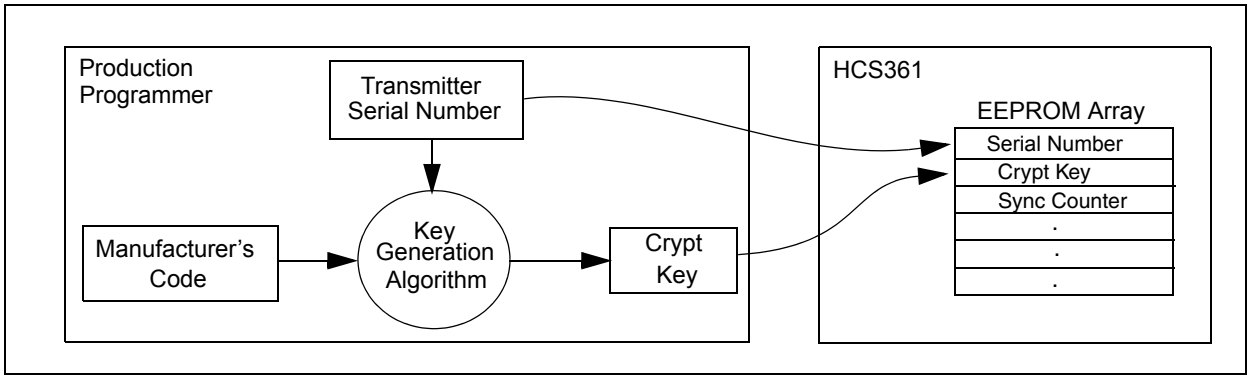
coded transmission will be completely different. Statistically, if only one bit in the 32-bit string of information changes, greater than 50 percent of the coded transmission bits will change.

As indicated in the block diagram on page one, the HCS361 has a small EEPROM array which must be loaded with several parameters before use; most often programmed by the manufacturer at the time of production. The most important of these are:

- A 28-bit serial number, typically unique for every encoder
- A crypt key
- An initial 16-bit synchronization value
- A 16-bit configuration value

The crypt key generation typically inputs the transmitter serial number and 64-bit manufacturer's code into the key generation algorithm (Figure 1-1). The manufacturer's code is chosen by the system manufacturer and must be carefully controlled as it is a pivotal part of the overall system security.

FIGURE 1-1: CREATION AND STORAGE OF CRYPT KEY DURING PRODUCTION



The 16-bit synchronization counter is the basis behind the transmitted code word changing for each transmission; it increments each time a button is pressed. Due to the code hopping algorithm's complexity, each increment of the synchronization value results in greater than 50% of the bits changing in the transmitted code word.

Figure 1-2 shows how the key values in EEPROM are used in the encoder. Once the encoder detects a button press, it reads the button inputs and updates the synchronization counter. The synchronization counter and crypt key are input to the encryption algorithm and the output is 32 bits of encrypted information. This data will change with every button press, its value appearing externally to 'randomly hop around', hence it is referred to as the hopping portion of the code word. The 32-bit hopping code is combined with the button information and serial number to form the code word transmitted to the receiver. The code word format is explained in greater detail in Section 4.2.

A receiver may use any type of controller as a decoder, but it is typically a microcontroller with compatible firmware that allows the decoder to operate in conjunction with an HCS361 based transmitter. Section 7.0 provides detail on integrating the HCS361 into a system.

A transmitter must first be 'learned' by the receiver before its use is allowed in the system. Learning includes calculating the transmitter's appropriate crypt key, decrypting the received hopping code and storing the serial number, synchronization counter value and crypt key in EEPROM.

In normal operation, each received message of valid format is evaluated. The serial number is used to determine if it is from a learned transmitter. If from a learned transmitter, the message is decrypted and the synchronization counter is verified. Finally, the button status is checked to see what operation is requested. Figure 1-3 shows the relationship between some of the values stored by the receiver and the values received from the transmitter.

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FIGURE 1-2: BUILDING THE TRANSMITTED CODE WORD (ENCODER)

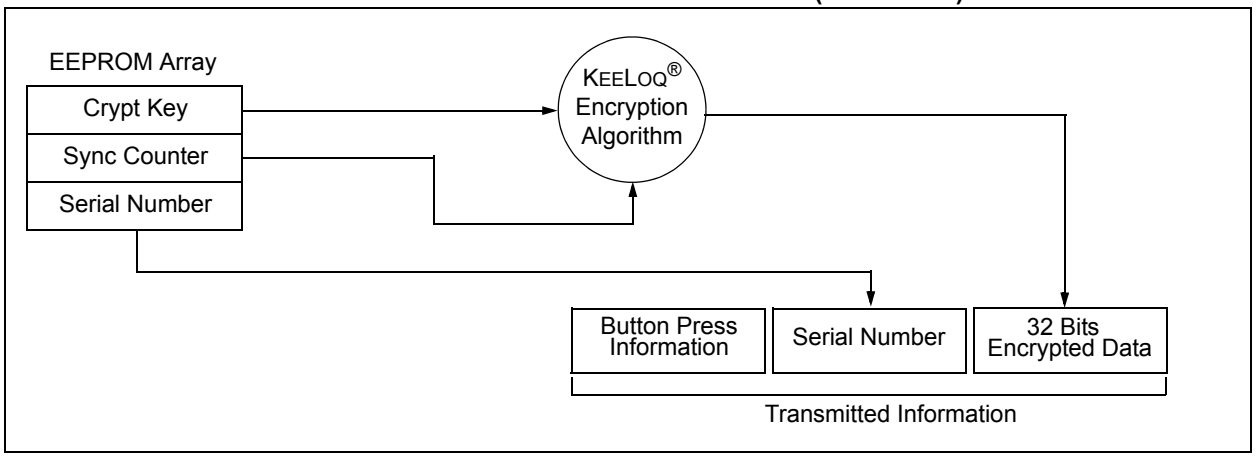
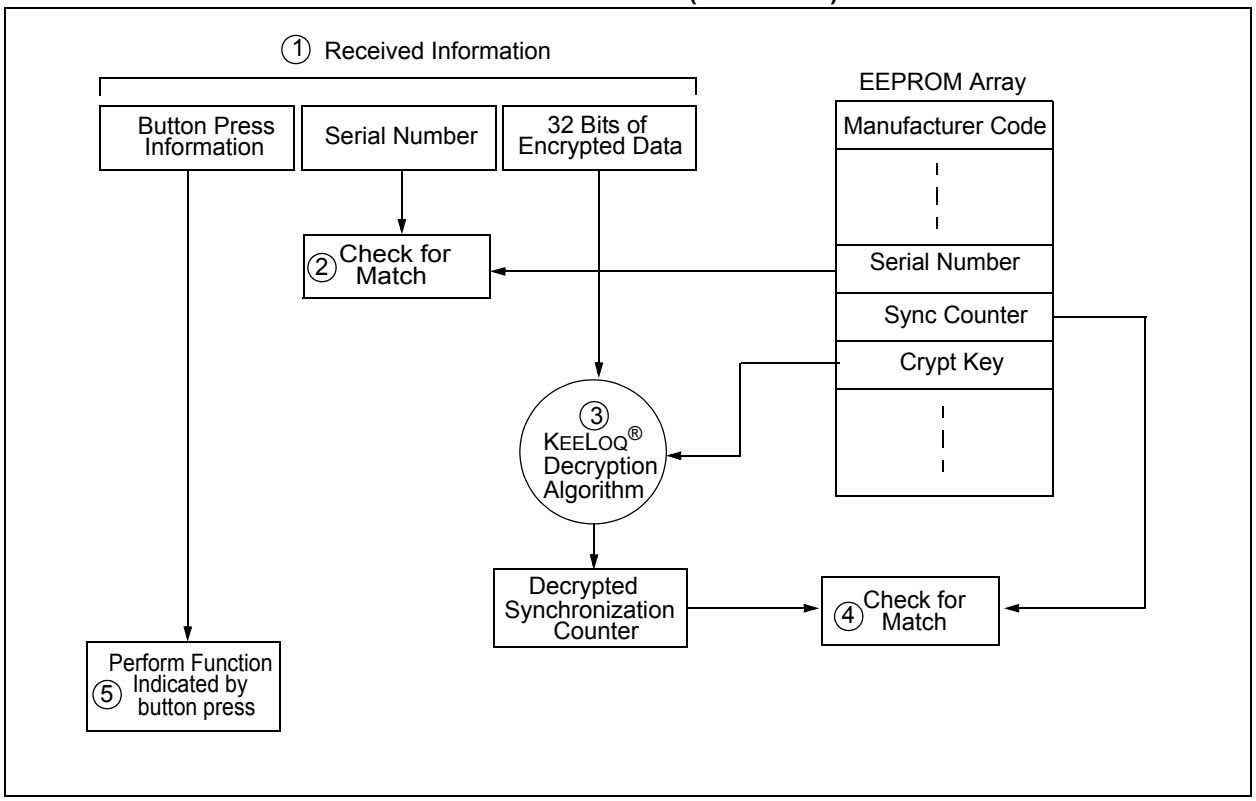


FIGURE 1-3: BASIC OPERATION OF RECEIVER (DECODER)



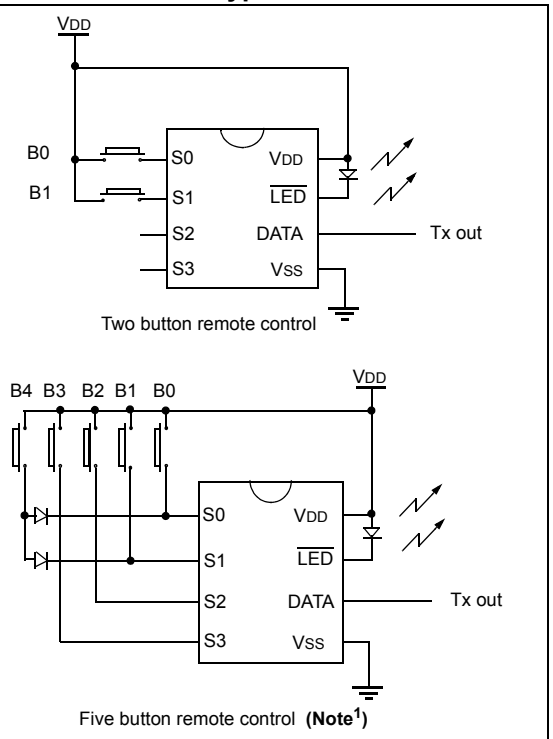
NOTE: Circled numbers indicate the order of execution.

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2.0 DEVICE OPERATION

As shown in the typical application circuits (Figure 2-1), the HCS361 is a simple device to use. It requires only the addition of buttons and RF circuitry for use as the transmitter in your security application. A description of each pin is described in Table 2-1.

FIGURE 2-1: Typical circuits



Note: Up to 15 functions can be implemented by pressing more than one button simultaneously or by using a suitable diode array.

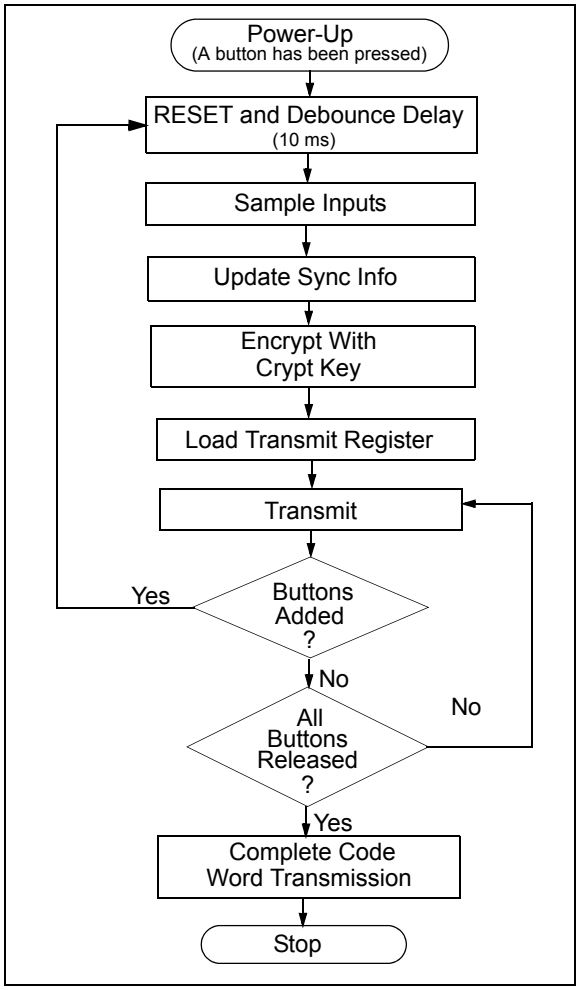
TABLE 2-1: PIN DESCRIPTIONS

Name	Pin Number	Description
S0	1	Switch input 0
S1	2	Switch input 1
S2	3	Switch input 2 / Clock pin when in Programming mode
S3	4	Switch input 3
VSS	5	Ground reference
DATA	6	Data output pin /Data I/O pin for Programming mode
$\overline{LED}$	7	Cathode connection for $\overline{LED}$
VDD	8	Positive supply voltage

The HCS361 will wake-up upon detecting a button press and delay approximately 10 ms for button debounce (Figure 2-2). The synchronization counter, discrimination value and button information will be encrypted to form the hopping code. The hopping code portion will change every transmission, even if the same button is pushed again. A code word that has been transmitted will not repeat for more than 64K transmissions. This provides more than 18 years of use before a code is repeated; based on 10 operations per day. Overflow information sent from the encoder can be used to extend the number of unique transmissions to more than 192K.

If in the transmit process it is detected that a new button(s) has been pressed, a RESET will immediately occur and the current code word will not be completed. Please note that buttons removed will not have any effect on the code word unless no buttons remain pressed; in which case the code word will be completed and the power-down will occur.

FIGURE 2-2: ENCODER OPERATION



3.0 EEPROM MEMORY ORGANIZATION

The HCS361 contains 192 bits (12 x 16-bit words) of EEPROM memory (Table 3-1). This EEPROM array is used to store the encryption key information, synchronization value, etc. Further descriptions of the memory array is given in the following sections.

TABLE 3-1: EEPROM MEMORY MAP

WORD ADDRESS	MNEMONIC	DESCRIPTION
0	KEY_0	64-bit crypt key (word 0) LSb's
1	KEY_1	64-bit crypt key (word 1)
2	KEY_2	64-bit crypt key (word 2)
3	KEY_3	64-bit crypt key (word 3) MSb's
4	SYNC_A	16-bit synch counter
5	SYNC_B/ SEED_2	16-bit synch counter B or Seed value (word 2)
6	RESERVED	Set to 0000H
7	SEED_0	Seed Value (word 0) LSb's
8	SEED_1	Seed Value (word 1) MSb's
9	SER_0	Device Serial Number (word 0) LSb's
10	SER_1	Device Serial Number (word 1) MSb's
11	CONFIG	Configuration Word

3.1 KEY_0 - KEY_3 (64-Bit Crypt Key)

The 64-bit crypt key is used to create the encrypted message transmitted to the receiver. This key is calculated and programmed during production using a key generation algorithm. The key generation algorithm may be different from the KEELOQ algorithm. Inputs to the key generation algorithm are typically the transmitter's serial number and the 64-bit manufacturer's code. While the key generation algorithm supplied from Microchip is the typical method used, a user may elect to create their own method of key generation. This may be done providing that the decoder is programmed with the same means of creating the key for decryption purposes.

3.2 SYNC_A, SYNC_B (Synchronization Counter)

This is the 16-bit synchronization value that is used to create the hopping code for transmission. This value is incremented after every transmission. Separate synchronization counters can be used to stay synchronized with different receivers.

3.3 SEED_0, SEED_1, and SEED_2 (Seed Word)

The three word (48 bits) seed code will be transmitted when seed transmission is selected. This allows the system designer to implement the Secure Learn feature or use this fixed code word as part of a different key generation/tracking process or purely as a fixed code transmission.

Note: Since SEED2 and SYNC_B share the same memory location, Secure Learn and Independent mode transmission (including IR mode) are mutually exclusive.

3.4 SER_0, SER_1 (Encoder Serial Number)

SER_0 and SER_1 are the lower and upper words of the device serial number, respectively. There are 32 bits allocated for the Serial Number and a selectable configuration bit determines whether 32 or 28 bits will be transmitted. The serial number is meant to be unique for every transmitter.

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3.5 CONFIG (Configuration Word)

The Configuration Word is a 16-bit word stored in EEPROM array that is used by the device to store information used during the encryption process, as well as the status of option configurations. Further explanations of each of the bits are described in the following sections.

TABLE 3-1: CONFIGURATION WORD

Bit Number	Symbol	Bit Description
0	BACW	Blank Alternate Code Word
1	BSEL	Baud Rate Selection
2	TXWAK	PWM mode: 1/6, 2/6 or 1/3, 2/3 select VPWM mode: Wake-up enable
3	SPM	Sync Pulse Modulation
4	SEED	Seed Transmission enable
5	DELM	Delay mode enable
6	TIMO	Time-out enable
7	IND	Independent mode enable
8	USRA0	User bit
9	USRA1	User bit
10	USRB0	User bit
11	USRB1	User bit
12	XSER	Extended serial number enable
13	TMPSD	Temporary seed transmission enable
14	MOD	Modulation format select
15	OVR	Overflow bit

3.5.1 MOD: MODULATION FORMAT

MOD selects between VPWM modulation and PWM modulation format.

If MOD = 1, VPWM modulation is selected as well as the following:

1. Enables the TXWAK bit to select the WAKE-UP transmission.
2. Extends the Guard Time.

If MOD = 0, PWM modulation is selected.

3.5.2 BSEL: BAUD RATE SELECT

BSEL selects the baud rate. If BSEL = 1, the baud rate is nominally 1667 bits per second and with BSEL = 0, 833 bits per second.

3.5.3 TXWAK: BIT FORMAT SELECT OR WAKE-UP

In PWM mode, this bit selects the bit format.

If TXWAK = 0, the PWM pulse duty cycle is 1/3-2/3.

If TXWAK = 1, the PWM pulse duty cycle is 1/6-2/6.

In VPWM mode, this bit enables the wake-up signal.

If TXWAK = 0, transmissions start normally with the preamble portion of the code word.

If TXWAK = 1, transmissions start with a Wake-up sequence followed by a dead time (see Figure 4-2).

Note:	The Wake-up sequence is transmitted before the first code word of each transmission only.

The following tables summarize the combined effect of TXWAK, BSEL and MOD option bits.

TABLE 3-1: PWM OPTIONS

MOD	TXWAK	BSEL	TE	Duty Cycle
0	0	0	400us	1/3-2/3
0	0	1	200us	1/3-2/3
0	1	0	200us	1/6-2/6
0	1	1	100us	1/6-2/6

TABLE 3-2: VPWM OPTIONS

MOD	TXWAK	BSEL	TE	Wake-up
1	0	0	400us	NO
1	0	1	200us	NO
1	1	0	400us	YES
1	1	1	200us	YES

3.5.4 SPM: SYNC PULSE MODULATION

Select Modulation mode of Sync Pulse. If SPM = 1, the sync pulse is modulated (Figure 4-1 and Figure 4-2).

3.5.5 OVR: OVERFLOW

The overflow bit is used to extend the number of possible synchronization values. The synchronization counter is 16 bits in length, yielding 65,536 values before the cycle repeats. Under typical use of 10 operations a day, this will provide nearly 18 years of use before a repeated value will be used. Should the system designer conclude that is not adequate, then the overflow bit can be utilized to extend the number of unique values. This can be done by programming OVR to 1 at the time of production. The encoder will automatically clear OVR the first time that the transmitted synchronization value wraps from 0xFFFF to 0x0000. Once cleared, OVR cannot be set again, thereby creating a permanent record of the counter overflow. This prevents fast cycling of 64K counter. If the decoder system is programmed to track the overflow bits, then the effective number of unique synchronization values can be extended to 128K. If programmed to zero, the system will be compatible with old encoder devices.

3.5.6 BACW: BLANK ALTERNATE CODE WORD

BACW = 1 selects the encoder to transmit every second code word. This can be used to reduce the average power transmitted over a 100 ms window and thereby transmit a higher peak power (see Section 5.2).

3.5.7 XSER: EXTENDED SERIAL NUMBER

If XSER = 0, the four Most Significant bits of the Serial Number are substituted by S[3:0] and the code word format is compatible with the HCS200/300/301.

If XSER = 1, the full 32-bit Serial Number [SER_1, SER_0] is transmitted.

Note:	Since the button status S[3:0] is used to detect a Seed transmission, Extended Serial Number and Secure Learn are mutually exclusive.

3.5.8 DISCRIMINATION VALUE

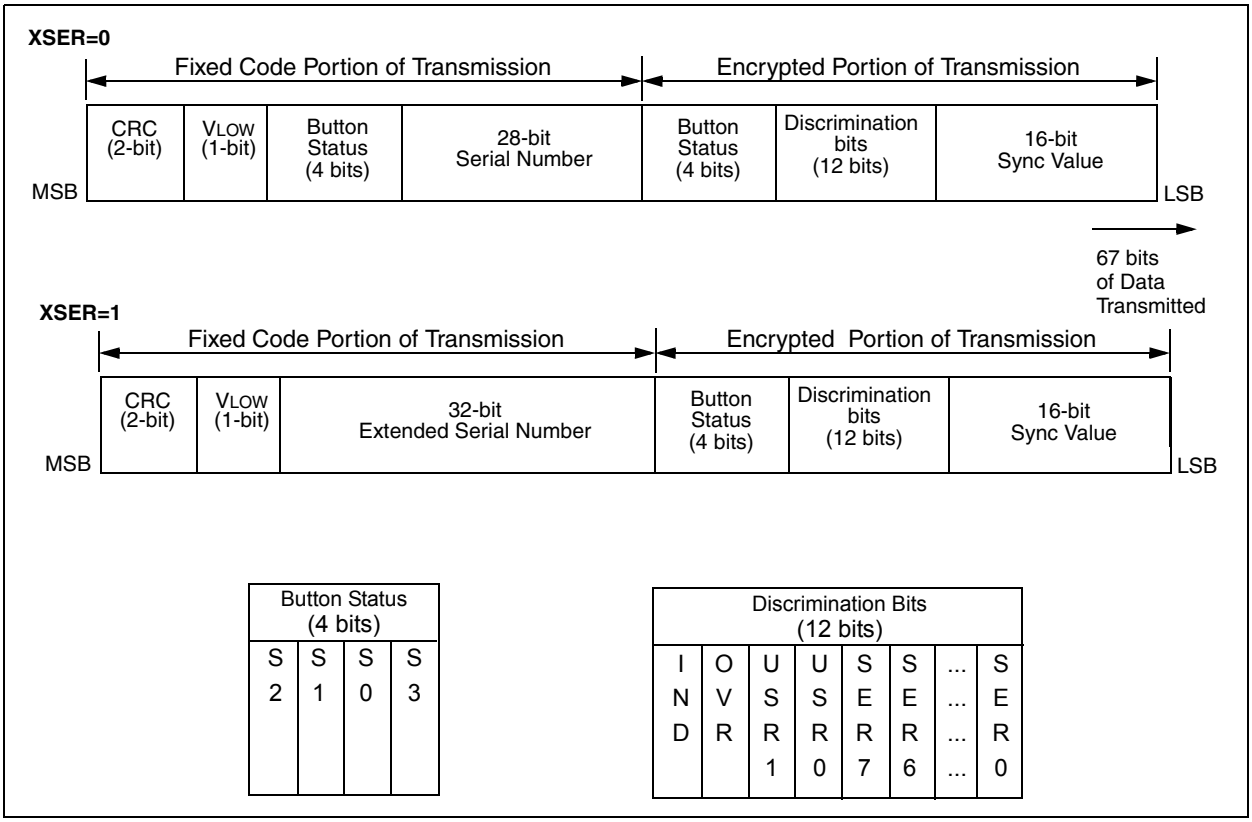
While in other KEELOQ encoders its value is user selectable, the HCS361 uses directly the 8 Least Significant bits of the Serial Number as part of the information that form the encrypted portion of the transmission (Figure 3-2).

The discrimination value aids the post-decryption check on the decoder end. After the receiver has decrypted a transmission, the discrimination bits are checked against the encoder Serial Number to verify that the decryption process was valid.

3.5.9 USRA,B: USER BITS

User bits form part of the discrimination value. The user bits together with the IND bit can be used to identify the counter that is used in Independent mode.

FIGURE 3-2: CODE WORD ORGANIZATION



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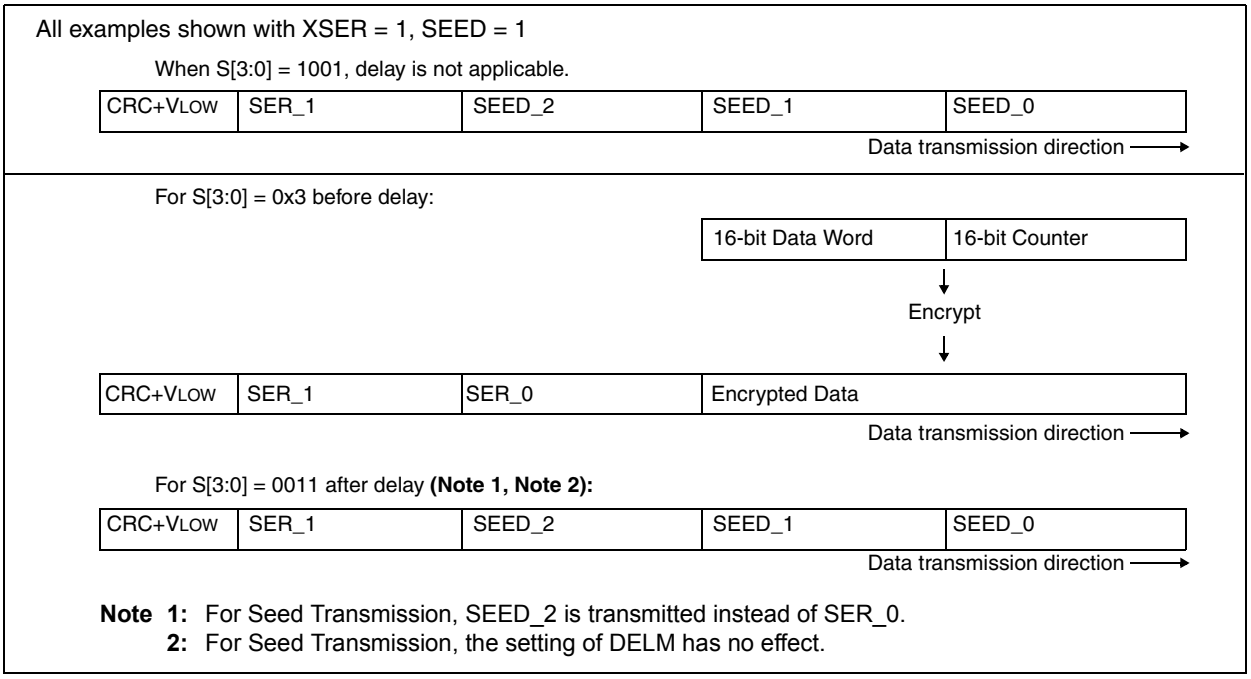
3.5.10 SEED: ENABLE SEED TRANSMISSION

If SEED = 0, seed transmission is disabled. The Independent Counter mode can only be used with seed transmission disabled since SEED_2 is shared with the second synchronization counter.

With SEED = 1, seed transmission is enabled. The appropriate button code(s) must be activated to transmit the seed information. In this mode, the seed information (SEED_0, SEED_1, and SEED_2) and the upper 12 or 16 bits of the serial number (SER_1)are transmitted instead of the hop code.

Seed transmission is available for function codes (Table 3-2) S[3:0] = 1001 and S[3:0] = 0011 (delayed). This takes place regardless of the setting of the IND bit. The two seed transmissions are shown in Figure 3-3.

FIGURE 3-3: Seed Transmission



Note 1: For Seed Transmission, SEED_2 is transmitted instead of SER_0.
2: For Seed Transmission, the setting of DELM has no effect.

3.5.11 TMPSD: TEMPORARY SEED TRANSMISSION

The temporary seed transmission can be used to disable learning after the transmitter has been used for a programmable number of operations. This feature can be used to implement very secure systems. After learning is disabled, the seed information cannot be accessed even if physical access to the transmitter is possible. If TMPSD = 1 the seed transmission will be disabled after a number of code hopping transmissions. The number of transmissions before seed transmission is disabled, can be programmed by setting the synchronization counter (SYNC_A or SYNC_B) to a value as shown in Table 3-4.

TABLE 3-4: SYNCHRONOUS COUNTER INITIALIZATION VALUES

Synchronous Counter Values	Number of Transmissions
0000H	128
0060H	64
0050H	32
0048H	16

3.5.12 DELM: DELAY MODE

If DELM = 1, delay transmission is enabled. A delayed transmission is indicated by inverting the lower nibble of the discrimination value. The Delay mode is primarily for compatibility with previous KEELOQ devices.

If DELM = 0, delay transmission is disabled (Table 3-1).

TABLE 3-1: TYPICAL DELAY TIMES

TXWAK	BSEL	Number of Code Words before Delay Mode	Time Before Delay Mode (MOD = 0)
0	0	28	≈ 2.8s
0	1	56	≈ 2.9s
1	0	28	≈ 2.6s
1	1	56	≈ 2.8s

3.5.13 TIMO: TIME-OUT OR AUTO-SHUTOFF

If TIMO = 1, the time-out is enabled. Time-out can be used to terminate accidental continuous transmissions. When time-out occurs, the PWM output is set low and the LED is turned off. Current consumption will be higher than in Standby mode since current will flow through the activated input resistors. This state can be exited only after all inputs are taken low. TIMO = 0, will enable continuous transmission (Table 3-5).

TABLE 3-5: TYPICAL TIME-OUT TIMES

TXWAK	BSEL	Maximum Number of Code Words Transmitted	Time Before Time-out (MOD = 0)
0	0	256	≈ 25.6s
0	1	512	≈ 27.2s
1	0	256	≈ 23.8s
1	1	512	≈ 25.4s

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3.5.14 IND: INDEPENDENT MODE

The Independent mode can be used where one encoder is used to control two receivers. Two counters (SYNC_A and SYNC_B) are used in Independent mode. As indicated in Table 3-2, function codes 1 to 7 use SYNC_A and 8 to 15 SYNC_B.

3.5.15 INFRARED MODE

The Independent mode also selects IR mode. In IR mode function codes 12 to 15 will use counter B. The PWM output signal is modulated with a 40 kHz carrier (see Table 3-1). It must be pointed out that the 40 kHz is derived from the internal clock and will therefore vary with the same percentage as the baud rate. If IND = 0, SYNC_A is used for all function codes. If IND = 1, Independent mode is enabled and counters for functions are used according to Table 3-2.

TABLE 3-1: IR MODULATION

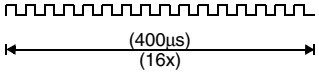
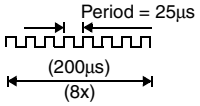
TE	Basic Pulse
400us	
200us	
100us	

TABLE 3-2: FUNCTION CODES

	S3	S2	S1	S0	IND = 0	IND = 1	Comments
					Counter		
1	0	0	0	1	A	A	
2	0	0	1	0	A	A	
3	0	0	1	1	A	A	If SEED = 1, transmit seed after delay.(1)
4	0	1	0	0	A	A	
5	0	1	0	1	A	A	
6	0	1	1	0	A	A	
7	0	1	1	1	A	A	
8	1	0	0	0	A	B	
9	1	0	0	1	A	B	If SEED = 1, transmit seed immediately.(1)
10	1	0	1	0	A	B	
11	1	0	1	1	A	B	
12	1	1	0	0	A	B(1)	
13	1	1	0	1	A	B(1)	
14	1	1	1	0	A	B(1)	
15	1	1	1	1	A	B(1)	

Note 1: IR mode

4.0 TRANSMITTED WORD

4.1 Transmission Format (PWM)

The HCS361 transmission is made up of several parts (Figure 4-1 and Figure 4-2). Each transmission is begun with a preamble and a header, followed by the encrypted and then the fixed data. The actual data is 67 bits which consists of 32 bits of encrypted data and 35 bits of fixed data. Each transmission is followed by a guard period before another transmission can begin. Refer to Table 9-6 and Table 9-6 for transmission timing specifications. The encrypted portion provides up to four billion changing code combinations and includes the function bits (based on which buttons were activated) along with the synchronization counter value and discrimination value. The non-encrypted portion is comprised of the CRC bits, VLOW bits, the function bits and the 28/32-bit serial number. The encrypted and non-encrypted sections combined increase the number of combinations to 1.47×10^{20}.

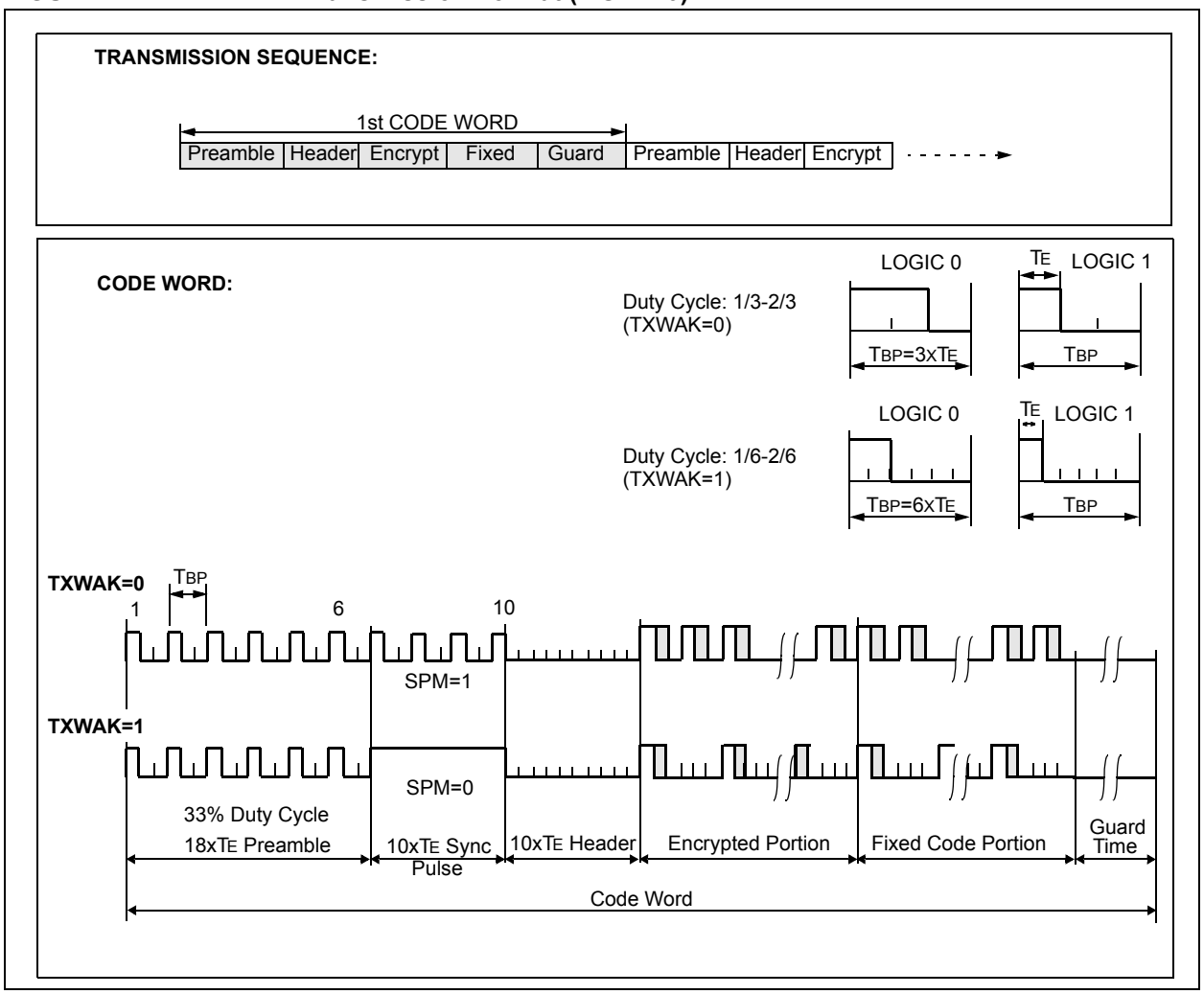
4.2 Code Word Organization

The HCS361 transmits a 67-bit code word when a button is pressed. The 67-bit word is constructed from a Fixed Code portion and an Encrypted Code portion (Figure 3-2).

The **Encrypted Data** is generated from 4 function bits, 2 user bits, overflow bit, Independent mode bit, and 8 serial number bits, and the 16-bit synchronization value (Figure 9-4).

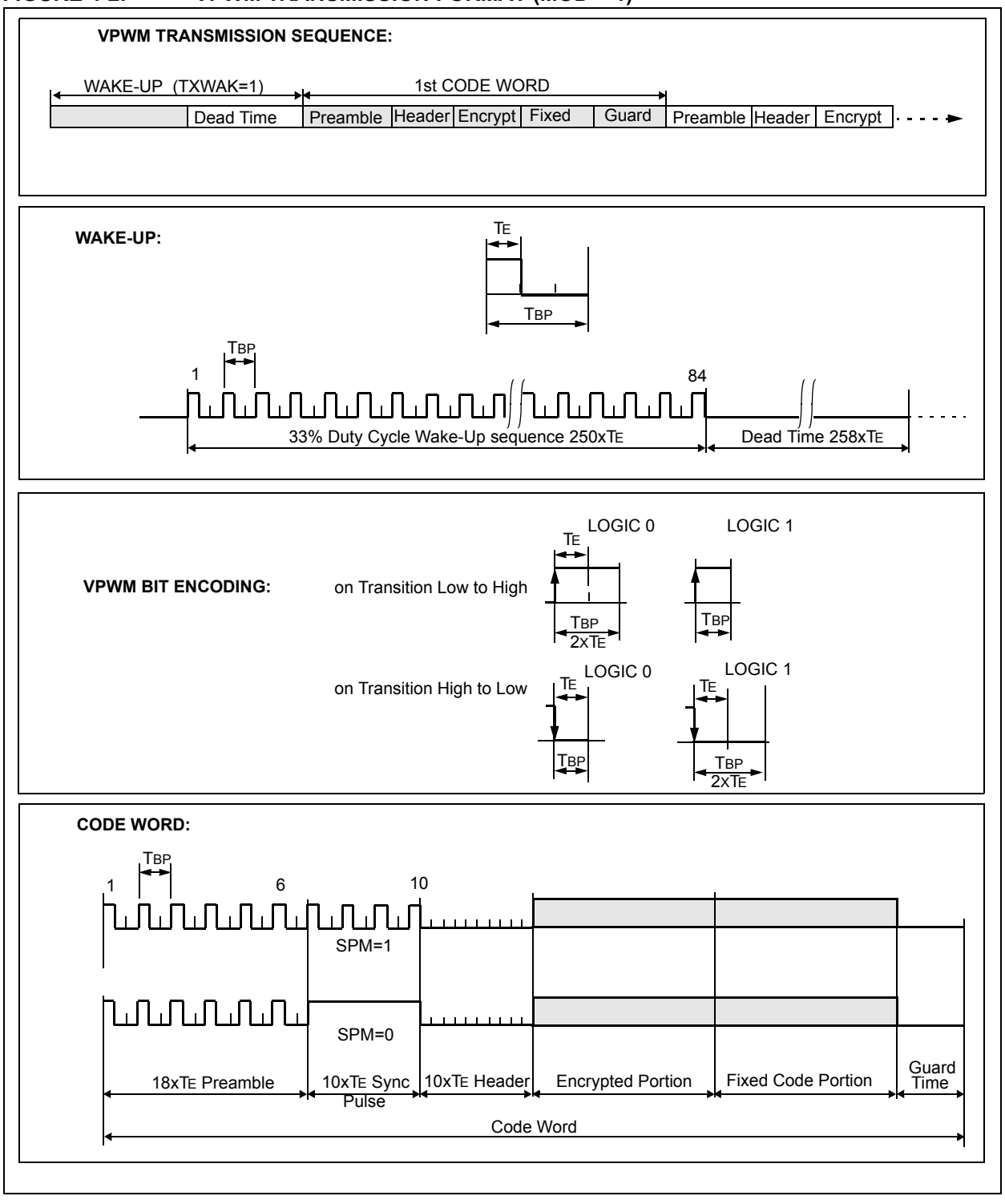
The **Non-encrypted Code Data** is made up of VLOW bit, 2 CRC bits, 4 function bits, and the 28-bit serial number. If the extended serial number (32 bits) is selected, the 4 function code bits will not be transmitted.

FIGURE 4-1: PWM Transmission Format (MOD = 0)



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FIGURE 4-2: VPWM TRANSMISSION FORMAT (MOD = 1)



5.0 SPECIAL FEATURES

5.1 Code Word Completion

Code word completion is an automatic feature that ensures that the entire code word is transmitted, even if the button is released before the transmission is complete and that a minimum of two words are completed. The HCS361 encoder powers itself up when a button is pushed and powers itself down after the current transmission is finished, if the user has already released the button. If the button is held down beyond the time for two transmissions, then multiple transmissions will result. The HCS361 transmits at least two transmissions before powering down. If another button is activated during a transmission, the active transmission will be aborted and the new code will be generated using the new button information.

5.2 Blank Alternate Code Word

Federal Communications Commission (FCC) part 15 rules specify the limits on fundamental power and harmonics that can be transmitted. Power is calculated on the worst case average power transmitted in a 100 ms window. It is therefore advantageous to minimize the duty cycle of the transmitted word. This can be achieved by minimizing the duty cycle of the individual bits and by blanking out consecutive words. Blank Alternate Code Word (BACW) is used for reducing the average power of a transmission (Figure 5-1). This is a selectable feature. Using the BACW allows the user to transmit a higher amplitude transmission if the transmission length is shorter. The FCC puts constraints on the average power that can be transmitted by a device, and BACW effectively prevents continuous transmission by only allowing the transmission of every second word. This reduces the average power transmitted and hence, assists in FCC approval of a transmitter device.

5.3 CRC (Cycle Redundancy Check) Bits

The CRC bits are calculated on the 65 previously transmitted bits. The CRC bits can be used by the receiver to check the data integrity before processing starts. The CRC can detect all single bit and 66% of double bit errors. The CRC is computed as follows:

EQUATION 5-1: CRC Calculation

$$CRC[1]_{n+1} = CRC[0]_n \wedge Di_n$$

and

$$CRC[0]_{n+1} = (CRC[0]_n \wedge Di_n) \wedge CRC[1]_n$$

with

$$CRC[1,\ 0]_0 = 0$$

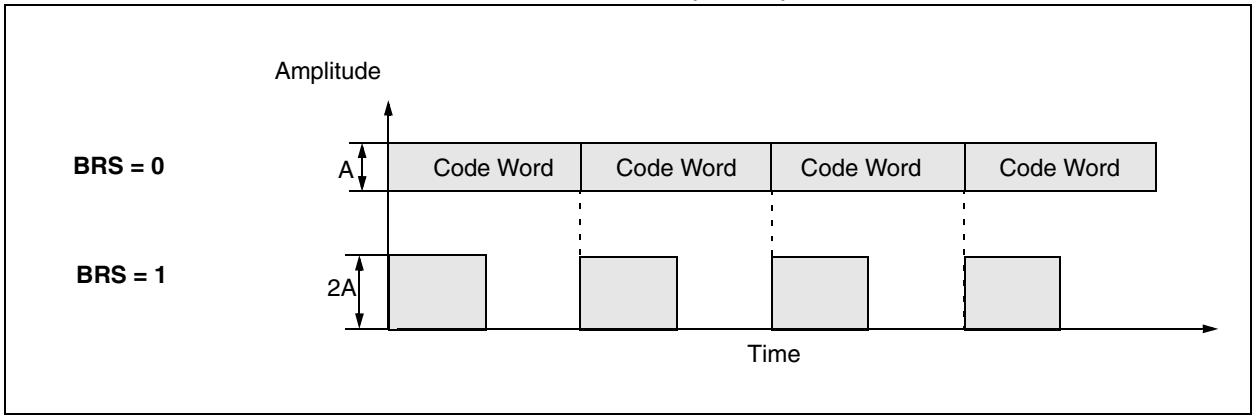
and

Di_n the nth transmission bit 0 ð n ð 64

Note: The CRC may be wrong when the battery voltage is around either of the VLOW trip points. This may happen because VLOW is sampled twice each transmission, once for the CRC calculation (PWM is low) and once when VLOW is transmitted (PWM is high). VDD tends to move slightly during a transmission which could lead to a different value for VLOW being used for the CRC calculation and the transmission

. Work around: If the CRC calculation is incorrect, recalculate for the opposite value of VLOW.

FIGURE 5-1: BLANK ALTERNATE CODE WORD (BACW)



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5.4 Auto-shutoff

The Auto-shutoff function automatically stops the device from transmitting if a button inadvertently gets pressed for a long period of time. This will prevent the device from draining the battery if a button gets pressed while the transmitter is in a pocket or purse. This function can be enabled or disabled and is selected by setting or clearing the time-out bit (Section 3.5.13). Setting this bit will enable the function (turn Auto-shutoff function on) and clearing the bit will disable the function. Time-out period is approximately 25 seconds.

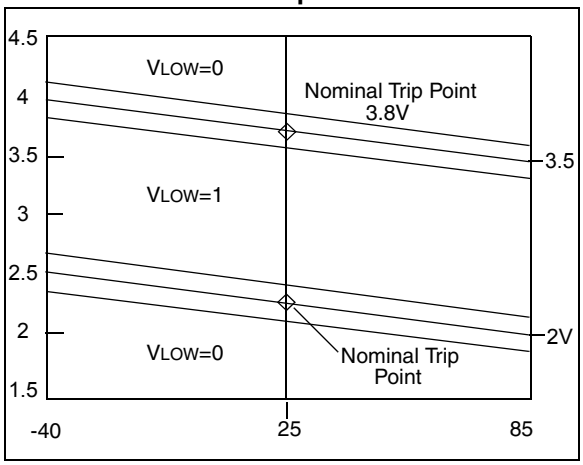
5.5 VLOW: Voltage LOW Indicator

The VLOW bit is transmitted with every transmission (Figure 3-2) and will be transmitted as a one if the operating voltage has dropped below the low voltage trip point, typically 3.8V at 25°C. This VLOW signal is transmitted so the receiver can give an indication to the user that the transmitter battery is low.

5.6 $\overline{\text{LED}}$ Output Operation

During normal transmission the $\overline{\text{LED}}$ output is LOW while the data is being transmitted and high during the guard time. Two voltage indications are combined into one bit: VLOW. Table 5-1 indicates the operation value of VLOW while data is being transmitted.

FIGURE 5-2: VLOW Trip Point VS. Temperature



If the supply voltage drops below the low voltage trip point, the $\overline{\text{LED}}$ output will be toggled at approximately 1Hz during the transmission.

TABLE 5-1: VLOW AND LED VS. VDD

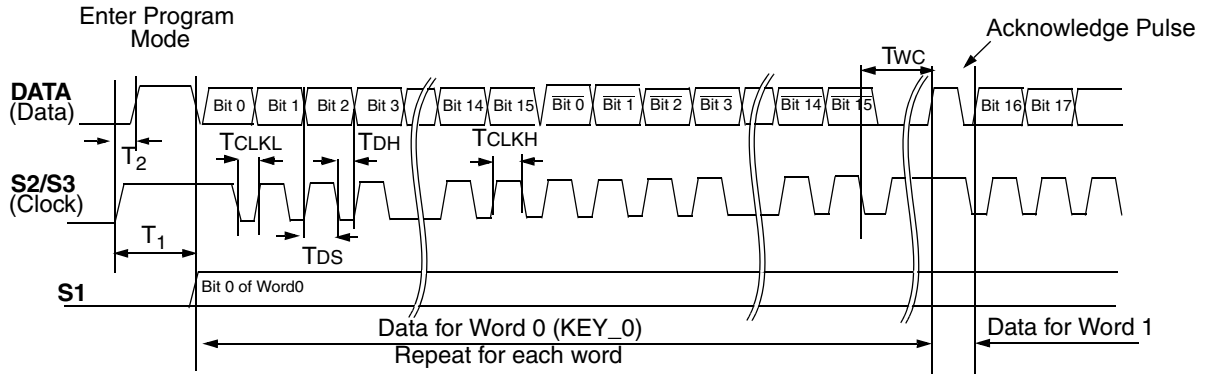
Approximate Supply Voltage	Vlow Bit	LED Operation*
Max →3.8V	0	Normal
3.8V →2.2V	1	Flashing
2.2V →Min	0	Normal

*See also FLASH operating modes.

6.0 PROGRAMMING THE HCS361

When using the HCS361 in a system, the user will have to program some parameters into the device including the serial number and the secret key before it can be used. The programming cycle allows the user to input all 192 bits in a serial data stream, which are then stored internally in EEPROM. Programming will be initiated by forcing the PWM line high, after the S3 line has been held high for the appropriate length of time. S0 should be held low during the entire program cycle. The S1 line on the HCS361 part needs to be set or cleared depending on the LS bit of the memory map (Key 0) before the key is clocked in to the HCS361. S1 must remain at this level for the duration of the programming cycle. The device can then be programmed by clocking in 16 bits at a time, followed by the word's complement using S3 or S2 as the clock line and PWM as the data in line. After each 16-bit word is loaded, a programming delay is required for the internal program cycle to complete. An Acknowledge bit can be read back after the programming delay (TWC). After the first word and its complement have been downloaded, an automatic bulk write is performed. This delay can take up to Twc. At the end of the programming cycle, the device can be verified (Figure 6-1) by reading back the EEPROM. Reading is done by clocking the S3 line and reading the data bits on PWM. For security reasons, it is not possible to execute a Verify function without first programming the EEPROM. **A Verify operation can only be done once, immediately following the Program cycle**.

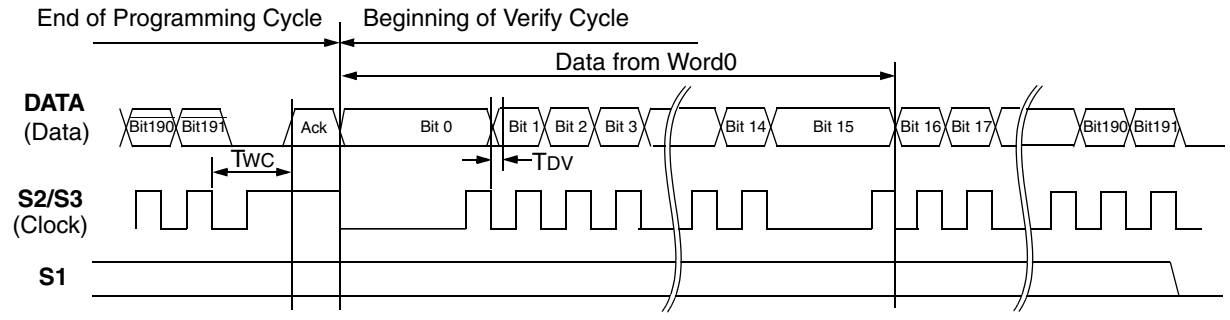
FIGURE 6-1: Programming Waveforms



Note 1: Unused button inputs to be held to ground during the entire programming sequence.

2: The VDD pin must be taken to ground after a Program/Verify cycle.

FIGURE 6-2: Verify Waveforms



Note: A Verify sequence is performed only once immediately after the Program cycle.

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TABLE 6-3: PROGRAMMING/VERIFY TIMING REQUIREMENTS

V_{DD} = 5.0V ±10% 25° C ±5 °C				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**
Program mode setup time	T_2	0	4.0	ms
Hold time 1	T_1	9.0	—	ms
Program cycle time	TWC	50	—	ms
Clock low time	TCLKL	50	—	µs
Clock high time	TCLKH	50	—	µs
Data setup time	TDS	0	—	µs(1)
Data hold time	TDH	30	—	µs(1)
Data out valid time	TDV	—	30	µs(1)

Note 1: Typical values - not tested in production.

7.0 INTEGRATING THE HCS361 INTO A SYSTEM

Use of the HCS361 in a system requires a compatible decoder. This decoder is typically a microcontroller with compatible firmware. Microchip will provide (via a license agreement) firmware routines that accept transmissions from the HCS361 and decrypt the hopping code portion of the data stream. These routines provide system designers the means to develop their own decoding system.

7.1 Learning a Transmitter to a Receiver

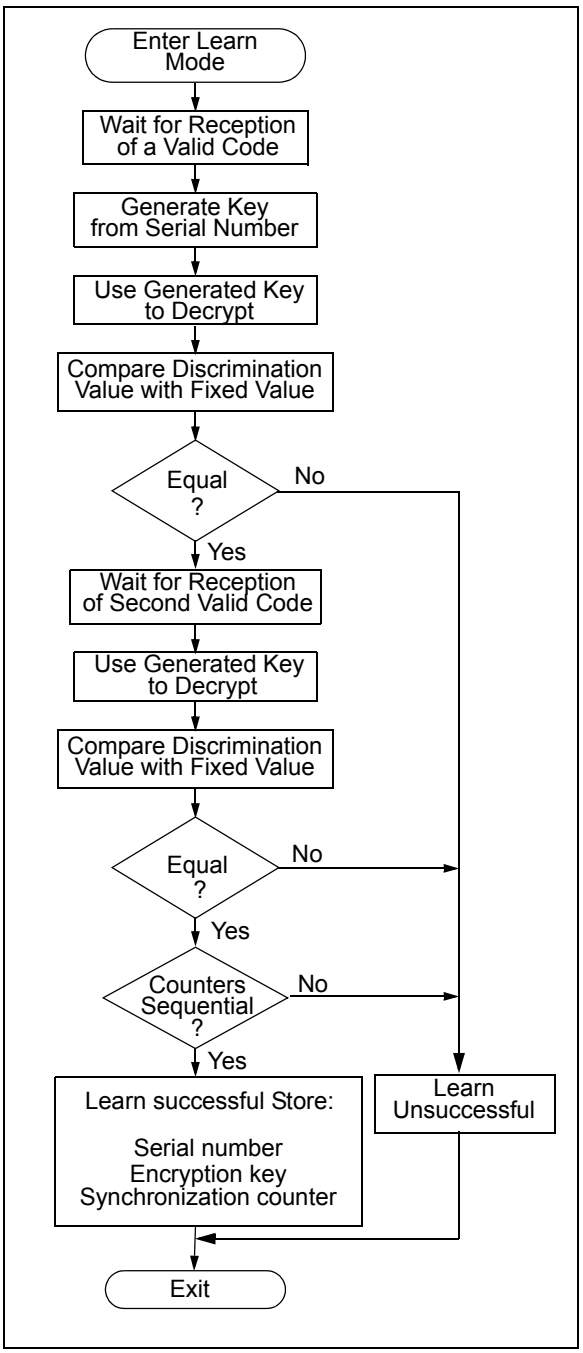
A transmitter must first be 'learned' by a decoder before its use is allowed in the system. Several learning strategies are possible, Figure 7-1 details a typical learn sequence. Core to each, the decoder must minimally store each learned transmitter's serial number and current synchronization counter value in EEPROM. Additionally, the decoder typically stores each transmitter's unique crypt key. The maximum number of learned transmitters will therefore be relative to the available EEPROM.

A transmitter's serial number is transmitted in the clear but the synchronization counter only exists in the code word's encrypted portion. The decoder obtains the counter value by decrypting using the same key used to encrypt the information. The KEELOQ algorithm is a symmetrical block cipher so the encryption and decryption keys are identical and referred to generally as the crypt key. The encoder receives its crypt key during manufacturing. The decoder is programmed with the ability to generate a crypt key as well as all but one required input to the key generation routine; typically the transmitter's serial number.

Figure 7-1 summarizes a typical learn sequence. The decoder receives and authenticates a first transmission; first button press. Authentication involves generating the appropriate crypt key, decrypting, validating the correct key usage via the discrimination bits and buffering the counter value. A second transmission is received and authenticated. A final check verifies the counter values were sequential; consecutive button presses. If the learn sequence is successfully complete, the decoder stores the learned transmitter's serial number, current synchronization counter value and appropriate crypt key. From now on the crypt key will be retrieved from EEPROM during normal operation instead of recalculating it for each transmission received.

Certain learning strategies have been patented and care must be taken not to infringe.

FIGURE 7-1: TYPICAL LEARN SEQUENCE

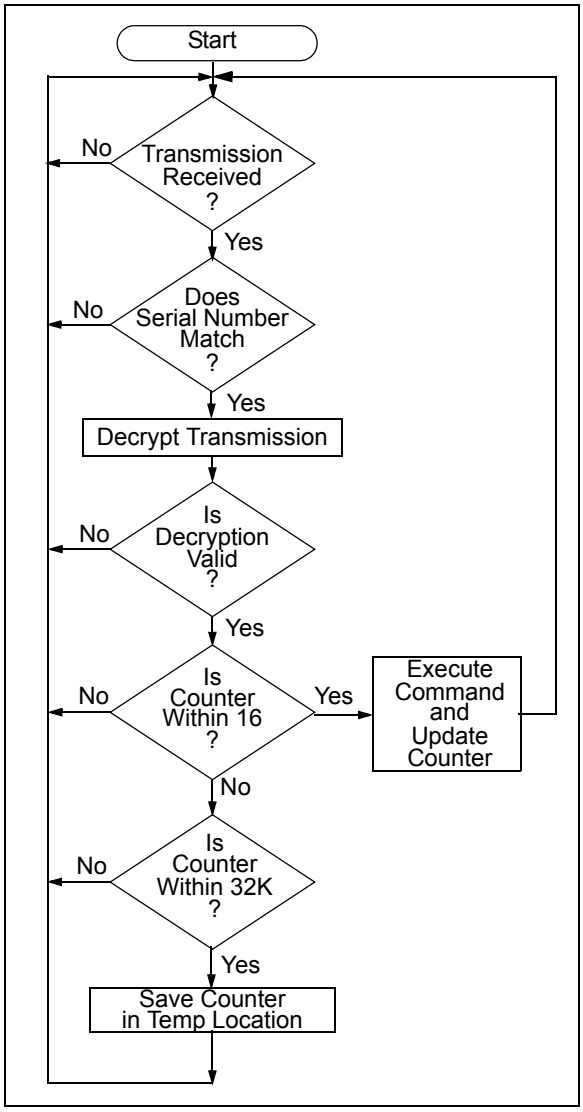


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7.2 Decoder Operation

Figure 7-2 summarizes normal decoder operation. The decoder waits until a transmission is received. The received serial number is compared to the EEPROM table of learned transmitters to first determine if this transmitter's use is allowed in the system. If from a learned transmitter, the transmission is decrypted using the stored crypt key and authenticated via the discrimination bits for appropriate crypt key usage. If the decryption was valid the synchronization value is evaluated.

FIGURE 7-2: TYPICAL DECODER OPERATION



7.3 Synchronization with Decoder (Evaluating the Counter)

The KEELOQ technology patent scope includes a sophisticated synchronization technique that does not require the calculation and storage of future codes. The technique securely blocks invalid transmissions while providing transparent resynchronization to transmitters inadvertently activated away from the receiver.

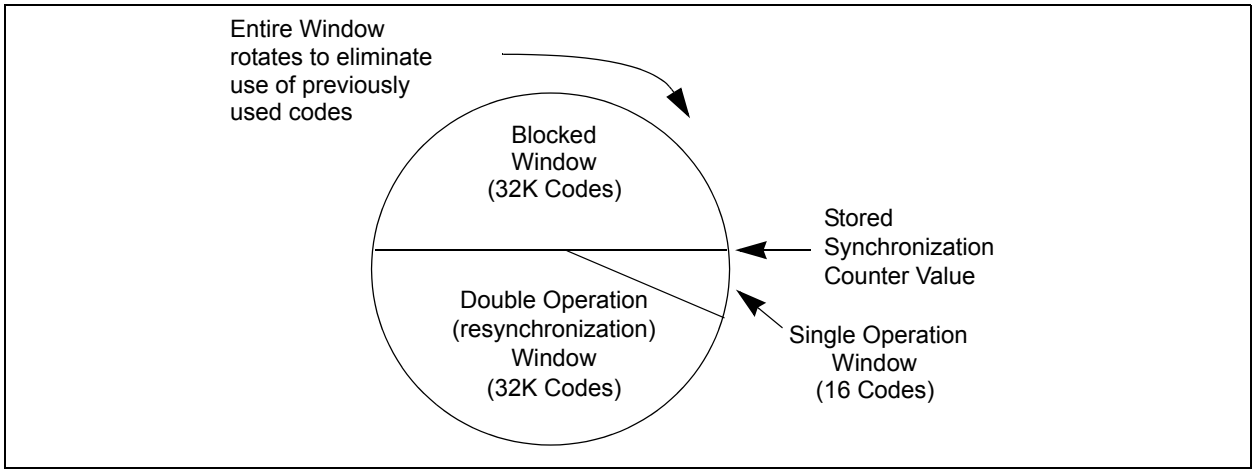
Figure 7-3 shows a 3-partition, rotating synchronization window. The size of each window is optional but the technique is fundamental. Each time a transmission is authenticated, the intended function is executed and the transmission's synchronization counter value is stored in EEPROM. From the currently stored counter value there is an initial "Single Operation" forward window of 16 codes. If the difference between a received synchronization counter and the last stored counter is within 16, the intended function will be executed on the single button press and the new synchronization counter will be stored. Storing the new synchronization counter value effectively rotates the entire synchronization window.

A "Double Operation" (resynchronization) window further exists from the Single Operation window up to 32K codes forward of the currently stored counter value. It is referred to as "Double Operation" because a transmission with synchronization counter value in this window will require an additional, sequential counter transmission prior to executing the intended function. Upon receiving the sequential transmission the decoder executes the intended function and stores the synchronization counter value. This resynchronization occurs transparently to the user as it is human nature to press the button a second time if the first was unsuccessful.

The third window is a "Blocked Window" ranging from the double operation window to the currently stored synchronization counter value. Any transmission with synchronization counter value within this window will be ignored. This window excludes previously used, perhaps code-grabbed transmissions from accessing the system.

Note:	The synchronization method described in this section is only a typical implementation and because it is usually implemented in firmware, it can be altered to fit the needs of a particular system.

FIGURE 7-3: SYNCHRONIZATION WINDOW



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8.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers and dsPIC® digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB C Compiler for Various Device Families
  - HI-TECH C for Various Device Families
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
  - MPLAB ICD 3
  - PICkit™ 3 Debug Express
- Device Programmers
  - PICkit™ 2 Programmer
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits, and Starter Kits

8.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
  - Simulator
  - Programmer (sold separately)
  - In-Circuit Emulator (sold separately)
  - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- Debug using:
  - Source files (C or assembly)
  - Mixed C and assembly
  - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

8.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

8.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, preprocessor, and one-step driver, and can run on multiple platforms.

8.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

8.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

8.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

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8.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC® MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

8.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC® Flash MCUs and dsPIC® Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

8.9 MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and microcontroller (MCU) devices. It debugs and programs PIC® Flash microcontrollers and dsPIC® DSCs with the powerful, yet easy-to-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

8.10 PICkit 3 In-Circuit Debugger/ Programmer and PICkit 3 Debug Express

The MPLAB PICkit 3 allows debugging and programming of PIC® and dsPIC® Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming™.

The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

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8.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit™ 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit™ 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

8.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

8.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

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9.0 ELECTRICAL CHARACTERISTICS

TABLE 9-1: ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Units
V_{DD}	Supply voltage	-0.3 to 6.9	V
V_{IN}	Input voltage	-0.3 to V_{DD} + 0.3	V
V_{OUT}	Output voltage	-0.3 to V_{DD} + 0.3	V
I_{OUT}	Max output current	25	mA
T_{STG}	Storage temperature	-55 to +125	°C **(Note)**
T_{LSOL}	Lead soldering temp	300	°C **(Note)**
V_{ESD}	ESD rating	4000	V

Note: Stresses above those listed under “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device.

TABLE 9-2: DC CHARACTERISTICS

Commercial (C): Tamb = 0° C to +70° C Industrial (I): Tamb = -40° C to +85° C									
		2.0V < V_{DD} < 3.3			3.0 < V_{DD} < 6.6				
Parameter	**Sym.**	**Min**	**Typ[1]**	**Max**	**Min**	**Typ[1]**	**Max**	**Unit**	**Conditions**
Operating current (avg)	I_{CC}		0.3	1.2		0.7	1.6	mA	V_{DD} = 3.3V V_{DD} = 6.6V
Standby current	I_{CCS}		0.1	1.0		0.1	1.0	µA	
Auto-shutoff current [2,3]	I_{CCS}		40	75		160	350	µA	
High level Input voltage	V_{IH}	0.55V_{DD}		V_{DD}+0.3	0.55V_{DD}		V_{DD}+0.3	V	
Low level input voltage	V_{IL}	-0.3		0.15V_{DD}	-0.3		0.15V_{DD}	V	
High level output voltage	V_{OH}	0.7V_{DD}			0.7V_{DD}			V	I_{OH} = -1.0 mA, V_{DD} = 2.0V I_{OH} = -2.0 mA, V_{DD} = 6.6V
Low level output voltage	V_{OL}			0.08V_{DD}			0.08V_{DD}	V	I_{OL} = 1.0 mA, V_{DD} = 2.0V I_{OL} = 2.0 mA, V_{DD} = 6.6V
$\overline{LED}$ sink current	I_{LED}	0.15	1.0	4.0	0.15	1.0	4.0	mA	V_{LED}[4] = 1.5V, V_{DD} = 6.6V
Pull-Down Resistance; S0-S3	R_{S0-3}	40	60	80	40	60	80	KΩ	V_{DD} = 4.0V
Pull-Down Resistance; PWM	R_{PWM}	80	120	160	80	120	160	KΩ	V_{DD} = 4.0V

Note 1: Typical values are at 25° C.
2: Auto-shutoff current specification does not include the current through the input pull-down resistors.
3: Auto-shutoff current is periodically sampled and not 100% tested
4: V_{LED} is the voltage between the V_{DD} pin and the $\overline{LED}$ pin.

FIGURE 9-1: POWER-UP AND TRANSMIT TIMING

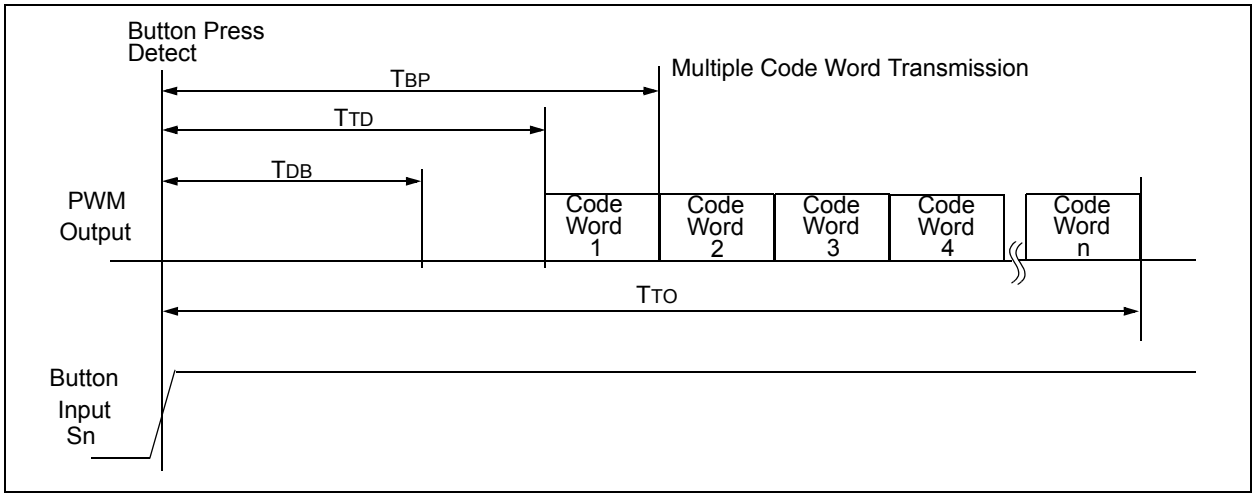


TABLE 9-3: POWER-UP AND TRANSMIT TIMING REQUIREMENTS

VDD = +2.0 to 6.6V Commercial (C): Tamb = 0° C to +70° C Industrial (I): Tamb = -40° C to +85° C					
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Remarks**
Time to second button press	TBP	10 + Code Word Time	26 + Code Word Time	ms	**(Note 1)**
Transmit delay from button detect	TTD	4.5	26	ms	**(Note 2)**
Debounce delay	TDB	4	13	ms	
Auto-shutoff time-out period	TTO	15	35	s	**(Note 3)**

Note 1: TBP is the time in which a second button can be pressed without completion of the first code word and the intention was to press the combination of buttons.

2: Transmit delay maximum value if the previous transmission was successfully transmitted.

3: The Auto-shutoff time-out period is not tested.

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FIGURE 9-2: PWM FORMAT SUMMARY (MOD = 0)

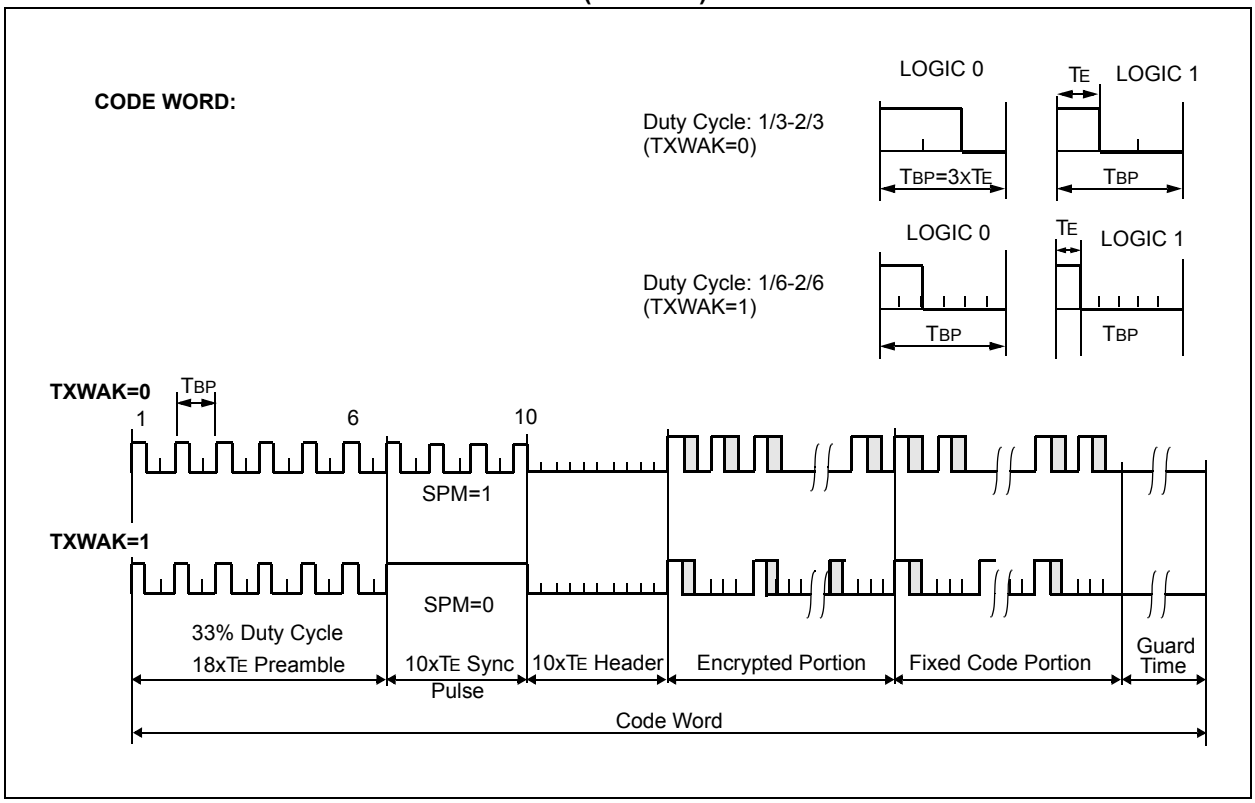


FIGURE 9-3: PWM PREAMBLE/HEADER FORMAT (MOD=0)

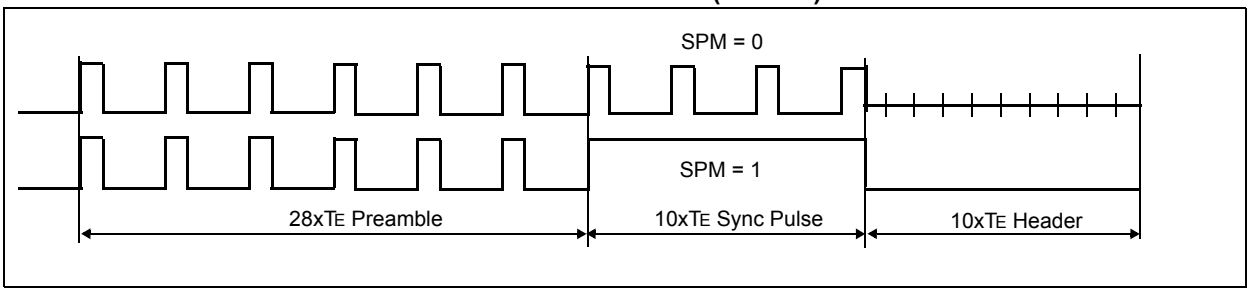


FIGURE 9-4: PWM DATA FORMAT (MOD=0)

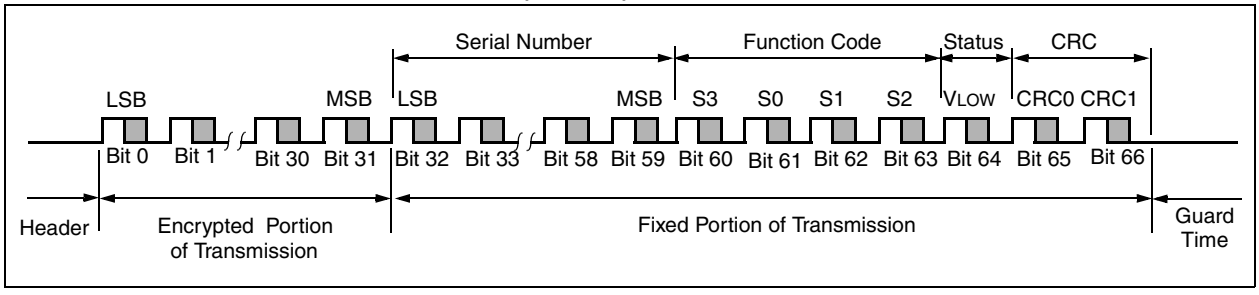


FIGURE 9-5: VPWM FORMAT SUMMARY (MOD = 1)

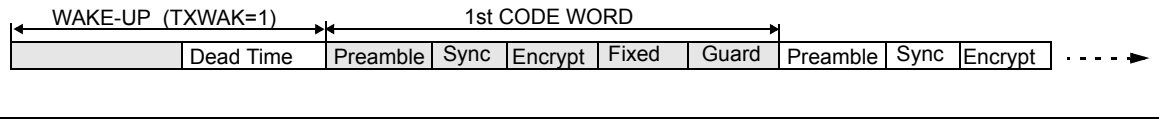


FIGURE 9-6: VPWM WAKE-UP FORMAT (MOD=1)

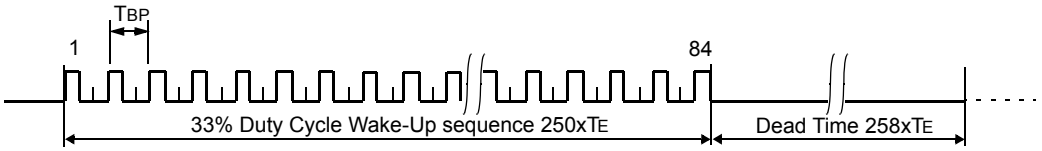


FIGURE 9-7: VPWM PREAMBLE/HEADER FORMAT (MOD=1)

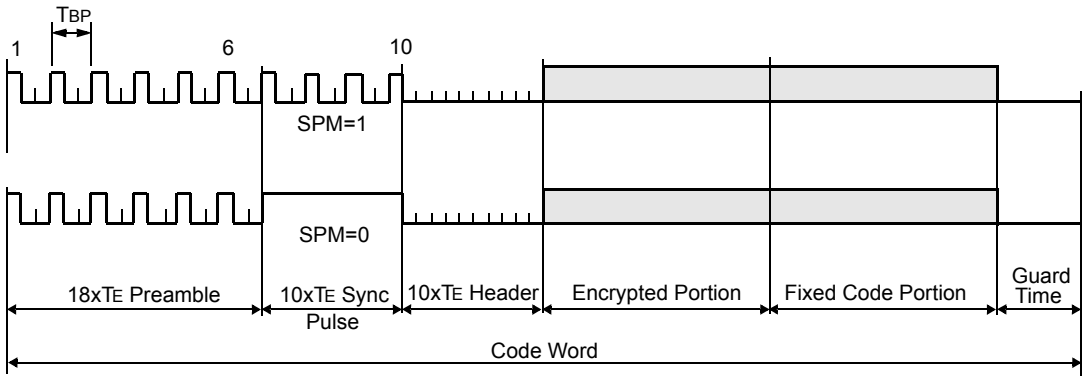
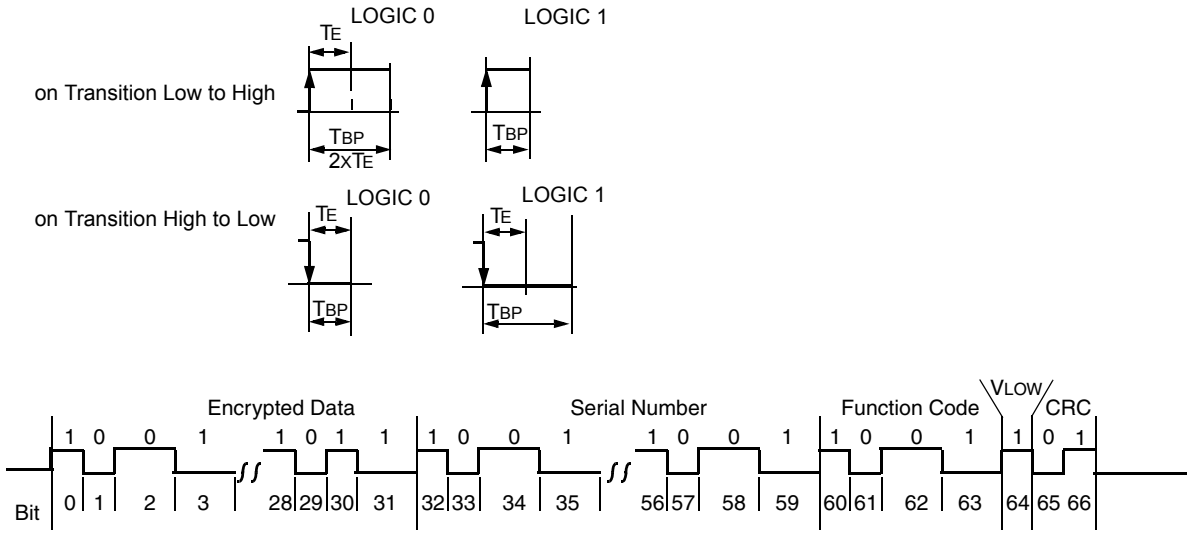


FIGURE 9-8: VPWM DATA WORD FORMAT (MOD=1)



Note: The bit values are only shown as an example.

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FIGURE 9-9: HCS361 NORMALIZED TE VS. TEMP

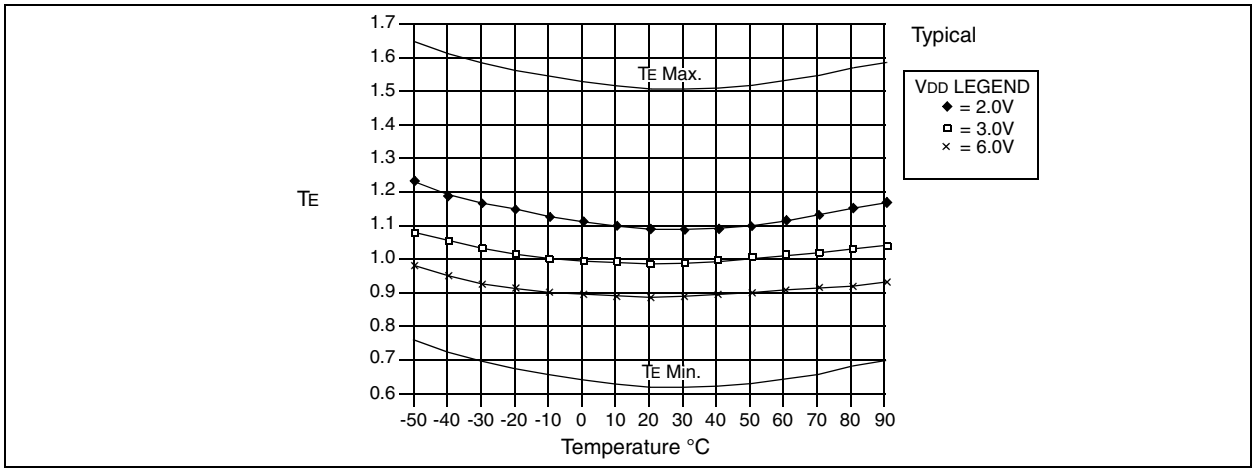


TABLE 9-4: TIMING PARAMETERS: PWM MODE (TXWAK=0)

VDD = +2.0 to 6.6V Commercial (C):Tamb = 0° C to +70° C Industrial (I):Tamb = -40° C to +85° C		Code Words Transmitted						
		BSEL = 0			BSEL = 1			
Symbol	**Characteristic**	**Min**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**
TE	Basic pulse element	260	400	620	130	200	310	µs
TBP	PWM bit pulse width		3			3		TE
TP	Preamble duration		28			28		TE
TS	Sync Pulse duration		10			10		TE
TH	Header duration		10			10		TE
THOP	Hopping code duration		96			96		TE
TFIX	Fixed code duration		105			105		TE
TG	Guard Time		18			34		TE
—	Total Transmit Time		267			283		TE
—	Total Transmit Time	69.4	106.8	165.5	36.7	56.6	87.7	ms
—	PWM data rate	1282	833	538	2564	1667	1075	bps

Note: The timing parameters are not tested but derived from the oscillator clock.

TABLE 9-5: TIMING PARAMETERS: PWM MODE (TXWAK=1)

VDD = +2.0 to 6.6V Commercial (C):Tamb = 0° C to +70° C Industrial (I):Tamb = -40° C to +85° C		Code Words Transmitted						
		BSEL = 0			BSEL = 1			
Symbol	**Characteristic**	**Min**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**
TE	Basic pulse element	130	200	310	65	100	155	µs
TBP	PWM bit pulse width		6			6		TE
TP	Preamble duration		28			28		TE
TS	Sync Pulse duration		10			10		TE
TH	Header duration		10			10		TE
THOP	Hopping code duration		192			192		TE
TFIX	Fixed code duration		210			210		TE
TG	Guard Time		34			66		TE
—	Total Transmit Time		484			516		TE
—	Total Transmit Time	62.9	96.8	150.0	33.5	51.6	79.9	ms
—	PWM data rate	1282	833	538	2564	1667	1075	bps

Note: The timing parameters are not tested but derived from the oscillator clock.

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TABLE 9-6: TIMING PARAMETERS: VPWM MODE (BSEL=0)

VDD = +2.0 to 6.6V Commercial (C): Tamb = 0° C to +70° C Industrial (I): Tamb = -40° C to +85° C		Code Words Transmitted						
		Shortest			Longest			
Symbol	**Characteristic**	**Min**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**
TE	Basic pulse element	260	400	620	260	400	620	µs
TP	Preamble duration		28			28		TE
TS	Sync Pulse duration		10			10		TE
TH	Header duration		10			10		TE
THOP	Hopping code duration		32			64		TE
TFIX	Fixed code duration		35			70		TE
TG	Guard Time		114			114		TE
—	Total Transmit Time		229			296		TE
—	Total Transmit Time	59.5	91.6	141.9	76.9	118.4	183.5	ms
—	VPWM data rate	3846	2500	1613	3846	2500	1613	bps

Note: The timing parameters are not tested but derived from the oscillator clock.

TABLE 9-7: TIMING PARAMETERS: VPWM MODE (BSEL=1)

VDD = +2.0 to 6.6V Commercial (C): Tamb = 0° C to +70° C Industrial (I): Tamb = -40° C to +85° C		Code Words Transmitted						
		Shortest			Longest			
Symbol	**Characteristic**	**Min**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**
TE	Basic pulse element	130	200	310	130	200	310	µs
TP	Preamble duration		28			28		TE
TS	Sync Pulse duration		10			10		TE
TH	Header duration		10			10		TE
THOP	Hopping code duration		32			64		TE
TFIX	Fixed code duration		35			70		TE
TG	Guard Time		226			226		TE
—	Total Transmit Time		341			408		TE
—	Total Transmit Time	44.3	68.2	105.7	53.0	81.6	126.4	ms
—	VPWM data rate	7692	5000	3226	7692	5000	3226	bps

Note: The timing parameters are not tested but derived from the oscillator clock.

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10.0 PACKAGING INFORMATION

10.1 Package Marking Information

8-Lead PDIP



Example



8-Lead SOIC



Example



Legend:	XX...X	Customer specific information*
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

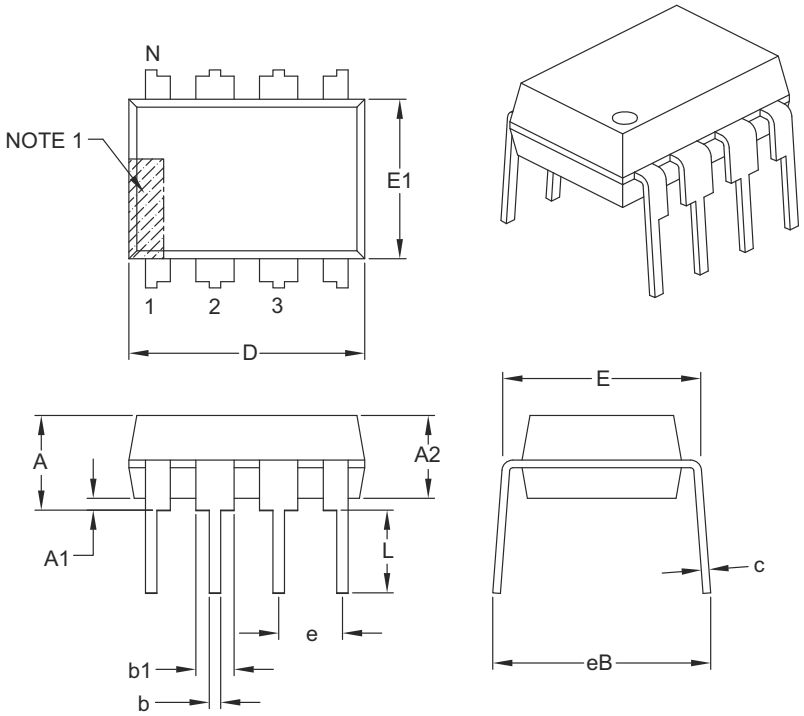
***** Standard PIC MCU device marking consists of Microchip part number, year code, week code, and traceability code. For PIC MCU device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

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10.2 Package Details

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

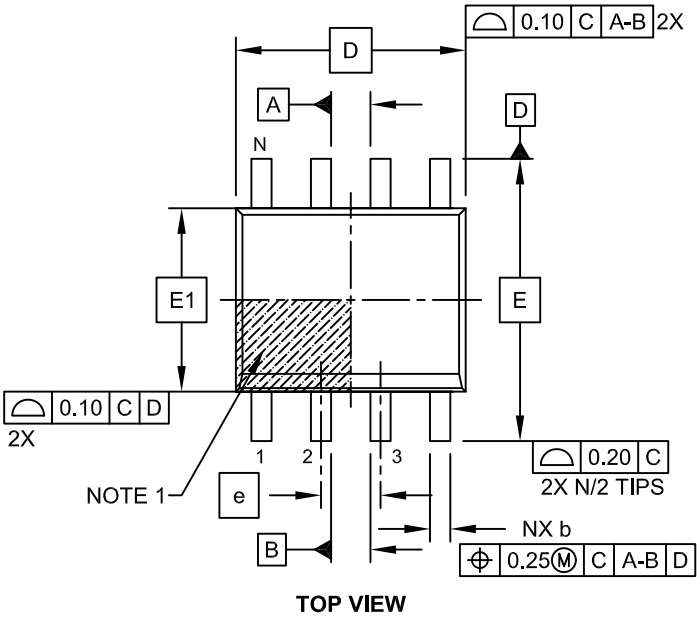
Notes:

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

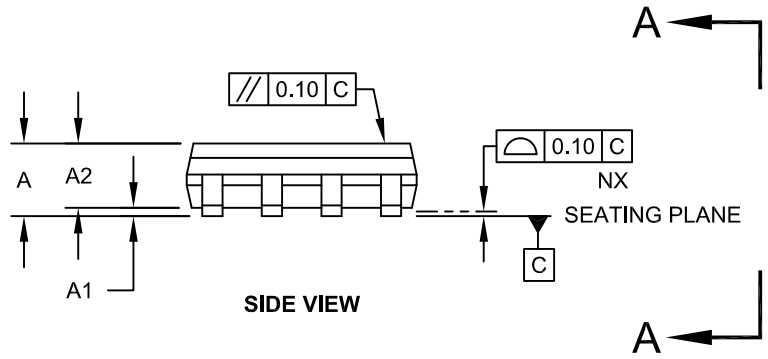
Microchip Technology Drawing C04-018B

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

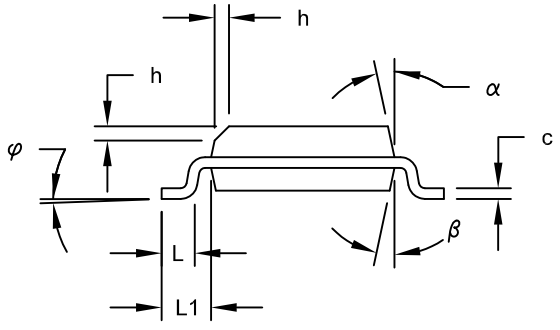
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



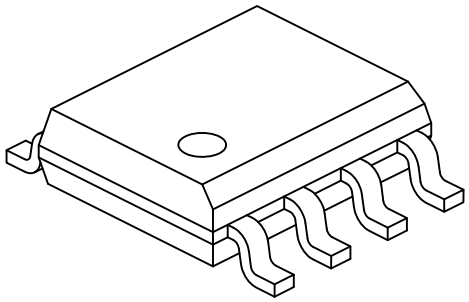
VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

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8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

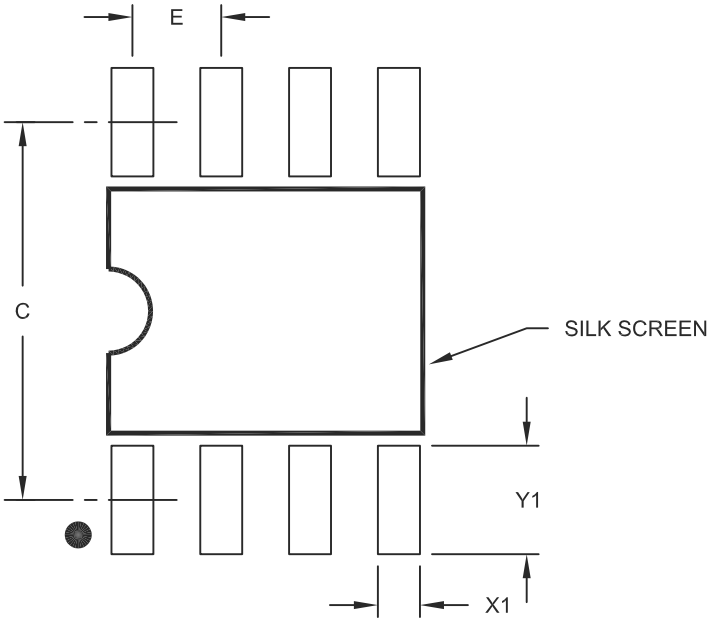
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

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8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

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APPENDIX A: ADDITIONAL INFORMATION

Microchip's Secure Data Products are covered by some or all of the following:

Code hopping encoder patents issued in European countries and U.S.A.

Secure learning patents issued in European countries, U.S.A. and R.S.A.

REVISION HISTORY

Revision F (June 2011)

- Updated the following sections: Development Support, The Microchip Web Site, Reader Response and HCS361 Product Identification System
- Added new section **Appendix A**
- Minor formatting and text changes were incorporated throughout the document

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4. What additions to the document do you think would enhance the structure and subject?

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7. How would you improve this document?

HCS361 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

HCS361 — __ /P

Package:	P =	Plastic DIP (300 mil Body), 8-lead
	SN =	Plastic SOIC (150 mil Body), 8-lead
Temperature Range:	Blank =	0°C to +70°C
	I =	–40°C to +85°C
Device:	HCS361	Code Hopping Encoder
	HCS361T	Code Hopping Encoder (Tape and Reel)

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