PIC16(L)F145X

14/20-Pin, 8-Bit Flash USB Microcontroller Product Brief

High-Performance RISC CPU:

- C Compiler Optimized Architecture
- Only 49 Instructions
- 14 Kbytes Linear Program Memory Addressing
- 1024 bytes Linear Data Memory Addressing
- Operating Speed:
  - DC – 48 MHz clock input
  - DC – 83 ns instruction cycle
  - Selectable 3x or 4x PLL for specific frequencies
- Interrupt Capability with Automatic Context Saving
- 16-Level Deep Hardware Stack with Optional Overflow/Underflow Reset
- Direct, Indirect and Relative Addressing modes:
  - Two full 16-bit File Select Registers (FSRs) capable of accessing both data or program memory
  - FSRs can read program and data memory

Special Microcontroller Features:

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF145X)
  - 2.3V to 5.5V (PIC16F145X)
- Self-Programmable under Software Control
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Programmable Brown-Out Reset (BOR)
- Low-Power BOR (LPBOR)
- Extended Watchdog Timer (WDT):
  - Programmable period from 1 ms to 256s
- Programmable Code Protection
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- Enhanced Low-Voltage Programming (LVP)
- Power-Saving Sleep mode

Universal Serial Bus (USB) Features:

- Self-tuning from USB host (eliminates need for external crystal)
- USB V2.0 Compliant SIE
- Low Speed (1.5 Mb/s) and Full Speed (12 Mb/s)
- Supports Control, Interrupt, Isochronous and Bulk Transfers
- Supports up to 8 Bidirectional Endpoints
- 512-Byte Dual Access RAM for USB
- Interrupt-on-Change (IOC) on D+/D- for USB Host Detection
- Configurable Internal Pull-up Resistors for use with USB

Low-Power Features PIC16LF145X with XLP:

- Standby Current:
  - 20 nA @ 1.8V, typical
- Watchdog Timer Current:
  - 300 nA @ 1.8V, typical
- Operating Current:
  - 30 μA/MHz @ 1.8V, typical
- Timer1 Oscillator:
  - 600 nA @ 32 kHz, 1.8V, typical

Flexible Oscillator Structure:

- 16 MHz Internal Oscillator Block:
  - Factory calibrated to ±0.25%, typical
  - Software selectable frequency range from 16 MHz to 31 kHz
  - Tunable to 0.25% across temperature range
  - 48 MHz with 3x PLL
- 31 kHz Low-Power Internal Oscillator
- Clock Switching with run from:
  - Primary Oscillator
  - Secondary Oscillator (SOSC)
  - Internal Oscillator
- Clock Reference Output:
  - Clock Prescaler
  - CLKOUT

Analog Features(1):

- Analog-to-Digital Converter (ADC):
  - 10-bit resolution
  - Up to 9 external channels
  - Two internal channels:
    - Fixed Voltage Reference channel
    - DAC output channel
  - Auto acquisition capability
  - Conversion available during Sleep
- Two Comparators:
  - Rail-to-rail inputs
  - Power mode control
  - Software controllable hysteresis
- Voltage Reference module:
  - Fixed Voltage Reference (FVR) with 1.024V, 2.048V and 4.096V output levels
- Up to one rail-to-rail resistive 5-bit DAC with positive reference selection

Note 1: Analog features are not available on PIC16(L)F1454 devices.

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Peripheral Features:

- Up to 14 I/O Pins and three Input-only Pins:
  - High current sink/source 25 mA/25 mA
  - Individually programmable weak pull-ups
  - Individually programmable Interrupt-On-Change (IOC) pins
- Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
- Timer2: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler
- Two 10-bit PWM modules
- Complementary Waveform Generator (CWG)**(1)**:
  - Up to four selectable signal sources
  - Selectable falling and rising edge dead-band control
  - Polarity control
  - Up to four auto-shutdown sources
  - Multiple input sources: PWM, Comparators
- Master Synchronous Serial Port (MSSP) with SPI and I^2C™ with:
  - 7-bit address masking
  - SMBus/PMBus™ compatibility
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART):
  - RS-232, RS-485 and LIN compatible
  - Auto-baud detect
  - Auto-wake-up on Start

Note 1: Not available on PIC16(L)F1454 devices.

PIC16(L)F145X Family Types

Device	Data Sheet Index	Program Memory Flash (words)	Data SRAM (bytes)	I/O's(2)	10-bit ADC (ch)	Comparators	DAC	Timers (8/16-bit)	PWM	EUSART	MSSP (I^2C™/SPI)	CWG	USB	Clock Reference	Debug(1)	XLP
PIC16(L)F1454	(1)	8192	1024	11	—	—	—	2/1	2	1	1	—	1	1	I/H	Y
PIC16(L)F1455	(1)	8192	1024	11	5	2	1	2/1	2	1	1	1	1	1	I/H	Y
PIC16(L)F1459	(1)	8192	1024	17	9	2	1	2/1	2	1	1	1	1	1	I/H	Y

Note 1: I - Debugging, Integrated on Chip; H - Debugging, Available using Debug Header; E - Emulation, Available using Emulation Header.

2: Three pins are input-only.

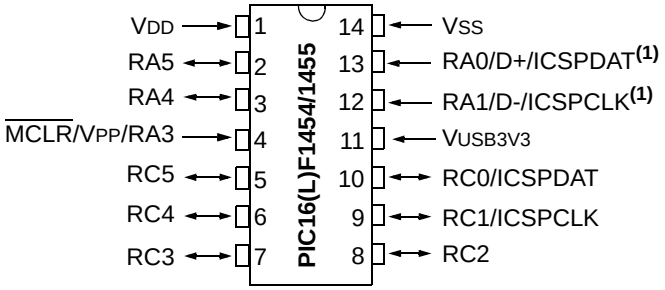
Data Sheet Index:

1: Future Product PIC16(L)F1454/1455/1459 Data Sheet, 14/20-Pin Flash, 8-Bit USB Microcontrollers.

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FIGURE 1: 14-PIN PDIP, SOIC, TSSOP DIAGRAM FOR PIC16(L)F1454/1455

PDIP, SOIC, TSSOP

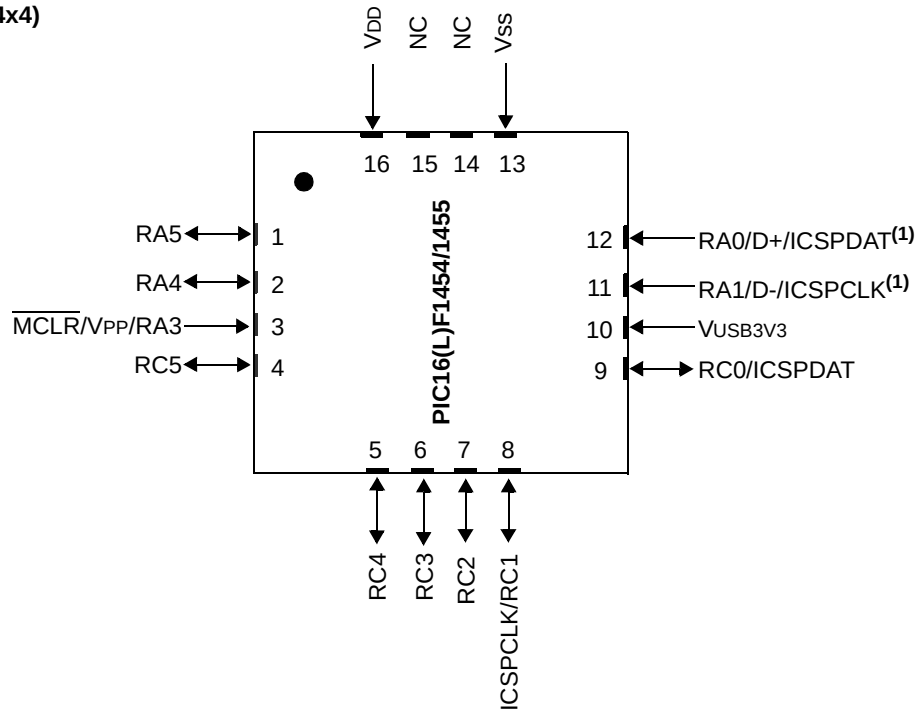


Note 1: LVP support for PIC18(L)F1XK50 legacy designs.

2: See Table 1 for location of all peripheral functions.

FIGURE 2: 16-PIN QFN DIAGRAM FOR PIC16(L)F1454/1455

QFN (4x4)

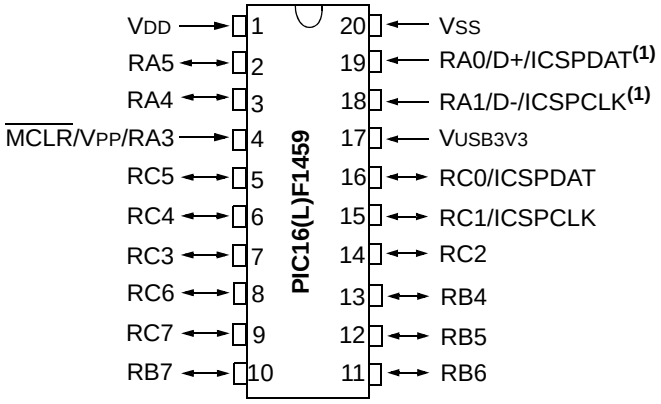


Note 1: LVP support for PIC18(L)F1XK50 legacy designs.

2: See Table 1 for location of all peripheral functions.

FIGURE 3: 20-PIN PDIP, SOIC, SSOP DIAGRAM FOR PIC16(L)F1459

PDIP, SOIC, SSOP

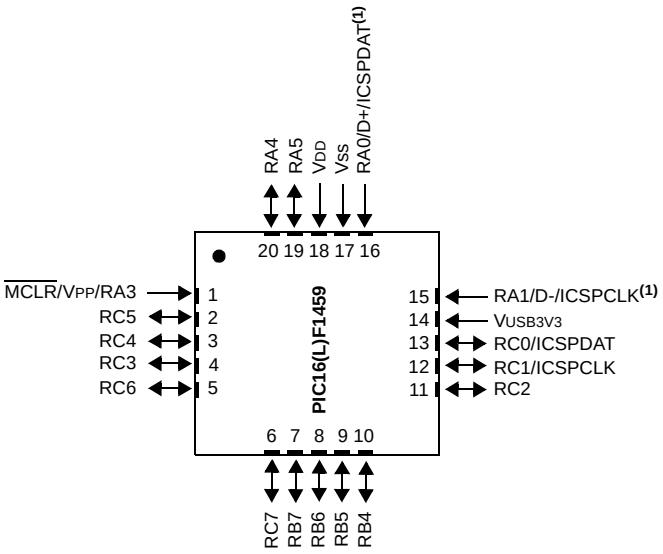


Note 1: LVP support for PIC18(L)F1XK50 legacy designs.

2: See Table 1 for location of all peripheral functions.

FIGURE 4: 20-PIN QFN DIAGRAM FOR PIC16(L)F1459

QFN (5x5)



Note 1: LVP support for PIC18(L)F1XK50 legacy designs.

2: See Table 1 for location of all peripheral functions.

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TABLE 1: 14-PIN ALLOCATION TABLE (PIC16(L)F1454)

I/O	14-Pin PDIP/SOIC/TSSOP	16-Pin QFN	ADC	Reference	Comparator	Timer	CWG	USB	EUSART	PWM	MSSP	Interrupt	Basic
RA0	13	12	—	—	—	—	—	D+	—	—	—	IOC	ICSPDAT(3)
RA1	12	11	—	—	—	—	—	D-	—	—	—	IOC	ICSPCLK(3)
RA2	—	—	—	—	—	—	—	—	—	—	—	—	—
RA3	4	3	—	—	—	T1G(2)	—	—	—	—	$\overline{SS}$(2)	IOC	$\overline{MCLR}$ V_{PP}
RA4	3	2	—	—	—	SOSCO T1G(1)	—	—	—	—	SDO(2)	IOC	CLKOUT OSC2 CLKR(1)
RA5	2	1	—	—	—	SOSCI T1CKI	—	—	—	PWM2(2)	—	IOC	CLKIN OSC1
RC0	10	9	—	—	—	—	—	—	—	—	SCL SCK	—	ICSPDAT
RC1	9	8	—	—	—	—	—	—	—	—	SDA SDI	INT	ICSPCLK
RC2	8	7	—	—	—	—	—	—	—	—	SDO(1)	—	—
RC3	7	6	—	—	—	—	—	—	—	PWM2(1)	$\overline{SS}$(1)	—	CLKR(2)
RC4	6	5	—	—	—	—	—	—	TK CK	—	—	—	—
RC5	5	4	—	—	—	T0CKI	—	—	RX DT	PWM1	—	—	—
V_{DD}	1	16	—	—	—	—	—	—	—	—	—	—	V_{DD}
V_{SS}	14	13	—	—	—	—	—	—	—	—	—	—	V_{SS}
V_{USB3V3}	11	10	—	—	—	—	—	V_{USB3V3}	—	—	—	—	—

Note 1: Default location for peripheral pin function. Alternate location can be selected using the APFCON register.
2: Alternate location for peripheral pin function selected by the APFCON register.
3: LVP support for PIC18(L)F1XK50 legacy designs.

TABLE 2: 14-PIN ALLOCATION TABLE (PIC16(L)F1455)

I/O	14-Pin PDIP/SOIC/TSSOP	16-Pin QFN	ADC	Reference	Comparator	Timer	CWG	USB	EUSART	PWM	MSSP	Interrupt	Basic
RA0	13	12	—	—	—	—	—	D+	—	—	—	IOC	ICSPDAT(3)
RA1	12	11	—	—	—	—	—	D-	—	—	—	IOC	ICSPCLK(3)
RA2	—	—	—	—	—	—	—	—	—	—	—	—	—
RA3	4	3	—	—	—	T1G(2)	—	—	—	—	$\overline{SS}$(2)	IOC	$\overline{MCLR}$ V_{PP}
RA4	3	2	AN3	—	—	SOSCO T1G(1)	—	—	—	—	SDO(2)	IOC	CLKOUT OSC2 CLKR(1)
RA5	2	1	—	—	—	SOSCI T1CKI	—	—	—	PWM2(2)	—	IOC	CLKIN OSC1
RC0	10	9	AN4	V_{REF+}	C1IN+ C2IN+	—	—	—	—	—	SCL SCK	—	ICSPDAT
RC1	9	8	AN5	—	C1IN1- C2IN1-	—	$\overline{CWGFLT}$	—	—	—	SDA SDI	INT	ICSPCLK
RC2	8	7	AN6	DACOUT1	C1IN2- C2IN2-	—	—	—	—	—	SDO(1)	—	—
RC3	7	6	AN7	DACOUT2	C1IN3- C2IN3-	—	—	—	—	PWM2(1)	$\overline{SS}$(1)	—	CLKR(2)
RC4	6	5	—	—	C1OUT C2OUT	—	CWG1B	—	TK CK	—	—	—	—
RC5	5	4	—	—	—	T0CKI	CWG1A	—	RX DT	PWM1	—	—	—
V_{DD}	1	16	—	—	—	—	—	—	—	—	—	—	V_{DD}
V_{SS}	14	13	—	—	—	—	—	—	—	—	—	—	V_{SS}
V_{USB3V3}	11	10	—	—	—	—	—	V_{USB3V3}	—	—	—	—	—

Note 1: Default location for peripheral pin function. Alternate location can be selected using the APFCON register.
2: Alternate location for peripheral pin function selected by the APFCON register.
3: LVP support for PIC18(L)F1XK50 legacy designs.

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TABLE 3: 20-PIN ALLOCATION TABLE (PIC16(L)F1459)

I/O	20-Pin PDIP/SOIC/SSOP	20-Pin QFN	ADC	Reference	Comparator	Timer	CWG	USB	EUSART	PWM	MSSP	Interrupt	Basic
RA0	19	16	—	—	—	—	—	D+	—	—	—	IOC	ICSPDAT(3)
RA1	18	15	—	—	—	—	—	D-	—	—	—	IOC	ICSPCLK(3)
RA2	—	—	—	—	—	—	—	—	—	—	—	—	—
RA3	4	1	—	—	—	T1G(2)	—	—	—	—	$\overline{SS}$(2)	IOC	$\overline{MCLR}$ V_{PP}
RA4	3	20	AN3	—	—	SOSCO T1G(1)	—	—	—	—	—	IOC	OSC2 CLKOUT CLKR(1)
RA5	2	19	—	—	—	SOSCI T1CKI	—	—	—	—	—	IOC	OSC1 CLKIN
RB4	13	10	AN10	—	—	—	—	—	—	—	SDA SDI	IOC	—
RB5	12	9	AN11	—	—	—	—	—	RX DX	—	—	IOC	—
RB6	11	8	—	—	—	—	—	—	—	—	SCL SCK	IOC	—
RB7	10	7	—	—	—	—	—	—	TX CK	—	—	IOC	—
RC0	16	13	AN4	V_{REF+}	C1IN+ C2IN+	—	—	—	—	—	—	—	ICSPDAT
RC1	15	12	AN5	—	C1IN1- C2IN1-	—	$\overline{CWGFLT}$	—	—	—	—	INT	ICSPCLK
RC2	14	11	AN6	DACOUT1	C1IN2- C2IN2-	—	—	—	—	—	—	—	—
RC3	7	4	AN7	DACOUT2	C1IN3- C2IN3-	—	—	—	—	—	—	—	CLKR(2)
RC4	6	3	—	—	C1OUT C2OUT	—	CWG1B	—	—	—	—	—	—
RC5	5	2	—	—	—	T0CKI	CWG1A	—	—	PWM1	—	—	—
RC6	8	5	AN8	—	—	—	—	—	—	PWM2	$\overline{SS}$(1)	—	—
RC7	9	6	AN9	—	—	—	—	—	—	—	SDO	—	—
V_{DD}	1	18	—	—	—	—	—	—	—	—	—	—	V_{DD}
V_{SS}	20	17	—	—	—	—	—	—	—	—	—	—	V_{SS}
V_{USB3V3}	17	14	—	—	—	—	—	V_{USB3V3}	—	—	—	—	—

Note 1: Default location for peripheral pin function. Alternate location can be selected using the APFCON register.
2: Alternate location for peripheral pin function selected by the APFCON register.
3: LVP support for PIC18(L)F1XK50 legacy designs.

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