Negative Low Voltage Hot Swap Controllers

FEATURES

- **Allows Safe Board Insertion and Removal from a Live Backplane**
- **Controls Supplies from 0V to –16V**
- **Adjustable Analog Current Limit With Circuit Breaker Timer**
- **Fast Response Time Limits Peak Fault Current**
- **Adjustable Soft-Start Current Limit**
- **Adjustable Timer with Drain Voltage Accelerated Response**
- Adjustable Undervoltage/Overvoltage Protection
- LTC4214-1: Latch Off After Fault
- LTC4214-2: Automatic Retry After Fault
- Available in the 10-Pin MSOP Package

APPLICATIONS

- Hot Board Insertion
- Electronic Circuit Breaker
- Negative Power Supply Control
- Central Office Switching
- High Availability Servers
- Disk Arrays
- Optical Networking/Switching
- ECL

DESCRIPTION

The LTC®4214 negative voltage Hot Swap™ controller allows a board to be safely inserted and removed from a live backplane. Output current is controlled by three stages of current limiting: a timed circuit breaker, active current limiting and a fast feedforward path that limits peak current under worst-case catastrophic fault conditions.

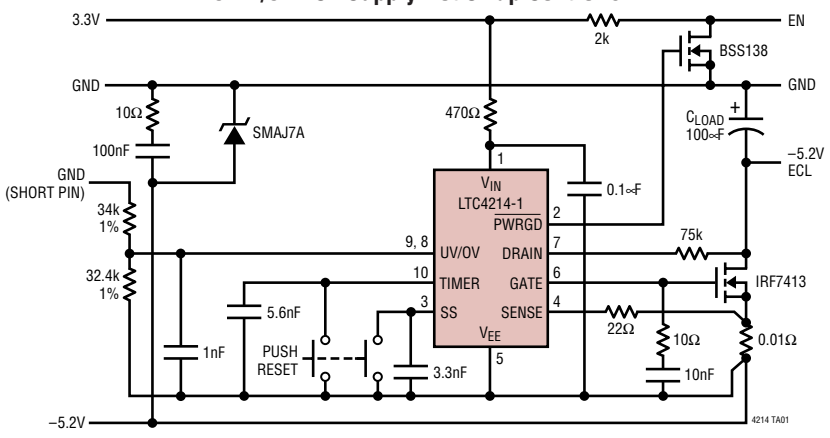
Adjustable undervoltage and overvoltage detectors disconnect the load whenever the input supply exceeds the desired operating range. The LTC4214 controls negative supplies ranging from near zero to –16V. A multifunction timer delays initial start-up and controls the circuit breaker's response time. This response time is accelerated by sensing excessive MOSFET drain voltage, keeping the MOSFET within its safe operating area (SOA). An adjustable soft-start circuit controls MOSFET inrush current at start-up. A power good status output can enable a power module at start-up or disable it if the circuit breaker trips.

The LTC4214-1 latches off after a circuit breaker fault times out. The LTC4214-2 provides automatic retry after a fault. The LTC4214 is available in the 10-pin MSOP package.

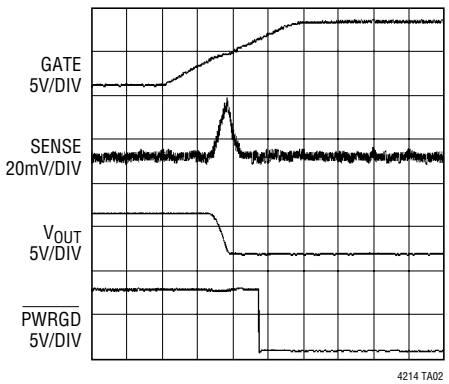
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Hot Swap is a trademark of Linear Technology Corporation.

TYPICAL APPLICATION

–5.2V/5A ECL Supply Hot Swap Controller



Start-Up Behavior

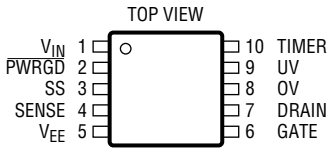


ABSOLUTE MAXIMUM RATINGS

All Voltages Referred to V_{EE} (Note 1)

V_{IN} ..... –0.3V to 17V
Input/Output Pins
(Except SENSE and DRAIN) Voltage .....–0.3V to 17V
SENSE Pin Voltage ..... –0.6V to 17V
Current Out of SENSE Pin (20µs Pulse)..... –200mA
DRAIN Pin Minimum Voltage ..... –0.3V
Current into DRAIN Pin (100µs Pulse) 5mA
Maximum Junction Temperature ..... 125°C
Operating Temperature Range
LTC4214-1C/LTC4214-2C ..... 0°C to 70°C
LTC4214-1I/LTC4214-2I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



MS PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 160°C/W

ORDER PART NUMBER
LTC4214-1CMS LTC4214-2CMS LTC4214-1IMS LTC4214-2IMS
MS PART MARKING
LTABH LTABK LTABJ LTABL

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, UV = OV = 2.5V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Supply Voltage		●	6		16	V
I_{IN}	V_{IN} Supply Current	UV = OV = 2.5V	●		0.8	2	mA
V_{LKO}	V_{IN} Undervoltage Lockout	Coming Out of UVLO (Rising V_{IN})	●		5.1	5.6	V
V_{LKH}	V_{IN} Undervoltage Lockout Hysteresis				0.3		V
V_{CB}	Circuit Breaker Current Limit Voltage	$V_{CB} = (V_{SENSE} – V_{EE})$	●	44	50	56	mV
V_{ACL}	Analog Current Limit Voltage	$V_{ACL} = (V_{SENSE} – V_{EE})$, SS = Open	●	60	70	80	mV
V_{FCL}	Fast Current Limit Voltage	$V_{FCL} = (V_{SENSE} – V_{EE})$	●	150	200	300	mV
V_{SS}	SS Voltage	After End of SS Timing Cycle			1.6		V
R_{SS}	SS Output Impedance				73		kΩ
I_{SS}	SS Pin Current	UV = OV = 2.5V, $V_{SENSE} = V_{EE}$, V_{SS} = 0V (Sourcing) UV = OV = 0V, $V_{SENSE} = V_{EE}$, V_{SS} = 1V (Sinking)			–22 14		µA mA
V_{OS}	Analog Current Limit Offset Voltage				10		mV
$\frac{V_{ACL}+V_{OS}}{V_{SS}}$	Ratio ($V_{ACL} + V_{OS}$) to SS Voltage				0.05		V/V
I_{GATE}	GATE Pin Output Current	$V_{SENSE} = V_{EE}$, V_{GATE} = 0V (Sourcing) $V_{SENSE} – V_{EE}$ = 0.15V, V_{GATE} = 3V (Sinking) $V_{SENSE} – V_{EE}$ = 0.3V, V_{GATE} = 1V (Sinking)	●	–30	–50 17 190	–70	µA mA mA
V_{GATE}	External MOSFET Gate Drive	$V_{GATE} – V_{EE}$	●	10	11	12	V
V_{GATEH}	Gate High Threshold	$V_{GATEH} = V_{IN} – V_{GATE}$ for $\overline{PWRGD}$ Status			2.8		V
V_{GATEL}	Gate Low Threshold	(Before Gate Ramp-Up)			0.5		V
V_{UVHI}	UV Pin Threshold	UV Rising	●	2.137	2.25	2.363	V
V_{UVHST}	UV Pin Hysteresis		●	0.22	0.25	0.28	V
V_{OVHI}	OV Pin Threshold	OV Rising	●	2.85	3	3.15	V
V_{OVHST}	OV Pin Hysteresis		●	0.12	0.15	0.18	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, UV = OV = 2.5V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SENSE}	SENSE Pin Input Current	V_{SENSE} = 50mV	●		–15	–30	µA
I_{INP}	UV, OV Pin Input Current	UV = OV = 2.5V	●		±0.1	±1	µA
V_{TMRH}	TIMER Pin Voltage High Threshold				3		V
V_{TMRL}	TIMER Pin Voltage Low Threshold				1.7		V
I_{TMR}	TIMER Pin Current	Timer On (Initial Cycle/Latchoff/ Shutdown Cooling, Sourcing), V_{TMR} = 2.2V			–5		µA
		Timer Off (Initial Cycle, Sinking), V_{TMR} = 2.2V			28		mA
		Timer On (Circuit Breaker, Sourcing, I_{DRN} = 0µA), V_{TMR} = 2.2V			–40		µA
		Timer On (Circuit Breaker, Sourcing, I_{DRN} = 20µA), V_{TMR} = 2.2V			–200		µA
		Timer Off (Circuit Breaker/ Shutdown Cooling, Sinking), V_{TMR} = 2.2V			5		µA
$\frac{\Delta I_{TMRACC}}{\Delta I_{DRN}}$	$\frac{[(I_{TMR} \text{ at } I_{DRN} = 20\mu A) - (I_{TMR} \text{ at } I_{DRN} = 0\mu A)]}{20\mu A}$	Timer On (Circuit Breaker with I_{DRN} = 20µA)			8		µA/µA
V_{DRNL}	DRAIN Pin Voltage Low Threshold	For $\overline{PWRGD}$ Status	●	1.109	1.232	1.355	V
I_{DRNL}	DRAIN Leakage Current	V_{DRAIN} = 2.5V			±0.1	±1	µA
V_{DRNCL}	DRAIN Pin Clamp Voltage	I_{DRN} = 20µA		3.5	4.2	5	V
V_{PGL}	$\overline{PWRGD}$ Output Low Voltage	I_{PG} = 1.6mA I_{PG} = 5mA	● ●		0.2	0.4 1.1	V V
I_{PGH}	$\overline{PWRGD}$ Pull-Up Current	$V_{\overline{PWRGD}}$ = 0V (Sourcing)	●	–30	–50	–70	µA
t_{SS}	SS Default Ramp Period	SS Pin Floating, V_{SS} Ramps from 0.2V to 1.4V			130		µs
t_{PLLUG}	UV Low to Gate Low				0.4		µs
t_{PHLOG}	OV High to Gate Low				0.4		µs

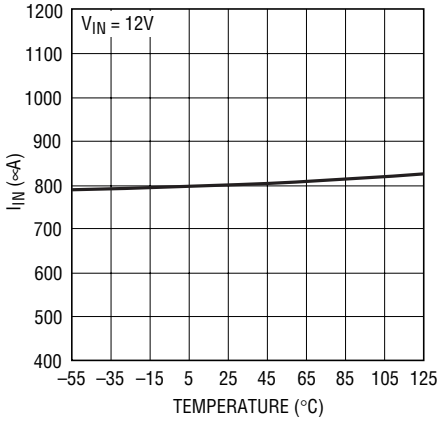
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to V_{EE} unless otherwise specified.

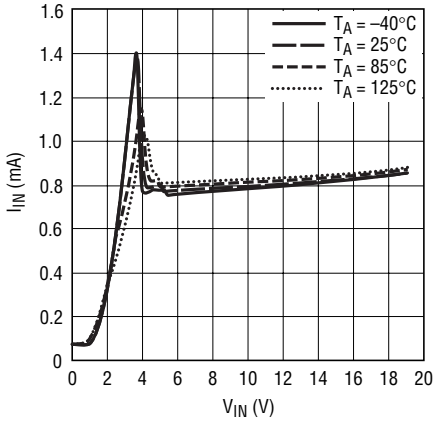
TYPICAL PERFORMANCE CHARACTERISTICS

All voltages are referenced to V_{EE} Unless otherwise specified.

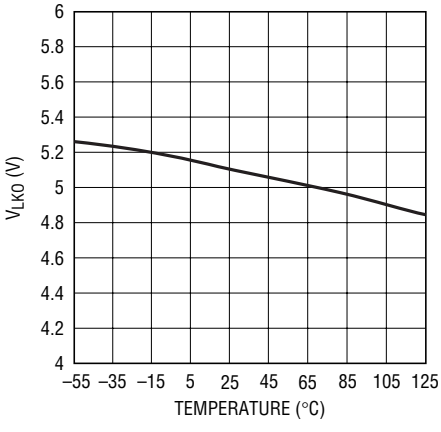
I_{IN} vs Temperature



I_{IN} vs V_{IN}



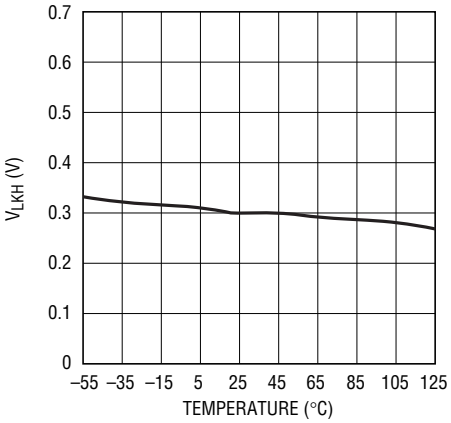
Undervoltage Lockout V_{LKO} vs Temperature



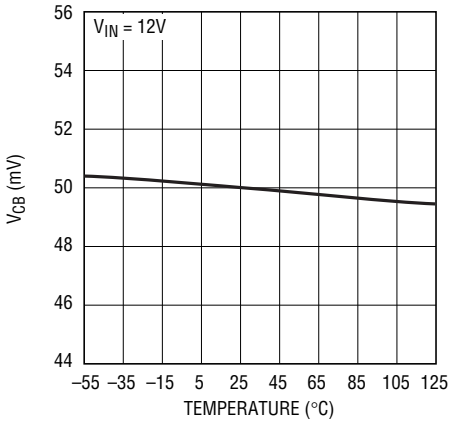
TYPICAL PERFORMANCE CHARACTERISTICS

All voltages are referenced to V_{EE} Unless otherwise specified.

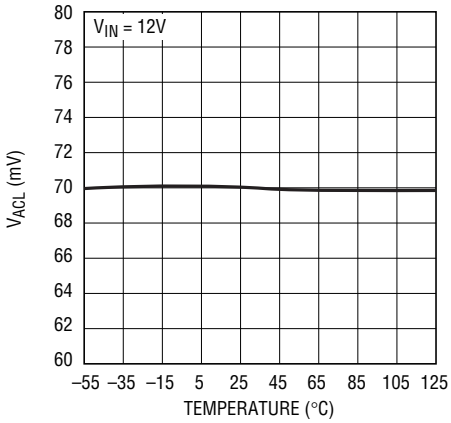
Undervoltage Lockout Hysteresis V_{LKH} vs Temperature



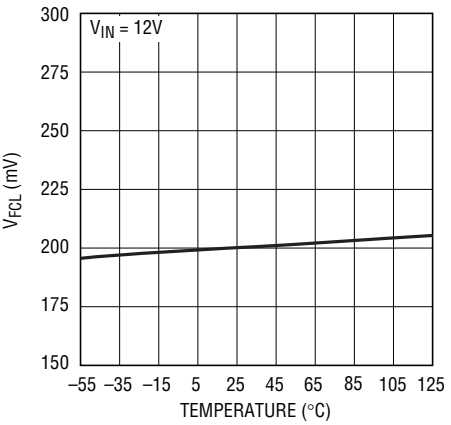
Circuit Breaker Current Limit Voltage V_{CB} vs Temperature



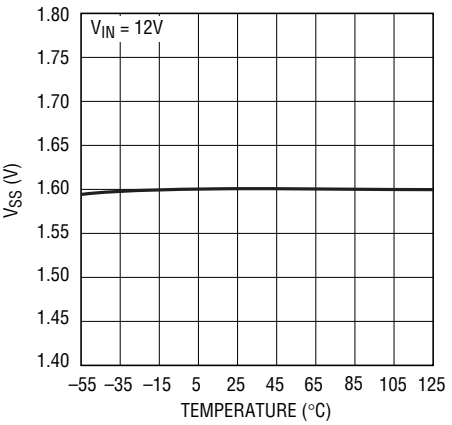
Analog Current Limit Voltage V_{ACL} vs Temperature



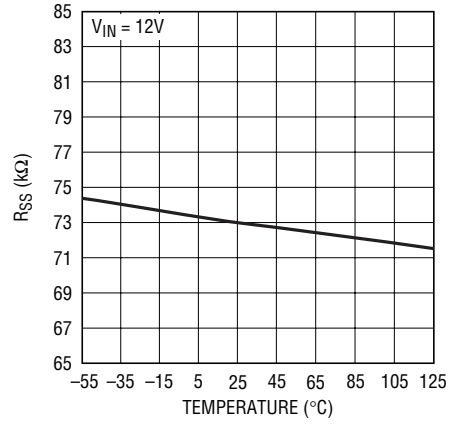
Fast Current Limit Voltage V_{FCL} vs Temperature



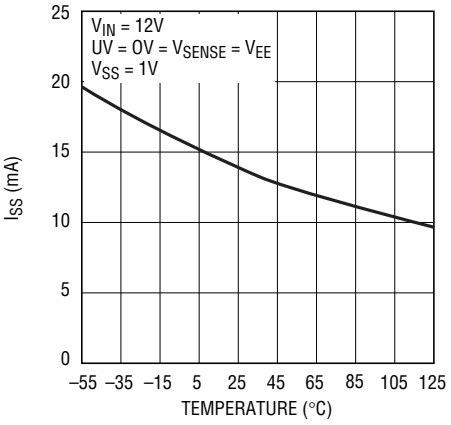
V_{SS} vs Temperature



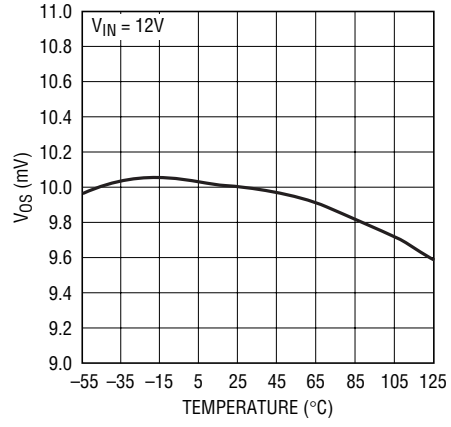
R_{SS} vs Temperature



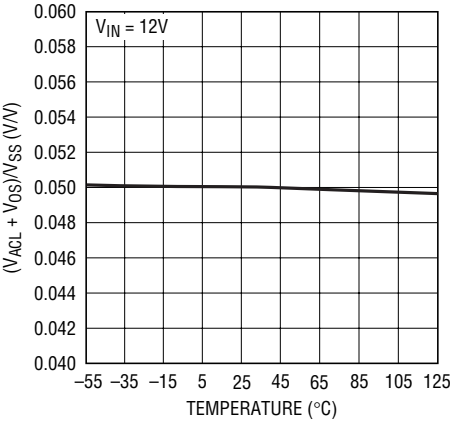
I_{SS} (Sinking) vs Temperature



V_{OS} vs Temperature



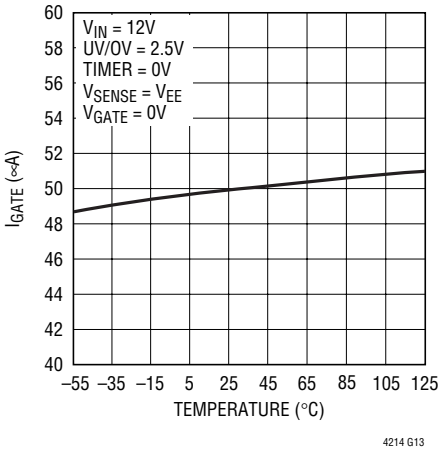
$(V_{ACL} + V_{OS})/V_{SS}$ vs Temperature



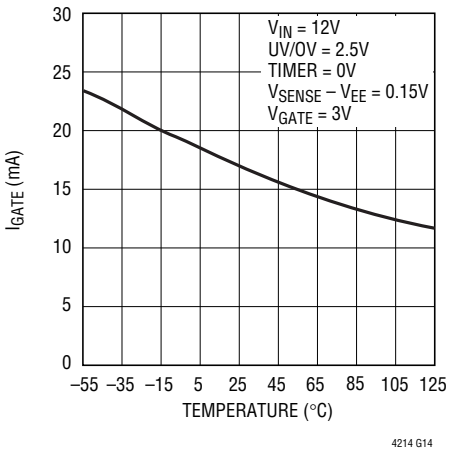
TYPICAL PERFORMANCE CHARACTERISTICS

All voltages are referenced to V_{EE} Unless otherwise specified.

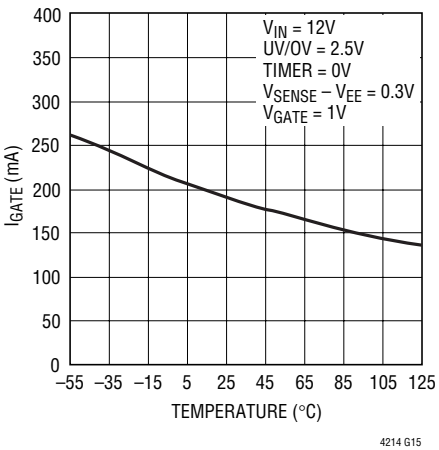
I_{GATE} (Sourcing) vs Temperature



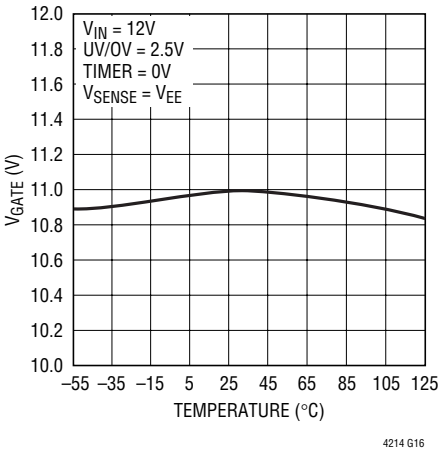
I_{GATE} (ACL, Sinking) vs Temperature



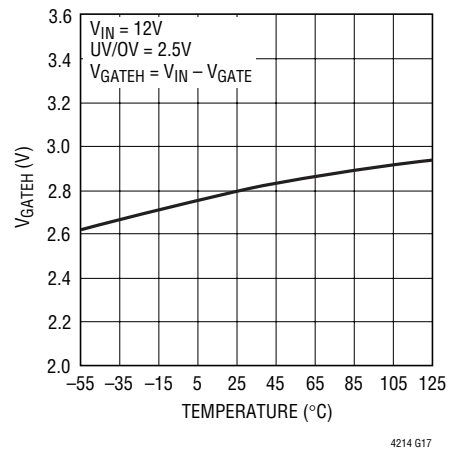
I_{GATE} (FCL, Sinking) vs Temperature



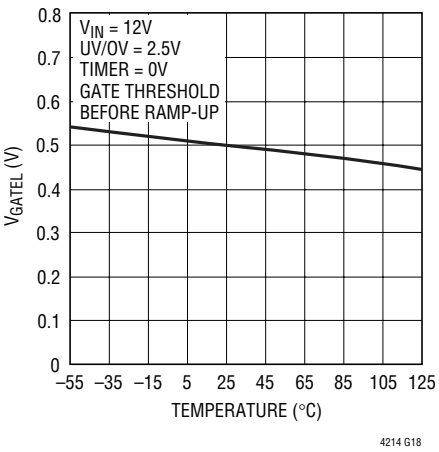
V_{GATE} vs Temperature



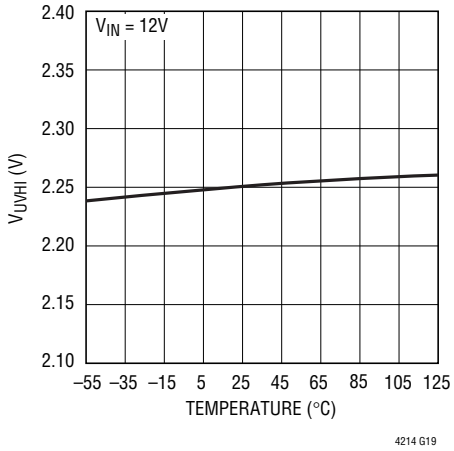
V_{GATEH} vs Temperature



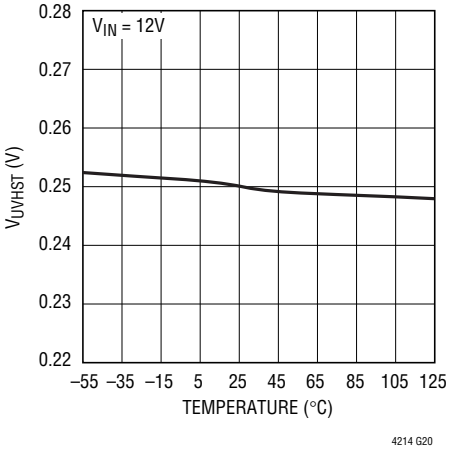
V_{GATEL} vs Temperature



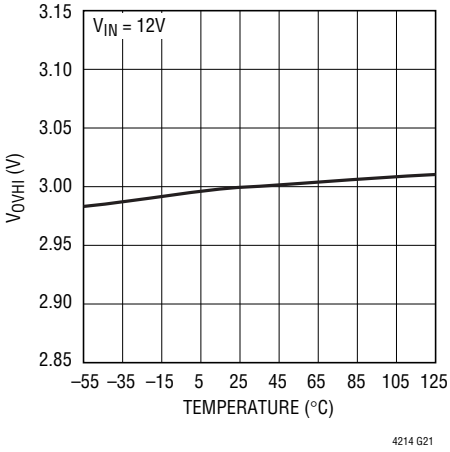
V_{UVHI} vs Temperature



V_{UVHST} vs Temperature



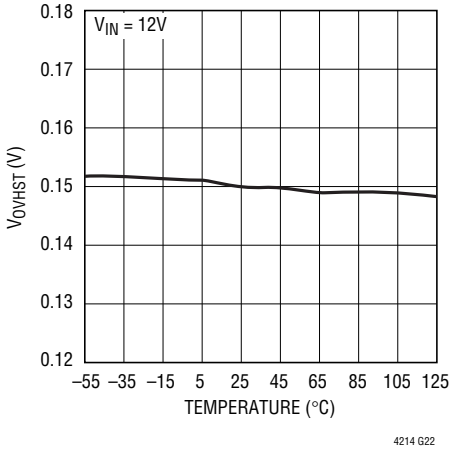
V_{OVHI} vs Temperature



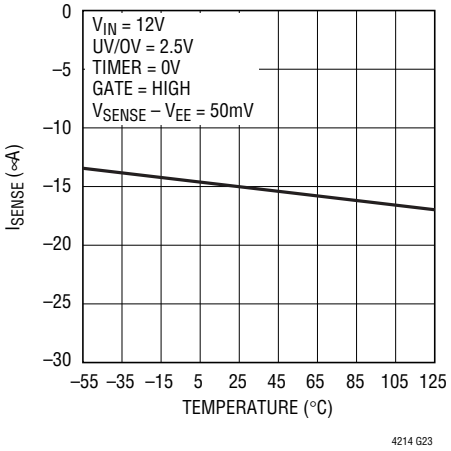
TYPICAL PERFORMANCE CHARACTERISTICS

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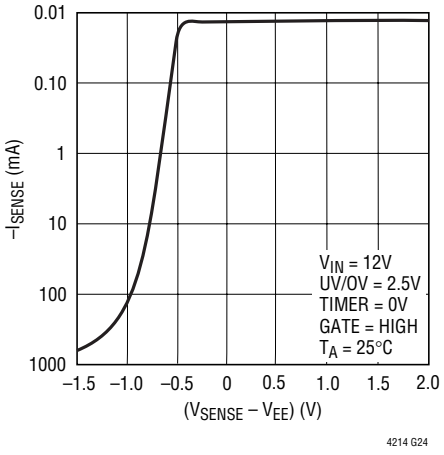
V_{OVHST} vs Temperature



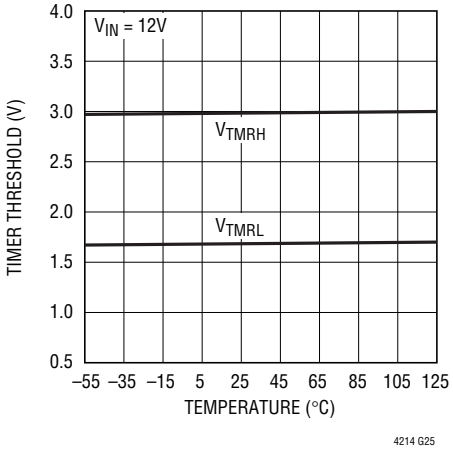
I_{SENSE} vs Temperature



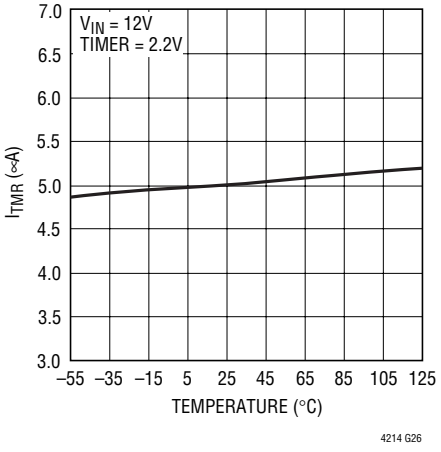
I_{SENSE} vs (V_{SENSE} – V_{EE})



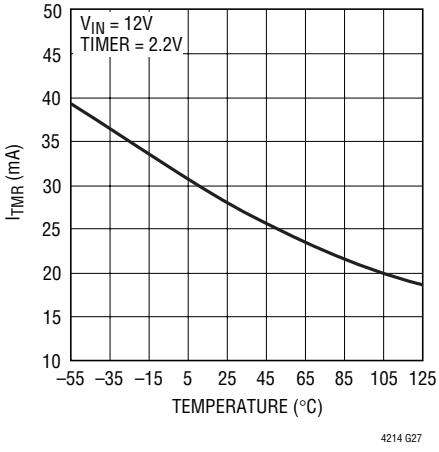
TIMER Threshold vs Temperature



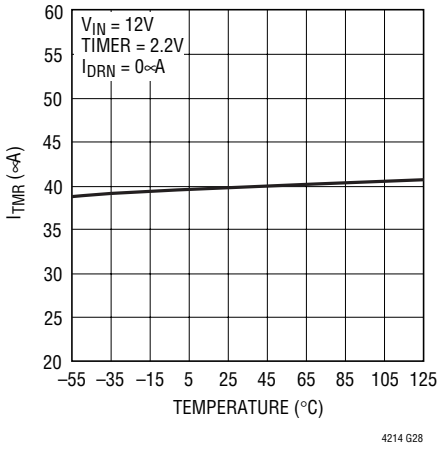
I_{TMR} (Initial Cycle, Sourcing) vs Temperature



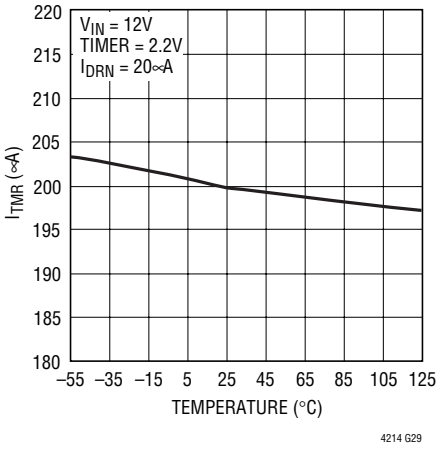
I_{TMR} (Initial Cycle, Sinking) vs Temperature



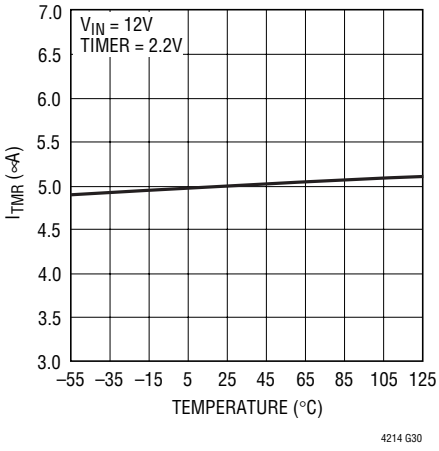
I_{TMR} (Circuit Breaker, Sourcing) vs Temperature



I_{TMR} (Circuit Breaker, I_{DRN} = 20μA, Sourcing) vs Temperature



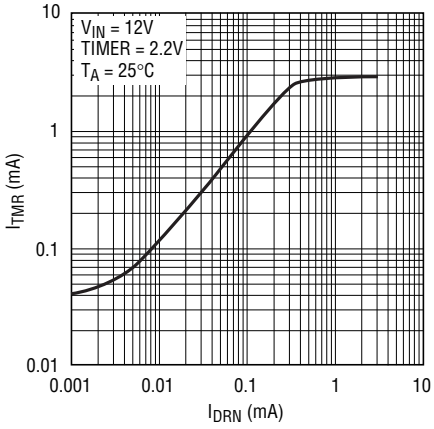
I_{TMR} (Cooling Cycle, Sinking) vs Temperature



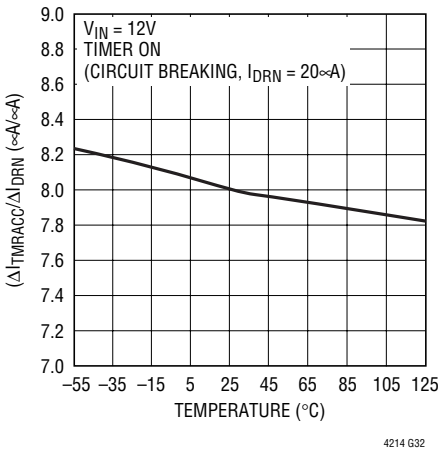
TYPICAL PERFORMANCE CHARACTERISTICS

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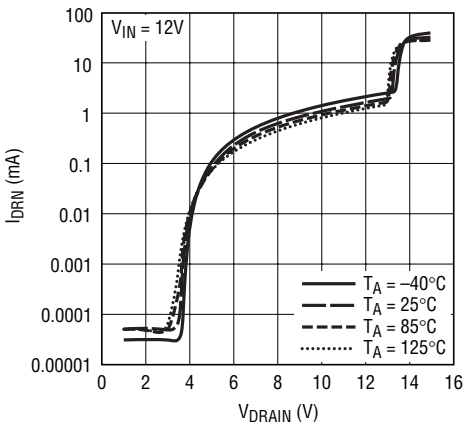
I_{TMR} (Circuit Breaker, Sourcing) vs I_{DRN}



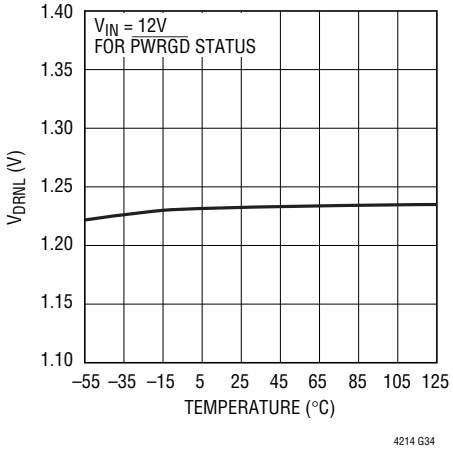
$\Delta I_{TMRACC}/\Delta I_{DRN}$ vs Temperature



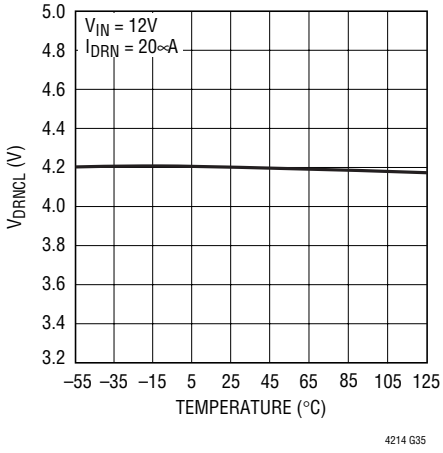
I_{DRN} vs V_{DRAIN}



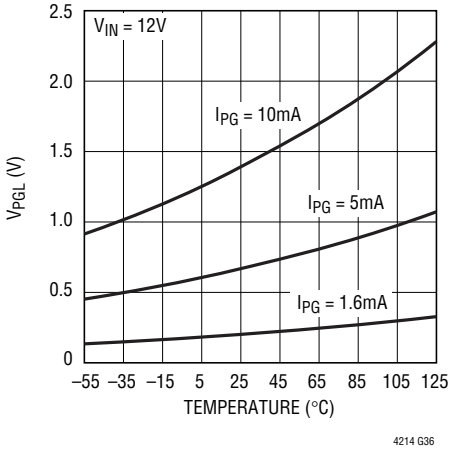
V_{DRNL} vs Temperature



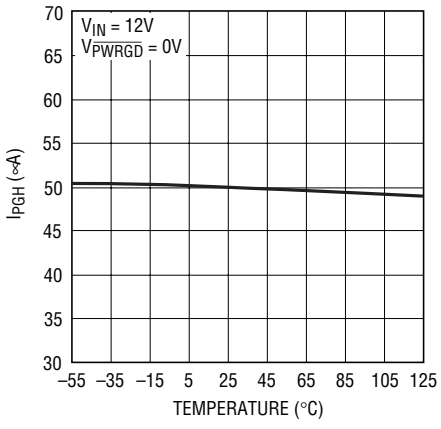
V_{DRNCL} vs Temperature



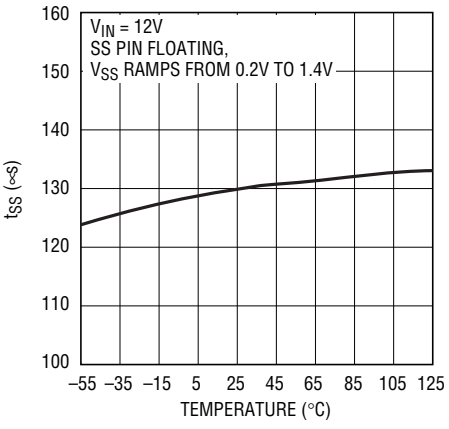
V_{PGL} vs Temperature



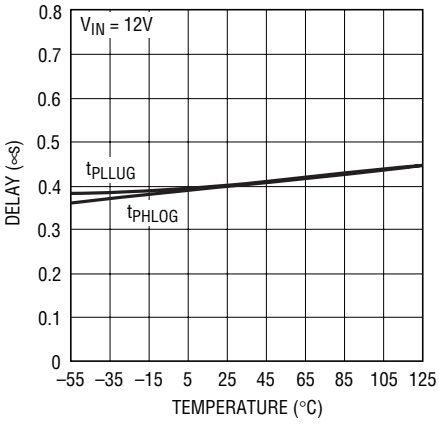
I_{PGH} (Sourcing) vs Temperature



t_{SS} vs Temperature



t_{PLLUG} and t_{PHLOG} vs Temperature



PIN FUNCTIONS

V_{IN} (Pin 1): Positive Supply Input. Connect this pin to the positive side of the supply via a resistor. An internal undervoltage lockout (UVLO) circuit holds GATE low until the V_{IN} pin is greater than V_{LKO} (5.1V), overriding UV and OV. If UV is high, OV is low and V_{IN} comes out of UVLO, TIMER starts an initial timing cycle before initiating a GATE ramp-up. If V_{IN} drops below approximately 4.8V, GATE pulls low immediately.

$\overline{\text{PWRGD}}$ (Pin 2): Power Good Status Output. At start-up, $\overline{\text{PWRGD}}$ latches low if DRAIN is below 1.232V and GATE is within 2.8V of V_{IN}. $\overline{\text{PWRGD}}$ status is reset by UV, V_{IN} (UVLO) or a circuit breaker fault timeout. This pin is internally pulled high by a 50µA current source.

SS (Pin 3): Soft-Start Pin. This pin is used to ramp inrush current during start up, thereby effecting control over di/dt. A 20x attenuated version of the SS pin voltage is presented to the current limit amplifier. This attenuated voltage limits the MOSFET's drain current through the sense resistor during the soft-start current limiting. At the beginning of a start-up cycle, the SS capacitor (C_{SS}) is ramped by a 22µA current source. The GATE pin is held low until SS exceeds 20 • V_{OS} = 0.2V. SS is internally shunted by a 73k resistor (R_{SS}) which limits the SS pin voltage to 1.6V. This corresponds to an analog current limit SENSE voltage of 70mV. If the SS capacitor is omitted, the SS pin ramps from 0V to 1.6V in about 220µs. The SS pin is pulled low under any of the following conditions: in UVLO, in an undervoltage condition, in an overvoltage condition, during the initial timing cycle or when the circuit breaker fault times out.

SENSE (Pin 4): Circuit Breaker/Current Limit Sense Pin. Load current is monitored by a sense resistor R_S connected between SENSE and V_{EE}, and controlled in three steps. If SENSE exceeds V_{CB} (50mV), the circuit breaker comparator activates a (40µA + 8 • I_{DRN}) TIMER pull-up current. If SENSE exceeds V_{ACL} (70mV), the analog current limit amplifier pulls GATE down to regulate the MOSFET current at V_{ACL}/R_S. In the event of a catastrophic short-circuit, SENSE may overshoot 70mV. If SENSE reaches V_{FCL} (200mV), the fast current limit comparator pulls GATE low with a strong pull-down. To disable the circuit breaker and current limit functions, connect SENSE to V_{EE}.

V_{EE} (Pin 5): Negative Supply Voltage Input. Connect this pin to the negative side of the power supply.

GATE (Pin 6): N-Channel MOSFET Gate Drive Output. This pin is pulled high by a 50µA current source. GATE is pulled low by invalid conditions at V_{IN} (UVLO), UV, OV, or a circuit breaker fault timeout. GATE is actively servoed to control the fault current as measured at SENSE. A compensation capacitor at GATE stabilizes this loop. A comparator monitors GATE to ensure that it is low before allowing an initial timing cycle, GATE ramp-up after an overvoltage event or restart after a current limit fault. During GATE start-up, a second comparator detects if GATE is within 2.8V of V_{IN} before $\overline{\text{PWRGD}}$ is set.

DRAIN (Pin 7): Drain Sense Input. DRAIN measures the drain-source voltage of the external N-channel MOSFET switch for two purposes: first, a comparator detects when V_{DS} < 1.232V and together with the GATE high comparator, controls the status of the $\overline{\text{PWRGD}}$ output. Second, if V_{DS} is greater than the DRAIN clamp of approximately 4.2V (V_{DRNCL}), the current through resistor R_D is multiplied by 8 and added to the TIMER's 40µA pull-up current during a circuit breaker fault cycle. This reduces the fault time and MOSFET heating under conditions of high dissipation.

OV (Pin 8): Overvoltage Input. The active high threshold at the OV pin is set at 3V with respect to V_{EE} and exhibits 0.15V hysteresis. If OV > 3V, GATE pulls low. When OV returns below 2.85V, GATE start-up begins without an initial timing cycle. If an overvoltage condition occurs in the middle of an initial timing cycle, the initial timing cycle is restarted after the overvoltage condition goes away. An overvoltage condition does not reset the $\overline{\text{PWRGD}}$ flag. The internal UVLO at V_{IN} always overrides OV. A 1nF to 10nF capacitor at OV prevents transients and switching noise from affecting the OV thresholds and prevents glitches at the GATE pin.

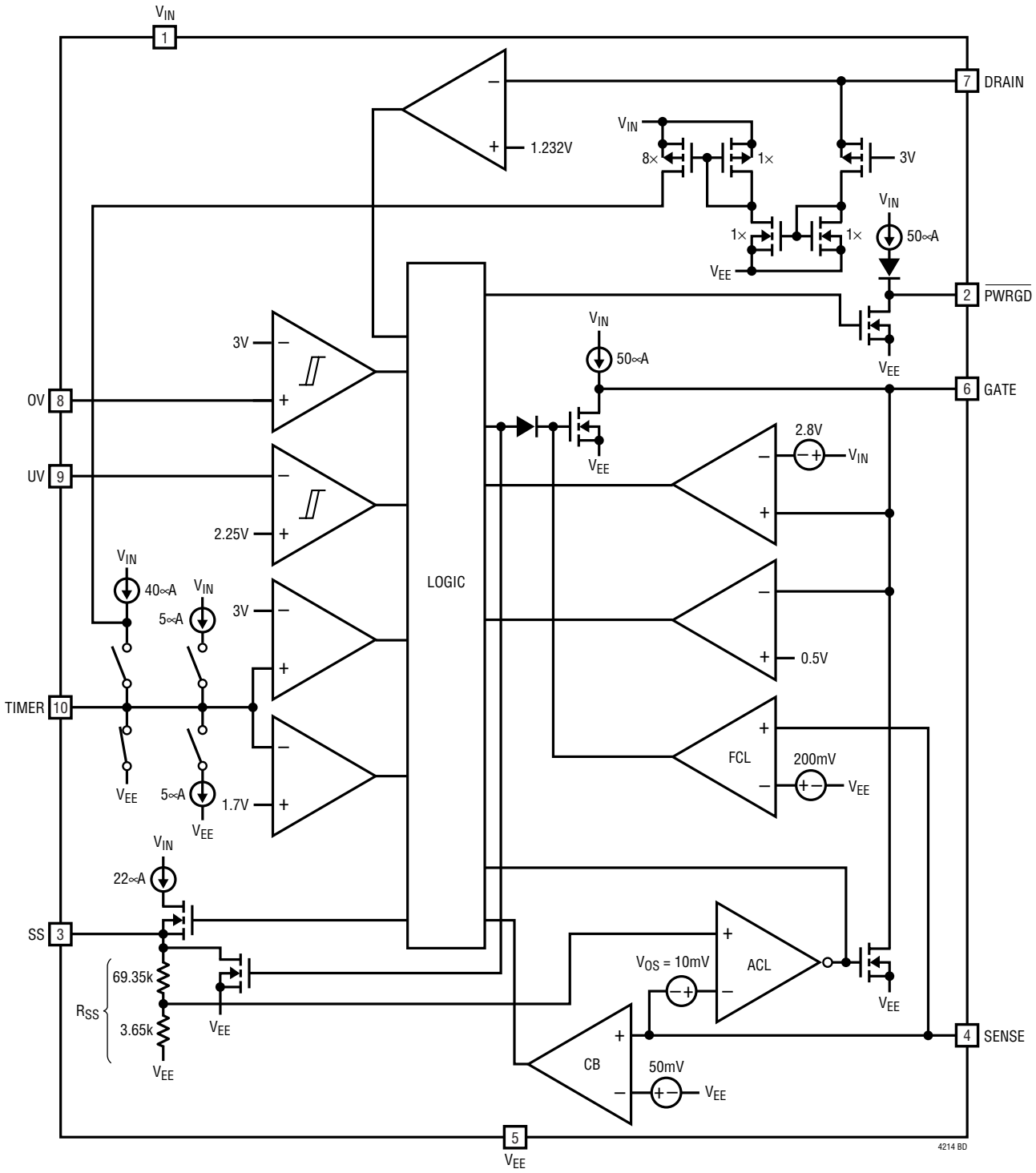
PIN FUNCTIONS

UV (Pin 9): Undervoltage Input. The active high threshold at the UV pin is set at 2.25V with respect to V_{EE} and exhibits 0.25V hysteresis. If UV < 2V, $\overline{PWRGD}$ pulls high, both GATE and TIMER pull low. If UV rises above 2.25V, this initiates an initial timing cycle followed by GATE start-up. The internal UVLO at V_{IN} always overrides UV. A low at UV resets an internal fault latch. A 1nF to 10nF capacitor at UV prevents transients and switching noise from affecting the UV thresholds and prevents glitches at the GATE pin.

TIMER (Pin 10): Timer Input. TIMER is used to generate an initial timing delay at start-up and to delay shutdown in the event of an output overload (circuit breaker fault). TIMER starts an initial timing cycle when the following conditions are met: UV is high, OV is low, V_{IN} clears UVLO, TIMER pin is low, GATE is lower than V_{GATEL}, SS < 0.2V, and $V_{SENSE} - V_{EE} < V_{CB}$. A pull-up current of 5μA then charges C_T, generating a time delay. If C_T charges to V_{TMRH} (3V), the timing cycle terminates, TIMER quickly pulls low and GATE is activated.

If SENSE exceeds 50mV while GATE is high, a circuit breaker cycle begins with a 40μA pull-up current charging C_T. If DRAIN is approximately 4.2V during this cycle, the timer pull-up has an additional current of $8 \bullet I_{DRN}$. If SENSE drops below 50mV before TIMER reaches 3V, a 5μA pull-down current slowly discharges the C_T. In the event that C_T eventually integrates up to the V_{TMRH} threshold, the circuit breaker trips, GATE quickly pulls low and $\overline{PWRGD}$ pulls high. The LTC4214-1 TIMER pin latches high with a 5μA pull-up source. This latched fault is cleared by either pulling TIMER low with an external device or by pulling UV below 2V. The LTC4214-2 starts a shutdown cooling cycle following an overcurrent fault. This cycle consists of 4 discharging ramps and 3 charging ramps. The charging and discharging currents are 5μA and TIMER ramps between its 1.7V and 3V thresholds. At the completion of a shutdown cooling cycle, the LTC4214-2 attempts a start-up cycle.

BLOCK DIAGRAM



OPERATION

Hot Circuit Insertion

When circuit boards are inserted into a live backplane, the supply bypass capacitors can draw huge transient currents from the power bus as they charge. The flow of current damages the connector pins and glitches the power bus, causing other boards in the system to reset. The LTC4214 is designed to turn on a circuit board supply in a controlled manner, allowing insertion or removal without glitches or connector damage.

Initial Start-Up

The LTC4214 resides on a removable circuit board and controls the path between the connector and the load with an external MOSFET switch (see Figure 1). Both inrush control and short-circuit protection are provided by the MOSFET.

A detailed schematic is shown in Figure 2. –12V and GND receive power through the longest connector pins and are the first to connect when the board is inserted. The GATE pin holds the MOSFET off during this time. UV/OV determines whether or not the MOSFET should be turned on based upon internal high accuracy thresholds and an external divider. UV/OV does double duty by also monitoring whether or not the connector is seated. The top of the divider detects GND by way of a short connector pin that is the last to mate during the insertion sequence.

Interlock Conditions

A start-up sequence commences once these "interlock" conditions are met.

1. The input voltage V_{IN} exceeds 5.1V (UVLO).
2. The voltage at UV > 2.25V.
3. The voltage at OV < 2.85V.
4. The (SENSE – V_{EE}) voltage is < 50mV (V_{CB}).
5. The voltage at SS is < 0.2V (20 • V_{OS}).
6. The voltage on the TIMER capacitor (C_T) is < 1.7V (V_{TMRL}).
7. The voltage at GATE is < 0.5V (V_{GATEL}).

The first three conditions are continuously monitored and the latter four are checked prior to initial timing or GATE ramp-up. Upon exiting an OV condition, the TIMER pin voltage requirement is inhibited. Details are described in the Applications Information, Timing Waveforms section.

TIMER begins the start-up sequence by sourcing 5µA into C_T. If V_{IN}, UV or OV falls out of range, the start-up cycle stops and TIMER discharges C_T to less than 1.7V, then waits until the aforementioned conditions are once again met. If C_T successfully charges to 3V, TIMER pulls low and both SS and GATE pins are released. GATE sources 50µA (I_{GATE}), charging the MOSFET gate and associated capacitance. The SS voltage ramp limits V_{SENSE} to control the inrush current. $\overline{PWRGD}$ pulls active low when GATE is within 2.8V of V_{IN} and DRAIN is lower than V_{DRNL}.

Two modes of operation are possible during the time the MOSFET is first turning on, depending on the values of external components, MOSFET characteristics and nominal design current. One possibility is that the MOSFET will

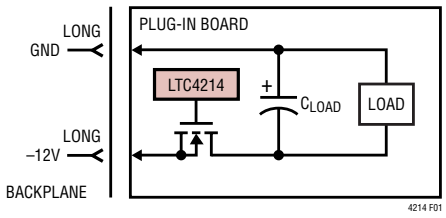


Figure 1. Basic LTC4214 Hot Swap Topology

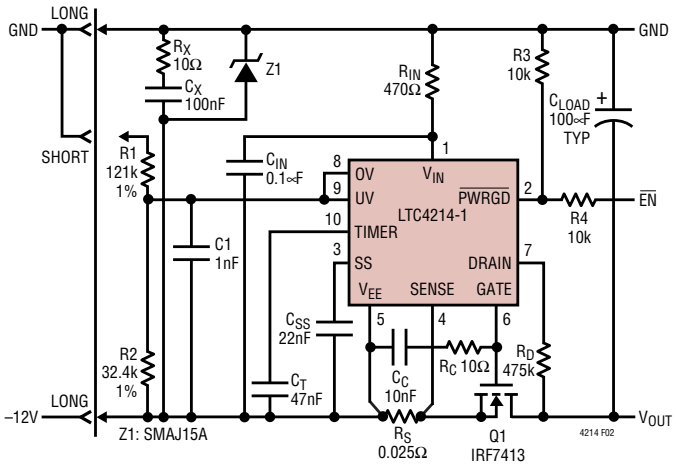


Figure 2. –12V, 2A Hot Swap Controller

OPERATION

turn on gradually so that the inrush into the load capacitance remains a low value. The output will simply ramp to –12V and the LTC4214 will fully enhance the MOSFET. A second possibility is that the load current exceeds the soft-start current limit threshold of $[V_{SS}(t)/20 – V_{OS}]/R_S$. In this case the LTC4214 will ramp the output by sourcing soft-start limited current into the load capacitance. If the soft-start voltage is below 1.2V, the circuit breaker TIMER is held low. Above 1.2V, TIMER ramps up. It is important to set the timer delay so that, regardless of which start-up mode is used, the TIMER ramp is less than one circuit breaker delay time. If this condition is not met, the LTC4214-1 may shut down after one circuit breaker delay time whereas the LTC4214-2 may continue to autoretry.

Board Removal

If the board is withdrawn from the card cage, the UV/OV divider is the first to lose connection. This shuts off the MOSFET and commutates the flow of current in the connector. When the power pins subsequently separate, there is no arcing.

Current Control

Three levels of protection handle short-circuit and overload conditions. Load current is monitored by SENSE and resistor R_S. There are three distinct thresholds at SENSE: 50mV for a timed circuit breaker function; 70mV for an analog current limit loop; and 200mV for a fast, feedforward comparator which limits peak current in the event of a catastrophic short-circuit.

If, owing to an output overload, the voltage drop across R_S exceeds 50mV, TIMER sources 40µA into C_T. C_T eventually charges to a 3V threshold and the LTC4214 shuts off. If the overload goes away before C_T reaches 3V and SENSE measures less than 50mV, C_T slowly discharges (5µA). In this way the LTC4214's circuit breaker function responds to low duty cycle overloads and accounts for fast heating and slow cooling characteristics of the MOSFET.

Higher overloads are handled by an analog current limit loop. If the drop across R_S reaches 70mV, the current limiting loop servos the MOSFET gate and maintains a constant output current of $70mV/R_S$. In current limit mode, V_{OUT} typically rises and this increases MOSFET heating. If $V_{OUT} > V_{DRNCL}$ (4.2V), connecting an external resistor, R_D, between V_{OUT} and DRAIN allows the fault timing cycle to be shortened by accelerating the charging of the TIMER capacitor. The TIMER pull-up current is increased by $8 \bullet I_{DRN}$. Note that because SENSE > 50mV, TIMER charges C_T during this time and the LTC4214 will eventually shut down.

Low impedance failures on the load side of the LTC4214 can produce high current slew rates. Under these conditions, overshoot is inevitable. A fast SENSE comparator with a threshold of 200mV detects overshoot and pulls GATE low much harder and hence much faster than the weaker current limit loop. The $70mV/R_S$ current limit loop then takes over and servos the current as previously described. As before, TIMER runs and shuts down the LTC4214 when C_T reaches 3V.

If C_T reaches 3V, the LTC4214-1 latches off with a 5µA pull-up current source whereas the LTC4214-2 starts a shutdown cooling cycle. The LTC4214-1 circuit breaker latch is reset by either pulling UV momentarily low or dropping the input voltage V_{IN} below the internal UVLO threshold of 4.8V or pulling TIMER momentarily low with a switch. The LTC4214-2 retries after its shutdown cooling cycle.

Although short-circuits are the most obvious fault type, several operating conditions may invoke overcurrent protection. Noise spikes from the backplane or load, transient currents caused by faults on adjacent circuit boards sharing the same power bus or the insertion of non-hot-swappable products could cause higher than anticipated input current and temporary detection of an overcurrent condition. The action of TIMER and C_T rejects these events allowing the LTC4214 to "ride out" temporary overloads and disturbances that could trip a simple current comparator and, in some cases, blow a fuse.

APPLICATIONS INFORMATION

SUPPLY VOLTAGE

The LTC4214 requires a (V_{IN} – V_{EE}) voltage of 6V to 16V to function. This can be derived from GND and –12V of a –12V system or the 3.3V and –5.2V of a –5.2V system. The positive supply is connected to V_{IN} via an RC network so that the LTC4214 can have a usable V_{IN} during load short or other transient events when (V_{IN} – V_{EE}) glitches below 6V.

INTERNAL UNDERVOLTAGE LOCKOUT (UVLO)

A hysteretic comparator, UVLO, monitors V_{IN} for undervoltage. The thresholds are defined by V_{LKO} and its hysteresis, V_{LKH}. When V_{IN} rises above 5.1V (V_{LKO}) the chip is enabled; below 4.8V (V_{LKO} – V_{LKH}) it is disabled and GATE is pulled low. The UVLO function at V_{IN} should not be confused with the UV/OV pins. These are completely separate functions.

UV/OV COMPARATORS

An UV hysteretic comparator detects undervoltage conditions at the UV pin, with the following thresholds:

UV low-to-high (V_{UVHI}) = 2.25V

UV high-to-low (V_{UVHI} – V_{UVHST}) = 2V

An OV hysteretic comparator detects overvoltage conditions at the OV pin, with the following thresholds:

OV low-to-high (V_{OVHI}) = 3V

OV high-to-low (V_{OVHI} – V_{OVHST}) = 2.85V

In Figure 2, a divider (R1-R2) is used to scale the supply voltage of 12V ±10%. Using R1 = 121k and R2 = 32.4k gives a typical operating range of 10.7V to 13.5V. The under and overvoltage shutdown thresholds are then 9.5V to 14.2V. 1% divider resistors are recommended to preserve threshold accuracy.

The R1-R2 divider values shown in Figure 2 set a standing current of slightly more than 75µA and define an impedance at UV/OV of 25kΩ. In most applications, 25kΩ impedance coupled with 250mV UV hysteresis makes the LTC4214 insensitive to noise. If more noise immunity is desired, add a 1nF to 10nF filter capacitor from UV/OV to V_{EE}.

Separate UV and OV pins can be used for a wider operating range such as 10V to 14V as shown in Figure 3. Other combinations are possible with different resistor arrangements.

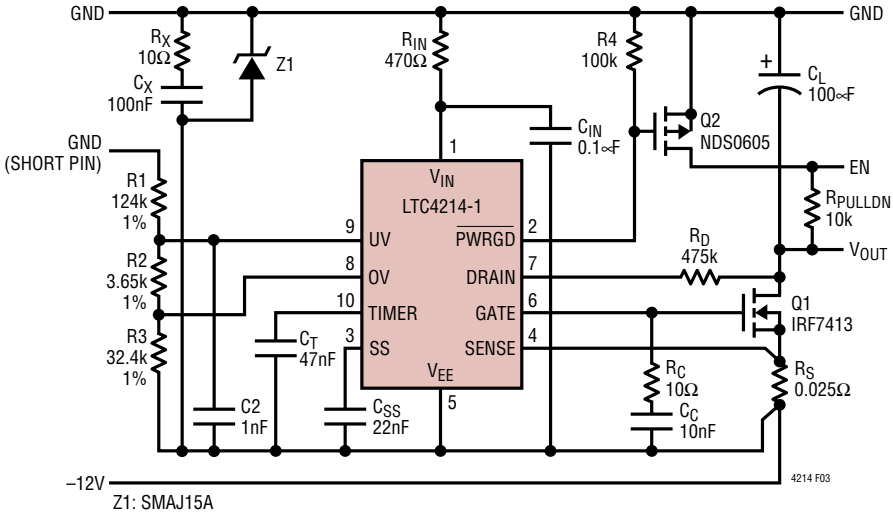


Figure 3. –12V/2A Application with Wider Input Operating Range

APPLICATIONS INFORMATION

UV/OV OPERATION

A low input to the UV comparator will reset the LTC4214 and pull the GATE and TIMER pins low. A low-to-high UV transition will initiate an initial timing sequence if the other interlock conditions are met. A high-to-low transition in the UV comparator immediately shuts down the LTC4214, pulls the MOSFET gate low and resets the latched $\overline{PWRGD}$ high.

Overvoltage conditions detected by the OV comparator will also pull GATE low, thereby shutting down the load. However, it will not reset the circuit breaker TIMER, $\overline{PWRGD}$ flag or shutdown cooling timer. Returning the supply voltage to an acceptable range restarts the GATE pin if all the interlock conditions except TIMER are met. Only during the initial timing cycle does an OV condition reset the TIMER.

DRAIN

Connecting an external resistor, R_D, to the dual function DRAIN pin allows V_{OUT} sensing without it being damaged by large voltage transients. Below 3V, negligible pin leakage allows a DRAIN low comparator to detect V_{OUT} less than 1.232V (V_{DRNL}). This condition, together with the GATE low comparator, sets the $\overline{PWRGD}$ flag.

If $V_{OUT} > V_{DRNCL}$ (4.2V), the DRAIN pin is clamped at about 4.2V and the current flowing in R_D is given by:

$$I_{DRN} \approx \frac{V_{OUT} - V_{DRNCL}}{R_D} \quad (1)$$

This current is scaled up 8 times during a circuit breaker fault and is added to the nominal 40µA TIMER current. This accelerates the fault TIMER pull-up when the MOSFET's drain-source voltage exceeds 4.2V and effectively shortens the MOSFET heating duration.

TIMER

The operation of the TIMER pin is somewhat complex as it handles several key functions. A capacitor C_T is used at TIMER to provide timing for the LTC4214. Four different charging and discharging modes are available at TIMER:

1) A 5µA slow charge; initial timing and shutdown cooling delay.

2) A (40µA + 8 • I_{DRN}) fast charge; circuit breaker delay.

3) A 5µA slow discharge; circuit breaker "cool off" and shutdown cooling.

4) Low impedance switch; resets the TIMER capacitor after an initial timing delay, in UVLO, in UV and in OV during initial timing.

For initial start-up, the 5µA pull-up is used. The low impedance switch is turned off and the 5µA current source is enabled when the interlock conditions are met. C_T charges to 3V in a time period given by:

$$t = \frac{3V \bullet C_T}{5\mu A} \quad (2)$$

When C_T reaches 3V (V_{TMRH}), the low impedance switch turns on and discharges C_T. A GATE start-up cycle begins and both SS and GATE are released.

CIRCUIT BREAKER TIMER OPERATION

If the SENSE pin detects more than a 50mV drop across R_S, the TIMER pin charges C_T with (40µA + 8 • I_{DRN}). If C_T charges to 3V, the GATE pin pulls low and the LTC4214-1 latches off while the LTC4214-2 starts a shutdown cooling cycle. The LTC4214-1 remains latched off until the UV pin is momentarily pulsed low or TIMER is momentarily discharged low by an external switch or V_{IN} dips below UVLO and is then restored. The circuit breaker timeout period is given by:

$$t = \frac{3V \bullet C_T}{40\mu A + 8 \bullet I_{DRN}} \quad (3)$$

If $V_{OUT} < 3V$, an internal PMOS device isolates any DRAIN pin leakage current, making I_{DRN} = 0µA in Equation (3). If $V_{OUT} > 4.2V$ (V_{DRNCL}) during the circuit breaker fault period, the charging of C_T accelerates by 8 • I_{DRN} of Equation (1).

Intermittent overloads may exceed the 50mV threshold at SENSE, but, if their duration is sufficiently short, TIMER will not reach 3V and the LTC4214 will not shut the external

APPLICATIONS INFORMATION

MOSFET off. To handle this situation, the TIMER discharges C_T slowly with a 5µA pull-down whenever the SENSE voltage is less than 50mV. Therefore, any intermittent overload with $V_{OUT} < 3V$ and an aggregate duty cycle of 12.5% or more will eventually trip the circuit breaker and shut down the LTC4214. Figure 4 shows the circuit breaker response time in seconds normalized to 1µF for $I_{DRN} = 0µA$. The asymmetric charging and discharging of C_T is a fair gauge of MOSFET heating.

The normalized circuit response time is estimated by

$$\frac{t}{C_T(\mu F)} = \frac{3}{\left[\left(40 + 8 \bullet I_{DRN}\right) \bullet D - 5\right]} \quad (4)$$

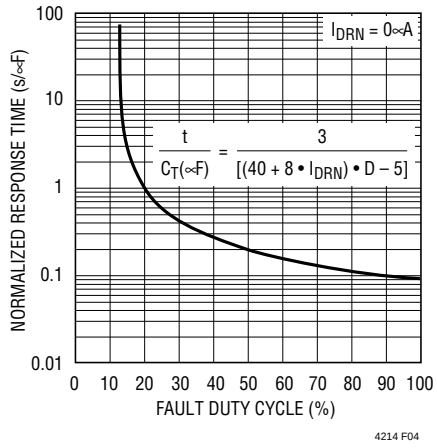


Figure 4. Circuit-Breaker Response Time

SHUTDOWN COOLING CYCLE

For the LTC4214-1 (latchoff version), TIMER latches high with a 5µA pull-up after the circuit breaker fault TIMER reaches 3V. For the LTC4214-2 (automatic retry version), a shutdown cooling cycle begins if TIMER reaches the 3V threshold. TIMER starts with a 5µA pull-down until it reaches the 1.7V threshold. Then, the 5µA pull-up turns back on until TIMER reaches the 3V threshold. Four 5µA pull-down cycles and three 5µA pull-up cycles occur between the 1.7V and 3V thresholds, creating a time interval given by:

$$t_{SHUTDOWN} = \frac{7 \bullet 1.3V \bullet C_T}{5\mu A} \quad (5)$$

At the 1.7V threshold of the last pull-down cycle, a GATE ramp-up is attempted.

SOFT-START

Soft-start limits the inrush current profile during GATE start-up. Unduly long soft-start intervals can exceed the MOSFET's SOA rating if powering up into an active load. If SS floats, an internal current source ramps SS from 0V to 1.6V in about 220µs. Connecting an external capacitor C_{SS} from SS to ground modifies the ramp to approximate an RC response of:

$$V_{SS}(t) \approx V_{SS} \bullet \left(1 - e^{\left(-\frac{t}{R_{SS} \bullet C_{SS}}\right)}\right) \quad (6)$$

An internal resistor divider (69.35k/3.65k) scales $V_{SS}(t)$ down by 20 times to give the analog current limit threshold:

$$V_{ACL}(t) = \frac{V_{SS}(t)}{20} - V_{OS} \quad (7)$$

This allows the inrush current to be limited to $V_{ACL}(t)/R_S$. The offset voltage, V_{OS} (10mV), ensures C_{SS} is sufficiently discharged and the ACL amplifier is in current limit before GATE start-up. SS is pulled low under any of the following conditions: in UVLO, in an undervoltage condition, in an overvoltage condition, during the initial timing cycle or when the circuit breaker fault times out.

APPLICATIONS INFORMATION

GATE

GATE is pulled low to V_{EE} under any of the following conditions: in UVLO, in an undervoltage condition, in an overvoltage condition, during the initial timing cycle or when the circuit breaker fault times out. When GATE turns on, a 50µA current source charges the MOSFET gate and any associated external capacitance. The gate drive is limited to no more than V_{IN}.

Gate-drain capacitance (C_{GD}) feedthrough at the first abrupt application of power can cause a gate-source voltage sufficient to turn on the MOSFET. A unique circuit pulls GATE low with practically no usable voltage at V_{IN} and eliminates current spikes at insertion. A large external gate-source capacitor is thus unnecessary for the purpose of compensating C_{GD}. Instead, a smaller value (≥ 5nF) capacitor C_C is adequate. C_C also provides compensation for the analog current limit loop.

GATE has two comparators: the GATE low comparator looks for < 0.5V threshold prior to initial timing or a GATE start-up cycle; the GATE high comparator looks for < 2.8V relative to V_{IN} and, together with the DRAIN low comparator, sets $\overline{PWRGD}$ status during GATE start-up.

SENSE

The SENSE pin is monitored by the circuit breaker (CB) comparator, the analog current limit (ACL) amplifier and the fast current limit (FCL) comparator. Each of these three measures the potential of SENSE relative to V_{EE}. When SENSE exceeds 50mV, the CB comparator activates the 40µA TIMER pull-up. At 70mV, the ACL amplifier servos the MOSFET current and, at 200mV, the FCL comparator abruptly pulls GATE low in an attempt to bring the MOSFET current under control. If any of these conditions persists long enough for TIMER to charge C_T to 3V (see Equation 3), the LTC4214 shuts down and pulls GATE low.

If the SENSE pin encounters a voltage greater than 70mV, the ACL amplifier will servo GATE downwards in an attempt to control the MOSFET current. Since GATE overdrives the MOSFET in normal operation, the ACL amplifier needs time to discharge GATE to the threshold of the MOSFET. For a mild overload the ACL amplifier can control the MOSFET current, but in the event of a severe overload the current may overshoot. At SENSE = 200mV the FCL comparator takes over, quickly discharging the GATE pin to near V_{EE} potential. FCL then releases and the ACL amplifier takes over. All the while TIMER is running. The effect of FCL is to add a nonlinear response to the control loop in favor of reducing MOSFET current.

Owing to inductive effects in the system, FCL typically overcorrects the current limit loop and GATE undershoots. A zero in the loop (resistor R_C in series with the gate capacitor) helps the ACL amplifier to recover.

SHORT-CIRCUIT OPERATION

Circuit behavior arising from a load side low impedance short is shown in Figure 5 for the LTC4214. Initially, the current overshoots the fast current limit level of V_{SENSE} = 200mV (Trace 2) as the GATE pin works to bring V_{GS} under control (Trace 3). The overshoot glitches the backplane in the negative direction and when the current is reduced to 70mV/R_S, the backplane responds by glitching in the positive direction.

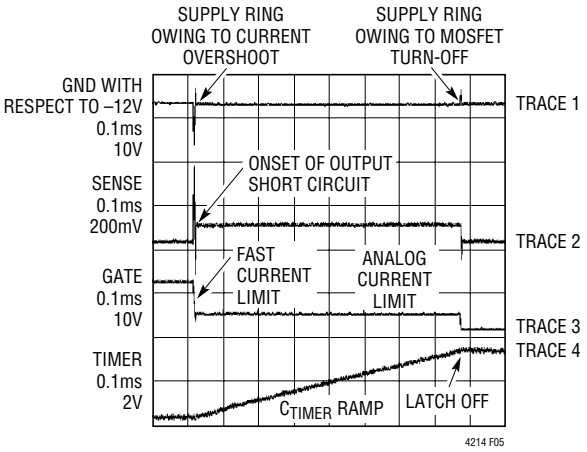


Figure 5. Output Short-Circuit Behavior of LTC4214

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TIMER commences charging C_T (Trace 4) while the analog current limit loop maintains the fault current at 70mV/R_S, which in this case is 3.5A (Trace 2). Note that the backplane voltage (Trace 1) sags under load. Timer pull-up is accelerated by V_{OUT}. When C_T reaches 3V, GATE turns off, $\overline{PWRGD}$ pulls high, the load current drops to zero and the backplane rings in the positive direction. The transient associated with the GATE turn off can be controlled with a snubber to reduce ringing and transient voltage suppressor to clip off large spikes. The choice of RC for the snubber is usually done experimentally. The value of the snubber capacitor is usually chosen between 10 to 100 times the MOSFET C_{OSS}. The value of the snubber resistor is typically between 3Ω to 100Ω. In many cases, a simple short-circuit test can be performed to determine the component values needed.

A low impedance short on one card may influence the behavior of others sharing the same backplane. The initial glitch and backplane sag as seen in Figure 5 Trace 1, can rob charge from output capacitors on adjacent cards. When the faulty card shuts down, current flows in to refresh the capacitors. If LTC4214s are used by the other cards, they respond by limiting the inrush current to a value of 70mV/R_S. If C_T is sized correctly, the capacitors will recharge long before C_T times out.

POWER GOOD, $\overline{PWRGD}$

$\overline{PWRGD}$ latches low if GATE charges up to within 2.8V of V_{IN} and DRAIN pulls below V_{DRNL} during start-up. $\overline{PWRGD}$ is reset in UVLO, in a UV condition or if C_T charges up to 3V. An overvoltage condition has no effect on $\overline{PWRGD}$ status. A 50µA current pulls this pin high during reset.

Various ways of using the $\overline{PWRGD}$ pin for interfacing with a Power Module load are shown in the Typical Application as well as Figures 2, 3, 18 and 19.

MOSFET SELECTION

The external MOSFET switch must have adequate safe operating area (SOA) to handle short-circuit conditions until TIMER times out. These considerations take precedence over DC current ratings. A MOSFET with adequate SOA for a given application can always handle the required current, but the opposite may not be true. Consult the manufacturer's MOSFET data sheet for safe operating area and effective transient thermal impedance curves.

MOSFET selection is a 3-step process by assuming the absense of a soft-start capacitor. First, R_S is calculated and then the time required to charge the load capacitance is determined. This timing, along with the maximum short-circuit current and maximum input voltage defines an operating point that is checked against the MOSFET's SOA curve.

To begin a design, first specify the required load current and load capacitance, I_L and C_L. The circuit breaker current trip point (V_{CB}/R_S) should be set to accommodate the maximum load current. Note that maximum input current to a DC/DC converter is expected at $V_{SUPPLY(MIN)}$. R_S is given by:

$$R_S = \frac{V_{CB(MIN)}}{I_{L(MAX)}} \quad (8)$$

where $V_{CB(MIN)}$ = 44mV represents the guaranteed minimum circuit breaker threshold.

During the initial charging process, the LTC4214 may operate the MOSFET in current limit, forcing (V_{ACL}) between 60mV to 80mV across R_S. The minimum inrush current is given by:

$$I_{INRUSH(MIN)} = \frac{60mV}{R_S} \quad (9)$$

Maximum short-circuit current limit is calculated using the maximum V_{SENSE}. This gives

$$I_{SHORTCIRCUIT(MAX)} = \frac{80mV}{R_S} \quad (10)$$

The TIMER capacitor C_T must be selected based on the slowest expected charging rate; otherwise TIMER might time out before the load capacitor is fully charged. A value

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for C_T is calculated based on the maximum time it takes the load capacitor to charge. That time is given by:

$$t_{CL(CHARGE)} = \frac{C \bullet V}{I} = \frac{C_L \bullet V_{SUPPLY(MAX)}}{I_{INRUSH(MIN)}} \quad (11)$$

The maximum current flowing in the DRAIN pin is given by:

$$I_{DRN(MAX)} = \frac{V_{SUPPLY(MAX)} - V_{DRNCL}}{R_D} \quad (12)$$

Approximating a linear charging rate as I_{DRN} drops from $I_{DRN(MAX)}$ to zero, the I_{DRN} component in Equation (3) can be approximated with $0.5 \bullet I_{DRN(MAX)}$. Rearranging equation, TIMER capacitor C_T is given by:

$$C_T = \frac{t_{CL(CHARGE)} \bullet \left(40\mu A + 4 \bullet I_{DRN(MAX)}\right)}{3V} \quad (13)$$

Returning to Equation (3), the TIMER period is calculated and used in conjunction with $V_{SUPPLY(MAX)}$ and $I_{SHORTCIRCUIT(MAX)}$ to check the SOA curves of a prospective MOSFET.

As a numerical design example, consider a 10W load, which requires 1.1A input current at –10.8V. If $V_{SUPPLY(MAX)}$ = 13.2V and C_L = 100µF, R_D = 475k, Equation (8) gives R_S = 40mΩ; Equation (13) gives C_T = 34nF. To account for errors in R_S, C_T, TIMER current (40µA), TIMER threshold (3V), R_D, DRAIN current multiplier and DRAIN voltage clamp (V_{DRNCL}), the calculated value should be multiplied by 1.5, giving the nearest standard value of C_T = 56nF.

If a short-circuit occurs, a current of up to 80mV/40mΩ = 2A will flow in the MOSFET for 0.9ms as dictated by C_T = 56nF in Equation (3). The MOSFET must be selected based on this criterion. The IRF7413 can handle 20V and 2A for 9ms and is safe to use in this application.

Computing the maximum soft-start capacitor value during soft-start to a load short is complicated by the nonlinear MOSFET's SOA characteristics and the $R_{SS}C_{SS}$ response. An overly conservative but simple approach begins with the maximum circuit breaker current, given by:

$$I_{CB(MAX)} = \frac{56mV}{R_S} \quad (14)$$

From the SOA curves of a prospective MOSFET, determine the time allowed, $t_{SOA(MAX)}$. C_{SS} is given by:

$$C_{SS} = \frac{t_{SOA(MAX)}}{1.61 \bullet R_{SS}} \quad (15)$$

In the above example, 56mV/40mΩ gives 1.4A. $t_{SOA(MAX)}$ for the IRF7413 is 8ms for 1.4A at 30V. From Equation (15), C_{SS} = 68nF. Actual board evaluation showed that C_{SS} = 33nF was appropriate. The ratio ($R_{SS} \bullet C_{SS}$) to $t_{CL(CHARGE)}$ is a good gauge as a large ratio may result in the time-out period expiring. This gauge is determined empirically with board level evaluation.

SUMMARY OF DESIGN FLOW

To summarize the design flow, consider the application shown in Figure 2. It was designed for 12W for a –10V to –14V supply.

Calculate the maximum load current: 12W/10V = 1.2A; allowing for 75% converter efficiency, $I_{IN(MAX)}$ = 1.6A.

Calculate R_S: from Equation (8) R_S = 25mΩ.

Calculate $I_{SHORTCIRCUIT(MAX)}$: from Equation (10) $I_{SHORTCIRCUIT(MAX)}$ = 3.2A.

Select a MOSFET that can handle 3.2A at 14V: IRF7413.

Calculate C_T: from Equation (13) C_T = 24nF. Select C_T = 47nF, which gives the circuit breaker time-out period t_{MAX} = 0.7ms.

Consult MOSFET SOA curves: the IRF7413 can handle 3.2A at 20V for 3.5ms, so it is safe to use in this application.

Calculate C_{SS}: using Equations (14) and (15) select C_{SS} = 22nF.

FREQUENCY COMPENSATION

The LTC4214 typical frequency compensation network for the analog current limit loop is a series R_C (10Ω) and C_C connected to V_{EE}. Figure 6 depicts the relationship be-

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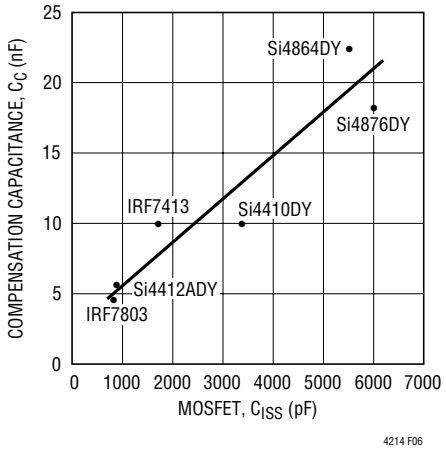


Figure 6. Recommended Compensation Capacitor C_C vs MOSFET C_{ISS}

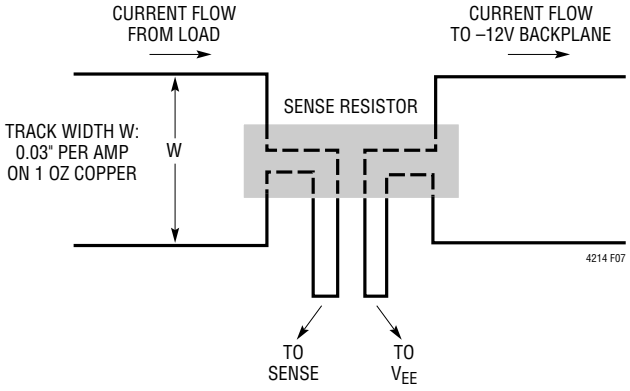


Figure 7. Making PCB Connections to the Sense Resistor

tween the compensation capacitor C_C and the MOSFET's C_{ISS}. The line in Figure 6 is used to select a starting value for C_C based upon the MOSFET's C_{ISS} specification. Optimized values for C_C are shown for several popular MOSFETs. Differences in the optimized value of C_C versus the starting value are small. Nevertheless, compensation values should be verified by board level short-circuit testing.

As seen in Figure 5 previously, at the onset of a short-circuit event, the input supply voltage can ring dramatically owing to series inductance. If this voltage avalanches the MOSFET, current continues to flow through the MOSFET to the output. The analog current limit loop cannot control this current flow and therefore the loop undershoots. This effect cannot be eliminated by frequency compensation. A zener diode is required to clamp the input supply voltage and prevent MOSFET avalanche.

SENSE RESISTOR CONSIDERATIONS

For proper circuit breaker operation, Kelvin-sense PCB connections between the sense resistor and the LTC4214's V_{EE} and SENSE pins are strongly recommended. The drawing in Figure 7 illustrates the correct way of making connections between the LTC4214 and the sense resistor. PCB layout should be balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistor should include good thermal management techniques for optimal sense resistor power dissipation.

TIMING WAVEFORMS

System Power-Up

Figure 8 details the timing waveforms for a typical power-up sequence in the case where a board is already installed in the backplane and system power is applied abruptly. At time point 1, the supply ramps up, together with UV/OV, V_{IN}, V_{OUT}, DRAIN and $\overline{PWRGD}$. At time point 2, V_{IN} exceeds V_{LKO} and the internal logic checks for UV > V_{UVHI}, OV < V_{OVHI}, GATE < V_{GATEL}, SENSE < V_{CB}, SS < 20 • V_{OS} and TIMER < V_{TMRL}. If all conditions are met, an initial timing cycle starts and the TIMER capacitor is charged by a 5µA current source pull-up. At time point 3, TIMER reaches the V_{TMRH} threshold and the initial timing cycle terminates. The TIMER capacitor is quickly discharged. At time point 4, the V_{TMRL} threshold is reached and the conditions of GATE < V_{GATEL}, SENSE < V_{CB} and SS < 20 • V_{OS} must be satisfied before a GATE ramp-up cycle begins. SS ramps up as dictated by R_{SS} • C_{SS} (as in Equation 6); GATE is held low by the analog current limit (ACL) amplifier until SS crosses 20 • V_{OS}. Upon releasing GATE, 50µA sources into the external MOSFET gate and compensation network. When the GATE voltage reaches the MOSFET's threshold, current begins flowing into the load capacitor at time point 5. At time point 6, load current reaches the SS control level and the analog current limit loop activates. Between time points 6 and 8, the GATE voltage is servoed, the SENSE voltage is regulated at $V_{ACL}(t)$ (Equation 7) and soft-start limits the slew rate of

APPLICATIONS INFORMATION

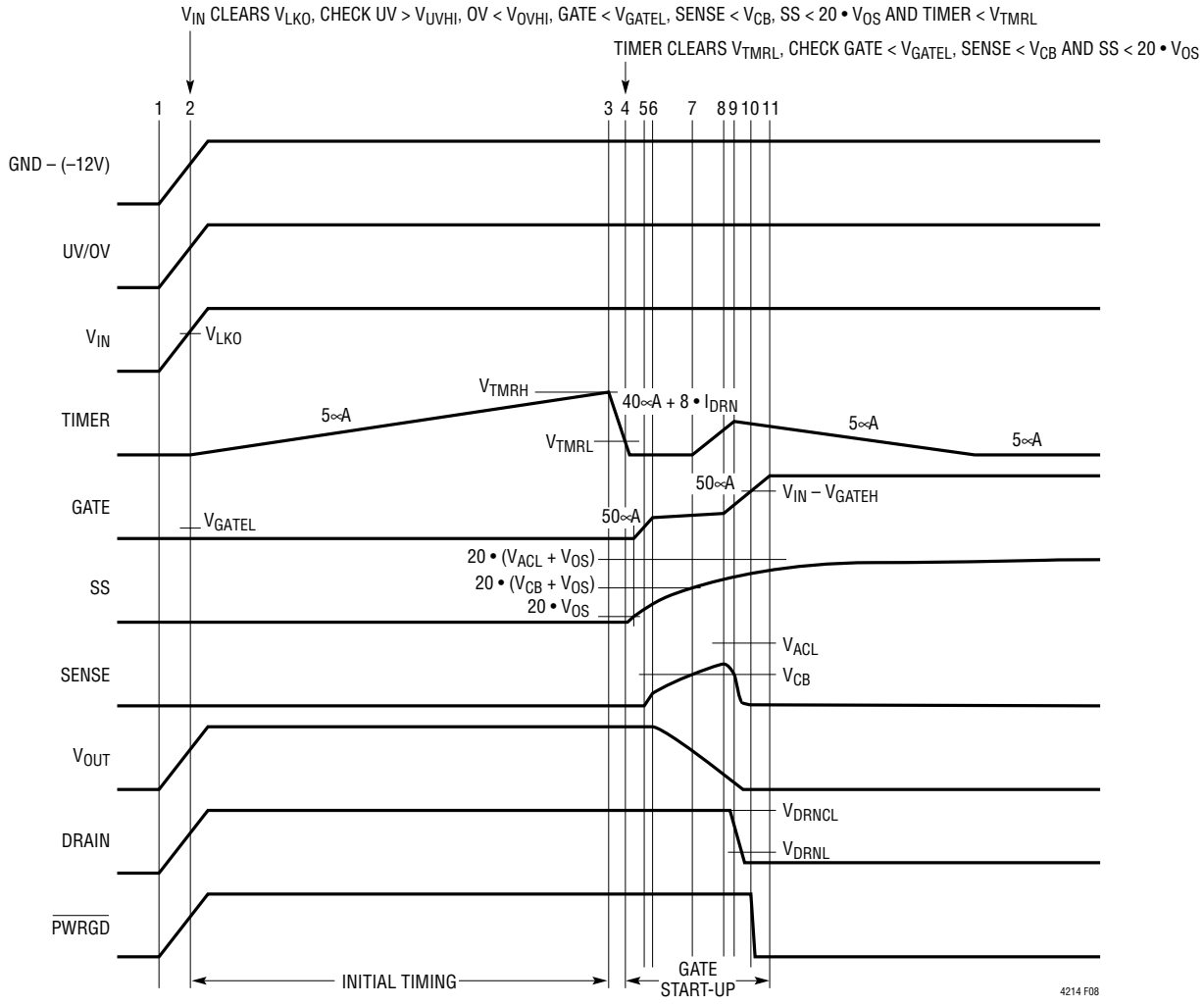


Figure 8. System Power-Up Timing (All Waveforms are Referenced to V_{EE})

the load current. If the SENSE voltage (V_{SENSE} – V_{EE}) reaches the V_{CB} threshold at time point 7, the circuit breaker TIMER activates. The TIMER capacitor, C_T, is charged by a (40µA + 8 • I_{DRN}) current pull-up. As the load capacitor nears full charge, load current begins to decline. At time point 8, the load current falls and the SENSE voltage drops below $V_{ACL}(t)$. The analog current limit loop shuts off and the GATE pin ramps further. At time point 9, the SENSE voltage drops below V_{CB}, the fault TIMER cycle ends, followed by a 5µA discharge cycle (cool off). The duration between time points 7 and 9 must be shorter than one circuit breaker delay to avoid a fault time out during GATE ramp-up. When GATE ramps past the V_{GATEH} threshold at time point 10, $\overline{PWRGD}$ pulls low. At time point 11, GATE reaches its maximum voltage as determined by V_{IN}.

Live Insertion with Short Pin Control of UV/OV

In the example shown in Figure 9, power is delivered through long connector pins whereas the UV/OV divider makes contact through a short pin. This ensures the power connections are firmly established before the LTC4214 is activated. At time point 1, the power pins make contact and V_{IN} ramps through V_{LKO}. At time point 2, the UV/OV divider

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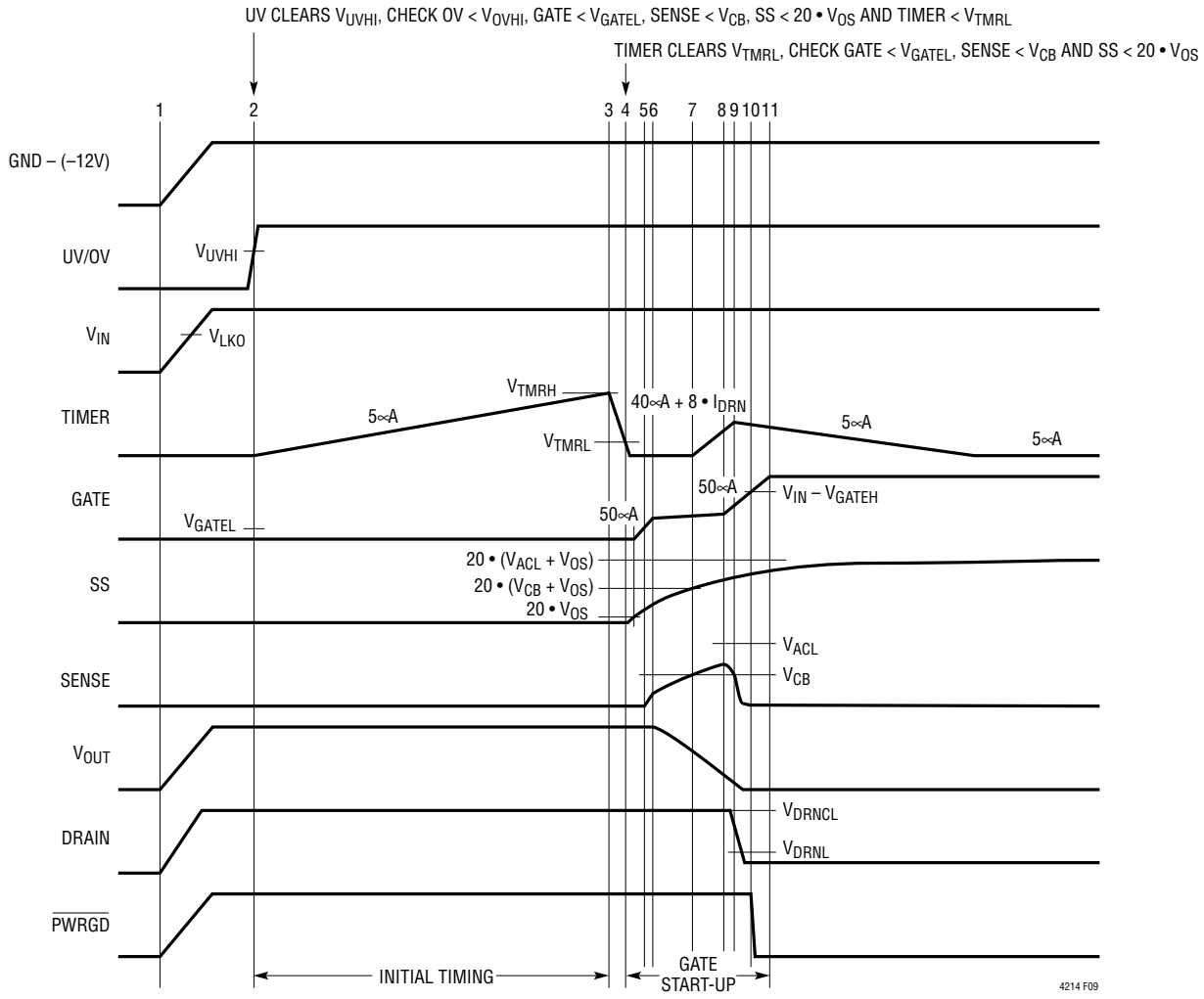


Figure 9. Power-Up Timing with a Short Pin (All Waveforms are Referenced to V_{EE})

makes contact and its voltage exceeds V_{UVHI}. In addition, the internal logic checks for OV < V_{OVHI}, GATE < V_{GATEL}, SENSE < V_{CB}, SS < 20 • V_{OS} and TIMER < V_{TMRL}. If all conditions are met, an initial timing cycle starts and the TIMER capacitor is charged by a 5µA current source pull-up. At time point 3, TIMER reaches the V_{TMRH} threshold and the initial timing cycle terminates. The TIMER capacitor is quickly discharged. At time point 4, the V_{TMRL} threshold is reached and the conditions of GATE < V_{GATEL}, SENSE < V_{CB} and SS < 20 • V_{OS} must be satisfied before a GATE start-up cycle begins. SS ramps up as dictated by R_{SS} • C_{SS}; GATE is held low by the analog current limit amplifier until SS crosses 20 • V_{OS}. Upon releasing GATE, 50µA sources into the external MOSFET gate and compensation network. When the GATE voltage reaches the MOSFET's threshold, current begins flowing into the load capacitor at time point 5. At time point 6, load current reaches the SS control level and the analog current limit loop activates. Between time points 6 and 8, the GATE voltage is servoed, the SENSE voltage is regulated at $V_{ACL}(t)$ and soft-start limits the slew rate of the load current. If the SENSE voltage (V_{SENSE} – V_{EE}) reaches the V_{CB} threshold at time point 7, the circuit breaker TIMER activates. The TIMER capacitor, C_T, is charged by a

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(40µA + 8 • I_{DRN}) current pull-up. As the load capacitor nears full charge, load current begins to decline. At point 8, the load current falls and the SENSE voltage drops below $V_{ACL}(t)$. The analog current limit loop shuts off and the GATE pin ramps further. At time point 9, the SENSE voltage drops below V_{CB} and the fault TIMER cycle ends, followed by a 5µA discharge cycle (cool off). When GATE ramps past V_{GATEH} threshold at time point 10, $\overline{PWRGD}$ pulls low. At time point 11, GATE reaches its maximum voltage as determined by V_{IN}.

Undervoltage Timing

In Figure 10 when the UV pin drops below $V_{UVHI} – V_{UVHST}$ (time point 1), the LTC4214 shuts down with TIMER, SS and GATE all pulling low. If current has been flowing, the SENSE pin voltage decreases to zero as GATE collapses. When UV recovers and clears V_{UVHI} (time point 2), an initial timer cycle begins followed by a start-up cycle.

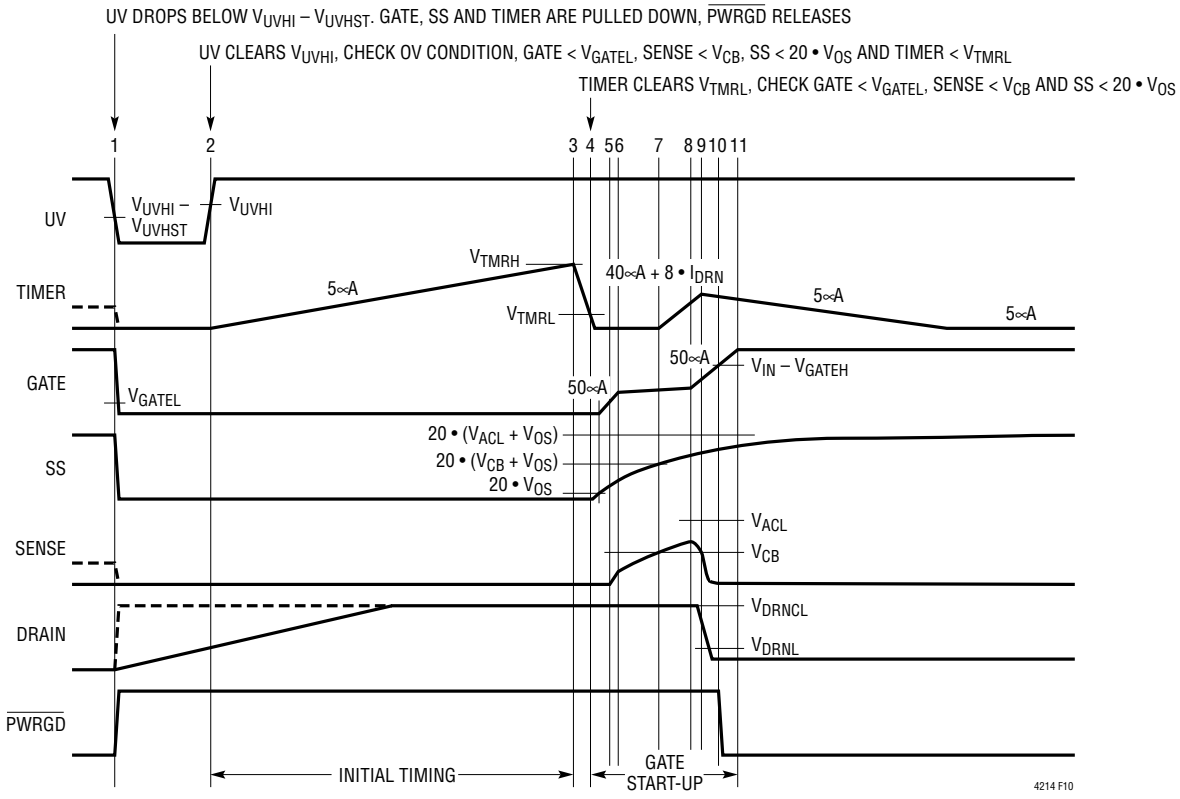


Figure 10. Undervoltage Timing (All Waveforms are Referenced to V_{EE})

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V_{IN} Undervoltage Lockout Timing

The V_{IN} undervoltage lockout comparator, UVLO, has a similar timing behavior as the UV pin timing except it looks for $V_{IN} < (V_{LKO} – V_{LKH})$ to shut down and $V_{IN} > V_{LKO}$ to start. In an undervoltage lockout condition, both UV and OV comparators are held off. When V_{IN} exits undervoltage lockout, the UV and OV comparators are enabled.

Undervoltage Timing with Overvoltage Glitch

In Figure 11, both UV and OV pins are connected together. When UV clears V_{UVHI} (time point 1), an initial timing cycle starts. If the system bus voltage overshoots V_{OVHI} as shown at time point 2, TIMER discharges. At time point 3, the supply voltage recovers and drops below the V_{OVHI} – V_{OVHST} threshold. The initial timing cycle restarts, followed by a GATE start-up cycle.

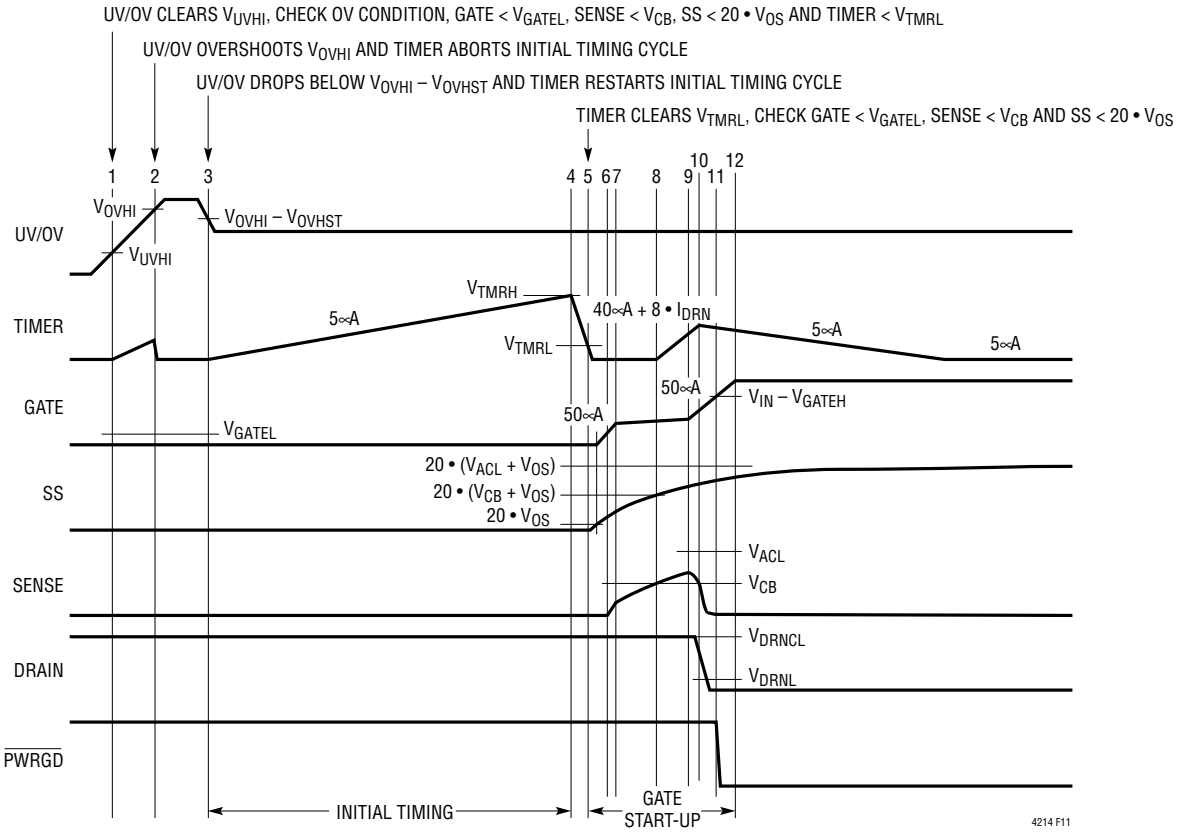


Figure 11. Undervoltage Timing with an Overvoltage Glitch (All Waveforms are Referenced to V_{EE})

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Overvoltage Timing

During normal operation, if the OV pin exceeds V_{OVHI} as shown at time point 1 of Figure 12, the TIMER and $\overline{PWRGD}$ status are unaffected. Nevertheless, SS and GATE pull down and the load is disconnected. At time point 2, OV recovers and drops below the $V_{OVHI} – V_{OVHST}$ threshold. A GATE start-up cycle begins. If the overvoltage glitch is long enough to deplete the load capacitor, a full start-up cycle as shown between time points 4 through 7 may occur.

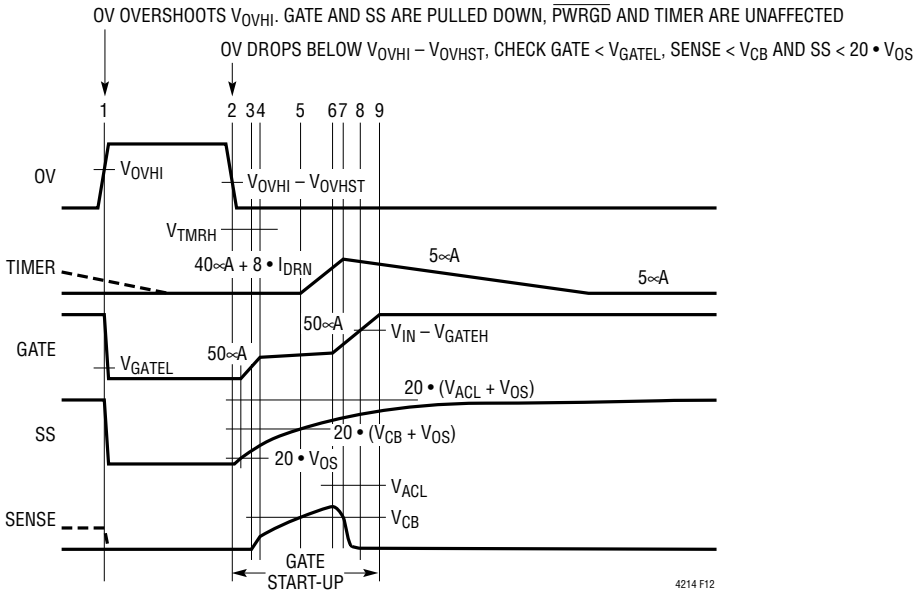
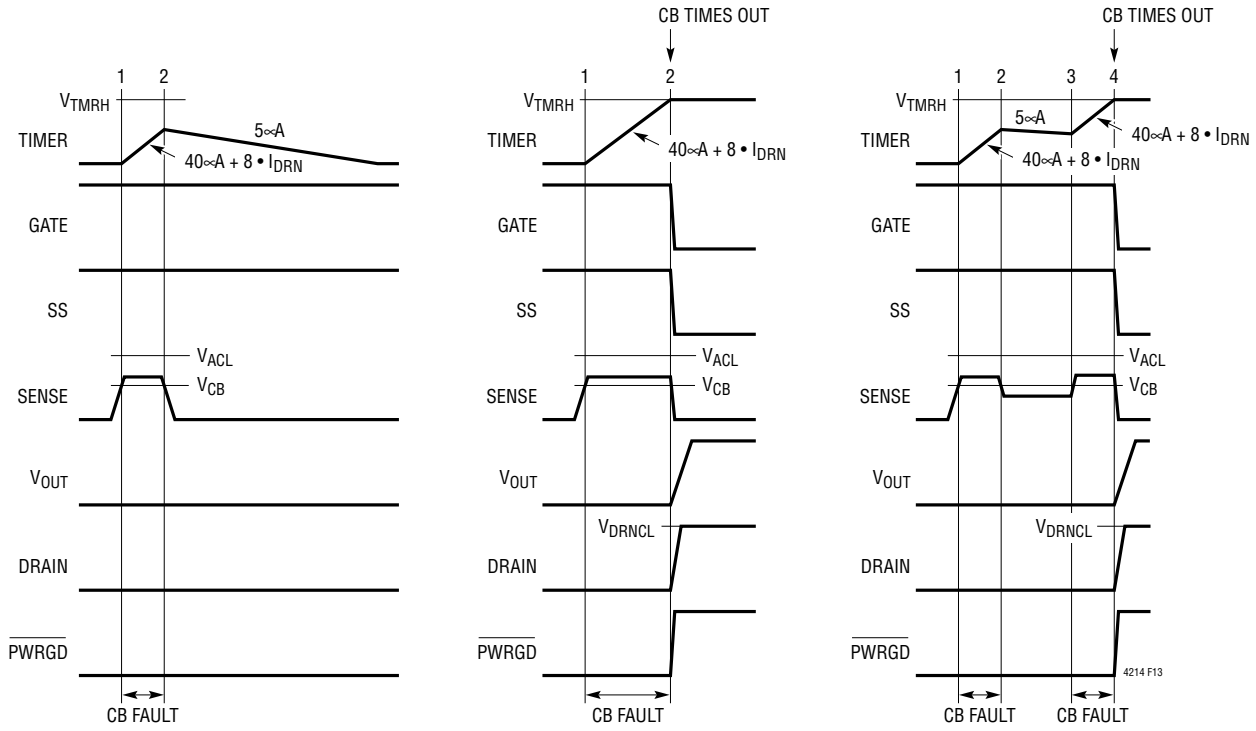


Figure 12. Overvoltage Timing (All Waveforms are Referenced to V_{EE})

APPLICATIONS INFORMATION

Circuit Breaker Timing

In Figure 13a, the TIMER capacitor charges at 40µA if the SENSE pin exceeds V_{CB} but V_{DRN} is less than 4.2V. If the SENSE pin drops below V_{CB} before TIMER reaches the V_{TMRH} threshold, TIMER is discharged by 5µA. In Figure 13b, when TIMER exceeds V_{TMRH}, GATE pulls down immediately and the LTC4214 shuts down. In Figure 13c, multiple momentary faults cause the TIMER capacitor to integrate and reach V_{TMRH}. GATE pull down follows and the LTC4214 shuts down. During shutdown, the LTC4214-1 latches TIMER high with a 5µA pull-up current source; the LTC4214-2 activates a shutdown cooling cycle.



(13a) Momentary Circuit-Breaker Fault **(13b) Circuit-Breaker Time Out** **(13c) Multiple Circuit-Breaker Fault**

Figure 13. Circuit-Breaker Timing Behavior (All Waveforms are Referenced to V_{EE})

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Resetting a Fault Latch (LTC4214-1)

The latched circuit breaker fault of LTC4214-1 benefits from long cooling time. It is reset by pulling the UV pin below $V_{UVHI} – V_{UVHST}$ with a switch. Reset is also accomplished by pulling the V_{IN} pin momentarily below ($V_{LKO} – V_{LKH}$). A third reset method involves pulling the TIMER pin below V_{TMRL} as shown in Figure 14. An initial timing cycle is skipped if TIMER is used for reset. An initial timing cycle is generated if reset by the UV pin or the V_{IN} pin.

The duration of the TIMER reset pulse should be smaller than the time taken to reach 0.2V at SS pin. With a single pole mechanical pushbutton switch, this may not be feasible. A double pole, single throw pushbutton switch removes this restriction by connecting the second switch to the SS pin. With this method, both the SS and TIMER pins are released at the same time.

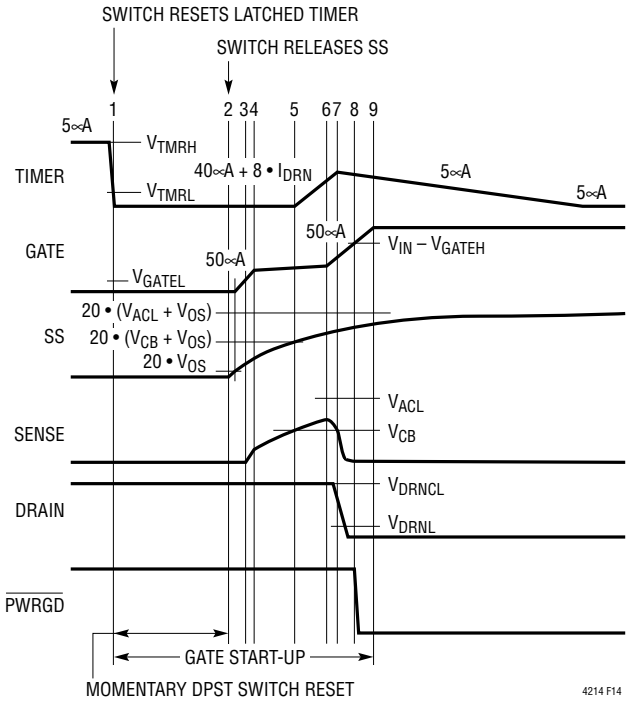


Figure 14. Pushbutton Reset of LTC4214-1's Latched Fault (All Waveforms are Referenced to V_{EE})

APPLICATIONS INFORMATION

Shutdown Cooling Cycle (LTC4214-2)

Figure 15 shows the timer behavior of the LTC4214-2. At time point 2, TIMER exceeds V_{TMRH}, GATE pulls down immediately and the LTC4214 shuts down. TIMER starts a shutdown cooling cycle by discharging TIMER with 5µA to the V_{TMRL} threshold. TIMER then charges with 5µA to the V_{TMRH} threshold. There are four 5µA discharge phases and three 5µA charge phases in this shutdown cooling cycle spanning time points 2 and 3. At time point 3, the LTC4214 automatic retry occurs with a start-up cycle. Good thermal management techniques are highly recommended; power and thermal dissipation must be carefully evaluated when implementing the automatic retry scheme.

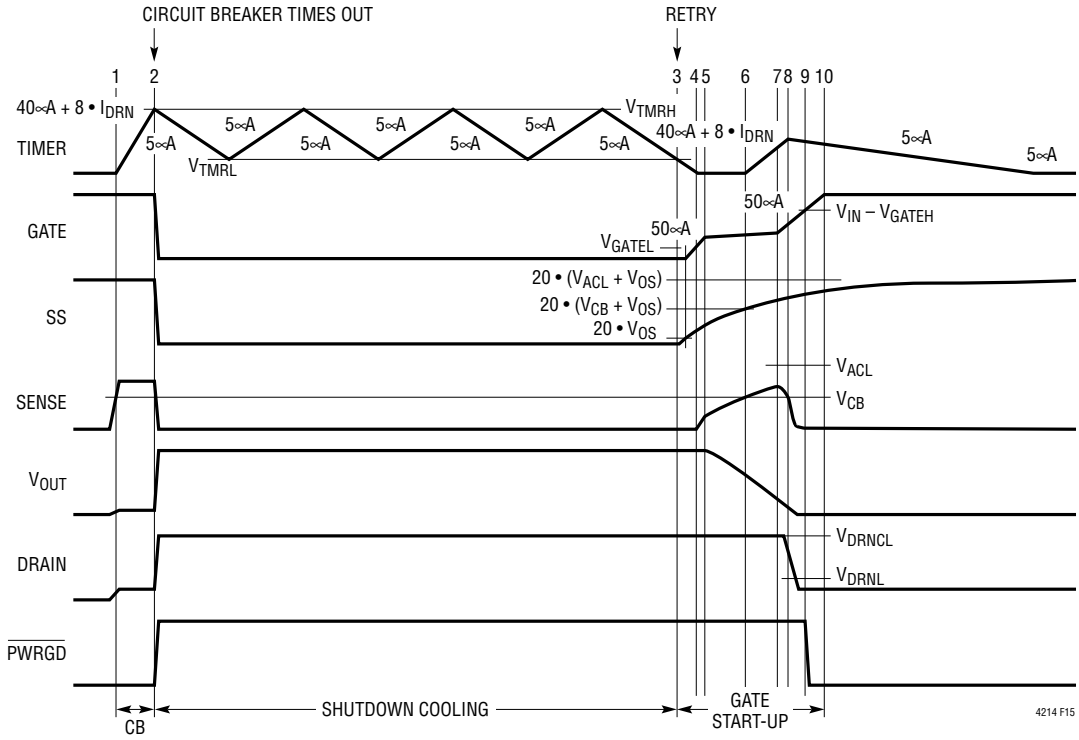
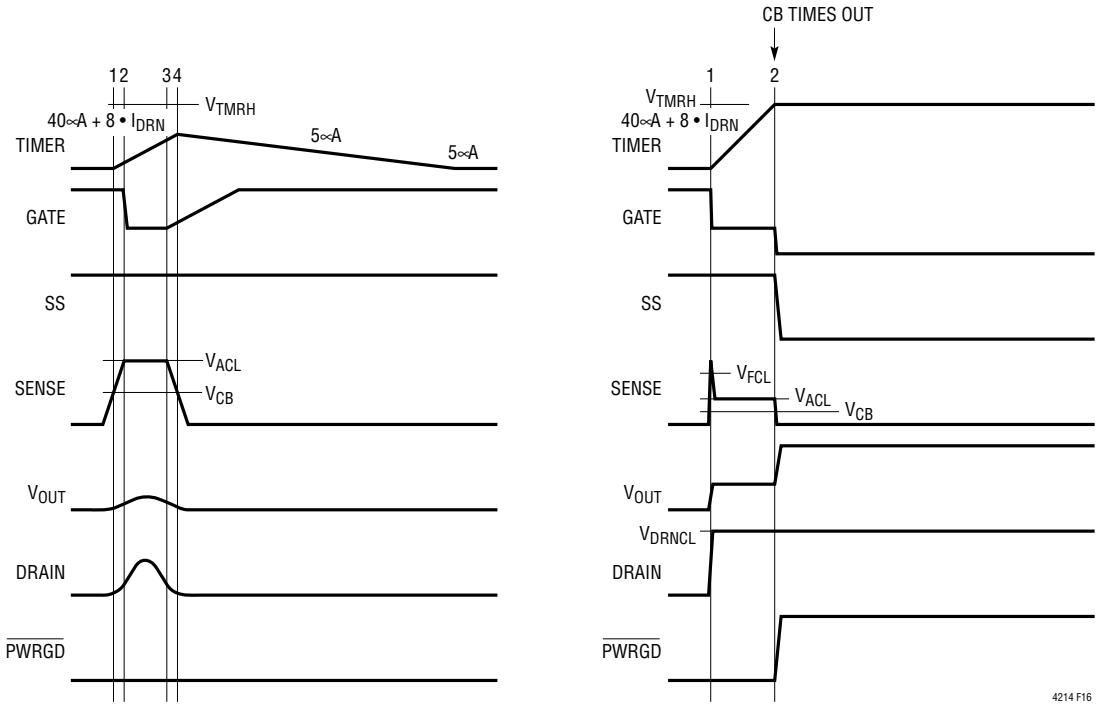


Figure 15. Shutdown Cooling Timing Behavior of LTC4214-2 (All Waveforms are Referenced to V_{EE})

APPLICATIONS INFORMATION

Analog Current Limit and Fast Current Limit

In Figure 16a, when SENSE exceeds V_{ACL}, GATE is regulated by the analog current limit amplifier loop. When SENSE drops below V_{ACL}, GATE is allowed to pull up. In Figure 16b, when a severe fault occurs, SENSE exceeds V_{FCL} and GATE immediately pulls down until the analog current amplifier can establish control. If the severe fault causes V_{OUT} to exceed V_{DRNCL}, the DRAIN pin is clamped at V_{DRNCL}. I_{DRN} flows into the DRAIN pin and is multiplied by 8. This extra current is added to the TIMER pull-up current of 40µA. This accelerated TIMER current of [40µA+8 • I_{DRN}] produces a shorter circuit breaker fault delay. Careful selection of C_T, R_D and MOSFET can help prevent SOA damage in a low impedance fault condition.



(16a) Analog Current Limit Fault

(16b) Fast Current Limit Fault

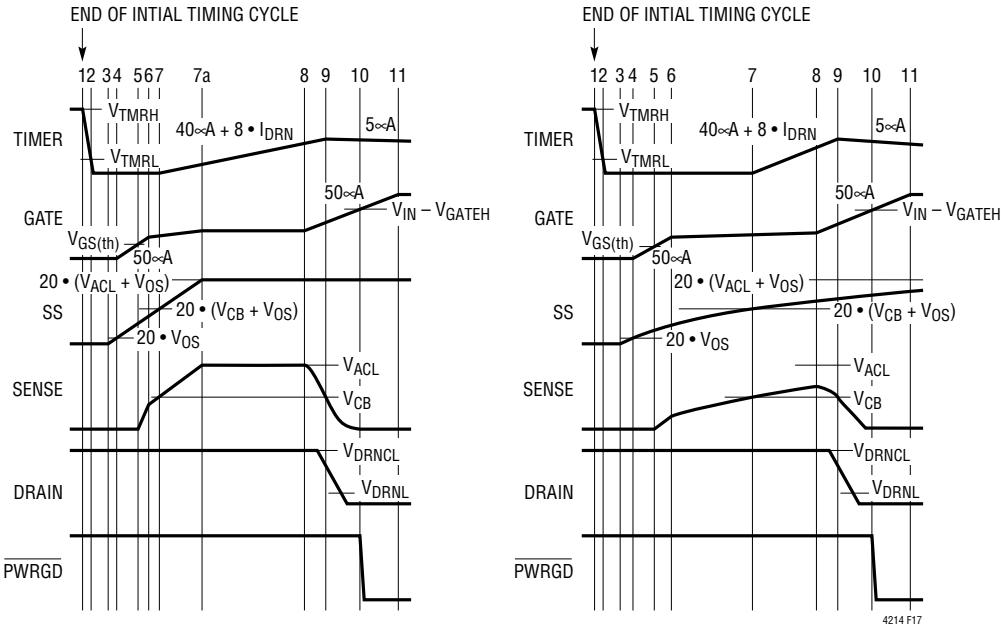
Figure 16. Current Limit Behavior (All Waveforms are Referenced to V_{EE})

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Soft-Start

If the SS pin is not connected, this pin defaults to a linear voltage ramp, from 0V to 1.6V in about 220µs at GATE start-up, as shown in Figure 17a. If a soft-start capacitor, C_{SS}, is connected to this SS pin, the soft-start response is modified from a linear ramp to an RC response (Equation 6), as shown in Figure 17b. This feature allows load current to slowly ramp-up at GATE start-up. Soft-start is initiated at time point 3 by a TIMER transition from V_{TMRH} to V_{TMRL} (time points 1 to 2) or by the OV pin falling below the $V_{OVHI} – V_{OVHST}$ threshold after an OV condition. When the SS pin is below 0.2V, the analog current limit amplifier holds GATE low. Above 0.2V, GATE is released and 50µA ramps up the compensation network and GATE capacitance at time point 4. Meanwhile, the SS pin voltage continues to ramp up. When GATE reaches the MOSFET's threshold, the MOSFET begins to conduct. Due to the MOSFET's high g_m, the MOSFET current quickly reaches the soft-start control value of $V_{ACL}(t)$ (Equation 7). At time point 6, the GATE voltage is controlled by the current limit amplifier. The soft-start control voltage reaches the circuit breaker voltage, V_{CB}, at time point 7 and the circuit breaker TIMER activates. As the load capacitor nears full charge, load current begins to decline below $V_{ACL}(t)$. The current limit loop shuts off and GATE releases at time point 8. At time point 9, the SENSE voltage falls below V_{CB} and TIMER deactivates.

Large values of C_{SS} can cause premature circuit breaker time out as $V_{ACL}(t)$ may exceed the V_{CB} potential during the circuit breaker delay. The load capacitor is unable to achieve full charge in one GATE start-up cycle. A more serious side effect of large C_{SS} values is SOA duration may be exceeded during soft-start into a low impedance load. A soft-start voltage below V_{CB} will not activate the circuit breaker TIMER.



(17a) Without External C_{SS} **(17b) With External C_{SS}**

Figure 17. Soft-Start Timing (All Waveforms are Referenced to V_{EE})

APPLICATIONS INFORMATION

Power Limit Circuit Breaker

Figure 18 shows the LTC4214-1 in a power limit circuit breaking application. The SENSE pin is modulated by the board supply voltage, V_{SUPPLY}. The zener voltage, V_Z is set to be the same as the low supply operating voltage, $V_{SUPPLY(MIN)}$ = 10V. If the goal is to have the high supply operating voltage, $V_{SUPPLY(MAX)}$ = 14V give the same power at $V_{SUPPLY(MIN)}$, then resistors R4 and R6 are selected using the ratio:

$$\frac{R6}{R4} = \frac{V_{CB}}{V_{SUPPLY(MAX)}} \quad (16)$$

If R6 is 20Ω, R4 is 5.6k. The peak circuit breaker power limit is:

$$POWER_{MAX} = \frac{\left(V_{SUPPLY(MIN)} + V_{SUPPLY(MAX)}\right)^2}{4 \bullet V_{SUPPLY(MIN)} \bullet V_{SUPPLY(MAX)}} \bullet POWER_{SUPPLY(MIN)} = 1.029 \bullet POWER_{SUPPLY(MIN)} \quad (17)$$

when

$$V_{SUPPLY} = 0.5 \bullet (V_{SUPPLY(MIN)} + V_{SUPPLY(MAX)}) = 12V.$$

The peak power at the fault current limit occurs at the supply overvoltage threshold. The fault current limited power is:

$$POWER_{FAULT} = \frac{V_{SUPPLY}}{R_S} \bullet \left(V_{ACL} - \left(V_{SUPPLY} - V_Z\right) \bullet \frac{R6}{R4}\right) \quad (18)$$

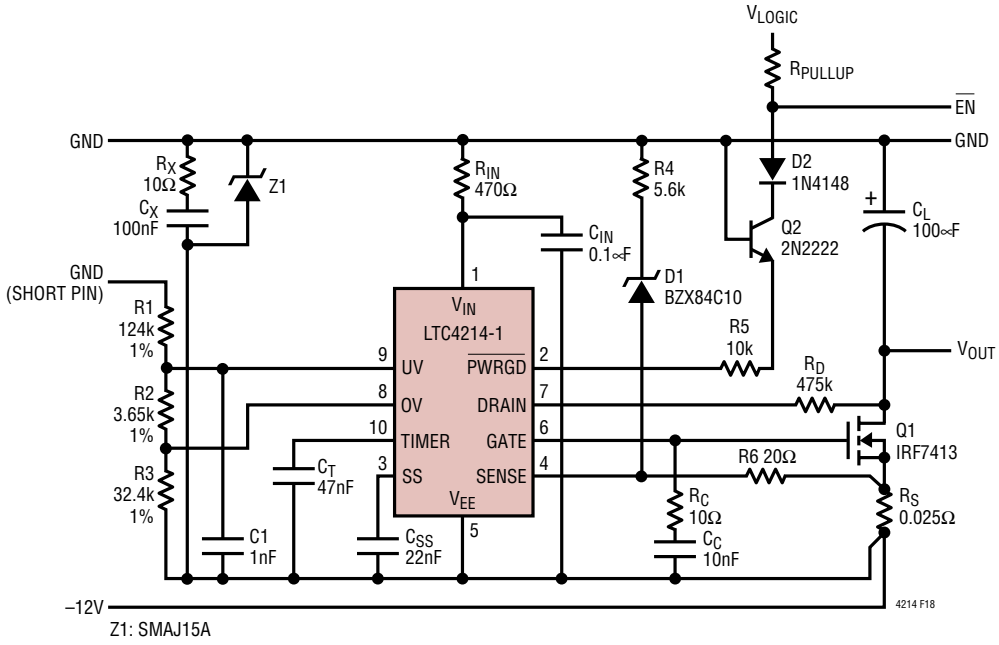
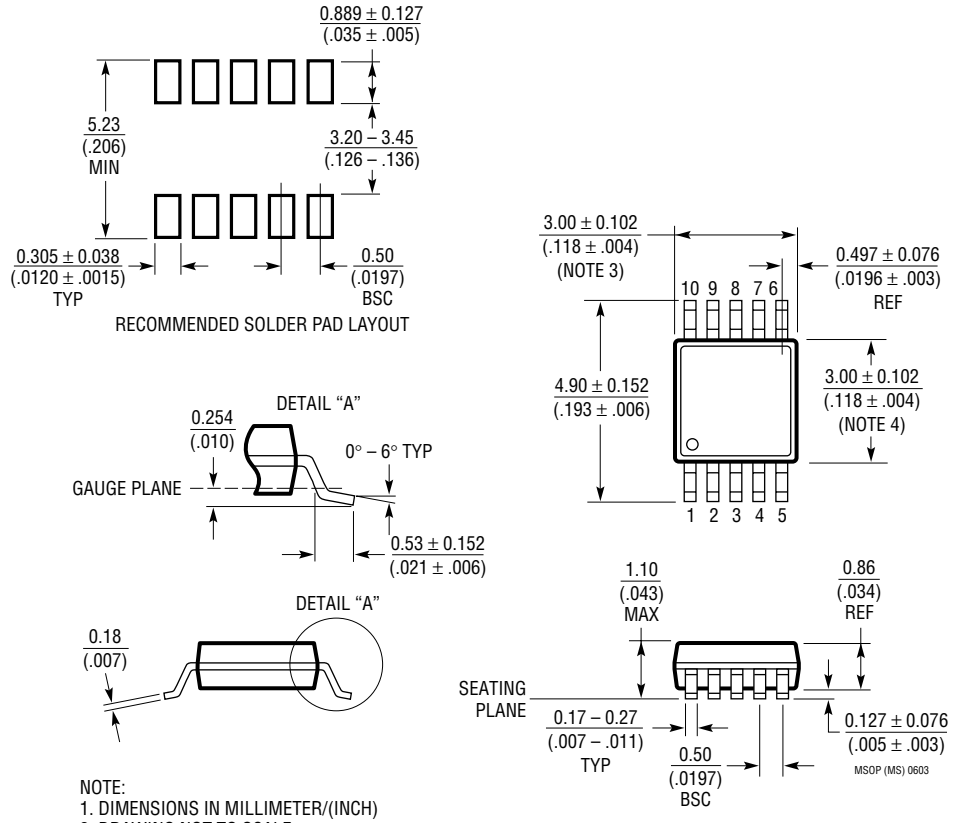


Figure 18. Power Limit Circuit Breaking Application

PACKAGE DESCRIPTION

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

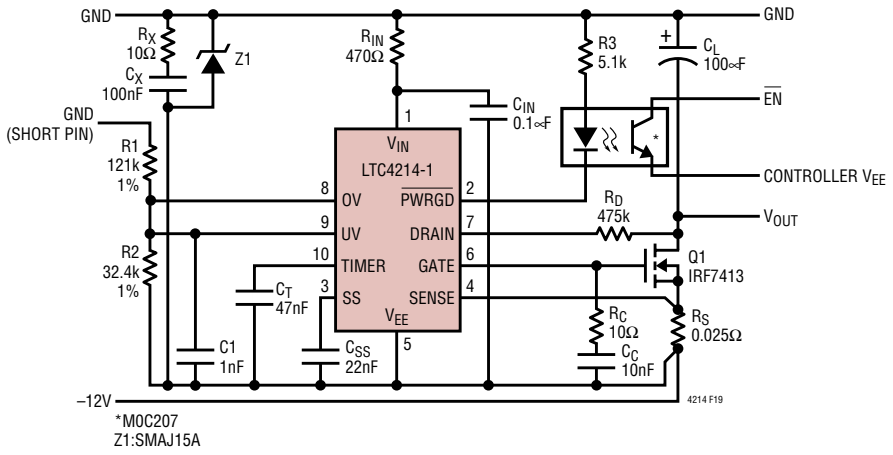
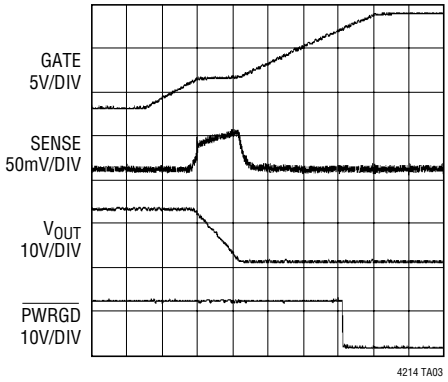


Figure 19. –12V/2A Hot Swap Controller

Start-Up Behavior



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1421	Two Channels, Hot Swap Controller	Operates from 3V to 12V and Supports –12V
LTC1642	Fault Protected Hot Swap Controller	3V to 16.5V, Overvoltage Protection up to 33V
LTC1644	PCI Hot Swap Controller	3.3V, 5V and ±12V; 1V Precharge; PCI Reset Logic
LTC4210	Hot Swap Controller in SOT-23	Active Current Limiting, 2.7V to 16.5V
LTC4211	Single Hot Swap with Multifunction Current Control	Operates from 2.5V to 16.5V
LT4220	Dual Hot Swap Controller for Positive/Negative Supplies	Operates from ±2.7V to ±16.5V
LTC4230	Triple Hot Swap Controller with Multifunction Current Control	Operates from 1.7V to 16.5V

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