5A Integrated Hot Swap Controller

FEATURES

- **Reduced 16ms Turn-On Delay**
- **Small Footprint**
- **33mΩ MOSFET with R_{SENSE}**
- **Wide Operating Voltage Range: 2.9V to 15V**
- **Adjustable, 10% Accurate Current Limit**
- Current and Temperature Monitor Outputs
- Overtemperature Protection
- Adjustable Current Limit Timer Before Fault
- Power Good and Fault Outputs
- Adjustable Inrush Current Control
- 2% Accurate Undervoltage and Overvoltage Protection
- Pin Compatible with LTC4217 (DFN Package Only)
- Available in 16-Lead 5mm × 3mm DFN Package

APPLICATIONS

- RAID Systems, Solid State Drives
- Server I/O Cards
- PCI Express Systems
- Industrial

DESCRIPTION

The LTC®4232-1 is an integrated solution for Hot Swap applications that allows a board to be safely inserted and removed from a live backplane. The part integrates a Hot Swap controller, power MOSFET and current sense resistor in a single package for small form factor applications.

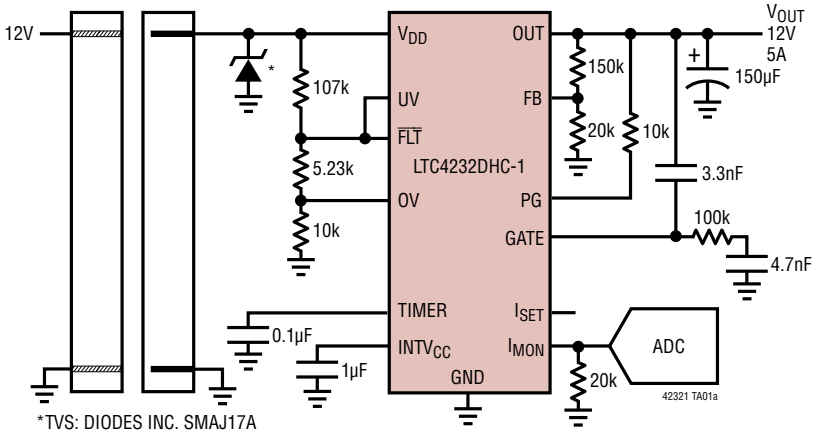
The LTC4232-1 provides separate inrush current control and a 10% accurate 5A current limit with foldback current limiting. The current limit threshold can be adjusted dynamically using an external pin. Additional features include a current monitor output that amplifies the sense resistor voltage for ground referenced current sensing and a MOSFET temperature monitor output. Thermal limit, overvoltage, undervoltage and power good monitoring are also provided.

The PCI Express compliant LTC4232-1 allows faster turn-on than the LTC4232 by providing a shorter (16ms) debounce delay and external control of the GATE ramp rate.

LT, LTC, LTM, Linear Technology and the Linear logo are registered trademarks of Linear Technology Corporation and PowerPath is a trademark of Linear Technology Corporation. All other trademarks are the property of their respective owners.

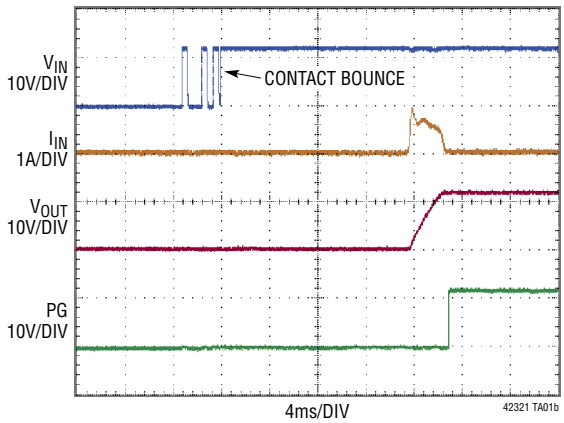
TYPICAL APPLICATION

12V, 5A Card Resident Application with Auto-Retry



*TVS: DIODES INC. SMAJ17A

Power-Up Waveforms

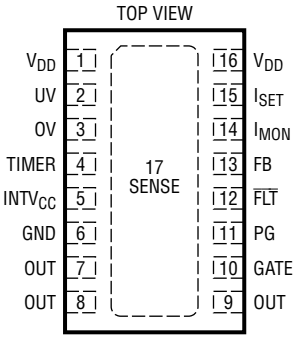


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD}) ..... –0.3V to 28V
Input Voltages
  FB, OV, UV ..... –0.3V to 12V
  TIMER ..... –0.3V to 3.5V
  SENSE ..... V_{DD} – 10V or – 0.3V to V_{DD}
Output Voltages
  I_{SET}, I_{MON} ..... –0.3V to 3V
  PG, $\overline{FLT}$ ..... –0.3V to 35V
  OUT ..... –0.3V to V_{DD} + 0.3V
  $INTV_{CC}$ ..... –0.3V to 3.5V
  GATE (Note 3) ..... –0.3V to 33V
Operating Ambient Temperature Range
  LTC4232C-1 ..... 0°C to 70°C
  LTC4232I-1 ..... –40°C to 85°C
Junction Temperature (Notes 4, 5) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DHC PACKAGE
16-LEAD (5mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 17) IS SENSE,
θ_{JA} = 43°C/W SOLDERED, OTHERWISE θ_{JA} = 140°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4232CDHC-1#PBF	LTC4232CDHC-1#TRPBF	42321	16-Lead (5mm × 3mm) Plastic DFN	0°C to 70°C
LTC4232IDHC-1#PBF	LTC4232IDHC-1#TRPBF	42321	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes those specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Characteristics							
V_{DD}	Input Supply Range		●	2.9		15	V
I_{DD}	Input Supply Current	MOSFET On, No Load	●		1.6	3	mA
$V_{DD(UVL)}$	Input Supply Undervoltage Lockout	V_{DD} Rising	●	2.63	2.73	2.85	V
I_{OUT}	OUT Leakage Current	V_{OUT} = V_{GATE} = 0V, V_{DD} = 15V V_{OUT} = V_{GATE} = 12V	● ●	 1	0 2	±150 4	µA µA
R_{ON}	MOSFET + Sense Resistor On-Resistance		●	15	33	50	mΩ
$I_{LIM(TH)}$	Current Limit Threshold	V = 1.23V, I_{SET} Open	●	5.0	5.6	6.1	A
		V_{FB} = 0V, I_{SET} Open	●	1.2	1.5	1.8	A
		V_{FB} = 1.23V, R_{SET} = 20kΩ	●	2.6	2.9	3.3	A

ELECTRICAL CHARACTERISTICS

The ● denotes those specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Inputs							
I_{IN}	OV, UV, FB Input Current	V = 1.2V	●		0	±1	µA
V_{TH}	OV, UV, FB Threshold Voltage	V_{PIN} Rising	●	1.21	1.235	1.26	V
$\Delta V_{OV(HYST)}$	OV Hysteresis		●	10	20	30	mV
$\Delta V_{UV(HYST)}$	UV Hysteresis		●	50	80	110	mV
$V_{UV(RTH)}$	UV Reset Threshold Voltage	V_{UV} Falling	●	0.55	0.62	0.7	V
$\Delta V_{FB(HYST)}$	FB Power Good Hysteresis		●	10	20	30	mV
R_{ISET}	I_{SET} Internal Resistor		●	19	20	21	kΩ
Outputs							
V_{INTVCC}	$INTV_{CC}$ Output Voltage	V_{DD} = 5V, 15V, I_{LOAD} = 0mA, –10mA	●	2.8	3.1	3.3	V
V_{OL}	PG, $\overline{FLT}$ Output Low Voltage	I_{SINK} = 2mA	●		0.4	0.8	V
I_{OH}	PG, $\overline{FLT}$ Input Leakage Current	V = 30V	●		0	±10	µA
$V_{TIMER(H)}$	TIMER High Threshold	V_{TIMER} Rising	●	1.2	1.235	1.28	V
$V_{TIMER(L)}$	TIMER Low Threshold	V_{TIMER} Falling	●	0.1	0.21	0.3	V
$I_{TIMER(UP)}$	TIMER Pull-Up Current	V_{TIMER} = 0V	●	–80	–100	–120	µA
$I_{TIMER(DN)}$	TIMER Pull-Down Current	V_{TIMER} = 1.2V	●	1.4	2	2.6	µA
$I_{TIMER(RATIO)}$	TIMER Current Ratio $I_{TIMER(DN)}/I_{TIMER(UP)}$		●	1.6	2	2.7	%
BW_{IMON}	I_{MON} Bandwidth				250		kHz
A_{IMON}	I_{MON} Current Gain	I_{OUT} = 2.5A	●	18.5	20	21.5	µA/A
$I_{OFF(IMON)}$	I_{MON} Offset Current	I_{OUT} = 150mA	●		0	±4.5	µA
$I_{GATE(UP)}$	Gate Pull-Up Current	Gate Drive On, V_{GATE} = V_{OUT} = 12V	●	–18	–24	–29	µA
$I_{GATE(DN)}$	Gate Pull-Down Current	Gate Drive Off, V_{GATE} = 18V, V_{OUT} = 12V	●	180	250	400	µA
$I_{GATE(FST)}$	Gate Fast Pull-Down Current	Fast Turn Off, V_{GATE} = 18V, V_{OUT} = 12V			140		mA
AC Characteristics							
$t_{PHL(GATE)}$	Input High (OV), Input Low (UV) to Gate Low Propagation Delay	V_{GATE} < 16.5V Falling	●		8	10	µs
$t_{PHL(ILIM)}$	Short-Circuit to Gate Low	V_{FB} = 0, Step I_{SENSE} to 6A, V_{GATE} < 15V Falling	●		1	5	µs
$t_{D(ON)}$	Turn-On Delay	Step V_{UV} to 2V, V_{GATE} > 13V	●	8	16	24	ms
$t_{D(FAULT)}$	UV_{LOW} to Clear Fault Latch Delay				1		µs
$t_{D(CB)}$	Circuit Breaker Filter Delay Time (Internal)	V_{FB} = 0V, Step I_{SENSE} to 3A	●	1.3	2	2.7	ms
$t_{D(AUTO-RETRY)}$	Auto-Retry Turn-On Delay (Internal)		●	8	16	24	ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive, all voltages are referenced to GND unless otherwise specified.

Note 3: An internal clamp limits the GATE pin to a maximum of 6.5V above OUT. Driving this pin to voltages beyond the clamp may damage the device.

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

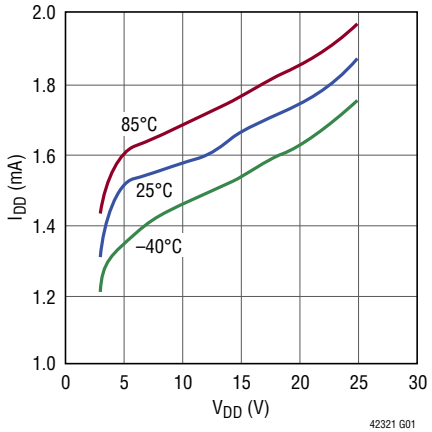
Note 5: T_J is calculated from the ambient temperature, T_A, and power dissipation, P_D, according to the formula:

$T_J = T_A + (P_D \bullet 43°C/W)$

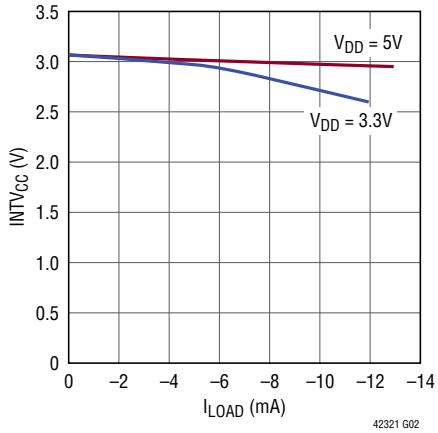
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 12V unless otherwise noted.

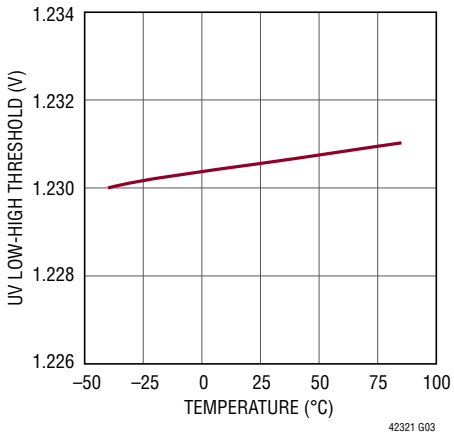
I_{DD} vs V_{DD}



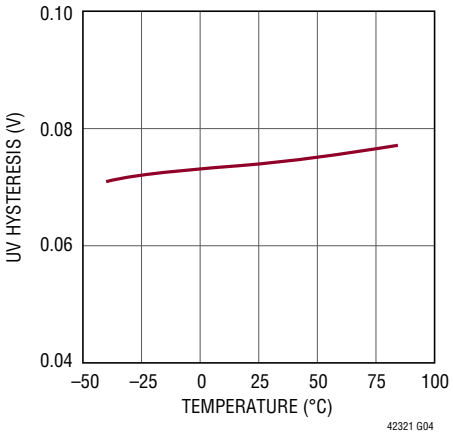
$INTV_{CC}$ Load Regulation



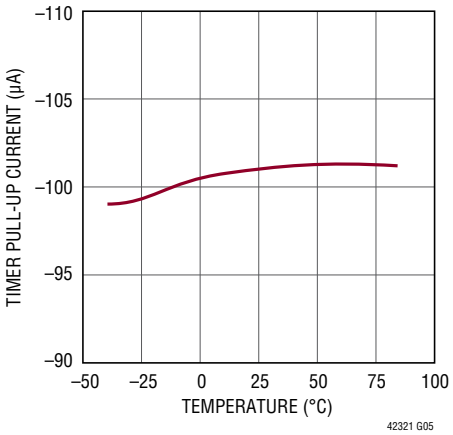
UV Low-High Threshold vs Temperature



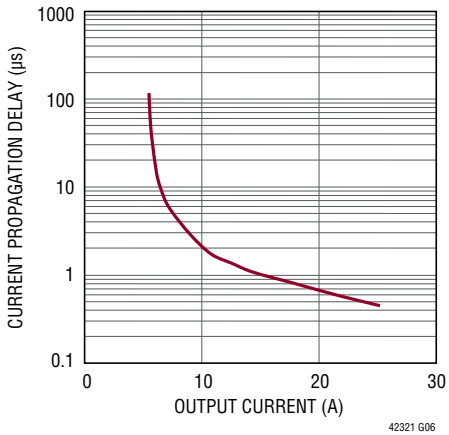
UV Hysteresis vs Temperature



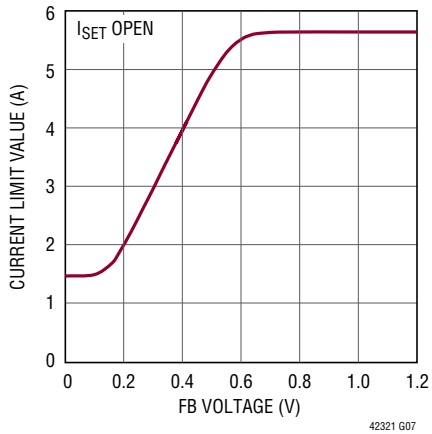
Timer Pull-Up Current vs Temperature



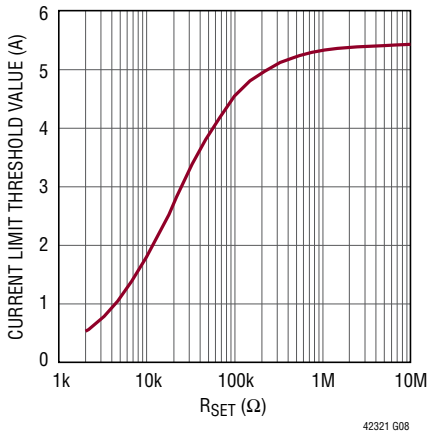
Current Limit Delay ($t_{PHL(ILIM)}$ vs Overdrive)



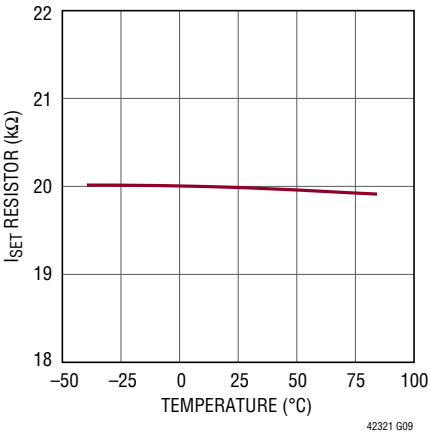
Current Limit Threshold Foldback



Current Limit Adjustment (I_{OUT} vs R_{SET})



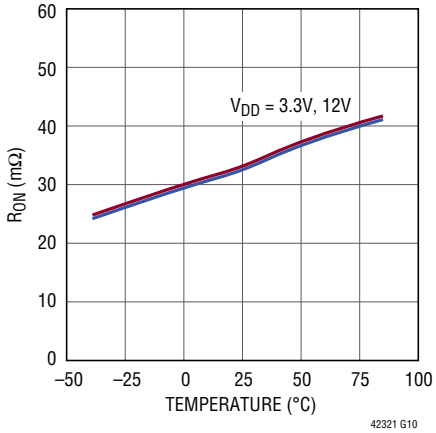
Internal I_{SET} Resistor (R_{ISET}) vs Temperature



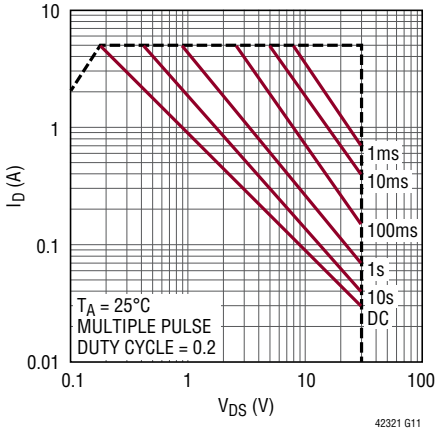
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 12V unless otherwise noted.

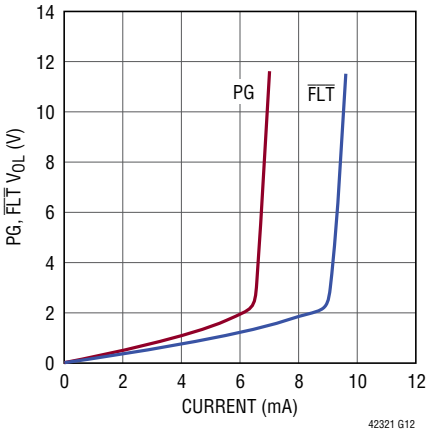
R_{ON} vs V_{DD} and Temperature



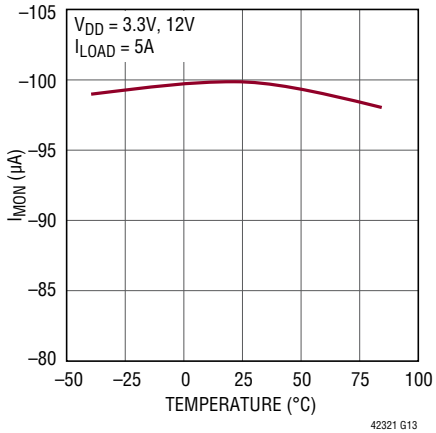
MOSFET SOA Curve



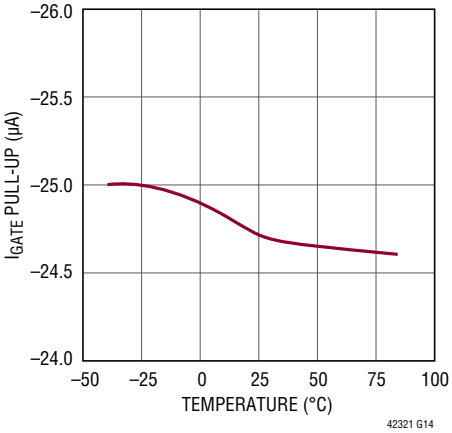
PG, $\overline{FLT}$ Output Low Voltage vs Current



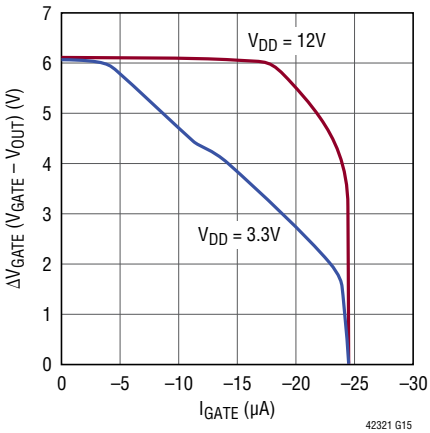
I_{MON} vs Temperature and V_{DD}



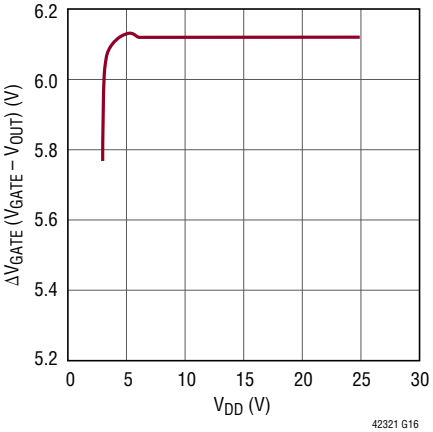
GATE Pull-Up Current vs Temperature



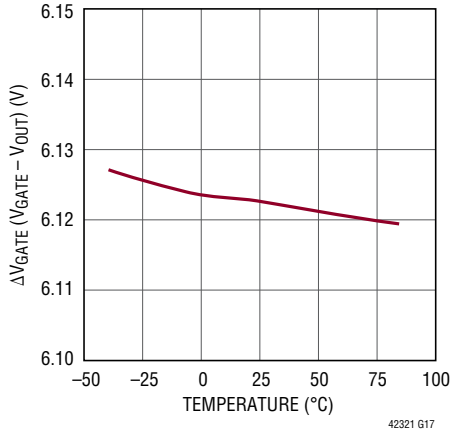
Gate Drive vs Gate Pull-Up Current



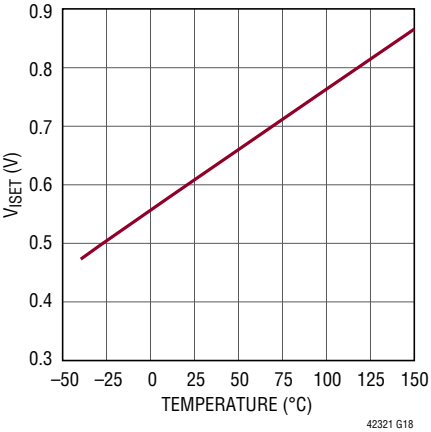
Gate Drive vs V_{DD}



Gate Drive vs Temperature



V_{ISET} vs Temperature



PIN FUNCTIONS

FB: Foldback and Power Good Input. Connect this pin to an external resistive divider from OUT. If the voltage falls below 0.6V, the current limit is reduced using a foldback profile (see the Typical Performance Characteristics section). If the voltage falls below 1.21V, the PG pin will pull low to indicate the power is bad.

$\overline{FLT}$: Overcurrent Fault Indicator. Open-drain output pulls low when an overcurrent fault has occurred and the circuit breaker trips. For overcurrent auto-retry tie to UV pin (see the Applications Information section for details).

GATE: Gate Drive for Internal N-channel MOSFET. An internal 24µA current source charges the gate of the N-channel MOSFET. A resistor and capacitor network from this pin sets the turn-on rate. During an undervoltage or overvoltage condition a 250µA pull-down current turns the MOSFET off. During a short-circuit or undervoltage lockout condition, a 140mA pull-down current source between GATE and OUT is activated.

GND: Device Ground.

I_{MON}: Current Monitor Output. The current in the internal MOSFET switch is divided by 50,000 and sourced from this pin. Placing a 20k resistor from this pin to GND creates a 0V to 2V voltage swing when current ranges from 0A to 5A.

$INTV_{CC}$: Internal 3.1V Supply Decoupling Output. This pin must have a 1µF or larger bypass capacitor. Overloading this pin can disrupt internal operation.

I_{SET}: Current Limit Adjustment Pin. For a 5.6A current limit value open this pin. This pin is driven by a 20k resistor in series with a voltage source. The pin voltage is used to generate the current limit threshold. The internal 20k resistor (R_{ISET}) and an external resistor (R_{SET}) between I_{SET} and ground create an attenuator that lowers the current limit value. Due to circuit tolerance, R_{SET} should not be less than 2k. In order to match the temperature variation of the sense resistor, the voltage on this pin increases at the same rate as the sense resistance increases. Therefore the voltage at I_{SET} pin is made proportional to temperature of the MOSFET switch.

OUT: Output of Internal MOSFET Switch. Connect this pin directly to the load.

OV: Overvoltage Comparator Input. Connect this pin to an external resistive divider from V_{DD}. If the voltage at this pin rises above 1.235V, an overvoltage is detected and the switch turns off. Tie to GND if unused.

PG: Power Good Indicator. Open-drain output pulls low when the FB pin drops below 1.21V indicating the power is bad. If the FB pin rises above 1.23V and the GATE to OUT voltage exceeds 4.2V, the open-drain pull-down releases the PG pin to go high.

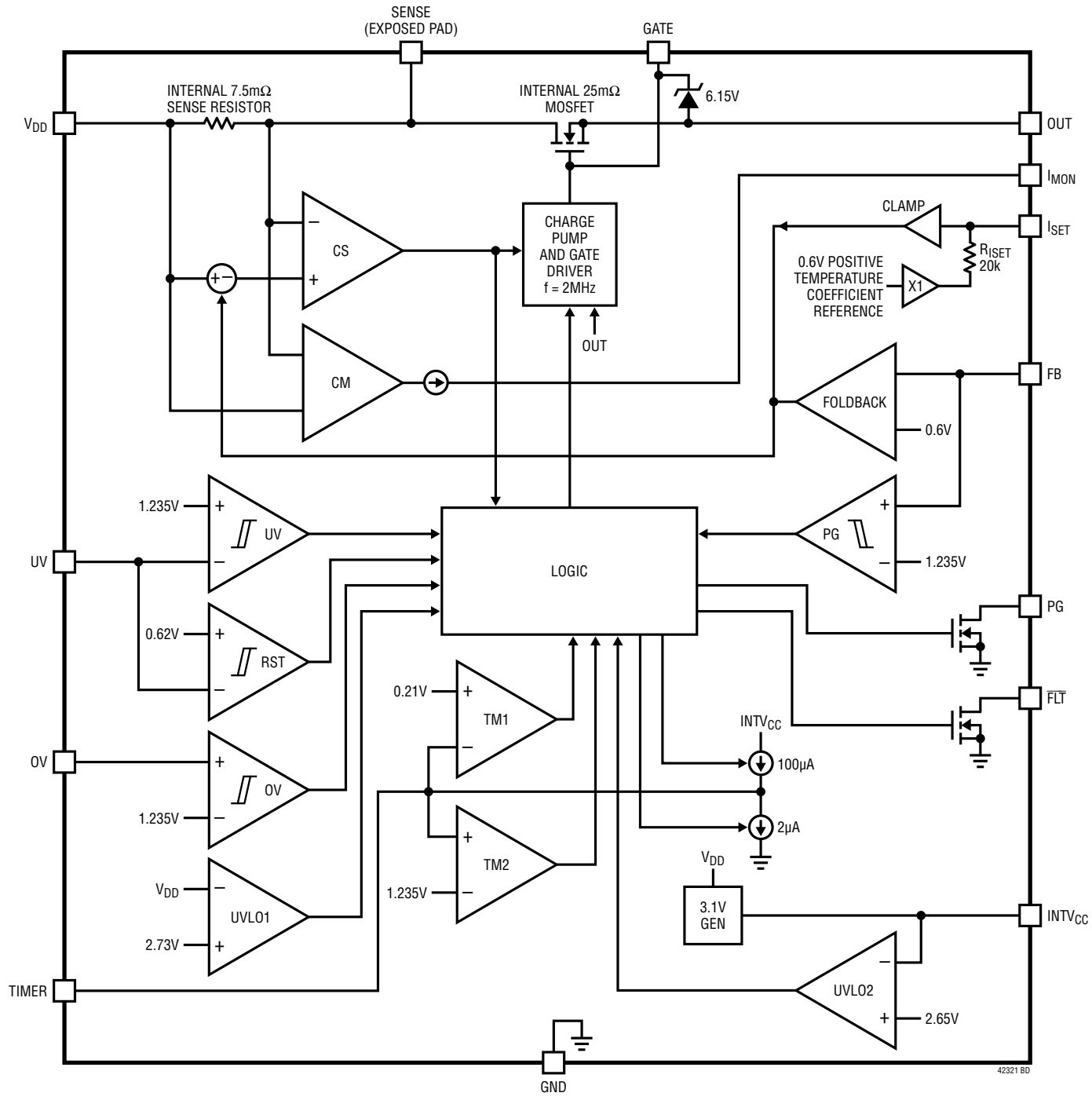
SENSE: Current Sense Node and MOSFET Drain. The current limit circuit controls the GATE pin to limit the sense voltage between the V_{DD} and SENSE pins to 42mV (5.6A) or less depending on the voltage at the FB pin. The exposed pad on DHC packages are connected to SENSE and must be soldered to an electrically isolated printed circuit board trace to properly transfer the heat out of the package.

TIMER: Timer Input. Connect a capacitor between this pin and ground to set a 12ms/µF duration for current limit before the switch is turned off. If the UV pin is toggled low while the MOSFET switch is off, the switch will turn on again following a cooldown time of 518ms/µF duration. Tie this pin to $INTV_{CC}$ for a fixed 2ms overcurrent delay. Note that the fixed 2ms overcurrent delay is not recommended when auto-retry is enabled (see Applications Information).

UV: Undervoltage Comparator Input. Tie high if unused. Connect this pin to an external resistive divider from V_{DD}. If the UV pin voltage falls below 1.15V, an undervoltage is detected and the switch turns off. Pulling this pin below 0.62V resets the overcurrent fault and allows the switch to turn back on (see the Applications Information section for details). If overcurrent auto-retry is desired then tie this pin to the $\overline{FLT}$ pin.

V_{DD}: Supply Voltage and Current Sense Input. This pin has an undervoltage lockout threshold of 2.73V.

FUNCTIONAL DIAGRAM



OPERATION

The Functional Diagram displays the main circuits of the device. The LTC4232-1 is designed to turn a board's supply voltage on and off in a controlled manner allowing the board to be safely inserted and removed from a live backplane. The LTC4232-1 includes a 25mΩ MOSFET and a 7.5mΩ current sense resistor. During normal operation, the charge pump and gate driver turn on the pass MOSFET's gate to provide power to the load. The inrush current control is accomplished by a resistor and capacitor network connected to the GATE pin. This circuit limits the GATE ramp rate and hence controls the voltage ramp rate of the output capacitor.

The current sense (CS) amplifier monitors the load current using the voltage sensed across the current sense resistor. The CS amplifier limits the current in the load by reducing the GATE-to-OUT voltage in an active control loop. It is simple to adjust the current limit threshold using the current limit adjustment (I_{SET}) pin. This allows a different threshold during other times such as start-up.

A short circuit on the output to ground causes significant power dissipation during active current limiting. To limit this power, the foldback amplifier reduces the current limit value from 5.6A to 1.5A in a linear manner as the FB pin drops below 0.6V (see the Typical Performance Characteristics section).

If an overcurrent condition persists, the TIMER pin ramps up with a 100µA current source until the pin voltage exceeds 1.235V (comparator TM2). This indicates to the logic that it is time to turn off the pass MOSFET to prevent overheating. At this point the TIMER pin ramps down using the 2µA current source until the voltage drops below 0.21V (Comparator TM1) which tells the logic to start an internal 16ms timer. At this point, the pass transistor has cooled and it is safe to turn it on again. Latchoff is the normal operating condition following overcurrent turn-off. Retry is initiated by pulling the UV pin low for a minimum of 1µs then high. Auto-retry is implemented by tying the $\overline{FLT}$ to the UV pin.

The output voltage is monitored using the FB pin and the PG comparator to determine if the power is available for the load. The power good condition is signaled by the PG pin using an open-drain pull-down transistor.

The Functional Diagram also shows the monitoring blocks of the LTC4232-1. The two comparators on the left side include the UV and OV comparators. These comparators determine if the external conditions are valid prior to turning on the MOSFET. But first the undervoltage lockout circuits UVLO1 and UVLO2 must validate the input supply and the internally generated 3.1V supply ($INTV_{CC}$) and generate the power up initialization to the logic circuits. If the external conditions remain valid for 16ms the MOSFET is allowed to turn on.

Other features include MOSFET current and temperature monitoring. The current monitor (CM) outputs a current proportional to the sense resistor current. This current can drive an external resistor or other circuits for monitoring purposes. A voltage proportional to the MOSFET temperature is output to the I_{SET} pin. The MOSFET is protected by a thermal shutdown circuit.

APPLICATIONS INFORMATION

The typical LTC4232-1 application is in a high availability system that uses a positive voltage supply to distribute power to individual cards. A complete application circuit is shown in Figure 1. External component selection is discussed in detail in the following sections.

Turn-On Sequence

Several conditions must be present before the internal pass MOSFET can be turned on. First the supply V_{DD} must exceed its undervoltage lockout level. Next the internally generated supply $INTV_{CC}$ must cross its 2.65V undervoltage threshold. This generates a 25µs power-on-reset pulse which clears the fault register and initializes internal latches.

After the power-on-reset pulse, the UV and OV pins must indicate that the input voltage is within the acceptable range. All of these conditions must be satisfied for the duration of 16ms to ensure that any contact bounce during the insertion has ended.

The MOSFET is turned on by charging up the GATE with a 24µA charge pump generated current source (Figure 2).

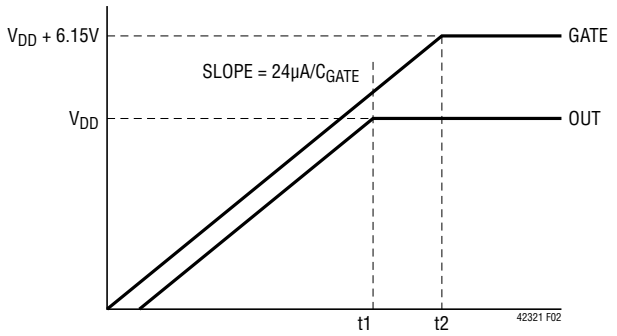


Figure 2. Supply Turn-On

The voltage at the GATE pin rises with a slope equal to $24\mu A/C_{GATE}$ and the supply inrush current is set at:

$$I_{INRUSH} = \frac{C_L}{C_{GATE}} \bullet 24\mu A$$

When the GATE voltage reaches the MOSFET threshold voltage, the switch begins to turn on and the OUT voltage follows the GATE voltage as it increases. Once OUT reaches V_{DD}, the GATE will ramp up until clamped by the 6.15V Zener between GATE and OUT.

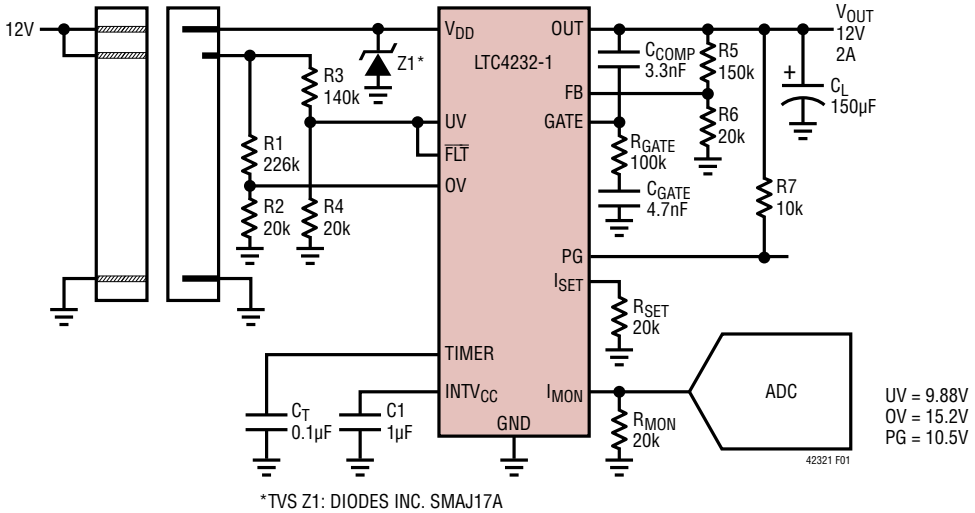


Figure 1. 2A, 12V Card Resident Application

APPLICATIONS INFORMATION

As the OUT voltage rises, so will the FB pin which is monitoring it. Once the FB pin crosses its 1.235V threshold and the GATE to OUT voltage exceeds 4.2V, the PG pin will cease to pull low and indicate that the power is good.

Parasitic MOSFET Oscillation

When the N-channel MOSFET ramps up the output during power-up it operates as a source follower. The source follower configuration may self-oscillate in the range of 25kHz to 300kHz when the load capacitance is less than 10µF, especially if the wiring inductance from the supply to the V_{DD} pin is greater than 3µH. The possibility of oscillation will increase as the load current (during power-up) increases. There are two ways to prevent this type of oscillation. The simplest way is to avoid load capacitances below 10µF. For wiring inductance larger than 20µH, the minimum load capacitance may extend to 100µF. A second choice is to connect an external gate capacitor C_P >1.5nF as shown in Figure 3.

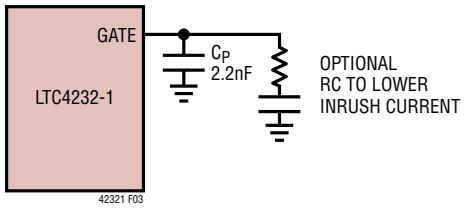


Figure 3. Compensation for Small C_{LOAD}

Turn-Off Sequence

The switch can be turned off by a variety of conditions. A normal turn-off is initiated by the UV pin going below its 1.235V threshold. Additionally, several fault conditions will turn off the switch. These include an input overvoltage (OV pin), overcurrent circuit breaker (SENSE pin) or overtemperature. Normally the switch is turned off with a 250µA current pulling down the GATE pin to ground. With the switch turned off, the OUT voltage drops which pulls the FB pin below its threshold. PG then pulls low to indicate output power is no longer good.

If V_{DD} drops below 2.65V for greater than 5µs or $INTV_{CC}$ drops below 2.5V for greater than 1µs, a fast shutdown of the switch is initiated. The GATE is pulled down with a 140mA current to the OUT pin.

Overcurrent Fault

The LTC4232-1 features an adjustable current limit with foldback that protects against short-circuits and excessive load current. To prevent excessive power dissipation in the switch during active current limit, the available current is reduced as a function of the output voltage sensed by the FB pin. A graph in the Typical Performance Characteristics curves shows the Current Limit Threshold Foldback.

An overcurrent fault occurs when the current limit circuitry has been engaged for longer than the timeout delay set by the TIMER. Current limiting begins when the MOSFET current reaches 1.5A to 5.6A (depending on the foldback). The GATE pin is then brought down with a 140mA GATE-to-OUT current. The voltage on the GATE is regulated in order to limit the current to less than 5.6A. At this point, a circuit breaker time delay starts by charging the external timing capacitor with a 100µA pull-up current from the TIMER pin. If the TIMER pin reaches its 1.235V threshold, the internal switch turns off (with a 250µA current from GATE to ground). Included in the Typical Performance Characteristics curves is a graph of the Safe Operating Area for the MOSFET. From this graph one can determine the MOSFET's maximum time in current limit for a given output power.

Tying the TIMER pin to $INTV_{CC}$ will force the part to use the internally generated (circuit breaker) delay of 2ms. In either case the $\overline{FLT}$ pin is pulled low to indicate an overcurrent fault has turned off the pass MOSFET. For a given circuit breaker time delay, the equation for setting the timing capacitor's value is as follows:

$$C_T = t_{CB} \bullet 0.083[\mu F/ms]$$

APPLICATIONS INFORMATION

After the switch is turned off, the TIMER pin begins discharging the timing capacitor with a 2µA pull-down current. When the TIMER pin reaches its 0.21V threshold, an internal 16ms timer is started. After the 16ms delay, the switch is allowed to turn on again if the overcurrent fault latch has been cleared. Bringing the UV pin below 0.6V for minimum of 1µs and then high will clear the fault latch. If the TIMER pin is tied to $INTV_{CC}$ then the switch is allowed to turn on again (after an internal 16ms delay), if the overcurrent fault latch is cleared.

Tying the $\overline{FLT}$ pin to the UV pin allows the part to self-clear the fault and turn the MOSFET on as soon as TIMER pin has ramped below 0.21V. In this auto-retry mode the LTC4232-1 repeatedly tries to turn on after an overcurrent at a period determined by the capacitor on the TIMER pin. When the TIMER pin is tied to $INTV_{CC}$ the internal 16ms turn-on delay is not sufficient to prevent overheating during auto-retry into a shorted load. Using an external timing capacitor is recommended when using auto-retry mode.

The waveform in Figure 4 shows how the output latches off following a short-circuit. The current in the MOSFET is 1.4A as the timer ramps up.

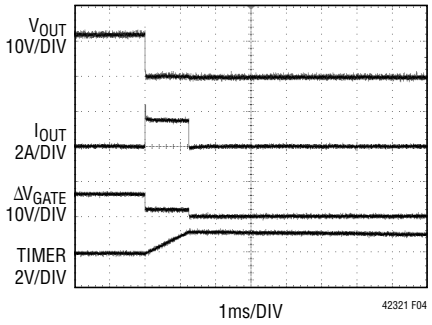


Figure 4. Short-Circuit Waveform

The R_{GATE}, C_{GATE} and C_{COMP} network on the GATE pin compensates the current limit regulation loop. It is possible to eliminate C_{COMP} and use only the R_{GATE} and C_{GATE} network, which will require R_{GATE} to reduce to 270Ω (see Figure 5). This alternate compensation with one less component allows the GATE pin to undershoot during a short circuit on the output and chatter as it settles. This chatter could last about 1µs to 2µs for every nF of C_{GATE} capacitance.

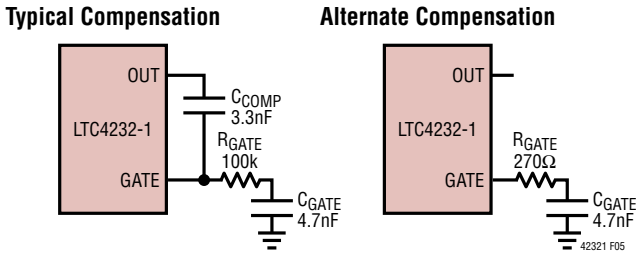


Figure 5. Compensation Components on the GATE Pin

Current Limit Adjustment

The default value of the active current limit is 5.6A. The current limit threshold can be adjusted lower by placing a resistor between the I_{SET} pin and ground. As shown in the Functional Block Diagram the voltage at the I_{SET} pin (via the clamp circuit) sets the CS amplifier's built-in offset voltage. This offset voltage directly determines the active current limit value. With the I_{SET} pin open, the voltage at the I_{SET} pin is determined by a positive temperature coefficient reference. This voltage is set to 0.618V at room temperature which corresponds to a 5.6A current limit at room temperature.

An external resistor R_{SET} placed between the I_{SET} pin and ground forms a resistive divider with the internal 20k R_{ISET} sourcing resistor. The divider acts to lower the voltage at the I_{SET} pin and therefore lower the current limit threshold. The overall current limit threshold precision is reduced to ±12% when using a 20k resistor to halve the threshold.

Using a switch (connected to ground) in series with R_{SET} allows the active current limit to change only when the switch is closed. This feature can be used to program a reduced running current while the maximum available current limit is used at startup.

APPLICATIONS INFORMATION

Monitor MOSFET Temperature

The voltage at the I_{SET} pin increases linearly with increasing temperature. The temperature profile of the I_{SET} pin is shown in the Typical Performance Characteristics section. Using a comparator or ADC to measure the I_{SET} voltage provides an indicator of the MOSFET temperature.

The I_{SET} voltage follows the formula:

$$V_{ISET} = \frac{R_{SET}}{R_{SET} + R_{ISET}} \bullet (T + 273°C) \bullet 2.093\,[mV/°C]$$

The MOSFET temperature is calculated using R_{ISET} of 20k.

$$T = \frac{(R_{SET} + 20k) \bullet V_{ISET}}{R_{SET} \bullet 2.093\,[mV/°C]} - 273°C$$

When R_{SET} is not present, T becomes:

$$T = \frac{V_{ISET}}{2.093\,[mV/°C]} - 273°C$$

There is an overtemperature circuit in the LTC4232-1 that monitors an internal voltage similar to the I_{SET} pin voltage. When the die temperature exceeds 145°C the circuit turns off the MOSFET until the temperature drops to 125°C.

Monitor MOSFET Current

The current in the MOSFET passes through an internal 7.5mΩ sense resistor. The voltage on the sense resistor is converted to a current that is sourced out of the I_{MON} pin. The gain of I_{SENSE} amplifier is 20µA/A referenced from the MOSFET current. This output current can be converted to a voltage using an external resistor to drive a comparator or ADC. The voltage compliance for the I_{MON} pin is from 0V to $INTV_{CC}$ – 0.7V.

A microcontroller with a built-in comparator can build a simple integrating single-slope ADC by resetting a capacitor that is charged with this current. When the capacitor voltage trips the comparator and the capacitor is reset, a timer is started. The time between resets will indicate the MOSFET current.

Monitor OV and UV Faults

Protecting the load from an overvoltage condition is the main function of the OV pin. In Figure 1 an external resistive divider (driving the OV pin) connects to a comparator to turn off the MOSFET when the V_{DD} voltage exceeds 15.2V. If the V_{DD} pin subsequently falls back below 14.9V, the switch will be allowed to turn on immediately. In the LTC4232-1 the OV pin threshold is 1.235V when rising, and 1.215V when falling out of overvoltage.

The UV pin functions as an undervoltage protection pin or as an "ON" pin. In the Figure 1 application the MOSFET turns off when V_{DD} falls below 9.23V. If the V_{DD} pin subsequently rises above 9.88V for 100ms, the switch will be allowed to turn on again. The LTC4232-1 UV turn-on/off thresholds are 1.235V (rising) and 1.155V (falling).

In the cases of an undervoltage or overvoltage the MOSFET turns off and there is indication on the PG status pin. When the overvoltage is removed the MOSFET's gate ramps up immediately.

Power Good Indication

In addition to setting the foldback current limit threshold, the FB pin is used to determine a power good condition. The Figure 1 application uses an external resistive divider on the OUT pin to drive the FB pin. The PG comparator indicates logic high when OUT pin rises above 10.5V. If the OUT pin subsequently falls below 10.3V the comparator toggles low. On the LTC4232-1 the PG comparator drives high when the FB pin rises above 1.235V and low when it falls below 1.215V.

APPLICATIONS INFORMATION

Once the PG comparator is high the GATE pin voltage is monitored with respect to the OUT pin. Once the GATE minus OUT voltage exceeds 4.2V the PG pin goes high. This indicates to the system that it is safe to load the OUT pin while the MOSFET is completely turned "on". The PG pin goes low when the GATE is commanded off (using the UV, OV or SENSE pins) or when the PG comparator drives low.

Design Example

Consider the following design example (Figure 6): V_{IN} = 12V, I_{MAX} = 5A. I_{INRUSH} = 750mA, C_L = 150µF, V_{UVON} = 9.88V, V_{OVOFF} = 15.2V, $V_{PGTHRESHOLD}$ = 10.5V. A current limit fault triggers an automatic restart of the power-up sequence.

The inrush current is set to 750mA using C_{GATE}:

$$C_{GATE} = C_L \frac{I_{GATE(UP)}}{I_{INRUSH}} = 150\mu F \frac{24\mu A}{750mA} \cong 4.7nF$$

Calculate the time it takes to charge C_L:

$$t_{CHARGEUP} = \frac{C_L \bullet V_{IN}}{I_{INRUSH}} = \frac{150\mu F \bullet 12V}{750mA} = 2.4ms$$

The peak power dissipation of 12V at 750mA (or 9W) must not exceed the SOA of the pass MOSFET for 2.4ms (see MOSFET SOA graph in the Typical Performance Characteristics section).

Next the power dissipated in the MOSFET during overcurrent must be limited. The active current limit uses a timer to prevent excessive energy dissipation in the MOSFET. The worst-case power dissipation occurs when the voltage versus current profile of the foldback current limit is at the maximum. This occurs when the current is 6.1A and the voltage is one half of the V_{IN} or 6V. See the Current Limit Threshold Foldback graph in the Typical Performance Characteristics section to view this profile. In order to survive 36W, the MOSFET SOA dictates a maximum time of 10ms (see SOA graph). Therefore, it is acceptable to set the current limit timeout using C_T to be 1.2ms:

$$C_T = \frac{1.2ms}{12[ms/\mu F]} = 0.1\mu F$$

After the 1.2ms timeout the $\overline{FLT}$ pin needs to pull-down on the UV pin to restart the power-up sequence.

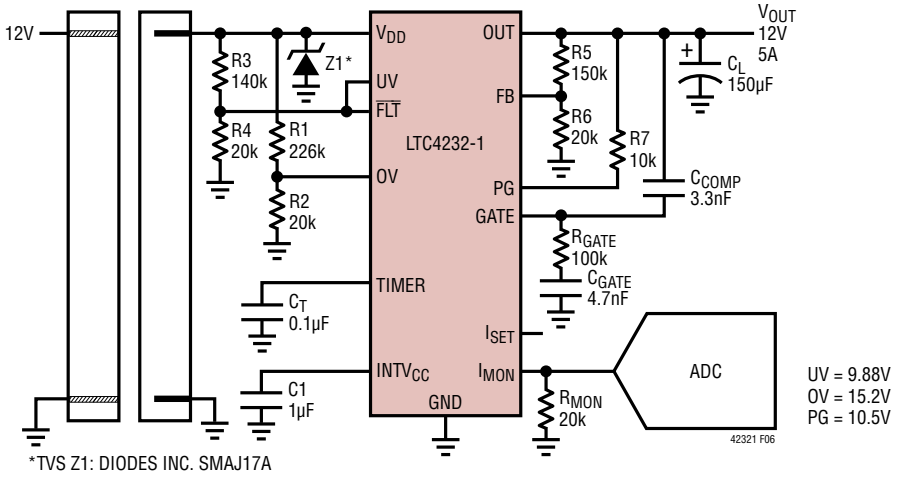


Figure 6. 5A, 12V Card Resident Application

APPLICATIONS INFORMATION

The values for overvoltage, undervoltage and power good thresholds using the resistive dividers on the UV, OV and FB pins match the requirements of turn-on at 9.88V and turn-off at 15.2V.

The final schematic in Figure 6 results in very few external components. The pull-up resistor, R7, connects to the PG pin while the 20k (R_{MON}) converts the I_{MON} current to a voltage at a ratio:

$$V_{IMON} = 20[\mu A/A] \bullet 20k \bullet I_{OUT} = 0.4[V/A] \bullet I_{OUT}$$

In addition there is a 1µF bypass (C1) on the $INTV_{CC}$ pin.

Layout Considerations

In Hot Swap applications where load currents can be 5A, narrow PCB tracks exhibit more resistance than wider tracks and operate at elevated temperatures. The minimum trace width for 1oz copper foil is 0.02" per amp to make sure the trace stays at a reasonable temperature. Using 0.03" per amp or wider is recommended. Note that 1oz copper exhibits a sheet resistance of about 0.5mΩ/square. Small resistances add up quickly in high current applications.

There are two V_{DD} pins on opposite sides of the package that connect to the sense resistor and MOSFET. The PCB layout should be balanced and symmetrical to each V_{DD} pin to balance current in the MOSFET bond wires. Figure 7 shows a recommended layout for the LTC4232-1.

Although the MOSFET is self protected from overtemperature, it is recommended to solder the backside of the package to a copper trace to provide a good heat sink. Note that the backside is connected to the SENSE pin and cannot be soldered to the ground plane. During normal loads the power dissipated in the MOSFET is as high as 1.9W. A 10mm × 10mm area of 1oz copper should be sufficient. This area of copper can be divided in many layers.

It is also important to put C1, the bypass capacitor for the $INTV_{CC}$ pin as close as possible between the $INTV_{CC}$ and GND.

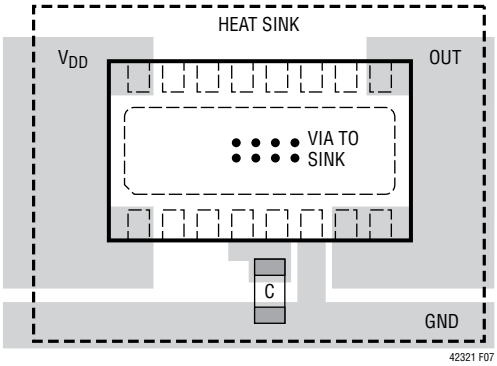


Figure 7. Recommended Layout

APPLICATIONS INFORMATION

Additional Applications

The LTC4232-1 has a wide operating range from 2.9V to 15V. The UV, OV and PG thresholds are set with few resistors. All other functions are independent of supply voltage.

In addition to Hot Swap applications, the LTC4232-1 also functions as a backplane resident switch for removable load cards (see Figure 8.)

The last page shows a 3.3V application with a UV threshold of 2.87V, an OV threshold of 3.77V and a PG threshold of 3.05V.

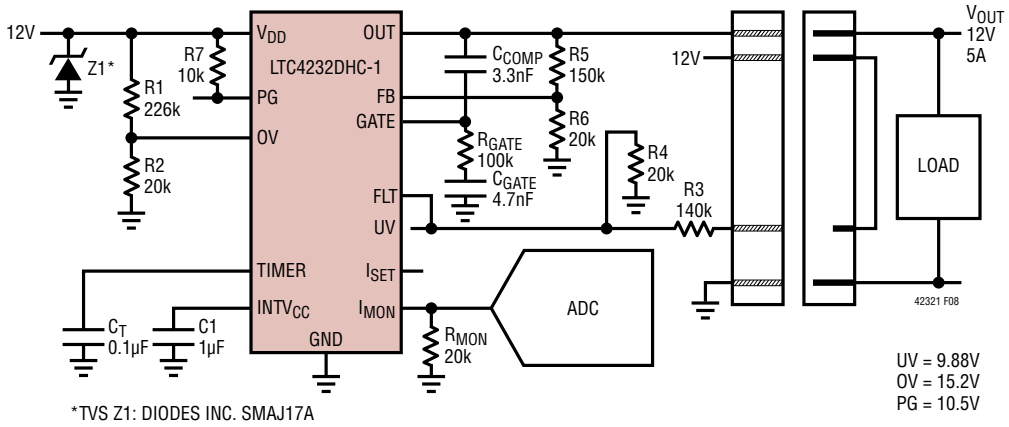
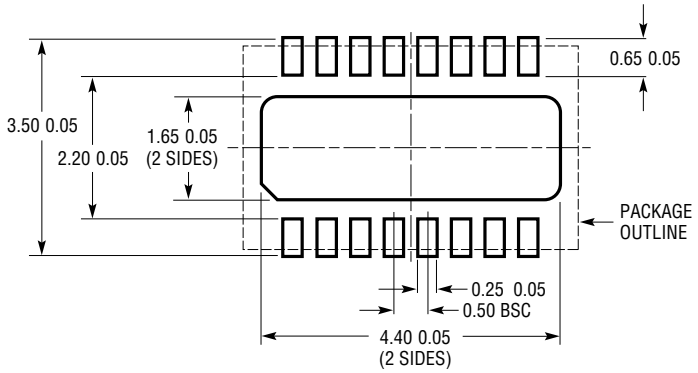


Figure 8. 12V, 5A Backplane Resident Application with Insertion Activated Turn-On

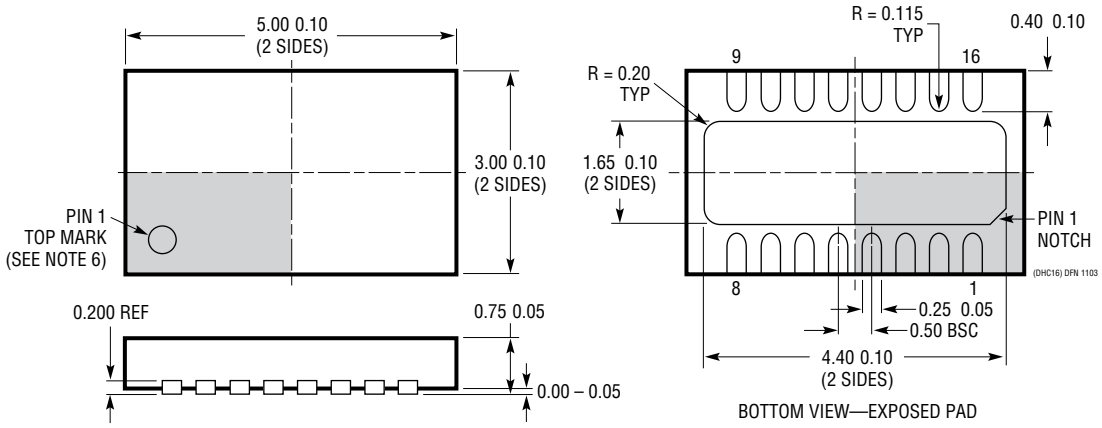
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC4232-1#packaging for the most recent package drawings.

DHC Package
16-Lead Plastic DFN (5mm × 3mm)
(Reference LTC DWG # 05-08-1706)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

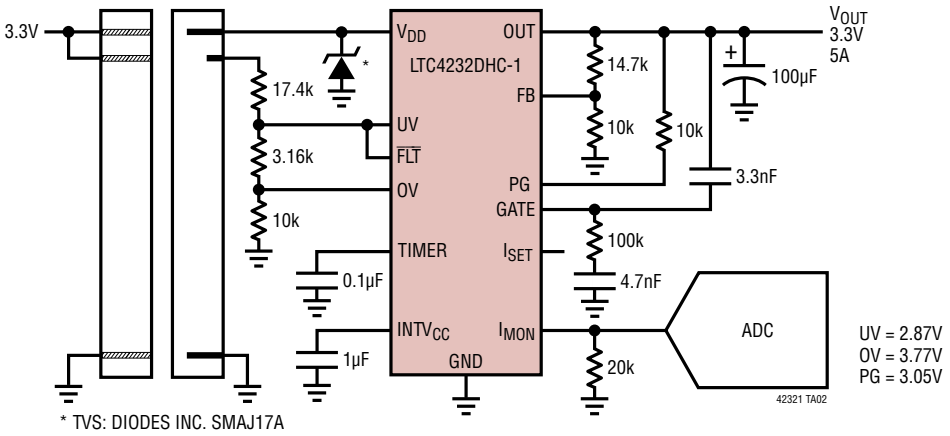
REV	DATE	DESCRIPTION	PAGE NUMBER
A	08/15	Raised $I_{GATE(DN)}$ maximum from 340µA to 400µA	3
B	01/16	Changed TVS to SMAJ17A in application circuit.	1, 9, 13, 15, 18
		Clarified that operating temperature range refers to ambient.	2
		Added BW_{IMON} and $t_{D(FAULT)}$ specifications.	3
		Updated $INTV_{CC}$ and I_{SET} pin functions.	6
		Added equations to calculate MOSFET temperature from V_{ISET}.	12

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

3.3V, 5A Card Resident Application with Auto-Retry



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4210	Single Channel, Hot Swap Controller	Operates from 2.7V to 16.5V, Active Current Limiting, SOT23-6
LTC4211	Single Channel, Hot Swap Controller	Operates from 2.5V to 16.5V, Multifunction Current Control, MSOP-8 or MSOP-10
LTC4212	Single Channel, Hot Swap Controller	Operates from 2.5V to 16.5V, Power-Up Timeout, MSOP-10
LTC4214	Negative Voltage, Hot Swap Controller	Operates from 0V to –16V, MSOP-10
LTC4215	Hot Swap Controller with I^2C Compatible Monitoring	Operates from 2.9V to 15V, 8-Bit ADC Monitors Current and Voltage
LTC4217	2A Integrated Hot Swap Controller	Operates from 2.9V to 26.5V, Adjustable 5% Accurate Current Limit
LTC4218	Hot Swap Controller with 5% Accurate (15mV) Current Limit	Operates from 2.9V to 26.5V, Adjustable Current Limit, SSOP-16, DFN-16
LTC4219	5A Integrated Hot Swap Controller	12V and 5V Preset Versions, 10% Accurate Current Limit
LT4220	Positive and Negative Voltage Dual Channels Hot Swap Controller	Operates from ±2.7V to ±16.5V, SSOP-16
LTC4221	Dual Hot Swap Controller/Sequencer	Operates from 1V to 13.5V, Multifunction Current Control, SSOP-16
LTC4230	Triple Channels Hot Swap Controller	Operates from 1.7V to 16.5V, Multifunction Current Control, SSOP-20
LTC4227	Dual Ideal Diode and Single Hot Swap Controller	Operates from 2.9V to 18V, PowerPath™ and Inrush Current Control for Redundant Supplies
LTC4228	Dual Ideal Diode and Hot Swap Controller	Operates from 2.9V to 18V, PowerPath and Inrush Current Control for Two Rails, MicroTCA, Redundant Power Supplies, and Supply Holdup Applications
LTC4233	10A Guaranteed SOA Hot Swap Controller	Operates from 2.9V to 15V, Adjustable 11% Accurate Current Limit
LTC4234	20A Guaranteed SOA Hot Swap Controller	Operates from 2.9V to 15V, Adjustable 11% Accurate Current Limit

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com/LTC4232-1
LT 0116 REV B • PRINTED IN USA
© LINEAR TECHNOLOGY CORPORATION 2014