20A Guaranteed SOA Hot Swap Controller

FEATURES

- **Allows Safe Board Insertion into Live Backplane**
- **Small Footprint**
- **4mΩ MOSFET Including R_{SENSE}**
- **Safe Operating Area Guaranteed at 81W, 30ms**
- **Wide Operating Voltage Range: 2.9V to 15V**
- **Adjustable, 11% Accurate Current Limit**
- Current and Temperature Monitor Outputs
- Overtemperature Protection
- Adjustable Current Limit Timer Before Fault
- Power Good and Fault Outputs
- Adjustable Inrush Current Control
- 2.5% Accurate Undervoltage and Overvoltage Protection
- Pin Compatible with LTC4233
- Available in a 38-Pin (5mm × 9mm) QFN Package

APPLICATIONS

- High Availability Servers
- Solid State Drives
- Industrial
- 240W, 12V Systems

DESCRIPTION

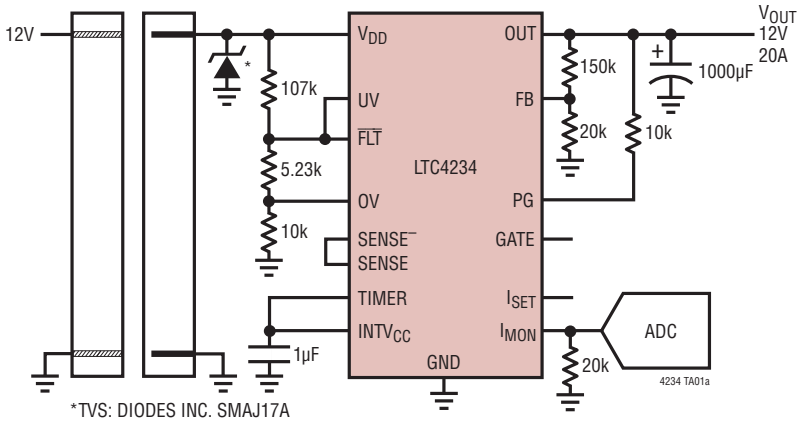
The LTC®4234 is an integrated solution for Hot Swap™ applications that allows a board to be safely inserted and removed from a live backplane. The part integrates a Hot Swap controller, power MOSFET and current sense resistor in a single package for small form factor applications. The MOSFET Safe Operating Area is production tested and guaranteed for the stresses in Hot Swap applications.

The LTC4234 provides separate inrush current control and an 11% accurate 22.5A current limit with output dependent foldback. The current limit threshold can be adjusted dynamically using the I_{SET} pin. Additional features include a current monitor output that amplifies the sense resistor voltage for ground referenced current sensing and a MOSFET temperature monitor output. Thermal limit, overvoltage, undervoltage and power good monitoring are also provided. For a 10A compatible version, see LTC4233.

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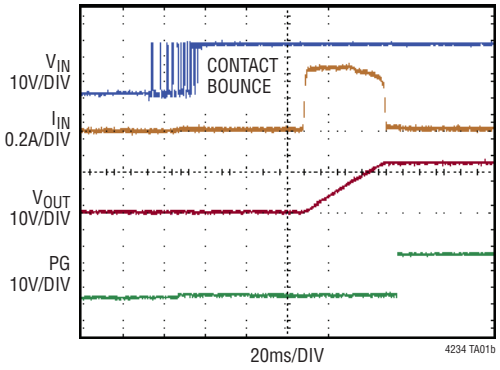
TYPICAL APPLICATION

12V, 20A Card Resident Application with Auto-Retry



*TVS: DIODES INC. SMAJ17A

Power-Up Waveform

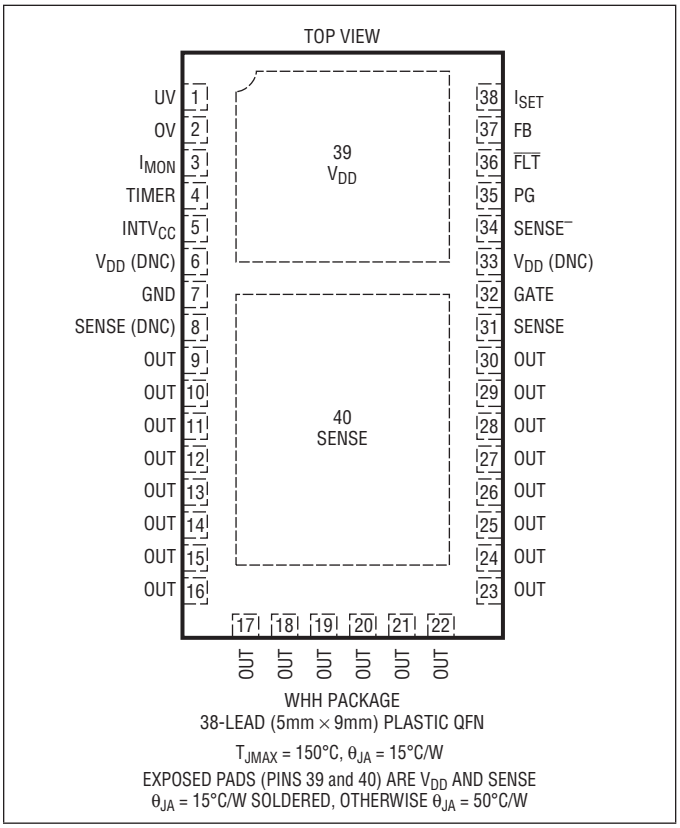


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD}) ..... –0.3V to 28V
Input Voltages
  FB, OV, UV ..... –0.3V to 12V
  TIMER ..... –0.3V to 3.5V
  $SENSE^-$, SENSE ..... V_{DD} – 10V or –0.3V to V_{DD} + 0.3V
Output Voltages
  I_{SET}, I_{MON} ..... –0.3V to 3V
  PG, $\overline{FLT}$ ..... –0.3V to 35V
  OUT ..... –0.3V to V_{DD} + 0.3V
  $INTV_{CC}$ ..... –0.3V to 3.5V
  GATE (Note 3) ..... –0.3V to 33V
Operating Ambient Temperature Range
  LTC4234C ..... 0°C to 70°C
  LTC4234I ..... –40°C to 85°C
  LTC4234H ..... –40°C to 125°C
Junction Temperature (Notes 4, 5) ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



WHH PACKAGE
38-LEAD (5mm × 9mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 15°C/W

EXPOSED PADS (PINS 39 and 40) ARE V_{DD} AND SENSE
θ_{JA} = 15°C/W SOLDERED, OTHERWISE θ_{JA} = 50°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4234CWHH#PBF	LTC4234CWHH#TRPBF	4234	38-Lead (5mm × 9mm) Plastic QFN	0°C to 70°C
LTC4234IWHH#PBF	LTC4234IWHH#TRPBF	4234	38-Lead (5mm × 9mm) Plastic QFN	–40°C to 85°C
LTC4234HWHH#PBF	LTC4234HWHH#TRPBF	4234	38-Lead (5mm × 9mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Characteristics							
V_{DD}	Input Supply Range		●	2.9		15	V
I_{DD}	Input Supply Current	MOSFET On, No Load	●		1.6	3	mA
$V_{DD(UVL)}$	Input Supply Undervoltage Lockout	V_{DD} Rising	●	2.63	2.73	2.85	V
I_{OUT}	OUT Leakage Current	V_{OUT} = V_{GATE} = 0V, V_{DD} = 15V V_{OUT} = V_{GATE} = 12V	● ●	 1	0 2	±700 4	µA µA
dV_{GATE}/dt	OUT Turn-On Ramp Rate	GATE Open	●	0.15	0.35	0.6	V/ms
R_{ON}	MOSFET + Sense Resistor On-Resistance	C-Grade, I-Grade H-Grade	● ●	2.3 2.3	4.0 4.0	7.2 8.2	mΩ mΩ
$I_{LIM(TH)}$	Current Limit Threshold	V_{FB} = 1.35V, I_{SET} Open V_{FB} = 0V, I_{SET} Open V_{FB} = 1.35V, R_{SET} = 20k	● ● ●	20 4 9.4	22.5 5.7 11.1	25 7.4 12.8	A A A
SOA	MOSFET Safe Operating Area	13.5V, 6A Folded Back, 200W^{2}s (Note 6) 7.5V, 22A Onset of Foldback, 200W^{2}s (Note 7)		30 7			ms ms
Inputs							
I_{IN}	OV, UV, FB Input Current	V = 1.2V	●		0	±1	µA
$I_{SENSE^-(IN)}$	$SENSE^-$ Input Current	V_{SENSE^-} = 12V	●		4	±10	µA
V_{TH}	OV, UV, FB Threshold Voltage	V_{PIN} Rising	●	1.205	1.235	1.265	V
$\Delta V_{OV(HYST)}$	OV Hysteresis		●	10	20	30	mV
$\Delta V_{UV(HYST)}$	UV Hysteresis		●	50	80	110	mV
$V_{UV(RTH)}$	UV Reset Threshold Voltage	V_{UV} Falling	●	0.55	0.62	0.7	V
$\Delta V_{FB(HYST)}$	FB Power Good Hysteresis		●	10	20	30	mV
R_{ISET}	I_{SET} Internal Resistor		●	19	20	21	kΩ
Outputs							
V_{INTVCC}	$INTV_{CC}$ Output Voltage	V_{DD} = 5V,15V, I_{LOAD} = 0mA, –10mA	●	2.8	3.1	3.3	V
V_{OL}	PG, $\overline{FLT}$ Output Low Voltage	I = 2mA	●		0.4	0.8	V
I_{OH}	PG , $\overline{FLT}$ Input Leakage Current	V = 30V	●		0	±10	µA
$V_{TIMER(H)}$	TIMER High Threshold	V_{TIMER} Rising	●	1.2	1.235	1.28	V
$V_{TIMER(L)}$	TIMER Low Threshold	V_{TIMER} Falling	●	0.1	0.21	0.3	V
$I_{TIMER(UP)}$	TIMER Pull-Up Current	V_{TIMER} = 0V	●	–80	–100	–120	µA
$I_{TIMER(DN)}$	TIMER Pull-Down Current	V_{TIMER} = 1.2V	●	1.4	2	2.6	µA
$I_{TIMER(RATIO)}$	TIMER Current Ratio $I_{TIMER(DN)}/I_{TIMER(UP)}$		●	1.6	2	2.7	%
A_{IMON}	I_{MON} Current Gain		●	4.5	5	5.25	µA/A
BW_{IMON}	I_{MON} Bandwidth				250		kHz
$I_{OFF(IMON)}$	I_{MON} Offset Current	I_{OUT} = 600mA	●		0	±9	µA
$I_{GATE(UP)}$	Gate Pull-Up Current	Gate Drive On, V_{GATE} = V_{OUT} = 12V	●	–18	–24	–29	µA
$I_{GATE(DN)}$	Gate Pull-Down Current	Gate Drive Off, V_{GATE} = 18V, V_{OUT} = 12V	●	180	250	500	µA
$I_{GATE(FST)}$	Gate Fast Pull-Down Current	Fast Turn Off, V_{GATE} = 18V, V_{OUT} = 12V			140		mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AC Characteristics							
$t_{PHL(GATE)}$	Input High (OV), Input Low (UV) to GATE Low Propagation Delay	V_{GATE} < 17.8V Falling	●		8	20	µs
$t_{PHL(ILIM)}$	Short Circuit to GATE Low	V_{FB} = 0, Step V_{DD} – SENSE⁻ to 50mV, V_{GATE} < 15V Falling	●		1	5	µs
$t_{D(ON)}$	Turn-On Delay	Step V_{UV} to 2V, V_{GATE} > 13V	●	24	48	72	ms
$t_{D(FAULT)}$	UV Low to Clear Fault Latch Delay				1		µs
$t_{D(CB)}$	Circuit Breaker Filter Delay Time (Internal)	V_{FB} = 0, Step V_{DD} – SENSE⁻ to 50mV	●	1.2	2	2.7	ms
$t_{D(COOL_DOWN)}$	Cool Down Delay (Internal)		●	600	900	1200	ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive; all voltages are referenced to GND unless otherwise specified.

Note 3: An internal clamp limits the GATE pin to a maximum of 6.5V above OUT. Driving this pin to voltages beyond the clamp may damage the device.

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 5: T_J is calculated from the ambient temperature, T_A, and power dissipation, P_D, according to the formula:

$$T_J = T_A + (P_D \bullet 15°C/W)$$

Note 6: SOA tested at room temperature. SOA (i.e. P^2t), is reduced at elevated temperatures according to the following formula:

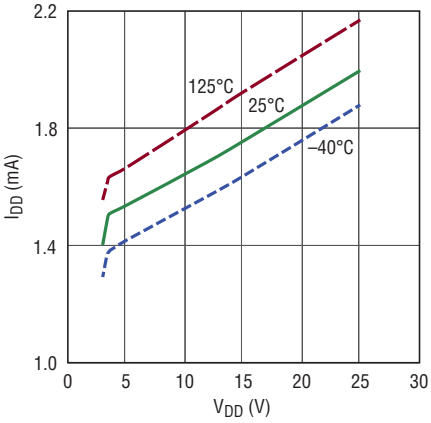
$$P^2t(T_J) = 200\left[W^2s\right] \bullet \left[\frac{150°C - T_J}{150°C - 25°C}\right]^2$$

Note 7: Guaranteed by design and extrapolated from P^2t limit of $200W^2s$.

TYPICAL PERFORMANCE CHARACTERISTICS

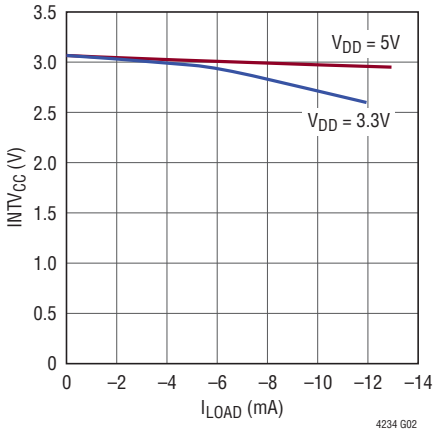
T_A = 25°C, V_{DD} = 12V unless otherwise noted.

I_{DD} vs V_{DD}



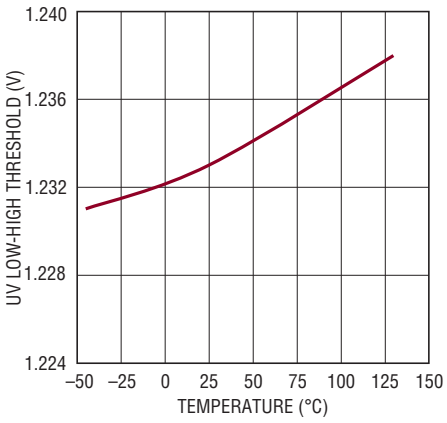
4234 G01

$INTV_{CC}$ Load Regulation



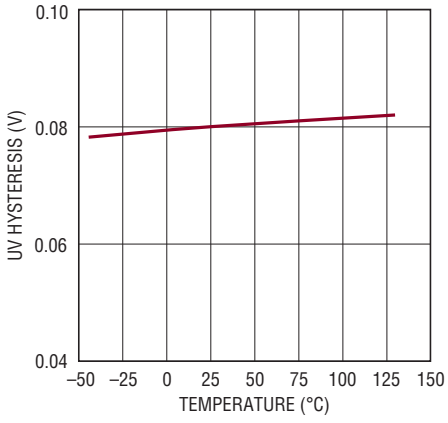
4234 G02

UV Low-High Threshold vs Temperature



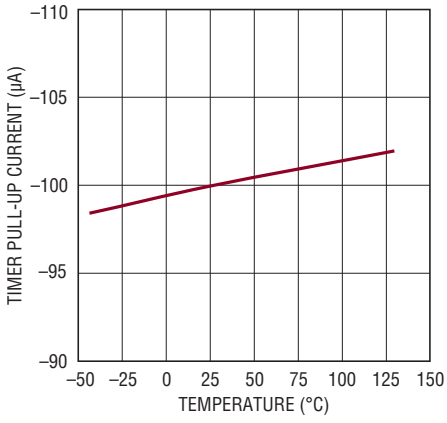
4234 G03

UV Hysteresis vs Temperature



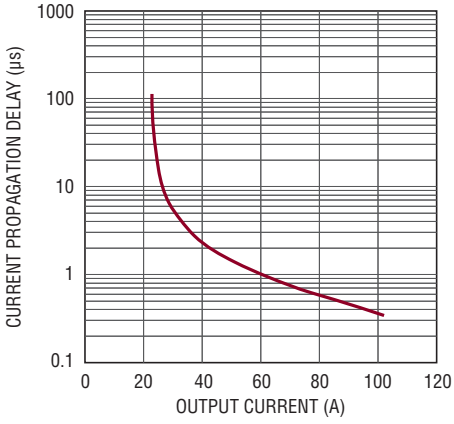
4234 G04

Timer Pull-Up Current vs Temperature



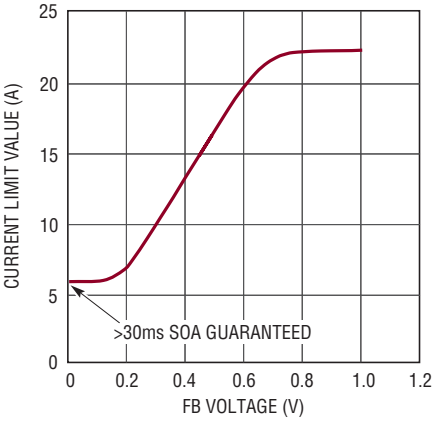
4234 G05

Current Limit Delay ($t_{PHL(ILIM)}$ vs Overdrive)



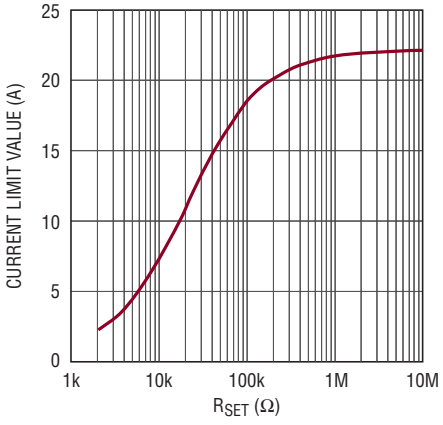
4234 G06

Current Limit Threshold Foldback



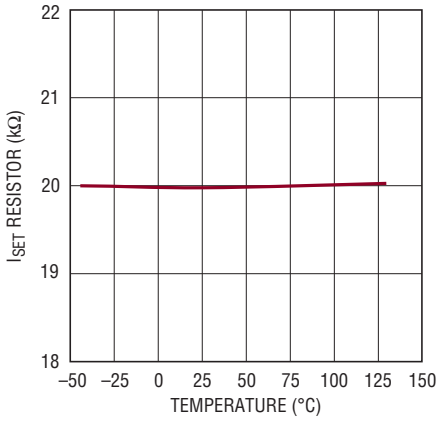
4234 G07

Current Limit Adjustment (I_{OUT} vs R_{SET})



4234 G08

R_{ISET} vs Temperature

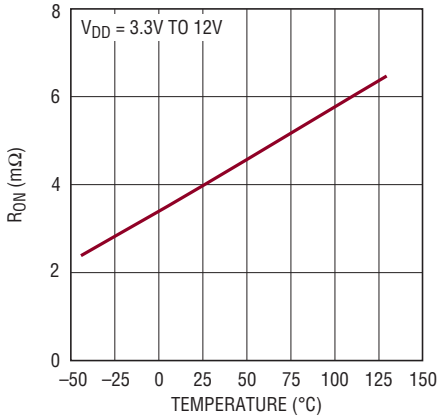


4234 G09

TYPICAL PERFORMANCE CHARACTERISTICS

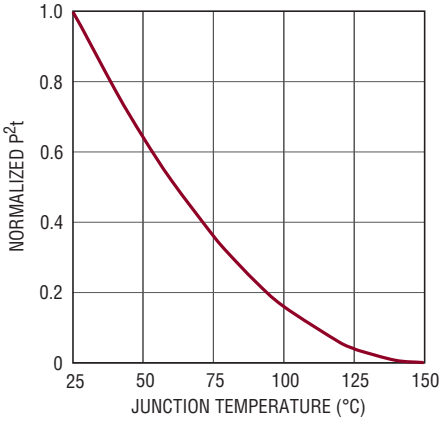
T_A = 25°C, V_{DD} = 12V unless otherwise noted.

R_{ON} vs V_{DD} and Temperature



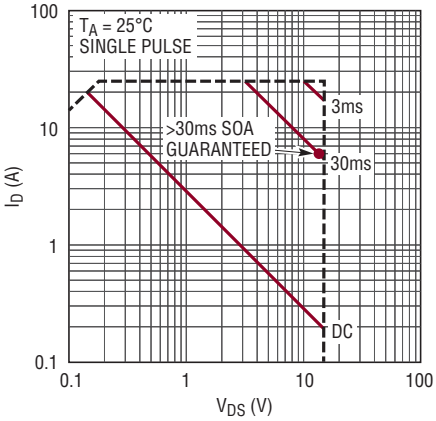
4234 G10

SOA Constant vs Junction Temperature



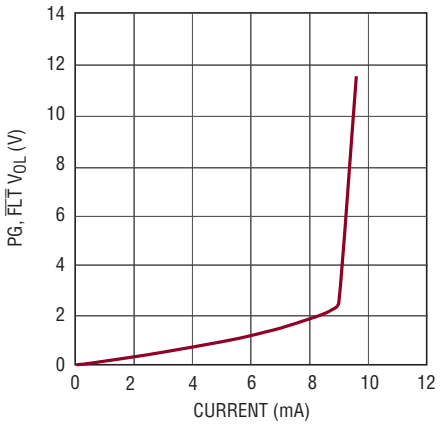
4234 G17

Guaranteed MOSFET SOA Curve



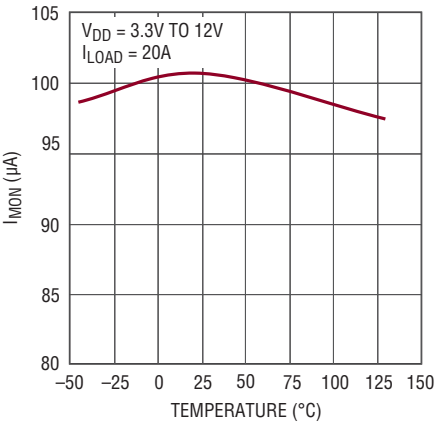
4234 G11

PG, $\overline{FLT}$ V_{OUT} Low vs I_{LOAD}



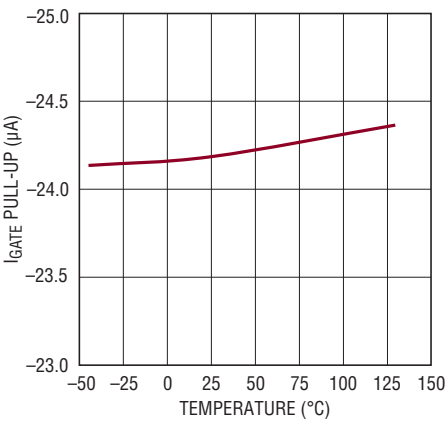
4234 G12

I_{MON} vs Temperature and V_{DD}



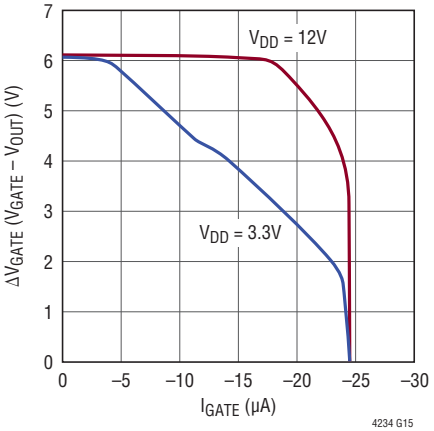
4234 G13

GATE Pull-Up Current vs Temperature



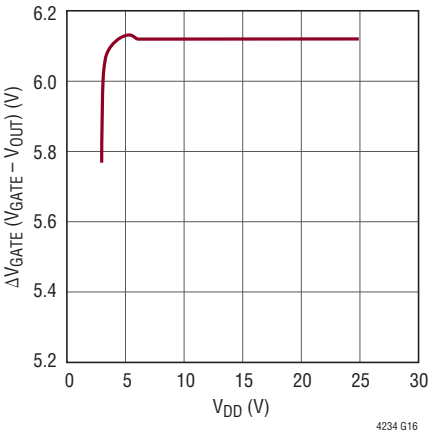
4234 G14

Gate Drive vs GATE Pull-Up Current



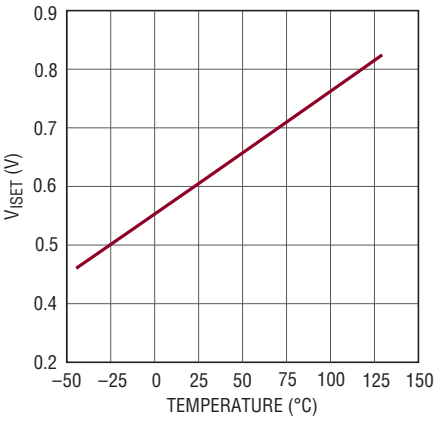
4234 G15

Gate Drive vs V_{DD}



4234 G16

V_{ISET} vs Temperature



4234 G18

PIN FUNCTIONS

DNC: Do Not Connect. Leave open.

FB: Foldback and Power Good Input. Connect this pin to an external resistive divider from OUT. If the voltage falls below 0.6V, the current limit is reduced using a foldback profile (see the Typical Performance Characteristics section). If the voltage falls below 1.21V, the PG pin will pull low to indicate the power is bad

$\overline{FLT}$: Overcurrent Fault Indicator. Open-drain output pulls low when an overcurrent fault has occurred and the circuit breaker trips. For overcurrent auto-retry tie to UV pin (see Applications Information section for details).

GATE: Gate Drive for Internal N-Channel MOSFET. An internal 24µA current source charges the gate of the N-channel MOSFET. At start-up the GATE pin ramps up at a 0.35V/ms rate determined by internal circuitry. During an undervoltage or overvoltage condition a 250µA pull-down current turns the MOSFET off. During a short circuit or undervoltage lockout condition, a 140mA pull-down current source between GATE and OUT is activated.

GND: Device Ground.

I_{MON}: Current Monitor Output. The current in the internal MOSFET switch is divided by 200,000 and sourced from this pin. Placing a 20k resistor on this pin allows a 0V to 2V voltage swing when current ranges from 0A to 20A.

$INTV_{CC}$: Internal 3.1V Supply Decoupling Output. This pin must have a 1.0µF or larger bypass capacitor. Overloading this pin can disrupt internal operation.

I_{SET}: Current Limit Adjustment Pin. For 22.5A current limit value, open this pin. This pin is driven by a 20k resistor in series with a voltage source. The pin voltage is used to generate the current limit threshold. The internal 20k resistor (R_{ISET}) and an external resistor (R_{SET}) between I_{SET} and ground create an attenuator that lowers the current limit value. Due to circuit tolerance R_{SET} should not be less than 2k. In order to match the temperature variation of the sense resistor, the voltage on this pin is made proportional to temperature of the MOSFET switch.

OUT: Output of Internal MOSFET Switch. Connect this pin directly to the load.

OV: Overvoltage Comparator Input. Connect this pin to an external resistive divider from V_{DD}. If the voltage at this pin rises above 1.235V, an overvoltage is detected and the switch turns off. Tie to GND if unused.

PG: Power Good Indicator. Open-drain output pulls low when the FB pin drops below 1.21V indicating the power is bad. If the voltage at FB rises above 1.235V and the GATE-to-OUT voltage exceeds 4.2V, the open-drain pull-down releases the PG pin to go high.

SENSE: Current Sense Node and MOSFET Drain. One exposed pad on the UH package is connected to SENSE and should be soldered to an electrically isolated printed circuit board trace to properly transfer the heat out of the package. Connect the SENSE pin 31 to the $SENSE^-$ pin 34.

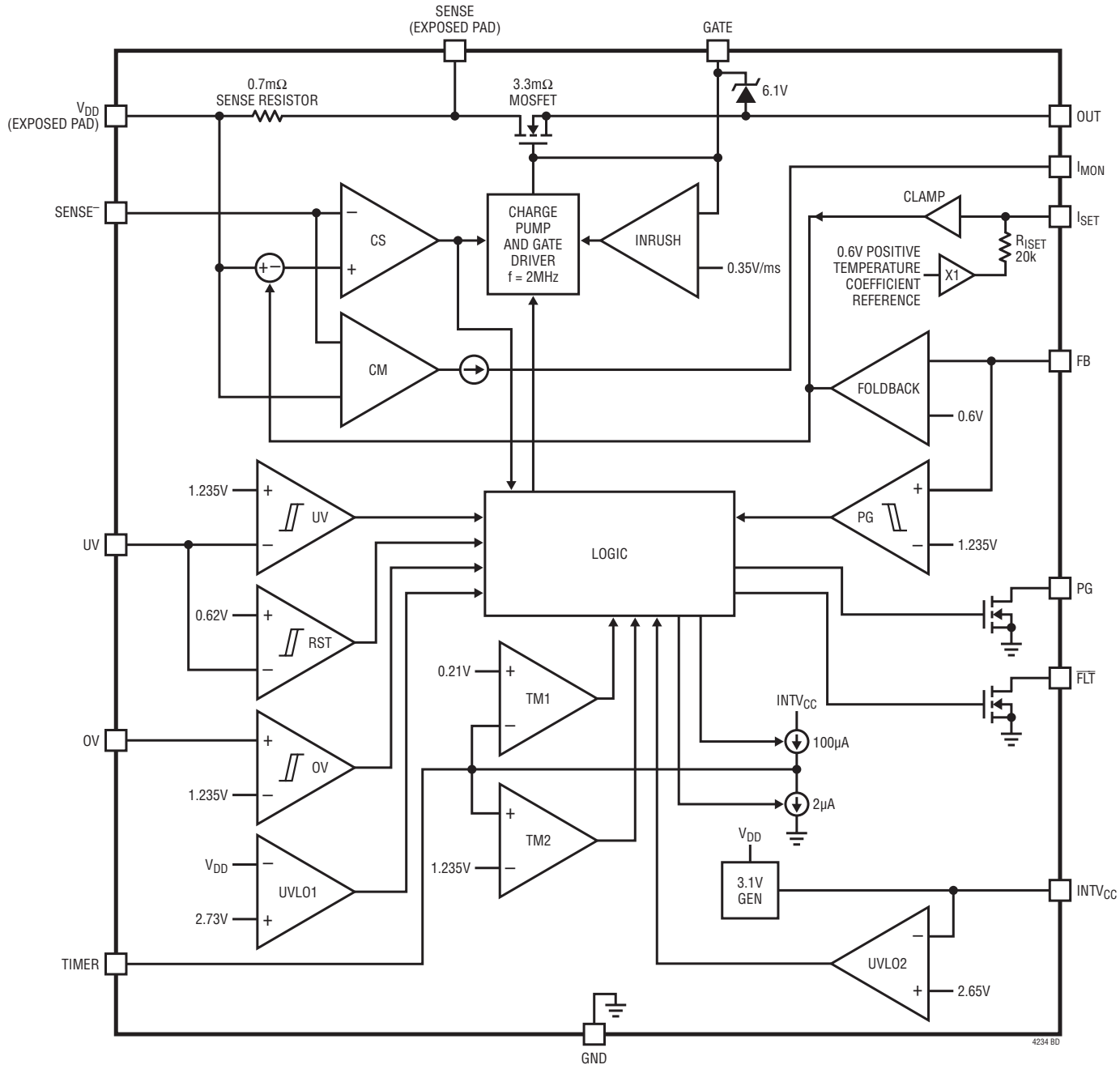
$SENSE^-$: Current Limit and Current Monitor Amplifier Input. The current limit circuit controls the GATE pin to limit the voltage between the V_{DD} and $SENSE^-$ pins to 15mV (22.5A) or less depending on the voltage at the FB pin. This pin must be connected to SENSE pin on the right side (connect Pin 34 to Pin 31).

TIMER: Current Limit Timer Input. Connect a capacitor between this pin and ground to set a 12ms/µF duration for current limit before the switch is turned off. If the UV pin is toggled low while the MOSFET switch is off, the switch will turn on again following cool down time of 4.14s/µF duration. Tie this pin to $INTV_{CC}$ for a fixed 2ms overcurrent delay and 900ms cool down time.

UV: Undervoltage Comparator Input. Tie high to $INTV_{CC}$ if unused. Connect this pin to an external resistive divider from V_{DD}. If the UV pin voltage falls below 1.15V, an undervoltage is detected and the switch turns off. Pulling this pin below 0.62V resets the overcurrent fault and allows the switch to turn back on (see Application Information section for details). If overcurrent auto-retry is desired then tie this pin to the $\overline{FLT}$ pin.

V_{DD}: Supply Voltage and Current Sense Input. This exposed pad must be soldered to input power. V_{DD} has an undervoltage lockout threshold of 2.73V.

FUNCTIONAL BLOCK DIAGRAM



OPERATION

The Functional Diagram displays the main circuits of the device. The LTC4234 is designed to turn a board's supply voltage on and off in a controlled manner allowing the board to be safely inserted and removed from a live backplane. The LTC4234 includes a 3.3mΩ MOSFET and a 0.7mΩ current sense resistor. During normal operation, the charge pump and gate driver turn on the pass MOSFET's gate to provide power to the load. The inrush current control is accomplished by the INRUSH circuit. This circuit limits the GATE ramp rate to 0.35V/ms and hence controls the voltage ramp rate of the output capacitor.

The current sense (CS) amplifier monitors the load current using the voltage sensed across the current sense resistor. The CS amplifier limits the current in the load by reducing the GATE-to-OUT voltage in an active control loop. It is simple to adjust the current limit threshold using the current limit adjustment (I_{SET}) pin. This allows a different threshold during other times such as start-up. Note there must be a connection between SENSE to $SENSE^-$ (Pin 34 to Pin 31) in order to monitor current.

A short circuit on the output to ground causes significant power dissipation during active current limiting. To limit this power, the foldback amplifier reduces the current limit value from 22.5A to 5.7A in a linear manner as the FB pin drops below 0.6V (see the Typical Performance Characteristics).

If an overcurrent condition persists, the TIMER pin ramps up with a 100µA current source until the pin voltage exceeds 1.235V (comparator TM2). This indicates to the logic that it is time to turn off the pass MOSFET to prevent overheating. At this point the TIMER pin ramps down using the 2µA current source until the voltage drops below 0.21V (Comparator TM1) which completes one timer cycle. After eight TIMER pin cycles (ramping to 1.235V and then below 0.21V) the logic starts the internal 48ms timer. At this point, the pass transistor has cooled and it is safe to turn it on again. It is suitable in many applications to use an internal 2ms overcurrent timer with a 900ms cool down period. Tying the TIMER pin to $INTV_{CC}$ sets this default timing. Latchoff is the normal operating condition following overcurrent turnoff. Retry is initiated by pulling the UV pin low for a minimum of 1µs then high. Auto-retry is implemented by tying the $\overline{FLT}$ to the UV pin.

The output voltage is monitored using the FB pin and the PG comparator to determine if power is available for the load. The power good condition is signaled by the PG pin using an open-drain pull-down transistor.

The Functional Diagram shows the monitoring blocks of the LTC4234. The two comparators on the left side include the UV and OV comparators. These comparators are used to determine if the external conditions are valid prior to turning on the MOSFET. But first the undervoltage lockout circuits UVLO1 and UVLO2 must validate the input supply and the internally generated 3.1V supply ($INTV_{CC}$) and generate the power up initialization to the logic circuits. If the external conditions remain valid for 48ms the MOSFET is allowed to turn on.

Other monitoring features include MOSFET current and temperature monitoring. The current monitor (CM) outputs a current proportional to the sense resistor current. This current can drive an external resistor or other circuits for monitoring purposes. A voltage proportional to the MOSFET temperature is output to the I_{SET} pin. The MOSFET is protected by a thermal shutdown circuit.

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The typical LTC4234 application is in a high availability system that uses a positive voltage supply to distribute power to individual cards. The complete application circuit is shown in Figure 1. External component selection is discussed in detail in the following sections.

Turn-On Sequence

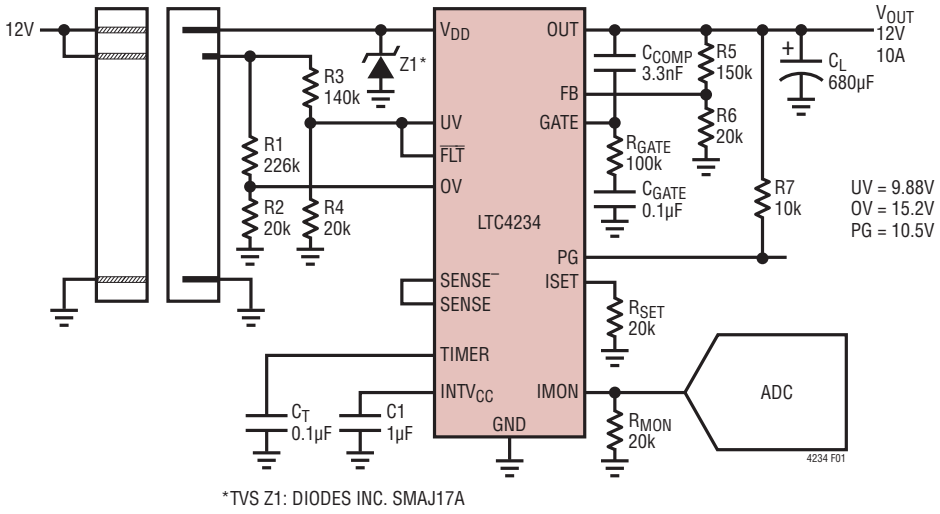
Several conditions must be present before the internal pass MOSFET can be turned on. First the supply V_{DD} must exceed its undervoltage lockout level. Next the internally generated supply $INTV_{CC}$ must cross its 2.65V undervoltage threshold. This generates a 25µs power-on-reset pulse which clears the fault register and initializes internal latches.

After the power-on-reset pulse, the UV and OV pins must indicate that the input voltage is within the acceptable range. All of these conditions must be satisfied for a duration of 48ms to ensure that any contact bounce during the insertion has ended.

The MOSFET is turned on by charging up the GATE with a charge pump generated 24µA current source whose value is adjusted by shunting a portion of the pull-up current to ground. The charging current is controlled by the INRUSH circuit that maintains a constant slope of GATE voltage versus time (Figure 2). The voltage at the GATE pin rises with a slope of 0.35[V/ms] and the supply inrush current is set at:

$$I_{INRUSH} = C_L \bullet 0.35[V/ms]$$

This gate slope is designed to charge up a 1000µF capacitor to 12V in 34ms, with an inrush current of 350mA. This



*TVS Z1: DIODES INC. SMAJ17A

Figure 1. 10A, 12V Card Resident Application

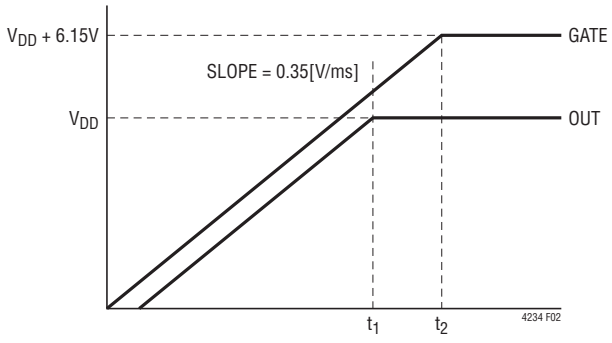


Figure 2. Supply Turn-On

APPLICATIONS INFORMATION

allows the inrush current to stay under the folded back current limit threshold (5.7A) for capacitors less than 10mF. Included in the Typical Performance Characteristics section is a graph of the Safe Operating Area for the MOSFET. It is evident from this graph that the power dissipation at 12V, 350mA for 34ms is in the safe region.

Adding a capacitor and a 100k series resistor from GATE to ground will lower the inrush current below the default value set by the INRUSH circuit. The 3.3nF capacitor, C_{COMP}, is necessary to compensate the current limit regulation loop when the R_{GATE} and C_{GATE} network is on the GATE pin. The GATE is charged with a 24µA current source (when the INRUSH circuit is not driving the GATE). The voltage at the GATE pin rises with a slope equal to 24µA/C_{GATE} and the supply inrush current is set at:

$$I_{INRUSH} = \frac{C_L}{C_{GATE}} \bullet 24\mu A$$

When the GATE voltage reaches the MOSFET threshold voltage, the switch begins to turn on and the OUT voltage follows the GATE voltage as it increases. Once OUT reaches V_{DD}, the GATE will ramp up until clamped by the 6.1V Zener between GATE and OUT.

As the OUT voltage rises, so will the FB pin which is monitoring it. Once the FB pin crosses its 1.235V threshold and the GATE to OUT voltage exceeds 4.2V, the PG pin will cease to pull low and indicate that the power is good.

Parasitic MOSFET Oscillation

When the N-channel MOSFET ramps up the output during power-up it operates as a source follower. The source follower configuration may self-oscillate in the range of 25kHz to 300kHz when the load capacitance is less than 10µF, especially if the wiring inductance from the supply to V_{DD} pin is greater than 3µH. The possibility of oscillations will increase as the load current (during power-up) increases. There are two ways to prevent this type of oscillation. The simplest way is to avoid load capacitances below 10µF. For wiring inductances larger than 20µH, the minimum load capacitance may extend to 100µF. A second choice is to connect an external gate capacitor C_P > 1.5nF as shown in Figure 3.

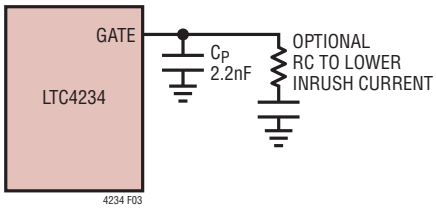


Figure 3. Compensation for Small C_{LOAD}

Turn-Off Sequence

The switch can be turned off by a variety of conditions. A normal turn-off is initiated by the UV pin going below its 1.235V threshold. Additionally, several fault conditions will turn off the switch. These include an input overvoltage (OV pin), overcurrent circuit breaker ($SENSE^-$ pin) or overtemperature. Normally the switch is turned off with a 250µA current pulling down the GATE pin to ground. With the switch turned off, the OUT voltage drops which pulls the FB pin below its threshold. The PG then pulls low to indicate output power is no longer good.

If V_{DD} drops below 2.65V for greater than 5µs or $INTV_{CC}$ drops below 2.5V for greater than 1µs, a fast shut down of the switch is initiated. The GATE is pulled down with a 140mA current to the OUT pin.

Overcurrent Fault

The LTC4234 features an adjustable current limit with foldback that protects against short circuits and excessive load current. To protect against excessive power dissipation in the switch during active current limit, the available current is reduced as a function of the output voltage sensed by the FB pin. A graph in the Typical Performance Characteristics curves shows the Current Limit Threshold Foldback.

An overcurrent fault occurs when the current limit circuitry has been engaged for longer than the timeout delay set by the TIMER. Current limiting begins when the MOSFET current reaches 5.7A to 22.5A (depending on the foldback). The GATE pin is then brought down with a 140mA GATE-to-OUT current. The voltage on the GATE is regulated in order to limit the current to 22.5A. At this point, a circuit breaker time delay starts by charging the external timing capacitor with a 100µA pull-up current from the TIMER

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pin. If the TIMER pin reaches its 1.235V threshold, the internal switch turns off (with a 250µA current from GATE to ground). Included in the Typical Performance Characteristics curves is a graph of the Safe Operating Area for the MOSFET. From this graph one can determine the MOSFET's maximum time in current limit for a given output power.

Tying the TIMER pin to $INTV_{CC}$ will force the part to use the internally generated (circuit breaker) delay of 2ms. In either case the $\overline{FLT}$ pin is pulled low to indicate an overcurrent fault has turned off the pass MOSFET. For a given circuit breaker time delay, the equation for setting the timing capacitor's value is as follows:

$$C_T = t_{CB} \bullet 0.083[\mu F/ms]$$

After the switch is turned off, the TIMER pin begins discharging the timing capacitor with a 2µA pull-down current. When the TIMER pin reaches its 0.21V threshold, it completes one timer cycle. After eight TIMER pin cycles (ramping to 1.235V and then below 0.21V) plus the 48ms debounce time, the switch is allowed to turn on again if the overcurrent fault latch has been cleared. Bringing the UV pin below 0.6V for a minimum of 1µs and then high will clear the fault latch. If the TIMER pin is tied to $INTV_{CC}$ then the switch is allowed to turn on again (after an internal 900ms cool down time plus the 48ms debounce time), if the overcurrent fault latch is cleared.

Tying the $\overline{FLT}$ pin to the UV pin allows the part to self-clear the fault and turn the MOSFET on as soon as TIMER pin has ramped below 0.21V for the eighth time followed by the 48ms debounce time. In this auto-retry mode the LTC4234 repeatedly tries to turn on after an overcurrent at a period determined by the capacitor on the TIMER pin. The auto retry mode also functions when the TIMER pin is tied to $INTV_{CC}$.

The waveform in Figure 4 shows how the output latches off following a short-circuit. The current in the MOSFET is 5.7A as the TIMER pin ramps up.

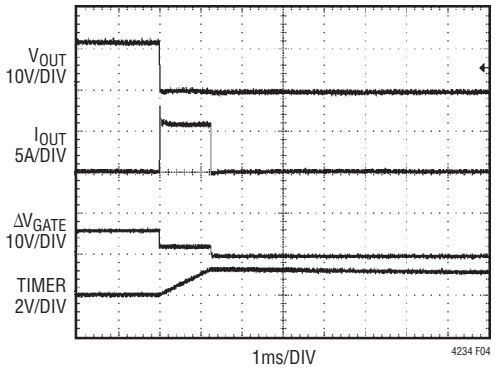


Figure 4. Short-Circuit Waveform

Current Limit Adjustment

The default value of the active current limit is 22.5A. The current limit threshold can be adjusted lower by placing a resistor between the I_{SET} pin and ground. As shown in the Functional Block Diagram the voltage at the I_{SET} pin (via the clamp circuit) sets the CS amplifier's built-in offset voltage. This offset voltage directly determines the active current limit value. With the I_{SET} pin open, the voltage at the I_{SET} pin is determined by a positive temperature coefficient reference. This voltage is set to 0.618V which corresponds to a 22.5A current limit at room temperature.

An external resistor R_{SET} placed between the I_{SET} pin and ground forms a resistive divider with the internal 20k R_{ISET} sourcing resistor. The divider acts to lower the voltage at the I_{SET} pin and therefore lower the current limit threshold. The overall current limit threshold precision is reduced to ±15% when using a 20k resistor to halve the threshold.

Using a switch (connected to ground) in series with R_{SET} allows the active current limit to change only when the switch is closed. This feature can be used to program a reduced running current while the maximum available current limit is used at start-up.

Monitor MOSFET Temperature

The voltage at the I_{SET} pin increases linearly with increasing temperature. The temperature profile of the I_{SET} pin is shown in the Typical Performance Characteristics section.

APPLICATIONS INFORMATION

Using a comparator or ADC to measure the I_{SET} voltage provides an accurate indication of the MOSFET temperature. The I_{SET} voltage follows the formula:

$$V_{ISET} = \frac{R_{SET}}{R_{SET} + R_{ISET}} \bullet (T + 273°C) \bullet 2.093[mV/°C]$$

The MOSFET temperature is calculated using R_{ISET} of 20k.

$$T = \frac{(R_{SET} + 20k) \bullet V_{ISET}}{R_{SET} \bullet 2.093[mV/°C]} - 273°C$$

When R_{SET} is not present, T becomes:

$$T = \frac{V_{ISET}}{2.093[mV/°C]} - 273°C$$

There is an overtemperature circuit in the LTC4234 that monitors an internal voltage similar to the I_{SET} pin voltage. When the die temperature exceeds 155°C the circuit turns off the MOSFET until the temperature drops to 135°C.

Monitor MOSFET Current

The current in the MOSFET passes through an internal 0.7mΩ sense resistor. The voltage on the sense resistor is converted to a current that is sourced out of the I_{MON} pin. The gain of I_{SENSE} amplifier is 5µA/A referenced from the MOSFET current. This output current can be converted to a voltage using an external resistor to drive a comparator or ADC. The voltage compliance for the I_{MON} pin is from 0V to $INTV_{CC}$ – 0.7V.

A microcontroller with a built-in comparator can build a simple integrating single-slope ADC by resetting a capacitor that is charged with this current. When the capacitor voltage trips the comparator and the capacitor is reset, a timer is started. The time between resets will indicate the MOSFET current.

Monitor OV and UV Faults

Protecting the load from an overvoltage condition is the main function of the OV pin. In Figure 1 an external resistive divider (driving the OV pin) connects to a comparator to turn off the MOSFET when the V_{DD} voltage exceeds 15.2V. If the V_{DD} pin subsequently falls back below 14.9V, the switch will be allowed to turn on immediately. In the LTC4234 the OV pin threshold is 1.235V when rising, and 1.215V when falling out of overvoltage.

The UV pin functions as an undervoltage protection pin or as an "ON" pin. In the Figure 1 application the MOSFET turns off when V_{DD} falls below 9.23V. If the V_{DD} pin subsequently rises above 9.88V for 48ms, the switch will be allowed to turn on again. The LTC4234 UV turn-on/off threshold are 1.235V (rising) and 1.155V (falling).

In the case of an undervoltage or overvoltage, the MOSFET turns off and there is indication on the PG status pin. When the overvoltage is removed, the MOSFET's gate ramps up immediately at the rate determined by the INRUSH circuit.

Power Good Indication

In addition to setting the foldback current limit threshold, the FB pin is used to determine a power good condition. The Figure 1 application uses an external resistive divider on the OUT pin to drive the FB pin. On the LTC4234 the PG comparator drives high when the FB pin rises above 1.235V and low when it falls below 1.215V.

Once the PG comparator is high the GATE pin voltage is monitored with respect to the OUT pin. Once the GATE minus OUT voltage exceeds 4.2V the PG pin goes high. This indicates to the system that it is safe to load the OUT pin while the MOSFET is completely turned "on". The PG pin goes low when the GATE is commanded off (using the UV, OV or $SENSE^-$ pins) or when the PG comparator drives low.

Design Example

Consider the following design example (Figure 5): T_A = 60°C, V_{IN} = 12V, I_{MAX} = 20A. I_{INRUSH} = 350mA, C_L = 1000µF, V_{UVON} = 9.88V, V_{OVOFF} = 15.2V, $V_{PGTHRESHOLD}$ = 10.5V. A current limit fault triggers an automatic restart of the power-up sequence.

APPLICATIONS INFORMATION

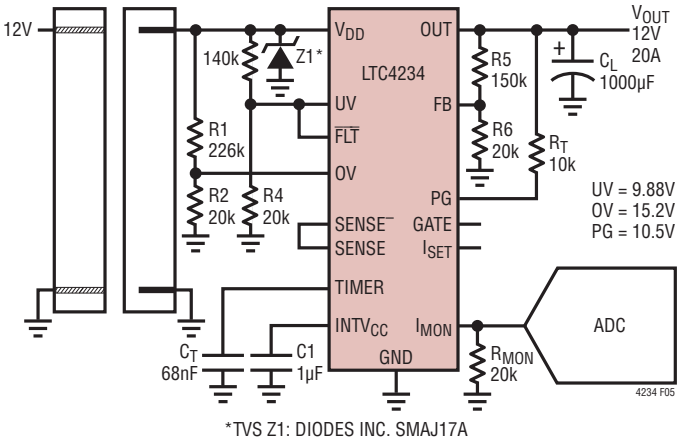


Figure 5. 20A, 12V Card Resident Application

The inrush current is defined by the current required to charge the output capacitor using the fixed 0.35V/ms GATE charge up rate. The inrush current is defined as:

$$I_{INRUSH} = C_L \bullet \left(\frac{0.35V}{ms}\right) = 1000\mu F \bullet \left(\frac{0.35V}{ms}\right) = 350mA$$

As mentioned previously the charge-up time is the output voltage (12V) divided by the output rate of 0.35V/ms resulting in 34ms. The peak power dissipation of 12V at 350mA (or 4.2W) must not exceed the SOA of the pass MOSFET for 34ms (see MOSFET SOA graph in the Typical Performance Characteristics). On the SOA graph the 30ms line crosses the 10V V_{DS} vertical line at 8A. This verifies that the 80W for 30ms is safe at room temperature. Each single point on the 8ms and 30ms lines represent a power (voltage times current) and time that follow a constant P^2t relationship of $200W^2s$. This constant P^2t number is valid for power pulses less than 50ms. Beyond 50ms the P^2t number will depend on the thermal characteristics of the board. If the MOSFET junction temperature is elevated, then the P^2t constant must be derated. At T_J = 60°C the new constant becomes:

$$P^2t(T_J = 60°C) = 200\left[W^2s\right] \bullet \left[\frac{150°C - 60°C}{150°C - 25°C}\right]^2 = 104\left[W^2s\right]$$

The maximum power for 34ms can be calculated from the derated constant:

$$P_{MAX} = \sqrt{\frac{P^2t(T_J = 60°C)}{\tau}} = \sqrt{\frac{104\left[W^2s\right]}{34ms}} = 55W$$

Therefore the power dissipation at charge-up is within the MOSFET SOA.

Next the power dissipated in the MOSFET during overcurrent must be limited. The active current limit uses a timer to prevent excessive energy dissipation in the MOSFET. The worst-case power dissipation occurs when the voltage versus current profile of the foldback current limit is at the maximum. This occurs when the current is 25A and the voltage is one-half of the V_{IN} or 6V. See the Current Limit Threshold Foldback in the Typical Performance Characteristics section to view this profile. In order to survive 150W, the MOSFET SOA dictates a maximum current limit timeout. If the MOSFET operating temperature is elevated prior to current limit the SOA constant must be derated according to the formula:

$$P^2t(T_J) = P^2t(25°C) \bullet \left[\frac{150°C - T_J}{150°C - 25°C}\right]^2$$

T_J is calculated from the ambient temperature, package thermal impedance (θ_{JA}) and the I^2R heating:

$T_J = (\theta_{JA} \bullet I^2 \bullet R_{ON}) + T_A = 15°C/W \bullet (20A)^2 \bullet 7.2m\Omega + 60°C = 103°C$

Use the SOA derating formula:

$$P^2t(T_J = 103°C) = 200\left[W^2S\right] \bullet \left[\frac{150°C - 103°C}{150°C - 25°C}\right]^2 = 28\left[W^2S\right]$$

So the SOA constant is derated to 28 W^2s. The maximum current limit timeout is calculated from the revised constant and the 150 W dissipated in current limit:

$$t_{MAX} = \frac{P^2t(T_J = 103°C)}{P^2} = \frac{28\left[W^2S\right]}{(150W)^2} = 1.2ms$$

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Therefore it is acceptable to set the current limit timeout using C_T to be 0.8ms:

$$C_T = \frac{0.8ms}{12[ms/\mu F]} = 68nF$$

To configure the LTC4234 for auto retry after overcurrent fault, connect the $\overline{FLT}$ to the UV pin.

After the 0.8ms timeout the $\overline{FLT}$ pin pulls down on the UV pin restart the power-up sequence.

The values for overvoltage, undervoltage and power good thresholds using the resistive dividers on the UV, OV and FB pins match the requirements of turn-on at 9.88V and turn-off at 15.2V.

The final schematic in Figure 5 results in very few external components. The pull-up resistor, R7, connects to the PG pin while the 20k (R_{MON}) converts the I_{MON} current to a voltage at a ratio:

$$V_{IMON} = 5[\mu A/A] \bullet 20k \bullet I_{OUT} = 0.1[V/A] \bullet I_{OUT}$$

In addition there is a 1µF bypass (C1) on the $INTV_{CC}$ pin and note the connection between SENSE to SENSE⁻ (Pin 34 to Pin 31).

Layout Considerations

In Hot Swap applications where load currents can be 20A, narrow PCB tracks exhibit more resistance than wider tracks and operate at elevated temperatures. The minimum trace width requirement for 1oz copper foil is 0.02" per amp to make sure the trace stays at a reasonable temperature. Using 0.03" per amp or wider is recommended. Note that 1oz copper exhibits a sheet resistance of about 0.5mΩ/square. Small resistances add up quickly in high current applications.

The input supply should be tied to V_{DD} exposed pad through a PCB trace that enters between Pin 1 and Pin 38. The V_{DD} pad connects to the sense resistor and MOSFET. Globally there are three DNC pins that are unconnected and left open (pins 6, 8, 33). Connect the SENSE⁻ pin (pin 34) to the SENSE pin (pin 31). Figure 6 shows a recommended layout for the LTC4234.

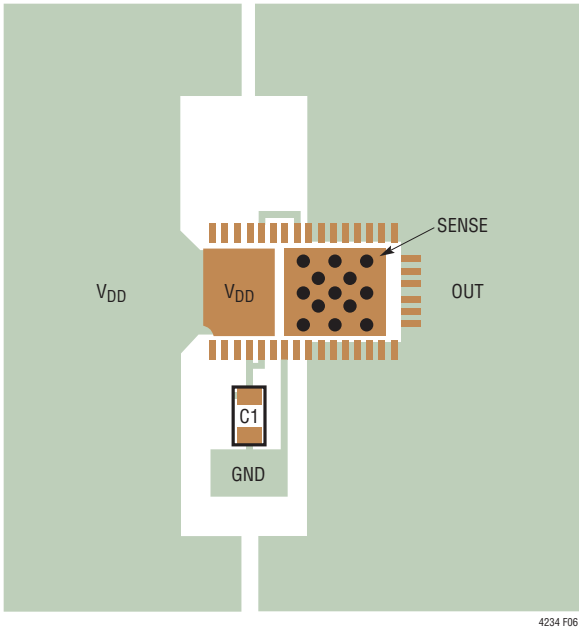


Figure 6. Recommended Layout

During normal operation the power dissipated in the MOSFET could be as high as 2.9W. To remove this heat solder the SENSE exposed pad to a copper trace that contains vias underneath the pad. The OUT pins conduct substantial heat from the MOSFET. Connect all the OUT pins to a plane of 1oz copper. Since the trace that connects OUT pins must accommodate high current, this area of copper is usually present. It is also important to put C1, the bypass capacitor for the $INTV_{CC}$ pin as close as possible between $INTV_{CC}$ and GND.

Thermal Considerations

The LTC4234 junction to board temperature rise in still air when the load current is 10A, 15A and 20A is shown in curves of Figure 7 and Figure 8. The junction temperature was measured at the package and the board temperature was measured at the board edge. This temperature rise falls as the board area is increases from 6.45cm^2 to 103cm^2. Two different SENSE pad areas are shown as separate figures.

This thermal test board uses 2oz copper on the top layer divided equally between V_{DD} and OUT traces similar to

APPLICATIONS INFORMATION

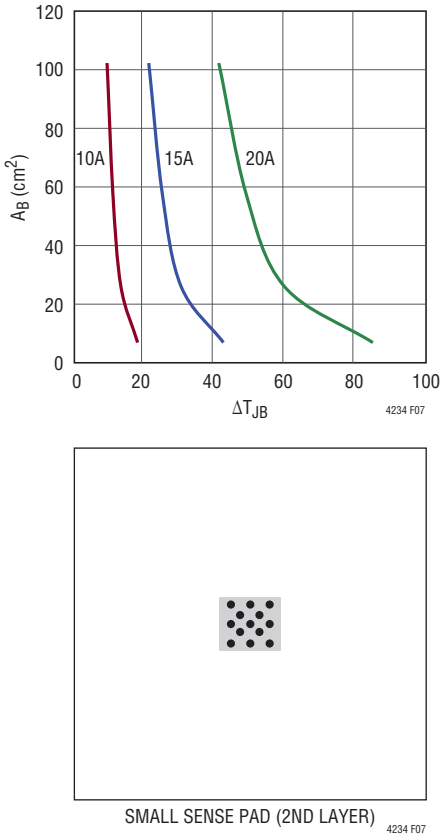


Figure 7. Temperature Rise for Small SENSE Pad

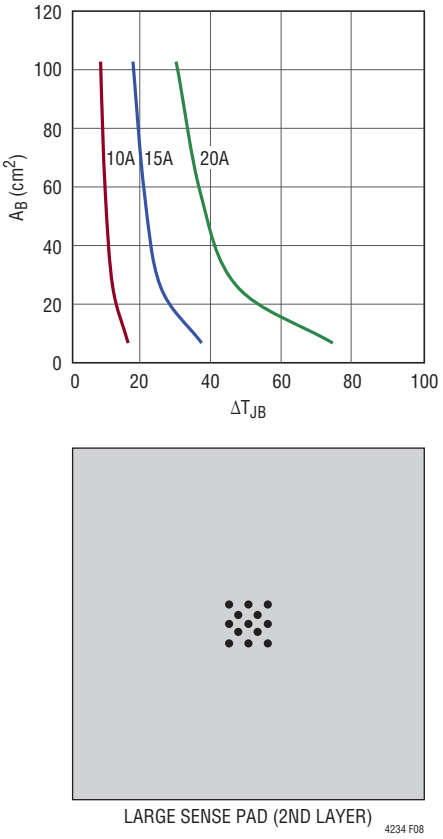


Figure 8. Temperature Rise for Large SENSE Pad

Figure 6. The second layer is 1oz copper connected to the vias to the SENSE pad on the top layer. Two versions of the second layer are considered. One uses a minimum sized SENSE pad that only covers the vias for the top layer while the remainder of the second layer is empty (see Figure 7). The other version fills the second layer with SENSE connected copper (see Figure 8). The third layer is 1oz copper tied to ground while the bottom layer is 2oz copper tied to ground except for a few signal traces.

The curves demonstrate that the heat from the MOSFET can be effectively transferred out of the package through the OUT pins and only requires a minimum sized SENSE pad under the package. However for small boards the larger SENSE area does reduce the junction temperature when sourcing higher currents.

Additional Applications

The LTC4234 has a wide operating range from 2.9V to 15V. The UV, OV and PG thresholds are set with few resistors. All other functions are independent of supply voltage.

In addition to Hot Swap applications, the LTC4234 also functions as a backplane resident switch for removable load cards (see Figure 9).

Figure 10 shows a 3.3V application with a UV threshold of 2.87V, an OV threshold of 3.77V and a PG threshold of 3.05V.

The last page shows a 40A parallel application where the two LTC4234 parts each provide 20A to the load. The PNPs prevent one LTC4234 from faulting off in current limit until both parts hit the 22.5A limit. The PNPs are disconnected when power good is false via the series MOSFETs M1 and M2

APPLICATIONS INFORMATION

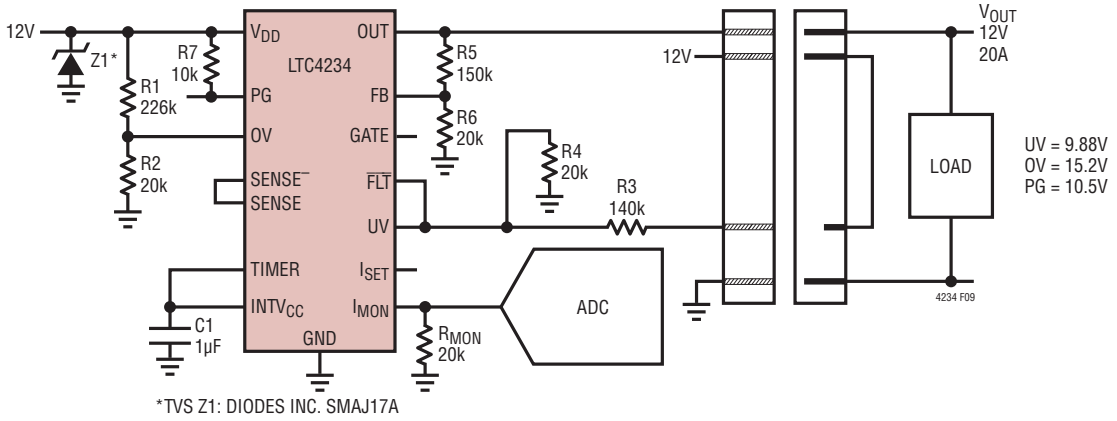


Figure 9. 12V, 20A Backplane Resident Application with Insertion Activated Turn-On

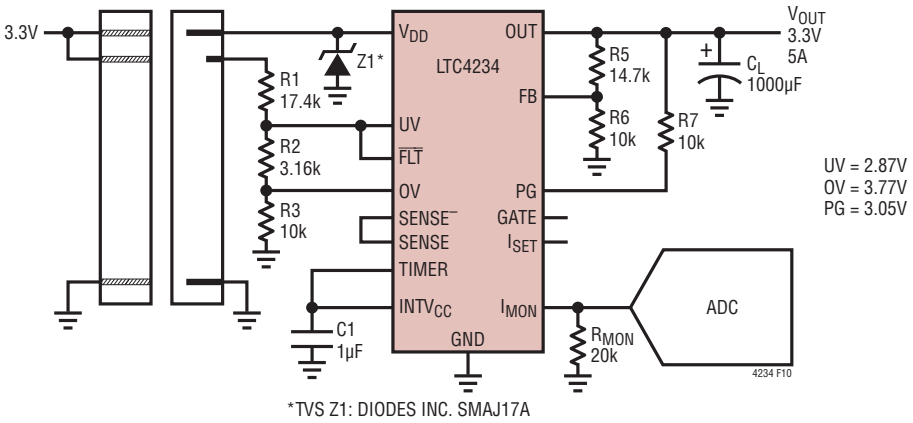
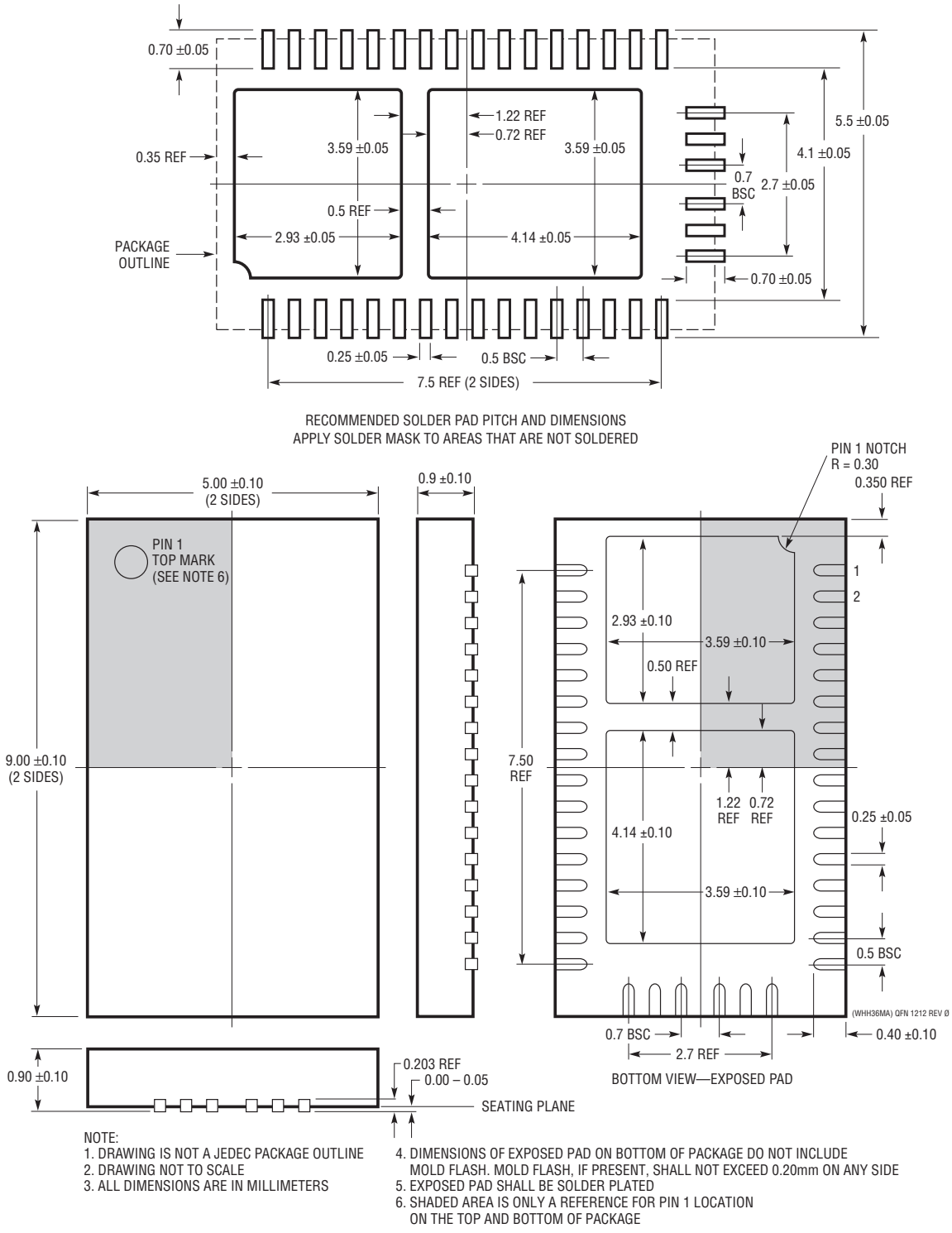


Figure 10. 3.3V, 20A Card Resident Application with Auto-Retry

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

WHH Package
Variation: WHH38MA
38-Lead Plastic QFN (5mm × 9mm)
(Reference LTC DWG # 05-08-1934 Rev Ø)



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

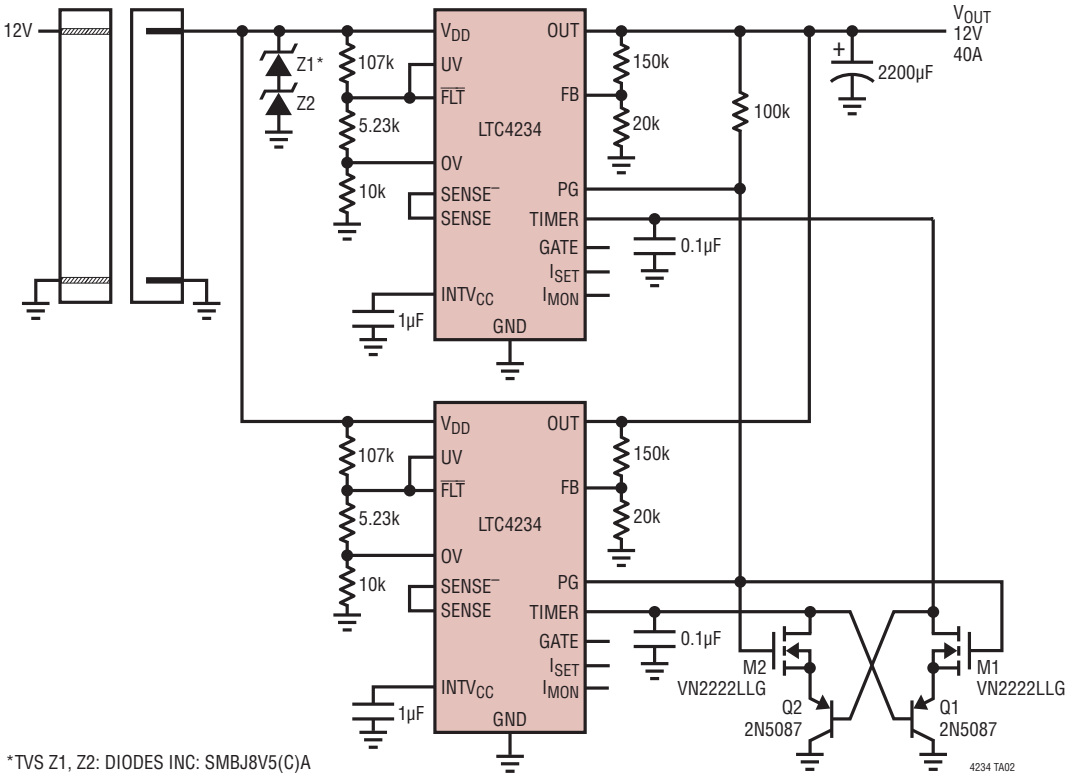
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/15	Changed input clamp to SMAJ17A in application circuit.	1, 10, 17
		Updated SOA specification; added BW_{IMON} and $t_{D(FAULT)}$ specifications.	3, 4
		Added SOA Constant vs Junction Temperature curve; updated MOSFET SOA curve.	6
		Updated $INTV_{CC}$, SENSE and V_{DD} pin functions.	7
		Clarified latchoff and auto-retry behavior.	9
		Added equations to calculate MOSFET temperature from V_{ISET}.	13
		Updated sections: Design Example, Layout Considerations, Typical Application.	14, 15, 20

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

12V, 40A Parallel Application



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4210	Single Channel Hot Swap Controller	Operates from 2.7V to 16.5V, Active Current Limiting, SOT23-6
LTC4211	Single Channel Hot Swap Controller	Operates from 2.5V to 16.5V, Multifunction Current Control, MSOP-8 or MSOP-10
LTC4215	Hot Swap Controller with I²C Compatible Monitoring	Operates from 2.9V to 15V, 8-Bit ADC Monitors Current and Voltage
LTC4217	2A Integrated Hot Swap Controller	Operates from 2.9V to 26.5V, Adjustable 5% Accurate Current Limit
LTC4218	Hot Swap Controller with 5% Accurate 15mV Current Limit	Operates from 2.9V to 26.5V, Adjustable Current Limit, SSOP-16, DFN-16
LTC4219	5A Integrated Hot Swap Controller	12V and 5V Preset Versions, 10% Accurate Current Limit
LTC4221	Dual Hot Swap Controller/Sequencer	Operates from 1V to 13.5V, Multifunction Current Control, SSOP-16
LTC4227	Dual Ideal Diode and Single Hot Swap Controller	Operates from 2.9V to 18V, PowerPath™ and Inrush Current Control for Redundant Supplies
LTC4228	Dual Ideal Diode and Hot Swap Controller	Operates from 2.9V to 18V, PowerPath and Inrush Current Control for MicroTCA, Redundant Supplies and Supply Holdup
LTC4232	5A Integrated Hot Swap Controller	Operates from 2.9V to 15V, Adjustable 10% Accurate Current Limit
LTC4233	10A Guaranteed SOA Hot Swap Controller	Operates from 2.9V to 15V, Adjustable 11% Accurate Current Limit

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