2M x 32Bits x 4Banks Mobile DDR SDRAM

Description

The IS43/46LR32800G is 268,435,456 bits CMOS Mobile Double Data Rate Synchronous DRAM organized as 4 banks of 2,097,152 words x 32 bits. This product uses a double-data-rate architecture to achieve high-speed operation. The Data Input/ Output signals are transmitted on a 32-bit bus. The double data rate architecture is essentially a 2*N* prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. This product offers fully synchronous operations referenced to both rising and falling edges of the clock. The data paths are internally pipelined and 2n-bits prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with LVCMOS.

Features

- JEDEC standard 1.8V power supply.
- VDD = 1.8V, VDDQ = 1.8V
- Four internal banks for concurrent operation
- MRS cycle with address key programs
  - CAS latency 2, 3 (clock)
  - Burst length (2, 4, 8, 16)
  - Burst type (sequential & interleave)
- Fully differential clock inputs (CK, /CK)
- All inputs except data & DM are sampled at the rising edge of the system clock
- Data I/O transaction on both edges of data strobe
- Bidirectional data strobe per byte of data (DQS)
- DM for write masking only
- Edge aligned data & data strobe output
- Center aligned data & data strobe input
- 64ms refresh period (4K cycle)
- Auto & self refresh
- Concurrent Auto Precharge
- Maximum clock frequency up to 200MHZ
- Maximum data rate up to 400Mbps/pin
- Power Saving support
  - PASR (Partial Array Self Refresh)
  - Auto TCSR (Temperature Compensated Self Refresh)
  - Deep Power Down Mode
  - Programmable Driver Strength Control by Full Strength or 3/4, 1/2, 1/4, 1/8 of Full Strength
- Status Register Read (SRR)
- LVCMOS compatible inputs/outputs
- Packages:
  - 90-Ball BGA
  - 152-Ball PoP BGA

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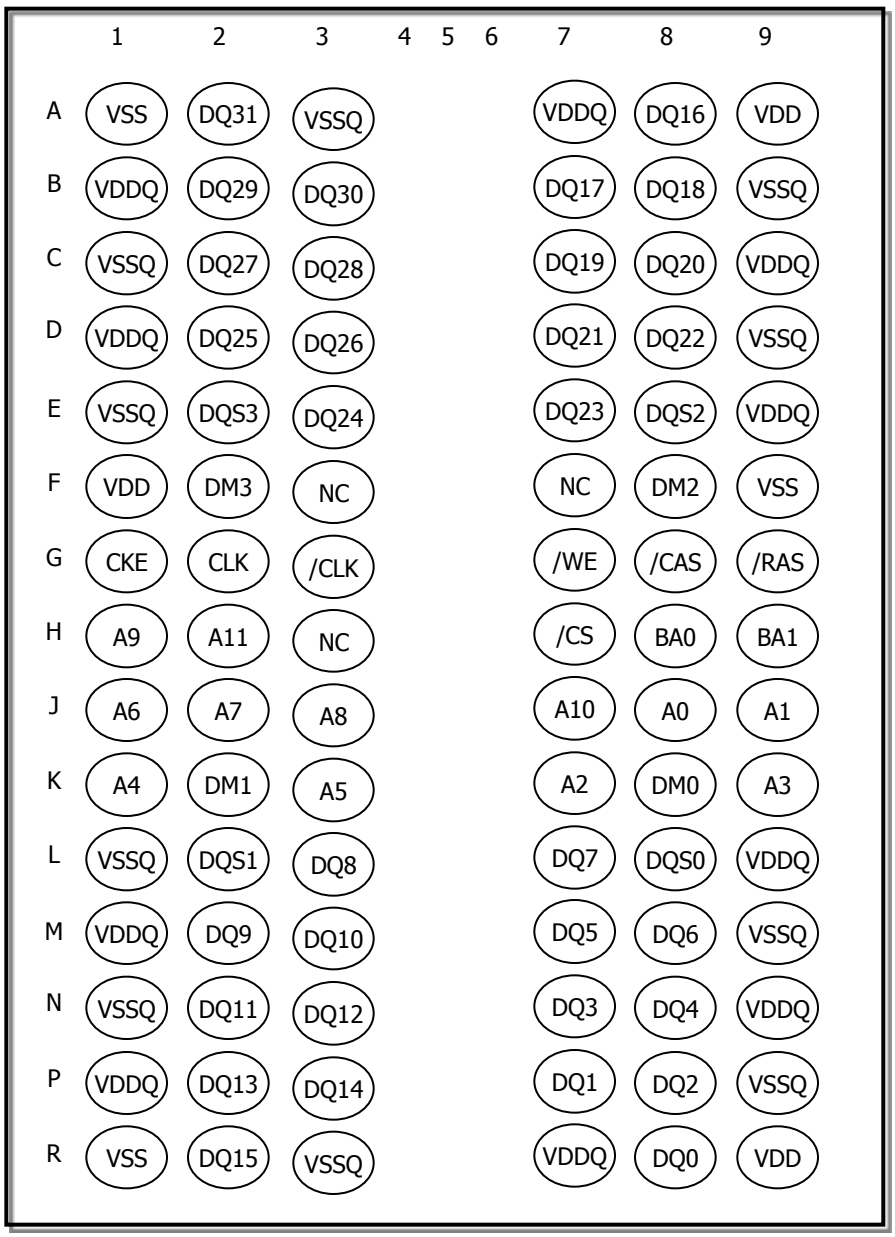
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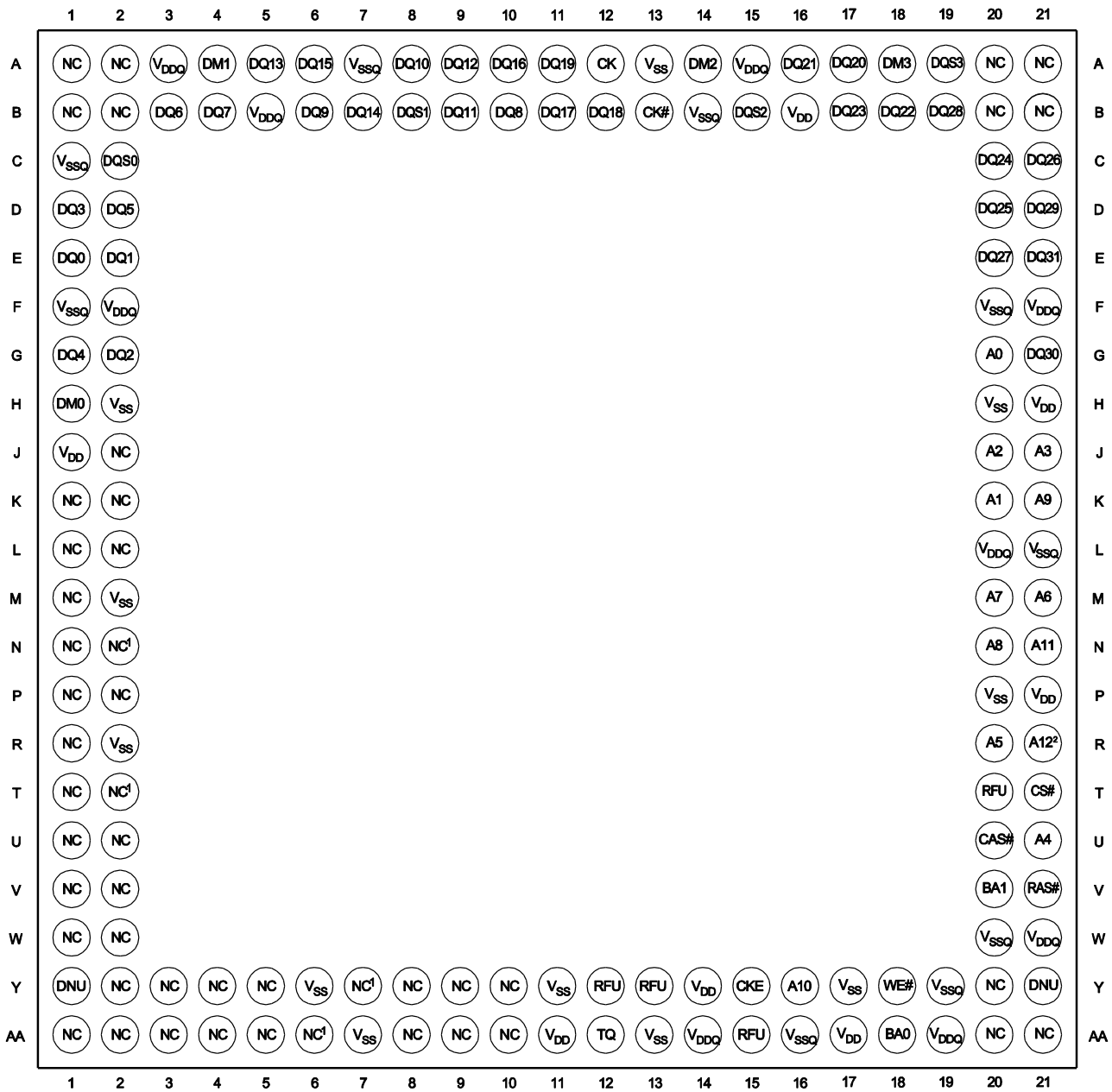
c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

Figure 1: 90Ball FBGA Ball Assignment



[Top View]

Figure 2: 152-Ball VFBGA Ball Assignment



[Top View]

Notes:
1. Although not bonded to the die, these pins may be connected on the package substrate.
2. A12 (R21) is used for 1Gb (32Mx32) and 512Mb (16Mx32), and is NC for 256Mb (8mx32).

Table2 : Pin Descriptions

Symbol	Type	Function	Descriptions
CK, /CK	Input	System Clock	The system clock input. CK and /CK are differential clock inputs. All address and control input signals are registered on the crossing of the rising edge of CK and falling edge of /CK. Input and output data is referenced to the crossing of CK and /CK.
CKE	Input	Clock Enable	CKE is clock enable controls input. CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. CKE is synchronous for all functions except for SELF REFRESH EXIT, which is achieved asynchronously.
/CS	Input	Chip Select	/CS enables (registered Low) and disables (registered High) the command decoder. All commands are masked when /CS IS REGISTERED high. /CS provides for external bank selection on systems with multiple banks. /CS is considered part of the command code.
BA0, BA1	Input	Bank Address	BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 also determine which mode register (standard mode register or extended mode register) is loaded during a LOAD MODE REGISTER command.
A0~A11	Input	Address	Row Address : RA0~RA11 Column Address : CA0~CA8 Auto Precharge : A10
/RAS, /CAS, /WE	Input	Row Address Strobe, Column Address Strobe, Write Enable	/RAS, /CAS and /WE define the operation. Refer function truth table for details.
DM0~DM3	Input	Data Input Mask	DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only.
DQ0~DQ31	In/Output	Data Input/Output	Data input/output pin.
DQS0~DQS3	In/Output	Data Input/Output Strobe	Output with read data, input with write data. DQS is edge-aligned with read data, centered in write data. Data strobe is used to capture data.
TQ	Output	Temperature Sensor	TQ goes High if Tj > 85°C
VDD	Supply	Power Supply	Power supply
VSS	Supply	Ground	Ground
VDDQ	Supply	DQ Power Supply	Power supply for DQ
VSSQ	Supply	DQ Ground	Ground for DQ
NC	NC	No Connection	No connection.

Figure 3 : Functional Block Diagram

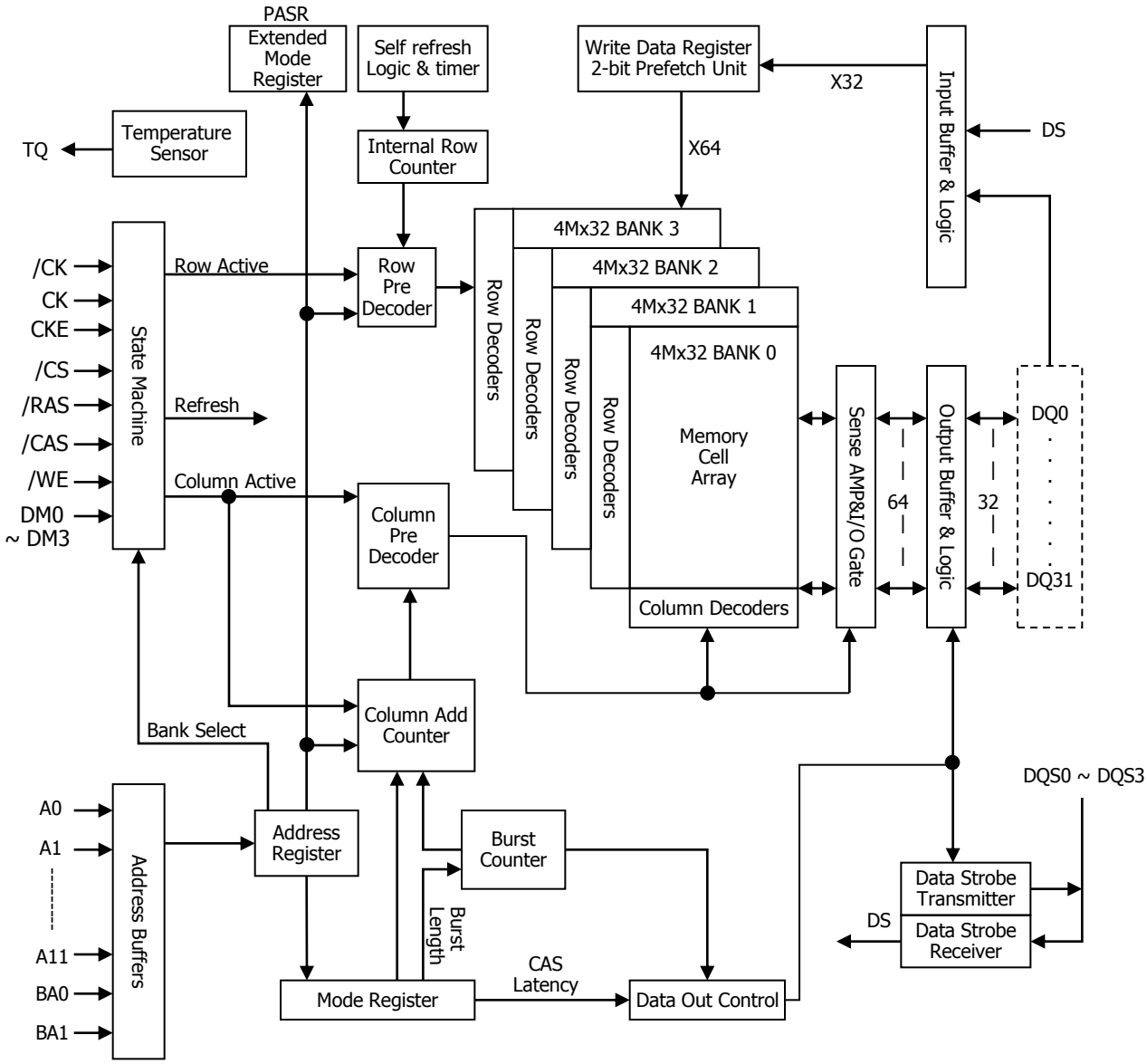
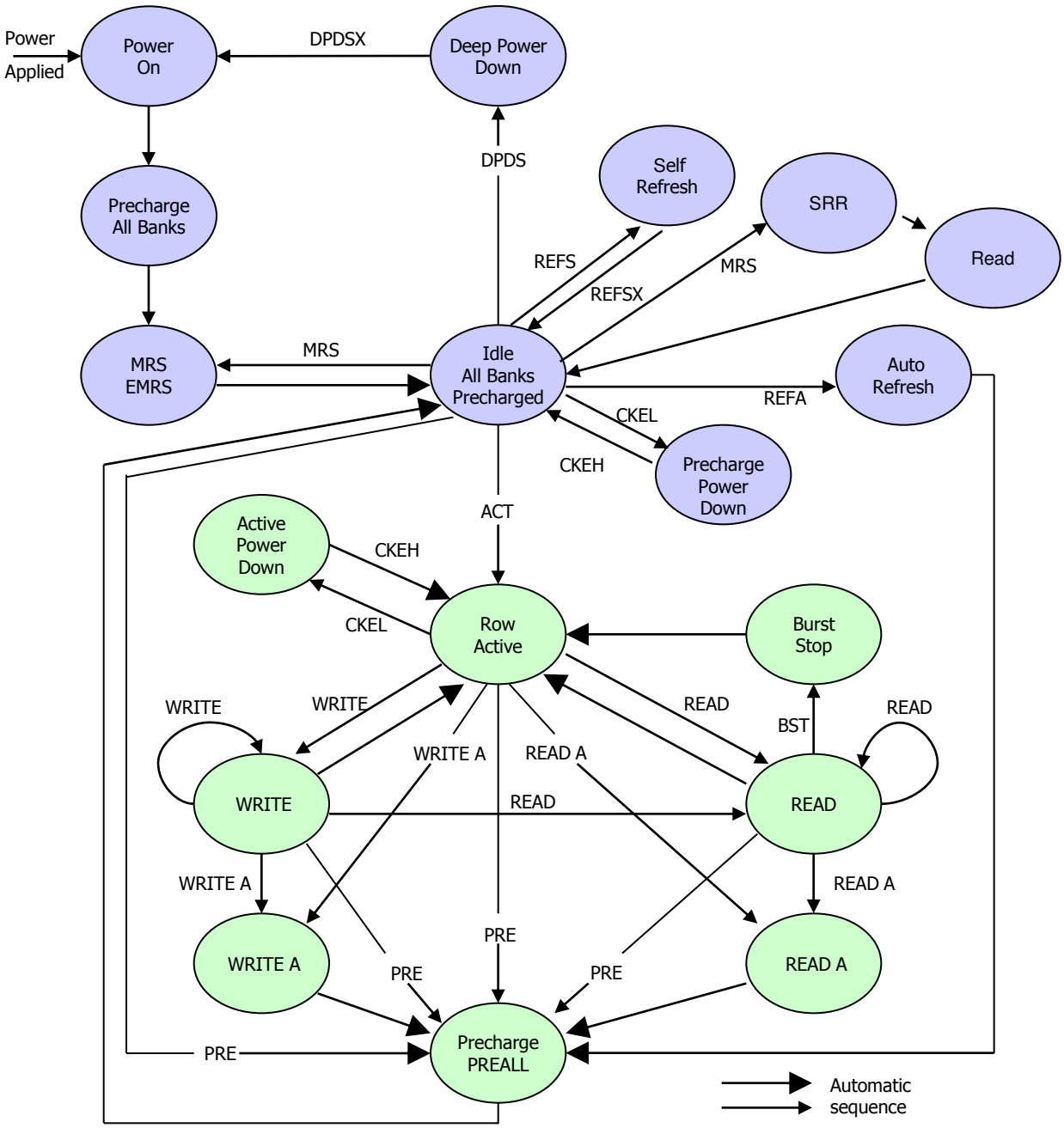


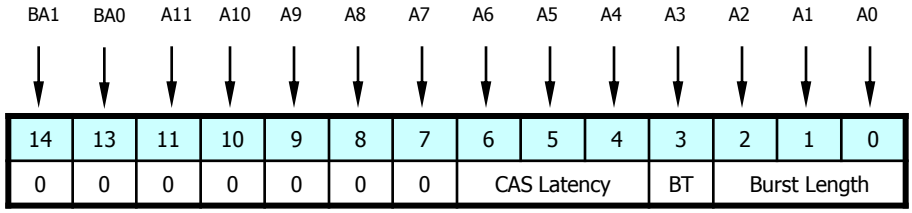
Figure4 : Simplified State Diagram



ACT = Active
BST = Burst
CKEL = Enter Power- Down
CKEH = Exit Power-Down
DPDS = Enter Deep Power-Down
DPDSX = Exit Deep Power- Down
EMRS = Ext. Mode Reg. Set
MRS = Mode Register Set
PRE = Precharge

PREALL= Precharge All Banks
REFA = Auto Refresh
REFS = Enter Self Refresh
REFSX = Exit Self Refresh
READ = Read w/o Auto Precharge
READ A = Read with Auto Precharge
SRR = Status Register Read
WRITE = Write w/o Auto Precharge
WRITE A = Write with Auto Precharge

Figure 5 : Mode Register Set (MRS) Definition



M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M3	Burst Type
0	Sequential
1	Interleave

M2	M1	M0	Burst Length	
			M3 = 0	M3 = 1
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	16	16
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

Note: M14(BA1) = 0 and M13(BA0) = 0 to select Mode Register

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 3.

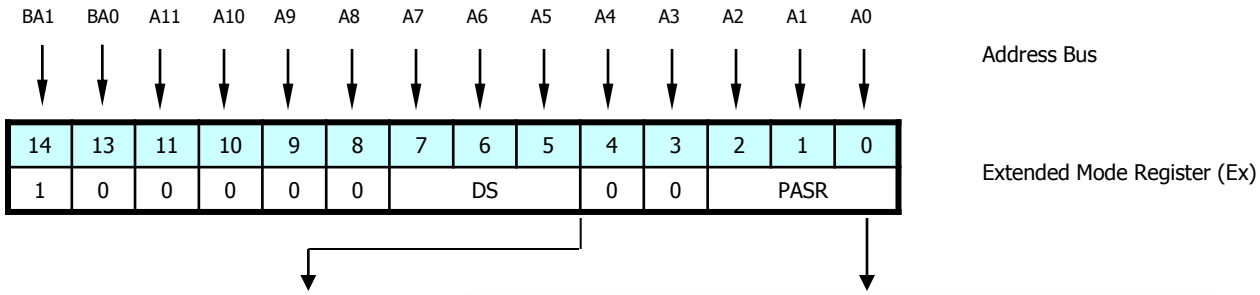
Table3 : Burst Definition

Burst Length	Starting Column Address				Order of Access within a Burst	
	A3	A2	A1	A0	Sequential Mode	Interleave Mode
2	x	x	x	0	0-1	0-1
	x	x	x	1	1-0	1-0
4	x	x	0	0	0-1-2-3	0-1-2-3
	x	x	0	1	1-2-3-0	1-0-3-2
	x	x	1	0	2-3-0-1	2-3-0-1
	x	x	1	1	3-0-1-2	3-2-1-0
8	x	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	x	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	x	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	x	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	x	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	x	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	x	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	x	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
16	0	0	0	0	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15
	0	0	0	1	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1-0-3-2-5-4-7-6-9-8-11-10-13-12-15-14
	0	0	1	0	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2-3-0-1-6-7-4-5-10-11-8-9-14-15-12-13
	0	0	1	1	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3-2-1-0-7-6-5-4-11-10-9-8-15-14-13-12
	0	1	0	0	4-5-6-7-8-9-10-11-12-13-14-15-0-1-2-3	4-5-6-7-0-1-2-3-12-13-14-15-8-9-10-11
	0	1	0	1	5-6-7-8-9-10-11-12-13-14-15-0-1-2-3-4	5-4-7-6-1-0-3-2-13-12-15-14-9-8-11-10
	0	1	1	0	6-7-8-9-10-11-12-13-14-15-0-1-2-3-4-5	6-7-4-5-2-3-0-1-14-15-12-13-10-11-8-9
	0	1	1	1	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0-15-14-13-12-11-10-9-8
	1	0	0	0	8-9-10-11-12-13-14-15-0-1-2-3-4-5-6-7	8-9-10-11-12-13-14-15-0-1-2-3-4-5-6-7
	1	0	0	1	9-10-11-12-13-14-15-0-1-2-3-4-5-6-7-8	9-8-11-10-13-12-15-14-1-0-3-2-5-4-7-6
	1	0	1	0	10-11-12-13-14-15-0-1-2-3-4-5-6-7-8-9	10-11-8-9-14-15-12-13-2-3-0-1-6-7-4-5
	1	0	1	1	11-12-13-14-15-0-1-2-3-4-5-6-7-8-9-10	11-10-9-8-15-14-13-12-3-2-1-0-7-6-5-4
	1	1	0	0	12-13-14-15-0-1-2-3-4-5-6-7-8-9-10-11	12-13-14-15-8-9-10-11-4-5-6-7-0-1-2-3
	1	1	0	1	13-14-15-0-1-2-3-4-5-6-7-8-9-10-11-12	13-12-15-14-9-8-11-10-5-4-7-6-1-0-3-2
	1	1	1	0	14-15-0-1-2-3-4-5-6-7-8-9-10-11-12-13	14-15-12-13-10-11-8-9-6-7-4-5-2-3-0-1
	1	1	1	1	15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14	15-14-13-12-11-10-9-8-7-6-5-4-3-2-1-0

Note :

1. For a burst length of two, A1-A8 select the block of two burst; A0 selects the starting column within the block.
2. For a burst length of four, A2-A8 select the block of four burst; A0-A1 select the starting column within the block.
3. For a burst length of eight, A3-A8 select the block of eight burst; A0-A2 select the starting column within the block.
4. For a burst length of sixteen, A4-A8 select the block of eight burst; A0-A3 select the starting column within the block.
5. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

Figure5 : Extended Mode Set (EMRS) Register



E7	E6	E5	Driver Strength
0	0	0	Full Strength
0	0	1	1/2 Strength
0	1	0	1/4 Strength
0	1	1	1/8 Strength
1	0	0	3/4 Strength
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

E2	E1	E0	Self Refresh Coverage
0	0	0	Four Banks
0	0	1	Two Bank (BA1=0)
0	1	0	One Bank (BA1=BA0=0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	One Eighth of Total Bank (BA1 = BA0 = Row Address MSB=0)
1	1	0	One Sixteenth of Total Bank (BA1 = BA0 = Row Address 2 MSBs=0)
1	1	1	Reserved

Note:
1. E14(BA1) = 1 and E13(BA0) = 0 to select Extended Mode Register

Functional Description

The 256Mb Mobile DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 268,435,456-bits. It is internally configured as a quad-bank DRAM. The 256Mb Mobile DDR SDRAM uses a double data rate architecture to achieve high speed operation. The double data rate architecture is essentially a 2n-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls, single read or write access for the 256Mb Mobile DDR SDRAM consists of a single 2n-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O balls.

Read and Write accesses to the Mobile DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0–A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

It should be noted that the DLL signal that is typically used on standard DDR devices is not necessary on the Mobile DDR SDRAM. It has been omitted to save power.

Prior to normal operation, the Mobile DDR SDRAM must be powered up and initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

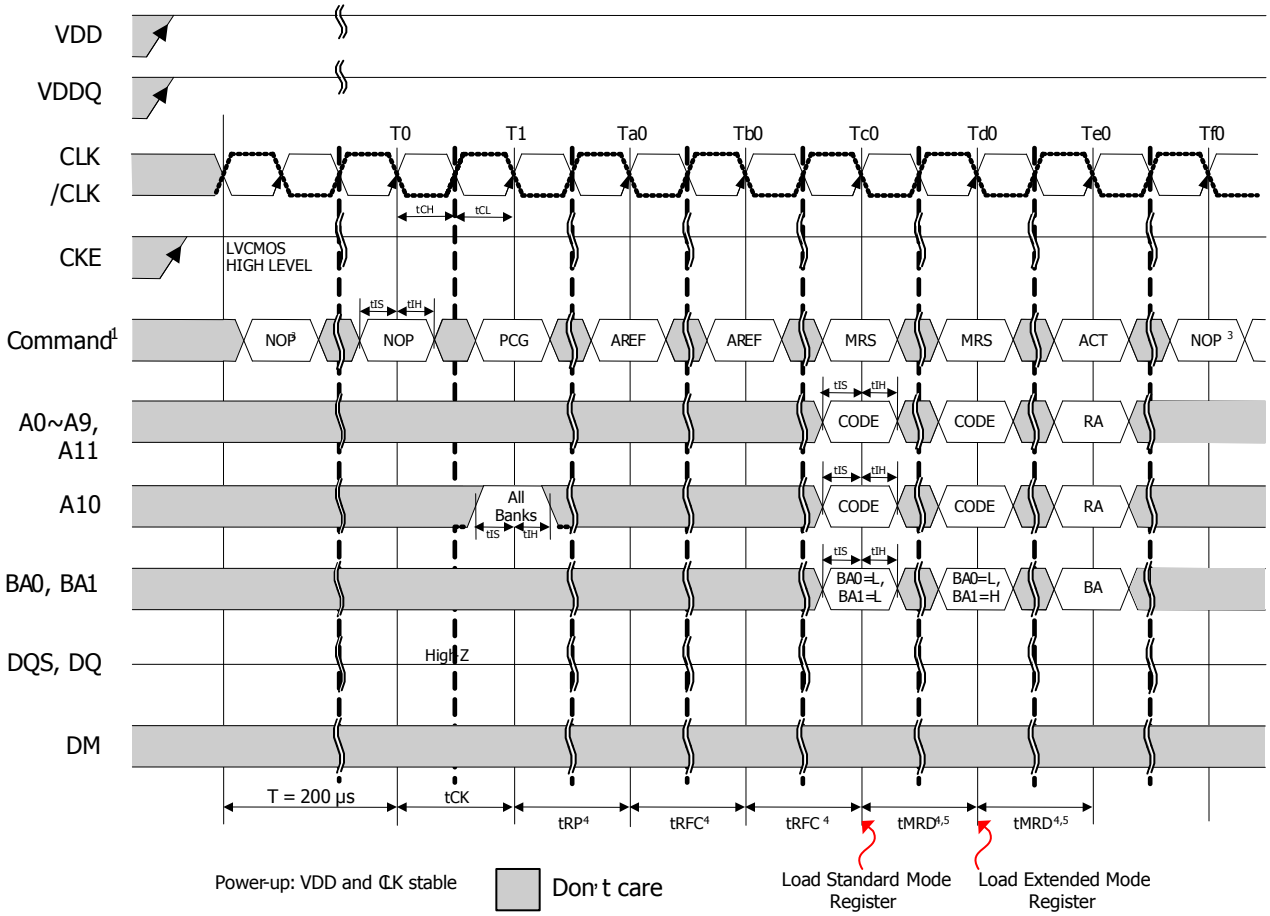
Power up and Initialization

Mobile DDR SDRAM must be powered up and initialized in a predefined manner. Power must be applied to VDD and VDDQ (simultaneously). After power up, an initial pause of 200 usec is required. And a precharge all command will be issued to the Mobile DDR. Then, 2 or more Auto refresh cycles will be provided. After the Auto refresh cycles are completed, a Mode Register Set(MRS) command will be issued to program the specific mode of operation (Cas Latency, Burst length, etc.) And a Extended Mode Register Set(EMRS) command will be issued to Partial Array Self Refresh(PASR). The following these cycles, the Mobile DDR SDRAM is ready for normal operation. To ensure device functionality, there is a predefined sequence that must occur at device power up or if there is any interruption of device power.

To properly initialize the Mobile DDR SDRAM, this sequence must be followed:

1. To prevent device latch-up, it is recommended the core power (VDD) and I/O power (VDDQ) be from the same power source and brought up simultaneously. If separate power sources are used, VDD must lead VDDQ.
2. Once power supply voltages are stable and the CKE has been driven HIGH, it is safe to apply the clock.
3. Once the clock is stable, a 200µs (minimum) delay is required by the Mobile DDR SDRAM prior to applying an executable command. During this time, NOP or DESELECT commands must be issued on the command bus.
4. Issue a PRECHARGE ALL command.
5. Issue NOP or DESELECT commands for at least tRP time.
6. Issue an AUTO REFRESH command followed by NOP or DESELECT commands for at least tRFC time. Issue a second AUTO REFRESH command followed by NOP or DESELECT commands for at least tRFC time. As part of the individualization sequence, two AUTO REFRESH commands must be issued. Typically, both of these commands are issued at this stage as described above.
7. Using the LOAD MODE REGISTER command, load the standard mode register as desired.
8. Issue NOP or DESELECT commands for at least tMRD time.
9. Using the LOAD MODE REGISTER command, load the extended mode register to the desired operating modes. Note that the order in which the standard and extended mode registers are programmed is not critical.
10. Issue NOP or DESELECT commands for at least tMRD time.
11. The Mobile DDR SDRAM has been properly initialized and is ready to receive any valid command.

Figure 7 : Power up sequence



Notes:

1. PCG = PRECHARGE command, MRS = LOAD MODE REGISTER command, AREF = AUTOREFRESH command, ACT = ACTIVE command, RA = Row address, BA = Bank address.
2. NOP or DESELECT commands are required for at least 200µs.
3. Other valid commands are possible.
4. NOPs or DESELECTs are required during this time.
5. Two clocks at minimum.

Mode Register

The mode register is used to define the specific mode of operation of the Mobile DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until programmed again, the device goes into deep power-down mode, or the device loses power.

Mode register bits A0-A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4-A6 specify the CAS latency, and A7-A12 should be set to zero. BA0 and BA1 must be zero to access the mode register.

The mode register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length

Read and write accesses to the Mobile DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Figure (Mode Register Set Definition). The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, 8 or 16 are available for both the sequential and the interleaved burst types.

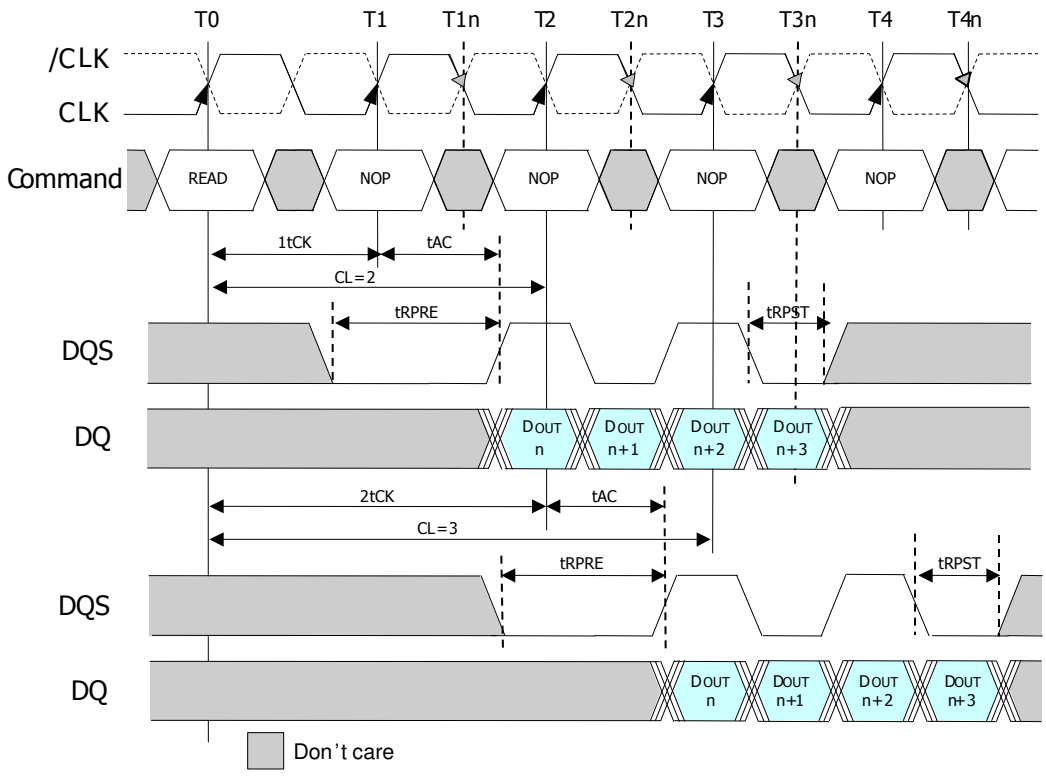
Reserved states should not be used, as unknown operation or incompatibility with future versions may result. When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-A8 when the burst length is set to two; by A2-A8 when the burst length is set to four; by A3-A8 when the burst length is set to eight; and by A4-A8 when the burst length is set to sixteen. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 2, 3 clocks, as shown in Figure (Standard Mode Register Definition).

For CL = 3, if the READ command is registered at clock edge n, then the data will be available at (n + 2 clocks + tAC). For CL = 2, if the READ command is registered at clock edge n, then the data will be available at (n + 1 clock + tAC).

Figure 8 : CAS Latency (BL=4)



Extended Mode Register

The Extended Mode Register controls the functions beyond those controlled by the Mode Register. These additional functions are special features of the Mobile DDR SDRAM. They include Partial Array Self Refresh (PASR) and Driver Strength (DS).

The Extended Mode Register is programmed via the Mode Register Set command (BA0=0, BA1=1) and retains the stored information until programmed again, the device goes into deep power-down mode, or the device loses power.

The Extended Mode Register must be programmed with A8 through A11 set to "0". The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements results in unspecified operation.

Partial Array Self Refresh

For further power savings during SELF REFRESH, the PASR feature allows the controller to select the amount of memory that will be refreshed during SELF REFRESH. The refresh options are as follows:

- Full array: banks 0, 1, 2, and 3
- Half array: banks 0 and 1
- Quarter array: bank 0
- One eighth array : half of bank 0
- One sixteenth array : quarter of bank 0

WRITE and READ commands can still occur during standard operation, but only the selected banks will be refreshed during SELF REFRESH. Data in banks that are disabled will be lost.

Output Driver Strength

Because the Mobile DDR SDRAM is designed for use in smaller systems that are mostly point to point, an option to control the drive strength of the output buffers is available. Drive strength should be selected based on the expected loading of the memory bus. Bits A5 and A6 of the extended mode register can be used to select the driver strength of the DQ outputs. There are four allowable settings for the output drivers.

Temperature Compensated Self Refresh

In the Mobile DDR SDRAM, a temperature sensor is implemented for automatic control of the self refresh oscillator on the device.

Temperature Compensated Self Refresh allows the controller to program the Refresh interval during SELF REFRESH mode, according to the case temperature of the Mobile SDRAM device. This allows great power savings during SELF REFRESH during most operating temperature ranges. Only during extreme temperatures would the controller have to select a TCSR level that will guarantee data during SELF REFRESH.

Every cell in the DRAM requires refreshing due to the capacitor losing its charge over time. The refresh rate is dependent on temperature. At higher temperatures a capacitor loses charge quicker than at lower temperatures, requiring the cells to be refreshed more often. Historically, during Self Refresh, the refresh rate has been set to accommodate the worst case, or highest temperature range expected.

Thus, during ambient temperatures, the power consumed during refresh was unnecessarily high, because the refresh rate was set to accommodate the higher temperatures.

This temperature compensated refresh rate will save power when the DRAM is operating at normal temperatures. It is not supported for any temperature grade with T_A above +85°C.

Commands

The following COMMANDS Truth Table and DM Operation Truth Table provide quick reference of available commands. This is followed by a written description of each command.

Deselect

The DESELECT function (/CS HIGH) prevents new commands from being executed by the Mobile DDR SDRAM. The Mobile DDR SDRAM is effectively deselected. Operations already in progress are not affected.

NO Operation (NOP)

The NO OPERATION (NOP) command is used to instruct the selected DDR SDRAM to perform a NOP (/CS = LOW, /RAS = /CAS = /WE = HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

Active

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A11 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

Read

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A8 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

Write

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A8 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

Precharge

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the precharge command is issued. Except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank (idle state), or if the previously open row is already in the process of precharging.

Auto Precharge

Auto precharge is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command. This device supports concurrent auto precharge if the command to the other bank does not interrupt the data transfer to the current bank. Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. This "earliest valid stage" is determined as if an explicit PRECHARGE command was issued at the earliest possible time, without violating tRAS (MIN). The user must not issue another command to the same bank until the precharge time (tRP) is completed.

Burst Terminate

The BURST TERMINATE command is used to truncate READ bursts (with auto precharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated. The open page which the READ burst was terminated from remains open.

Auto Refresh

AUTO REFRESH is used during normal operation of the Mobile DDR SDRAM and is analogous to /CAS-BEFORE-/RAS (CBR) REFRESH in FPM/EDO DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an AUTO REFRESH command. The 256Mb Mobile DDR SDRAM requires AUTO REFRESH cycles at an average interval of T_{REFI} (maximum). To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided.

Although not a JEDEC requirement, to provide for future functionality features, CKE must be active (HIGH) during the auto refresh period. The auto refresh period begins when the AUTO REFRESH command is registered and ends tRFC later.

Self Refresh

The SELF REFRESH command can be used to retain data in the Mobile DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the Mobile DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). All command and address input signals except CKE are "Don't Care" during SELF REFRESH.

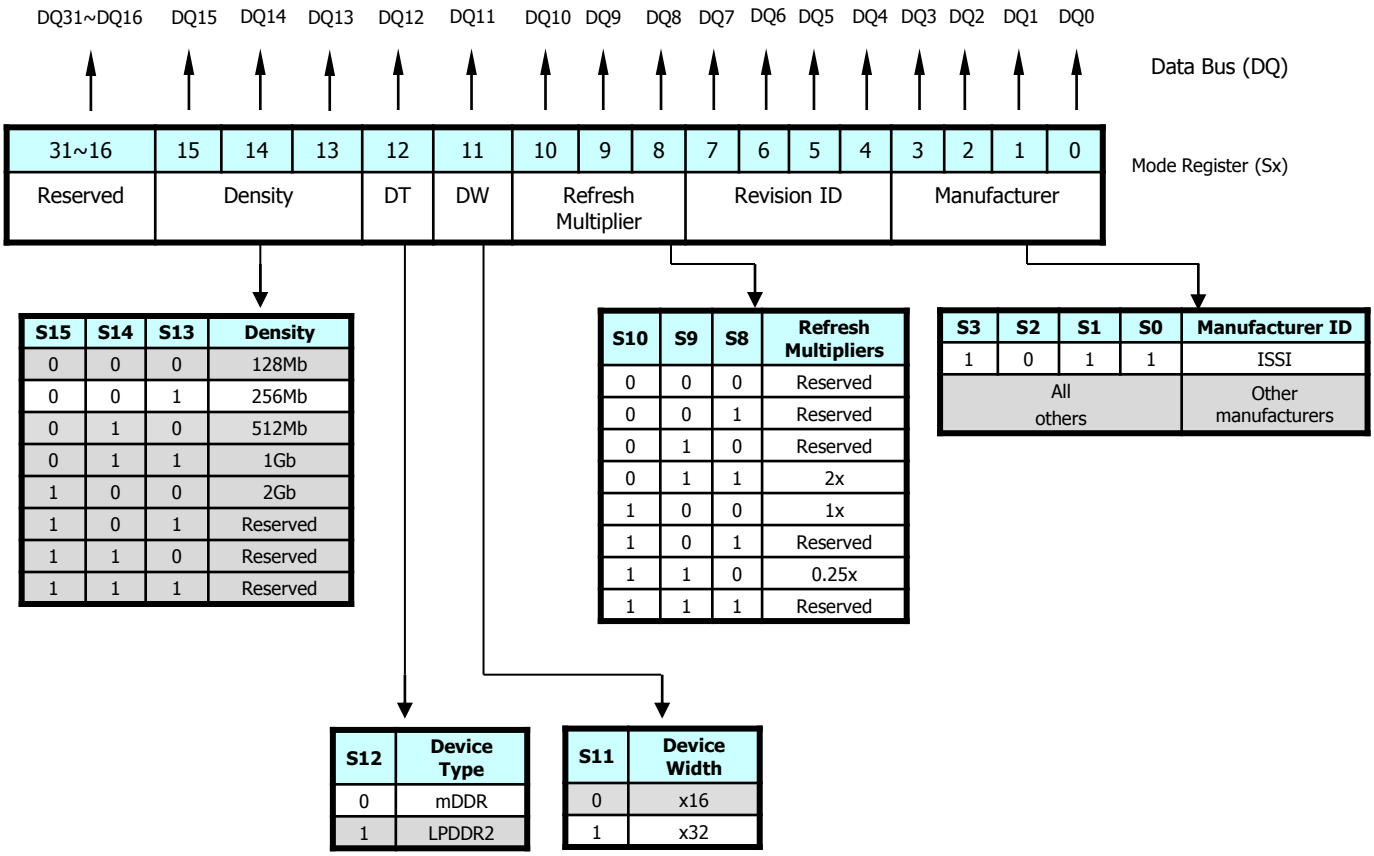
During SELF REFRESH, the device is refreshed as identified in the external mode register (see PASR setting). For a the full array refresh, all four banks are refreshed simultaneously with the refresh frequency set by an internal self refresh oscillator. This oscillator changes due to the temperature sensors input. As the case temperature of the Mobile DDR SDRAM increases, the oscillation frequency will change to accommodate the change of temperature. This happens because the DRAM capacitors lose charge faster at higher temperatures. To ensure efficient power dissipation during self refresh, the oscillator will change to refresh at the slowest rate possible to maintain the devices data. The procedure for exiting SELF REFRESH requires a sequence of commands. First, Clock must be stable prior to CKE going back HIGH. Once CKE is HIGH, the Mobile DDR SDRAM must have NOP commands issued for tXSR is required for the completion of any internal refresh in progress. The SELF REFRESH command is not applicable for operation with $T_A > 85^oC$.

Deep Power-down

Deep Power Down is an operating mode to achieve maximum power reduction by eliminating the power of the whole memory array of the devices. Data in the array and in the mode and extended mode registers will not be retained once the device enters Deep Power Down Mode.

This mode is entered by having all banks idle then /CS and /WE held low with /RAS and /CAS held high at the rising edge of the clock, while CKE is low. This mode is exited by asserting CKE high. After applying NOP commands for 200 μs, the Power Up and Initialization sequence must be followed. This mode is not applicable for operation with $T_A > 85^oC$.

Figure9 : Status Register Read (SRR)



S15	S14	S13	Density
0	0	0	128Mb
0	0	1	256Mb
0	1	0	512Mb
0	1	1	1Gb
1	0	0	2Gb
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

S10	S9	S8	Refresh Multipliers
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	2x
1	0	0	1x
1	0	1	Reserved
1	1	0	0.25x
1	1	1	Reserved

S3	S2	S1	S0	Manufacturer ID
1	0	1	1	ISSI
All others				Other manufacturers

S12	Device Type
0	mDDR
1	LPDDR2

S11	Device Width
0	x16
1	x32

Status Register Read

The Status Register Read (SRR) command allows the user to access the manfacturer device information. It is optional for the user. The 16-bit encoded data is stored in the Status Register, and can be output onto DQ0~DQ15, with a fixed burst length (BL) of 2. The Manufacturer's ID is on S0~S3, the Device Revision ID is on S4~S7, the Refresh Rate is on S8~S10, the Data Width is on S11, the Device Type is on S12, and the Density is on S13~S15. The register bit range S16~S31 is reserved. The SRR command sequence is as follows:

- All banks must be idle, and Reads and Writes completed
- A Mode Register Set (MRS) command is issued with BA0=1, BA1=0, and A0~A11=0 to initiate SRR
- After a time period tSRR, a Read command is issued to any bank or address
- The next valid command may be issued a time period tSRC after the Read command

The Read command causes the Status Register data to be output after two or three clock cycles, whichever corresponds to the CAS Latency setting. In the first half of the Read burst, the DQ16~DQ31 values are "Don't Care," and in the second half of the Read burst, the DQ0~DQ31 values are "Don't Care".

Table4: Command Truth Table

Function	/CS	/RAS	/CAS	/WE	BA	A10/AP	ADDR	Note
DESELECT (NOP)	H	X	X	X	X	X	X	2
NO OPERATION (NOP)	L	H	H	H	X	X	X	2
ACTIVE (Select Bank and activate Row)	L	L	H	H	V	Row	Row	
READ (Select bank and column and start read burst)	L	H	L	H	V	L	Col	
READ with AP (Read Burst with Auto recharge)	L	H	L	H	V	H	Col	3
WRITE (Select bank and column and start write burst)	L	H	L	L	V	L	Col	
WRITE with AP (Write Burst with Auto recharge)	L	H	L	L	V	H	Col	3
BURST TERMINATE or enter DEEP POWER DOWN	L	H	H	L	X	X	X	4,5
PRECHARGE (Deactivate Row in selected bank)	L	L	H	L	V	L	X	6
PRECHARGE ALL (Deactivate rows in all banks)	L	L	H	L	X	H	X	6
AUTO REFRESH or enter SELF REFRESH	L	L	L	H	X	X	X	7,8,9
MODE REGISTER SET	L	L	L	L	V	Op_Code		10

Table5 : DM Truth Table

Function	DM	DQ	Note
Write Enable	L	Valid	11
Write Inhibit	H	X	11

Note:

1. All states and sequences not shown are illegal or reserved.
2. DESLECT and NOP are functionally interchangeable.
3. Autoprecharge is non-persistent. A10 High enables Autoprecharge, while A10 Low disables Autoprecharge
4. Burst Terminate applies to only Read bursts with autoprecharge disabled.
   This command is undefined and should not be used for Read with Autoprecharge enabled, and for Write bursts.
5. This command is BURST TERMINATE if CKE is High and DEEP POWER DOWN entry if CKE is Low.
6. If A10 is low, bank address determines which bank is to be precharged. If A10 is high, all banks are precharged and BA0-BA1 are don't care.
7. This command is AUTO REFRESH if CKE is High, and SELF REFRESH if CKE is low.
8. All address inputs and I/O are "don't care" except for CKE. Internal refresh counters control Bank and Row addressing.
9. All banks must be precharged before issuing an AUTO-REFRESH or SELF REFRESH command.
10. BA0 and BA1 value select among Mode Register Set (MRS), Extended Mode Register (EMRS) or Status Register Read (SRR).
11. Used to mask write data, provided coincident with the corresponding data.
12. CKE is HIGH for all commands shown except SELF REFRESH and DEEP POWER-DOWN.

Table6 : CKE Truth Table

CKEn-1	CKEn	*Current State*	COMMAND*n*	ACTION*n*	Note
L	L	Power Down	X	Maintain Power Down	
L	L	Self Refresh	X	Maintain Self Refresh	
L	L	Deep Power Down	X	Maintain Deep Power Down	
L	H	Power Down	NOP or DESELECT	Exit Power Down	5,6,9
L	H	Self Refresh	NOP or DESELECT	Exit Self Refresh	5,7,10
L	H	Deep Power Down	NOP or DESELECT	Exit Deep Power Down	5,8
H	L	All Banks Idle	NOP or DESELECT	Precharge Power Down entry	5
H	L	Bank(s) Active	NOP or DESELECT	Active Power Down Entry	5
H	L	All Banks Idle	AUTO REFRESH	Self Refresh Entry	
H	L	All Banks Idle	BURST TERMINATE	Enter Deep Power Down	
H	H	See the other Truth Tables			

Note:

1. CKEn is the logic state of CKE at clock edge *n*; CKE*n*-1 was the state of CKE at the previous clock edge.
2. Current state is the state of Mobile DDR immediately prior to clock edge *n*.
3. COMMANDn is the command registered at clock edge n, and ACTION*n* is the result of COMMAND*n*.
4. All states and sequences not shown are illegal or reserved.
5. DESELECT and NOP are functionally interchangeable.
6. Power Down exit time (tXP) should elapse before a command other than NOP or DESELECT is issued.
7. SELF REFRESH exit time (tXSR) should elapse before a command other than NOP or DESELECT is issued.
8. The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Functional Description.
9. The clock must toggle at least one time during the tXP period.
10. The clock must toggle at least once during the tXSR time.

Table7 : Current State BANK*n* Truth Table(COMMAND TO BANK *n*)

Current State	Command					Action	Note
	/CS	/RAS	/CAS	/WE	Description		
Any	H	X	X	X	DESELECT(NOP)	Continue previous Operation	
	L	H	H	H	NOP	Continue previous Operation	
Idle	L	L	H	H	ACTIVE	Select and activate row	
	L	L	L	H	AUTO REFRESH	Auto refresh	10
	L	L	L	L	MODE REGISTER SET	Mode register set	10
	L	L	H	H	PRECHARGE	No action if bank is idle	
Row Active	L	H	L	H	READ	Select Column & start read burst	
	L	H	L	L	WRITE	Select Column & start write burst	
	L	L	H	L	PRECHARGE	Deactivate Row in bank (or banks)	4
Read (without Auto recharge)	L	H	L	H	READ	Truncate Read & start new Read burst	5,6
	L	H	L	L	WRITE	Truncate Read & start new Write burst	5,6,13
	L	L	H	L	PRECHARGE	Truncate Read, start Precharge	
	L	H	H	L	BURST TERMINATE	Burst terminate	11
Write (without Auto precharge)	L	H	L	H	READ	Truncate Write & start new Read burst	5,6,12
	L	H	L	L	WRITE	Truncate Write & start new Write burst	5,6
	L	L	H	L	PRECHARGE	Truncate Write, start Precharge	12

Note:

1. The table applies when both CKEn-1 and CKEn are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or Power Down.
2. DESELECT and NOP are functionally interchangeable.
3. All states and sequences not shown are illegal or reserved.
4. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
5. A command other than NOP should not be issued to the same bank while a READ or WRITE Burst with auto precharge is enabled.
6. The new Read or Write command could be auto precharge enabled or auto precharge disabled.
7. Current State Definitions:
   Idle: The bank has been precharged, and tRP has been met.
   Row Active: A row in the bank has been activated, and tRCD has been met.
   No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
   Write: a WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
8. The following states must not be interrupted by a command issued to the same bank.
   DESELECT or NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table3, and according to Truth Table 4.
   - Precharging: Starts with the registration of a PRECHARGE command and ends when tRP is met.
     Once tRP is met, the bank will be in the idle state.
   - Row Activating: Starts with registration of an ACTIVE command and ends when tRCD is met.
     Once tRCD is met, the bank will be in the "row active" state.
   - Read with AP Enabled: Starts with the registration of the READ command with AUTO PRECHARGE enabled and ends when tRP has been met. Once tRP has been met, the bank will be in the idle state.
   - Write with AP Enabled: Starts with registration of a WRITE command with AUTO PRECHARGE enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

9. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied to each positive clock edge during these states.
   - Refreshing: Starts with registration of an AUTO REFRESH command and ends when tRFC is met.
     Once tRFC is met, the Mobile DDR will be in an "all banks idle" state.
   - Accessing Mode Register: Starts with registration of a MODE REGISTER SET command and ends when tMRD has been met.
     Once tMRD is met, the Mobile DDR will be in an "all banks idle" state.
   - Precharging All: Starts with the registration of a PRECHARGE ALL command and ends when tRP is met.
     Once tRP is met, the bank will be in the idle state.
10. Not bank-specific; requires that all banks are idle and no bursts are in progress.
11. Not bank-specific. BURST TERMINATE affects the most recent READ burst, regardless of bank.
12. Requires appropriate DM masking.
13. A WRITE command may be applied after the completion of the READ burst; otherwise, a Burst terminate must be used to end the READ prior to asserting a WRITE command.

Table8 : Current State BANK*n* Truth Table (COMMAND TO BANK *m*)

Current State	Command					Action	Note
	/CS	/RAS	/CAS	/WE	Description		
Any	H	X	X	X	DESELECT(NOP)	Continue previous Operation	
	L	H	H	H	NOP	Continue previous Operation	
Idle	X	X	X	X	ANY	Any command allowed to bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	8
	L	H	L	L	WRITE	Start WRITE burst	8
	L	L	H	L	PRECHARGE	Precharge	
Read with Auto Precharge disabled	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	State READ burst	8
	L	H	L	L	WRITE	Start WRITE burst	8,10
	L	L	H	L	PRECHARGE	Precharge	
Write with Auto precharge disabled	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	8,9
	L	H	L	L	WRITE	Start WRITE burst	8
	L	L	H	L	PRECHARGE	Precharge	
Read with Auto Precharge	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	5,8
	L	H	L	L	WRITE	Start WRITE burst	5,8,10
	L	L	H	L	PRECHARGE	Precharge	
Write with Auto precharge	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	5,8
	L	H	L	L	WRITE	Start WRITE burst	5,8
	L	L	H	L	PRECHARGE	Precharge	

Note:

1. The table applies when both CKE*n*-1 and CKE*n* are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or Power Down.
2. DESELECT and NOP are functionally interchangeable.
3. All states and sequences not shown are illegal or reserved.
4. Current State Definitions:
   Idle: The bank has been precharged, and tRP has been met.
   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
   Write: a WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
5. Read with AP enabled and Write with AP enabled: The read with Autoprecharge enabled or Write with Autoprecharge enabled states can be broken into two parts: the access period and the precharge period. For Read with AP, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all the data in the burst.
   For Write with Auto precharge, the precharge period begins when tWR ends, with tWR measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or tRP) begins.
   During the precharge period, of the Read with Autoprecharge enabled or Write with Autoprecharge enabled states, ACTIVE, PRECHARGE, READ, and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other banks may be applied. In either case, all other related limitations apply
   (e.g. contention between READ data and WRITE data must be avoided).
6. AUTO REFRESH, SELF REFRESH, and MODE REGISTER SET commands may only be issued when all bank are idle.
7. A BURST TERMINATE command cannot be issued to another bank;
   It applies to the bank represented by the current state only.
8. READs or WRITEs listed in the Command column include READs and WRITEs with AUTO PRECHARGE enabled and READs and WRITEs with AUTO PRECHARGE disabled.
9. Requires appropriate DM masking.
10. A WRITE command may be applied after the completion of data output, otherwise a BURST TERMINATE command must be issued to end the READ prior to asserting a WRITE command.

Table9 : Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Storage Temperature	T_{STG}	-55 ~ 150	°C
Voltage on Any Pin relative to VSS	V_{IN}, V_{OUT}	-0.3 ~ 2.7	V
Voltage on VDD relative to VSS	VDD, VDDQ	-0.3 ~ 2.7	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D	0.7	W

Note :

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table10 : Operating Temperature

Parameter	Symbol	Rating	Unit
Ambient Temperature (Automotive, A2)	T_A	-40 ~ 105	°C
Ambient Temperature (Automotive, A1)		-40 ~ 85	
Ambient Temperature (Industrial)		-40 ~ 85	
Ambient Temperature (Commercial)		0 ~ 70	

Table11 : AC/DC Operating Conditions (1)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	VDD	1.7	1.8	1.95	V	
Power Supply Voltage	VDDQ	1.7	1.8	1.95	V	2
Input High Voltage	V_{IH} (DC)	0.7 x VDDQ		VDDQ + 0.3	V	
Input Low Voltage	V_{IL} (DC)	-0.3		0.3 x VDDQ	V	
Input Differential Voltage, for CK, /CK inputs	V_{ID} (DC)	0.4 x VDDQ		VDDQ + 0.6	V	3
Output High Voltage	V_{OH} (DC)	0.9 x VDDQ		-	V	I_{OH}=-0.1mA
Output Low Voltage	V_{OL} (DC)	-		0.1 x VDDQ	V	I_{OL}=0.1mA
Input Leakage Current	I_{LI}	-2		2	uA	
Output Leakage Current	I_{LO}	-5		5	uA	
Input High Voltage, all inputs	V_{IH} (AC)	0.8 x VDDQ		VDDQ + 0.3	V	
Input Low Voltage, all inputs	V_{IL} (AC)	-0.3		0.2 x VDDQ	V	
Input Differential Voltage, for CK, /CK inputs	V_{ID}(AC)	0.6 x VDDQ		VDDQ + 0.6	V	3
Input Differential Crosspoint Voltage for CK and /CK inputs	V_{IX}(AC)	0.4 x VDDQ		0.6 x VDDQ	V	4

Notes :

1. All Voltages are referenced to VSS = 0V
2. VDD and VDDQ must track each other, and VDDQ must not exceed the level of VDD.
3. The magnitude of difference between input level on CK and input level on /CK.
4. The value of V_{IX} is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the DC level of the same.

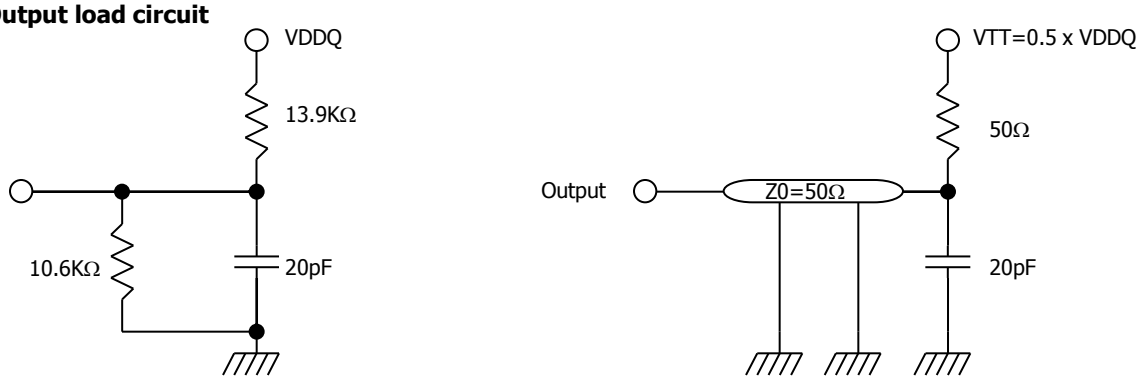
Table12 : Capacitance (T_A=25 °C, f=1MHz, VDD=1.8V)

Parameter	Pin	Symbol	Min	Max	Unit
Input Capacitance	CK, /CK	C_{I1}	1.5	7.0	pF
	A0~A12, BA0~BA1, CKE, /CS, /RAS, /CAS, /WE	C_{I2}	1.5	6.0	pF
	DM0~DM3	C_{I3}	2	4.5	pF
Data & DQS Input/Output Capacitance	DQ0~DQ31, DQS0~DQS3	C_{IO}	2	4.5	pF

Table13 : AC Operating Test Condition

Parameter	Symbol	Value	Unit
AC Input High/Low Level Voltage	V_{IH} / V_{IL}	0.8 x VDDQ / 0.2 x VDDQ	V
Input Timing Measurement Reference Level Voltage	V_{TRIP}	0.5 x VDDQ	V
Input Rise / Fall Time	t_R / t_F	1 / 1	ns
Output Timing Measurement Reference Level Voltage	V_{OUTREF}	0.5 x VDDQ	V
Output Load Capacitance for Access Time Measurement	C_L	20	pF

Figure10 : Output load circuit



DC Output Load Circuit

AC Output Load Circuit

Table14 : AC Overshoot/Undershoot Specification

Parameter	Specification
Maximum Peak Amplitude allowed for Overshoot Area	0.9V
Maximum Peak Amplitude allowed for Undershoot Area	0.9V
Maximum Overshoot Area above VDD/VDDQ	3V-ns
Maximum Undershoot Area below VSS/VSSQ	3V-ns

Figure11 : AC Overshoot/Undershoot Definition

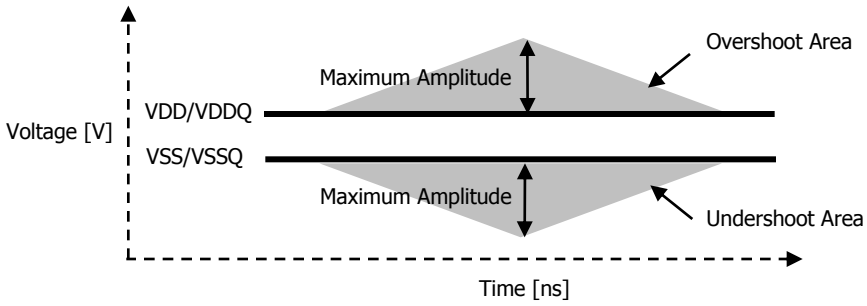


Table15B : DC Characteristic (DC operating conditions unless otherwise noted)

Parameter			Symbol	Test Condition	Speed			Unit	Note
					-5	-6	-75		
Operating one bank active-precharge current			IDD0	tRC = tRC(min), tCK = tCK(min), CKE is HIGH, /CS is HIGH between valid commands, address inputs are SWITCHING, data bus inputs are STABLE	70	60	55	mA	1
Precharge power-down standby current			IDD2P	All banks idle, CKE is LOW, /CS is HIGH, tCK = tCK(min), address and control inputs are SWITCHING, data bus inputs are STABLE	300			μA	
Precharge power-down standby current with clock stop			IDD2PS	All banks idle, CKE is LOW, /CS is HIGH, CK = LOW, /CK = HIGH, address and control inputs are SWITCHING, data bus inputs are STABLE	300			μA	
Precharge non power-down standby current			IDD2N	All banks idle, CKE is HIGH, /CS is HIGH, tCK = tCK(min) , address and control inputs are SWITCHING, data bus inputs are STABLE	10			mA	
Precharge non power-down standby current with clock stop			IDD2NS	All banks idle, CKE is HIGH, /CS is HIGH, CK = LOW, /CK = HIGH, address and control inputs are SWITCHING, data bus inputs are STABLE	4			mA	
Active power-down standby current			IDD3P	One bank active, CKE is LOW, /CS is HIGH, tCK = tCK(min), address and control inputs are SWITCHING, data bus inputs are STABLE	1			mA	
Active power-down standby current with clock stop			IDD3PS	One bank active, CKE is LOW, /CS is HIGH, CK = LOW, /CK = HIGH, address and control inputs are SWITCHING, data bus inputs are STABLE	1			mA	
Active non power-down standby current			IDD3N	One bank active, CKE is HIGH, /CS is HIGH, tCK = tCK(min), address and control inputs are SWITCHING, data bus inputs are STABLE	20			mA	
Active non power-down standby current with clock stop			IDD3NS	One bank active, CKE is HIGH, /CS is HIGH, CK = LOW, /CK = HIGH, address and control inputs are SWITCHING, data bus inputs are STABLE	10			mA	
Operating burst read current			IDD4R	One bank active, BL=4, CL=3, tCK = tCK(min), continuous read bursts, IOUT=0mA, address inputs are SWITCHING, 50% data change each burst transfer	140	130	120	mA	1
Operating burst write current			IDD4W	One bank active, BL=4, tCK=tCK(min), continuous write bursts, address inputs are SWITCHING, 50% data change each burst transfer	60	55	50	mA	1
Auto Refresh Current			IDD5	tRC=tRFC(min), tCK=tCK(min), burst refresh, CKE is HIGH, address and control inputs are SWITCHING, data bus inputs are STABLE	100			mA	2
Self Refresh Current	PASR	TCSR	IDD6	CKE is LOW CK=LOW, /CK=HIGH tCK=tCK(min) Extended Mode Register set to all 0's, address and control inputs are STABLE, data bus inputs are STABLE				uA	
	4 banks	85°C			400				
		45°C			350				
	2 Banks	85°C			380				
		45°C			340				
	1 Bank	85°C			360				
		45°C			330				
	Half Bank	85°C			340				
		45°C			310				
	Quarter Bank	85°C			320				
		45°C			300				
Standby Current in Deep Power Down Mode			IDD8	Address and control inputs are STABLE, data bus inputs are STABLE	10			uA	4

Note : 1. Measured with outputs open
2. Refresh period is 64ms, applicable for $T_A \leq 85°C$
3. All values applicable for application with $T_A \leq 85°C$
4. Typical value at room temperature

Table16: AC Characteristic (AC operation conditions unless otherwise noted)

Parameter		Symbol	-5		Unit	Note
			Min	Max		
System Clock Cycle time	CL=3	tCK	5	1000	ns	1
	CL=2		10		ns	1
DQ Output access time from CK, /CK	CL=3	tAC	2.0	5.0	ns	
	CL=2		2.0	8.0		
Clock High pulse width		tCH	0.45	0.55	tCK	
Clock Low pulse width		tCL	0.45	0.55	tCK	
CKE *min.* pulse width (High/Low pulse width)		tCKE	1		tCK	
DQ and DM Input Setup time		tDS	0.48		ns	2, 3, 4
DQ and DM Input Hold time		tDH	0.48		ns	2, 3, 4
DQ and DM Input Pulse width		tDIPW	1.6		ns	5
Address and Control Input Setup time		tIS	0.9		ns	4, 6, 7
Address and Control Input Hold time		tIH	0.9		ns	4, 6, 7
Address and Control Input Pulse Width		tIPW	2.3		ns	5
DQ & DQS Low-impedance time from CK, /CK		tLZ	1.0		ns	8
DQ & DQS High-impedance time from CK, /CK		tHZ		5.0	ns	8
DQS - DQ Skew		tDQSQ		0.4	ns	9
Half Clock Period		tHP	tCH, tCL		ns	
Data Hold Skew Factor		tQHS		0.5	ns	
DQ / DQS Output Hold time from DQS		tQH	tHP-tQHS		ns	
Write Command to first DQS Latching Transition		tDQSS	0.75	1.25	tCK	
DQS Input High pulse Width		tDQSH	0.35	0.6	tCK	
DQS Input Low pulse Width		tDQSL	0.35	0.6	tCK	
DQS Falling Edge to CK Setup Time		tDSS	0.2		tCK	
DQS Falling Edge Hold Time From CK		tDSH	0.2		tCK	
Access Window of DQS from CK, /CK	CL=3	tDQSCK	2.0	5.0	ns	
	CL=2		2.0	8.0	ns	
ACTIVE to PRECHARGE Command Period		tRAS	40		ns	
ACTIVE to ACTIVE Command Period		tRC	55		ns	
Mode Register Set command cycle time		tMRD	2		tCK	
SRR to Read		tSRR	2		tCK	
Read of SRR to next valid command		tSRC	CL+1		tCK	
Refresh Period		tREF		64	ms	15
Average periodic refresh interval		tREFI		15.6	us	10,15
Auto Refresh Period		tRFC	70		ns	
Active to Read or Write delay		tRCD	15		ns	
Precharge command period		tRP	15		ns	
Active Bank *A* to Active Bank *B* Delay		tRRD	10		ns	
Write Recovery time		tWR	15		ns	
Auto Precharge Write Recovery + Precharge time		tDAL	(tWR/tCK) + (tRP/tCK)			
Internal Write to Read Command Delay		tWTR	1		tCK	
DQS Read preamble	CL=3	tRPRE	0.9	1.1	tCK	11
	CL=2		0.5	1.1	tCK	11
DQS Read postamble		tRPST	0.4	0.6	tCK	
DQS Write preamble		tWPRE	0.25		tCK	
DQS Write preamble setup time		tWPRES	0		ns	12
DQS Write postamble		tWPST	0.4	0.6	tCK	13
Exit Power Down to next valid command Delay		tXP	1		tCK	14
Self Refresh Exit to next valid Command Delay		tXSR	120		ns	

Table16: AC Characteristic (AC operation conditions unless otherwise noted)

Parameter		Symbol	-6		-75		Unit	Note
			Min	Max	Min	Max		
System Clock Cycle time	CL=3	tCK	6	1000	7.5	1000	ns	1
	CL=2		10		10		ns	1
DQ Output access time from CK, /CK	CL=3	tAC	2.0	5.5	2.0	6.0	ns	
	CL=2		2.0	8.0	2.0	8.0		
Clock High pulse width		tCH	0.45	0.55	0.45	0.55	tCK	
Clock Low pulse width		tCL	0.45	0.55	0.45	0.55	tCK	
CKE *min.* pulse width (High/Low pulse width)		tCKE	1		1		tCK	
DQ and DM Input Setup time		tDS	0.6		0.9		ns	2, 3, 4
DQ and DM Input Hold time		tDH	0.6		0.9		ns	2, 3, 4
DQ and DM Input Pulse width		tDIPW	1.8		2.0		ns	5
Address and Control Input Setup time		tIS	1.0		1.3		ns	4, 6, 7
Address and Control Input Hold time		tIH	1.0		1.3		ns	4, 6, 7
Address and Control Input Pulse Width		tIPW	2.7		3.0		ns	5
DQ & DQS Low-impedance time from CK, /CK		tLZ	1.0		1.0		ns	8
DQ & DQS High-impedance time from CK, /CK		tHZ		5.5		6	ns	8
DQS - DQ Skew		tDQSQ		0.5		0.6	ns	9
Half Clock Period		tHP	tCH, tCL		tCH, tCL		ns	
Data Hold Skew Factor		tQHS		0.65		0.75	ns	
DQ / DQS Output Hold time from DQS		tQH	tHP-tQHS		tHP-tQHS		ns	
Write Command to first DQS Latching Transition		tDQSS	0.75	1.25	0.75	1.25	tCK	
DQS Input High pulse Width		tDQSH	0.35	0.6	0.4	0.6	tCK	
DQS Input Low pulse Width		tDQSL	0.35	0.6	0.4	0.6	tCK	
DQS Falling Edge to CK Setup Time		tDSS	0.2		0.2		tCK	
DQS Falling Edge Hold Time From CK		tDSH	0.2		0.2		tCK	
Access Window of DQS from CK, /CK	CL=3	tDQSCK	2.0	5.5	2.0	6.0	ns	
	CL=2		2.0	8.0	2.0	8.0	ns	
ACTIVE to PRECHARGE Command Period		tRAS	42		45		ns	
ACTIVE to ACTIVE Command Period		tRC	60		75		ns	
Mode Register Set command cycle time		tMRD	2		2		tCK	
SRR to Read		tSRR	2		2		tCK	
Read of SRR to next valid command		tSRC	CL+1		CL+1		tCK	
Refresh Period		tREF		64		64	ms	15
Average periodic refresh interval		tREFI		15.6		15.6	us	10,15
Auto Refresh Period		tRFC	70		70		ns	
Active to Read or Write delay		tRCD	18		22.5		ns	
Precharge command period		tRP	18		22.5		ns	
Active Bank *A* to Active Bank *B* Delay		tRRD	12		15		ns	
Write Recovery time		tWR	15		15		ns	
Auto Precharge Write Recovery + Precharge time		tDAL	(tWR/tCK) + (tRP/tCK)					
Internal Write to Read Command Delay		tWTR	1		1		tCK	
DQS Read preamble	CL=3	tRPRE	0.9	1.1	0.9	1.1	tCK	11
	CL=2		0.5	1.1	0.5	1.1	tCK	11
DQS Read postamble		tRPST	0.4	0.6	0.4	0.6	tCK	
DQS Write preamble		tWPRE	0.25		0.25		tCK	
DQS Write preamble setup time		tWPRES	0		0		ns	12
DQS Write postamble		tWPST	0.4	0.6	0.4	0.6	tCK	13
Exit Power Down to next valid command Delay		tXP	1		1		tCK	14
Self Refresh Exit to next valid Command Delay		tXSR	120		120		ns	

Note :

1. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including tDPL, and PRECHARGE commands). CKE may be used to reduce the data rate.
2. The transition time for DQ, DM and DQS inputs is measured between VIL(DC) to VIH(AC) for rising input signals, and VIH(DC) to VIL(AC) for falling input signals.
3. DQS, DM and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.
4. Input slew rate ≥ 0.5V/ns and < 1.0V/ns.

Input setup/hold slew rate [V/ns]	ΔtDS/ΔtIS [ps]	ΔtDH/ΔtIH [ps]
1.0	0	0
0.5	+150	+150

5. These parameters guarantee device timing but they are not necessarily tested on each device.
6. The transition time for address and command inputs is measured between VIH and VIL.
7. A CK,/CK slew rate must be ≥ 1.0V/ns (2.0V/ns if measured differentially) is assumed for this parameter.

CK,/CK setup/hold slew rate [V/ns]	ΔtDS/ΔtIS [ps]	ΔtDH/ΔtIH [ps]
1.0	0	0

8. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
9. tDQSQ consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
10. A maximum of eight Refresh commands can be posted to any given Low-Power DDR SDRAM, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 8*tREFI.
11. A low level on DQS may be maintained during High-Z states (DQS drivers disabled) by adding a weak pull-down element in the system. It is recommended to turn off the weak pull-down element during read and write bursts (DQS drivers enabled).
12. The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
13. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
14. At least one clock pulse is required during t_{XP}.
15. The specifications in the table for T_{REF} and T_{REFI} are applicable for all temperature grades with $T_A \leq +85°C$. Only A2 temperature grade supports operation with $T_A > 85°C$, and these values must be further constrained with $T_{REF\ max}$ of 32ms, and $T_{REFI\ max}$ of 7.8µs.

Timing Diagram

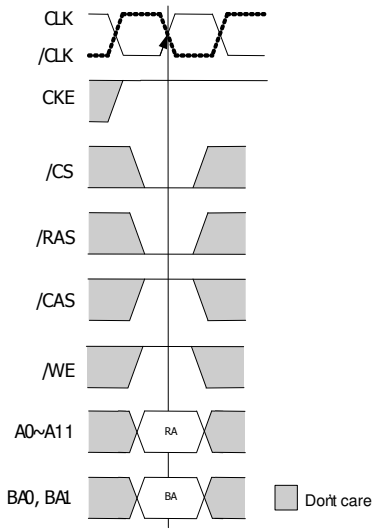
Bank/row Activation

The Active command is used to activate a row in particular bank for a subsequent Read or Write access. The value of the BA0,BA1 inputs selects the bank, and the address provided on A0-A12 (or the highest address bit) selects the row.

Before any READ or WRITE commands can be issued to a bank within the Mobile DDR SDRAM, a row in that bank must be opened. This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated. The row remains active until a PRECHARGE (or READ with AUTO PRECHARGE or WRITE with AUTO PRECHARGE) command is issued to the bank.

A PRECHARGE (or READ with AUTO PRECHARGE or WRITE with AUTO PRECHARGE) command must be issued before opening a different row in the same bank.

Figure 11 : Active command

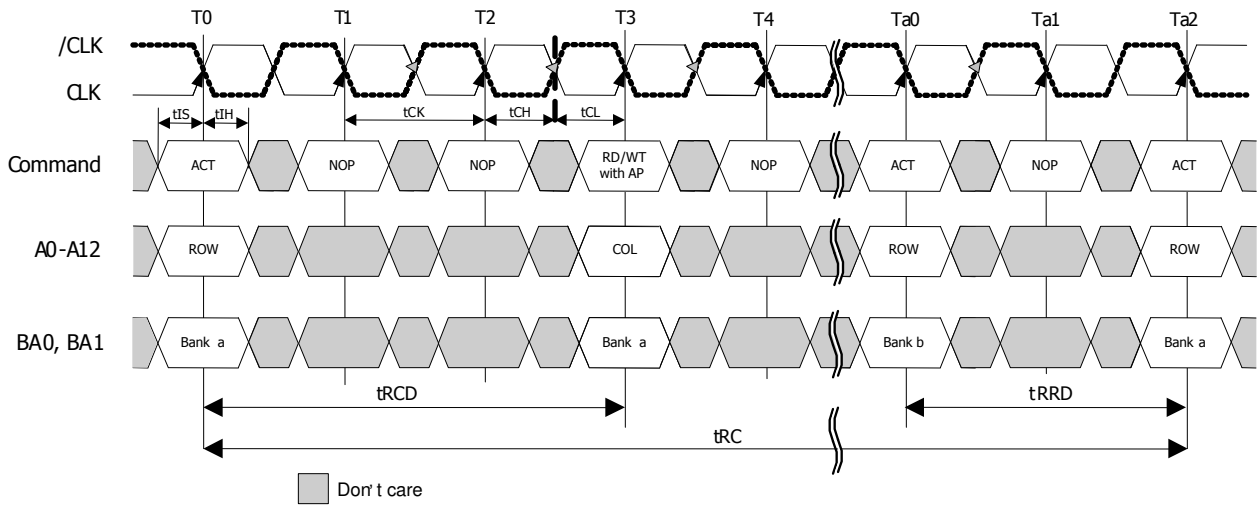


Notes :
1. RA : Row address
2. BA : Bank address

Once a row is Open(with an ACTIVE command) a READ or WRITE command may be issued to that row, subject to the tRCD specification. tRCD(min) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been closed(precharge). The minimum time interval between successive ACTIVE commands to the same bank is defined by tRC. A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by tRRD.

Figure 12: tRCD, tRRD, tRC



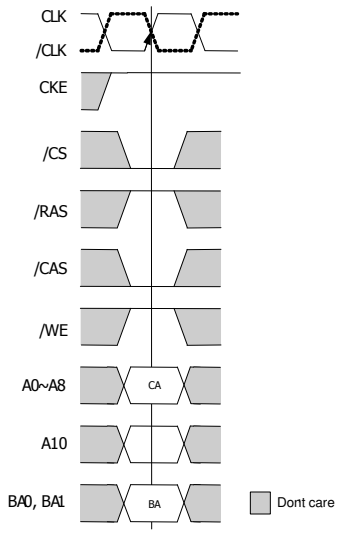
Read

The READ command is used to initiate a Burst Read to an active row. The value of BA0 and BA1 selects the bank and address inputs select the starting column location.

The value of A10 determines whether or not auto-precharge is used. If auto-precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent access. The valid data-out elements will be available CAS latency after the READ command is issued.

The Mobile DDR drives the DQS during read operations. The initial low state of the DQS is known as the read preamble and the last data-out element is coincident with the read postamble. DQS is edge-aligned with read data. Upon completion of a burst, assuming no new READ commands have been initiated, the I/O's will go high-Z.

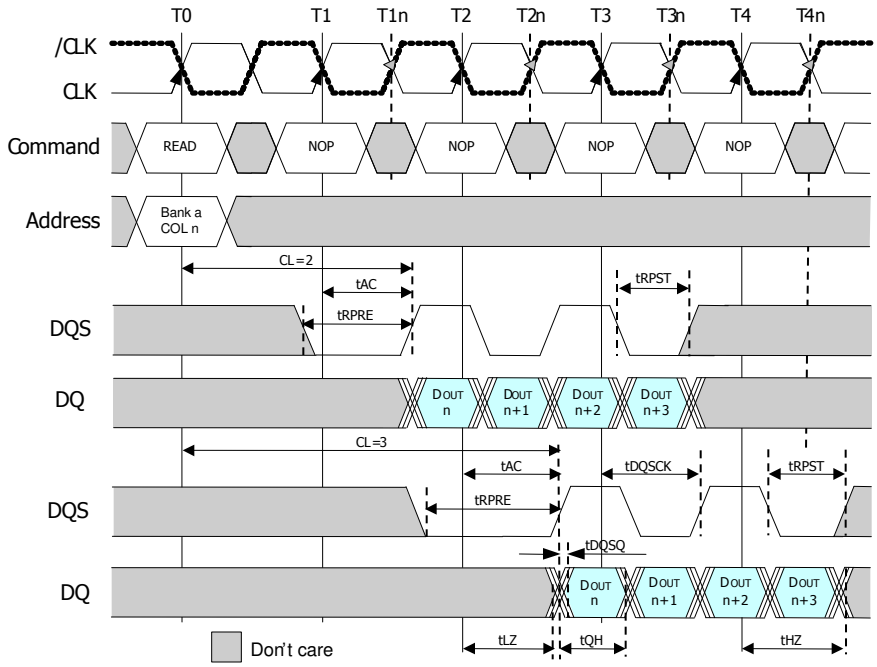
Figure 13 : Read command



Notes :

1. CA : Column address
2. BA : Bank address
3. A10=High : Enable Auto precharge
   A10=Low : Disable Auto precharge

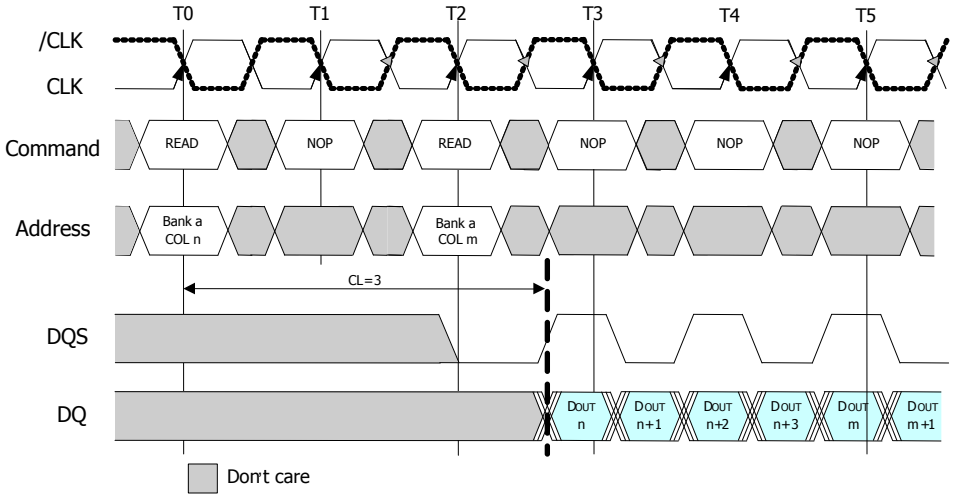
Figure 14 : Read Data out timing (BL=4)



Notes:

1. BL=4
2. Shown with nominal tAC, tDQSCK and tDQSQ

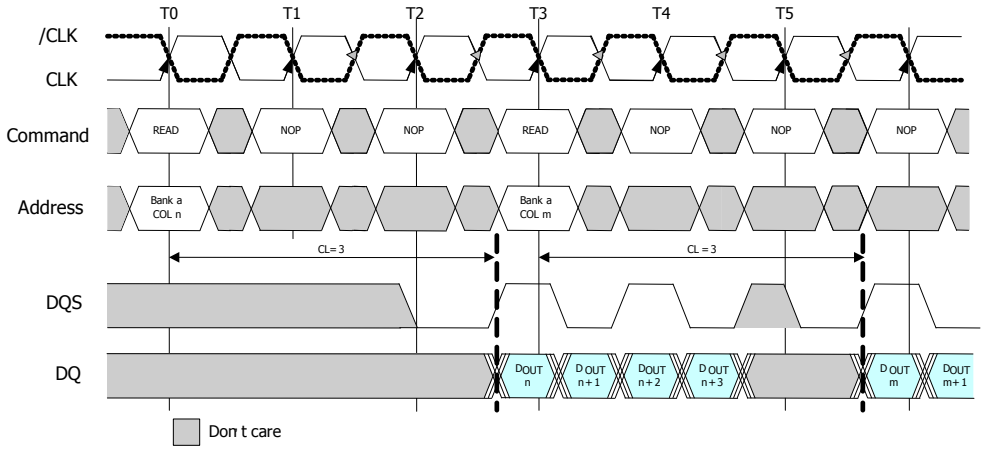
Figure 15 : Consecutive Read bursts (BL=4)



Notes:

1. Dout n or m = Data-Out from Column n or m
2. BL=4,8,16 (if 4, the bursts are concatenated; If 8 or 16, the second burst interrupts the first)
3. Shown with nominal tAC, tDQSCK and tDQSQ

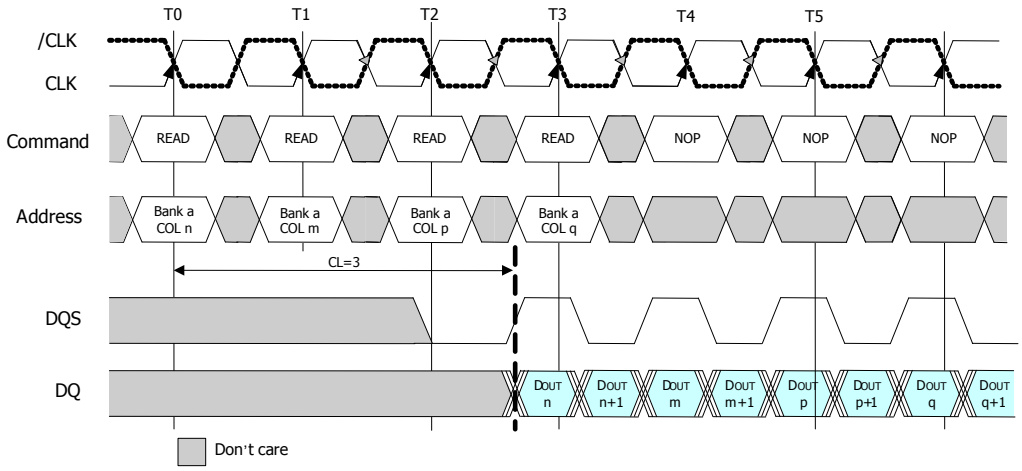
Figure 16 : Non-Consecutive Read bursts (BL=4)



Notes:

1. Dout n or m = Data-Out from Column n or m
2. BL=4,8,16 (if 4, the bursts are concatenated; If 8 or 16, the second burst interrupts the first)
3. Shown with nominal tAC, tDQSCK and tDQSQ

Figure 17 : Random Read access



Notes:

1. Dout n or m,p,q = Data-Out from Column n or m,p,q
2. BL=2,4,8,16 (if 4,8 or 16, the following burst interrupts the previous)
3. Reads are to an Active row in any bank.
4. Shown with nominal tAC, tDQSCK and tDQSQ

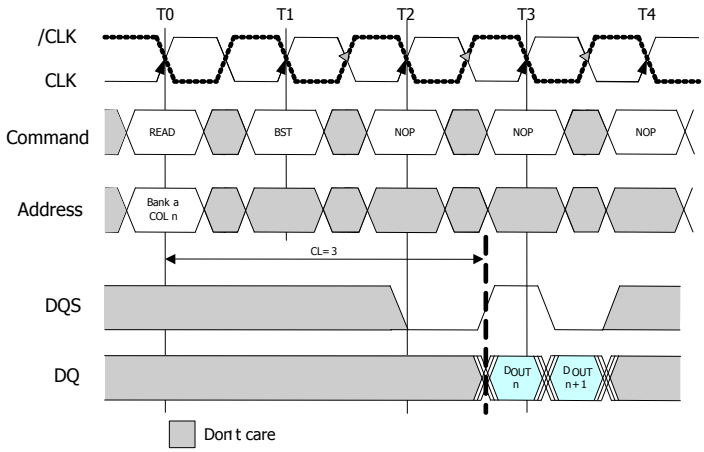
Truncated Reads

Data from any READ burst may be truncated with a BURST TERMINATE command, as shown in Figure16. The BURST TERMINATE latency is equal to the READ (CAS) latency, i.e., the BURST TERMINATE command should be issued x cycles after the READ command, where x equals the number of desired data element pairs (pairs are required by the 2n-prefetch architecture).

Data from any READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used.

A READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank provided that auto precharge was not activated. The PRECHARGE command should be issued x cycles after the READ command, where x equals the number of desired data element pairs (pairs are required by the n-prefetch architecture). This is shown in Figure (READ to PRECHARGE). Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.

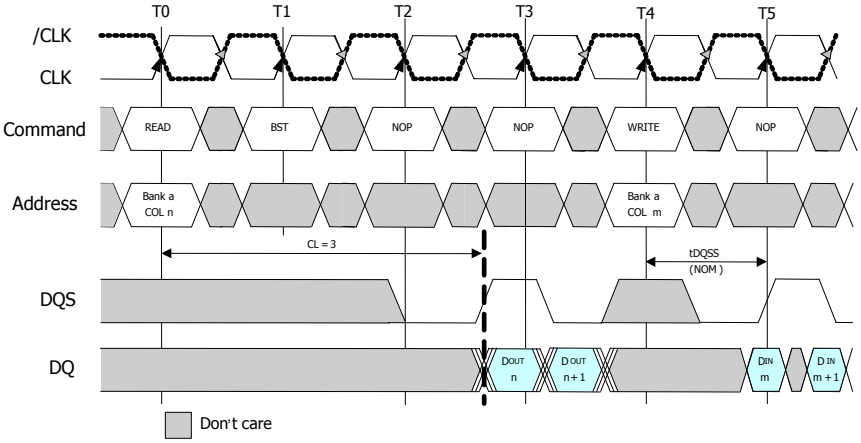
Figure 18 : Read Burst terminate (BL=4,8 or 16)



Notes:

1. Dout n = Data-Out from Column n
2. CKE=high
3. Shown with nominal tAC, tDQSCK and tDQSQ

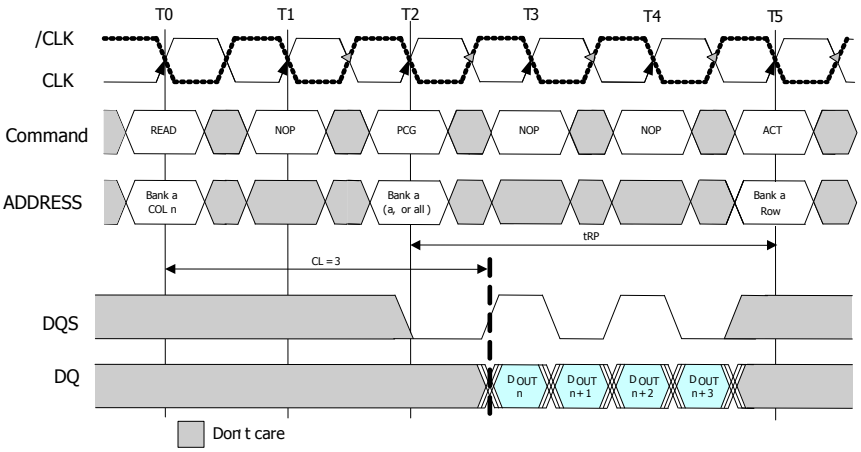
Figure 19 : Read to write terminate (BL=4,8 or 16)



Notes:

1. Dout n = Data-Out from Column n , Din m = Data-In from Column m.
2. CKE=high
3. Shown with nominal tAC, tDQSCK and tDQSQ

Figure 20 : Read to Precharge (BL=4)



Notes:

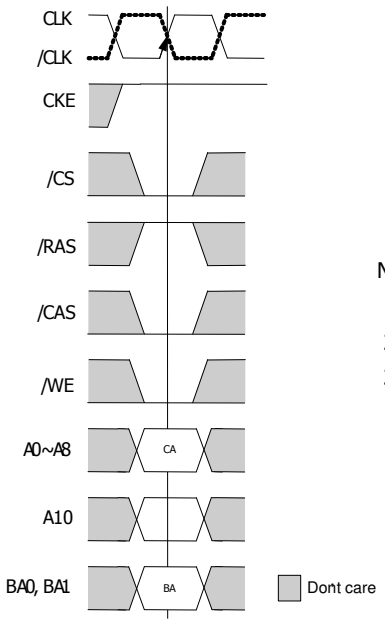
1. Dout n = Data-Out from Column n.
2. Read to Precharge equals 2 tCK, which allows 2 data pairs of Data-Out.
3. Shown with nominal tAC, tDQSCK and tDQSQ

Write

The WRITE command is used to initiate a Burst Write access to an active row. The value of BA0, BA1 selects the bank and address inputs select the starting column location.

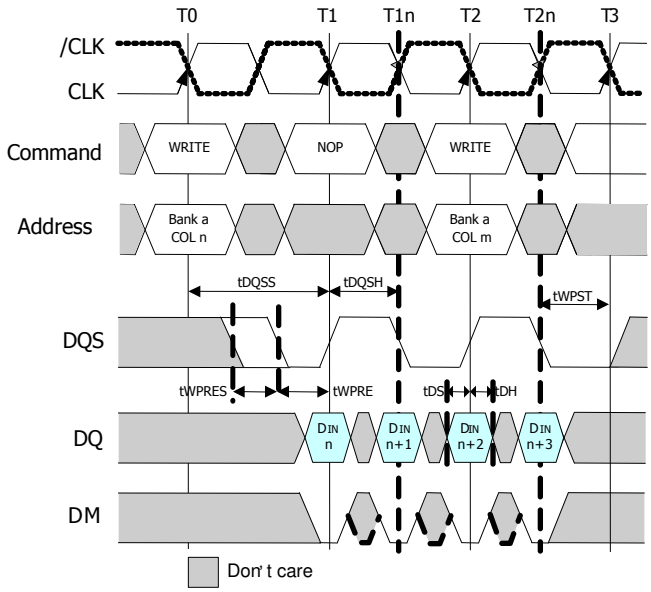
The value of A10 determines whether or not auto precharge is used.If autoprecharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent access. Input data appearing on the data bus, is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered low, the corresponding data will be written to the memory; if the DM signal is registered high, the corresponding data-inputs will be ignored, and a write will not be executed to that byte/column location. The memory controller drives the DQS during write operations. The initial low state of the DQS is known as the write preamble and the low state following the last data-in element is write postamble. Upon completion of a burst, assuming no new commands have been initiated, the I/O's will stay high-Z and any additional input data will be ignored.

Figure 21 : Write command



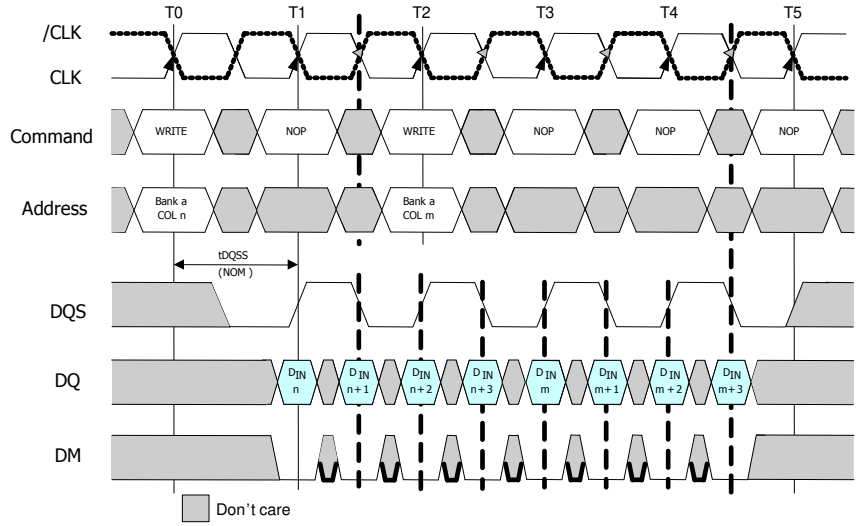
Notes :
1. CA : Column address
2. BA : Bank address
3. A10=High : Enable Auto precharge
   A10=Low : Disable Auto precharge

Figure 22 : Write Burst (BL=4)



Notes:
1. Din n = Data-In from Column n.

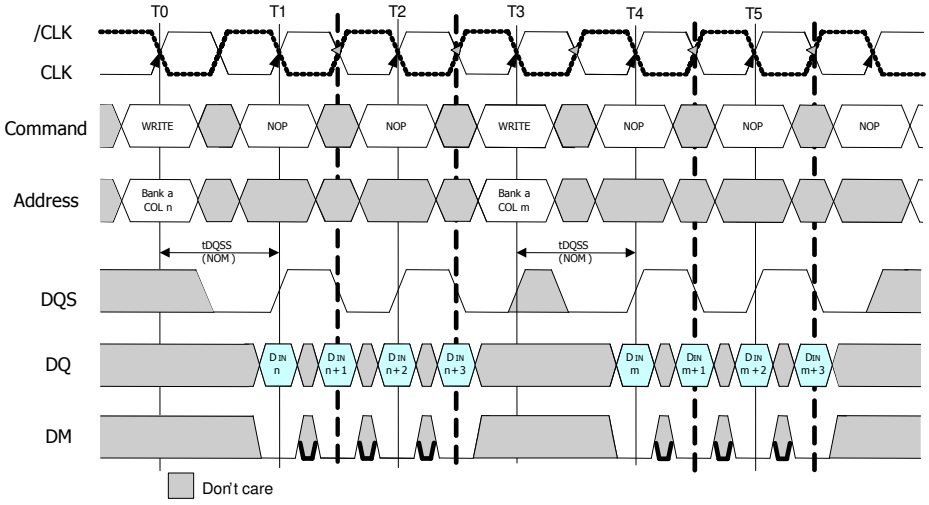
Figure 23 : Consecutive Write to write (BL=4)



Notes:

1. Din n = Data-In from Column n.
2. Each Write command may be to any banks.

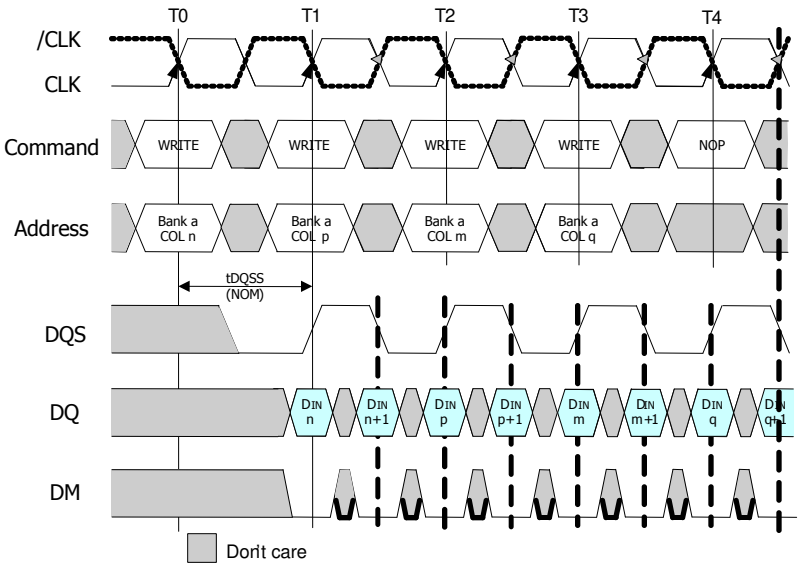
Figure 24 : Non-Consecutive Write to write (BL=4)



Notes:

1. Din n = Data-In from Column n.
2. Each Write command may be to any banks.

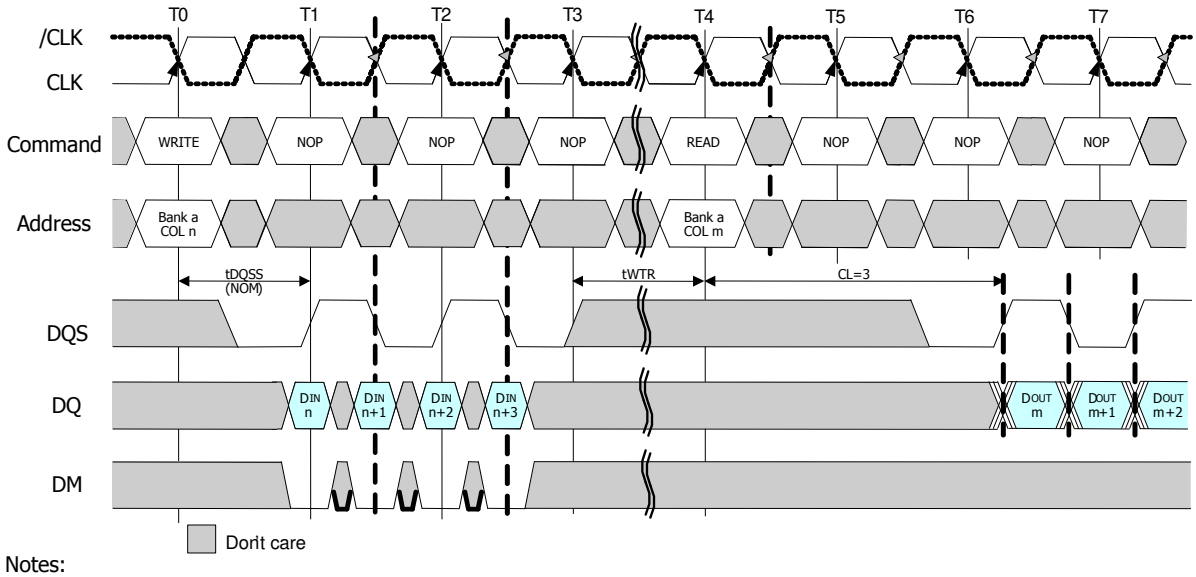
Figure 25 : Random Write to write



Notes:

1. Din n,p,m,q = Data-In from Column n,p,m,q.
2. Each Write command may be to any banks.

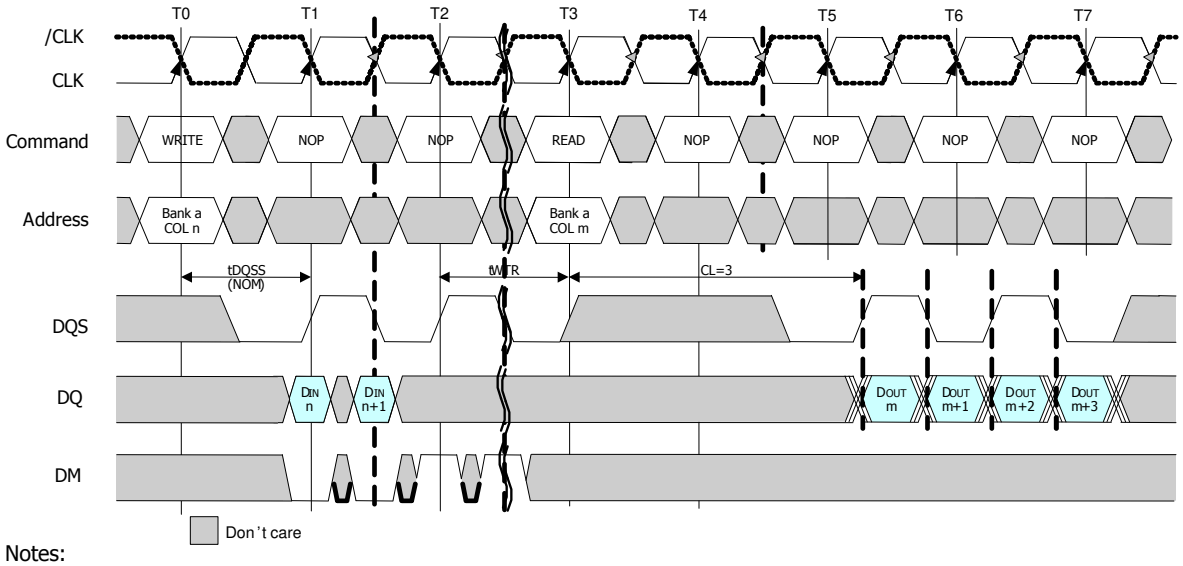
Figure 26 : Write to Read (Uninterrupting)



Notes:

1. Din n = Data-In from Column n, Dout m = Data-Out from Column m.
2. tWTR is referenced from the first positive CK edge after the last data-in pair.
3. Read and Write command can be directed to different banks, in which case tWTR is not required and the Read command could be applied ealier.

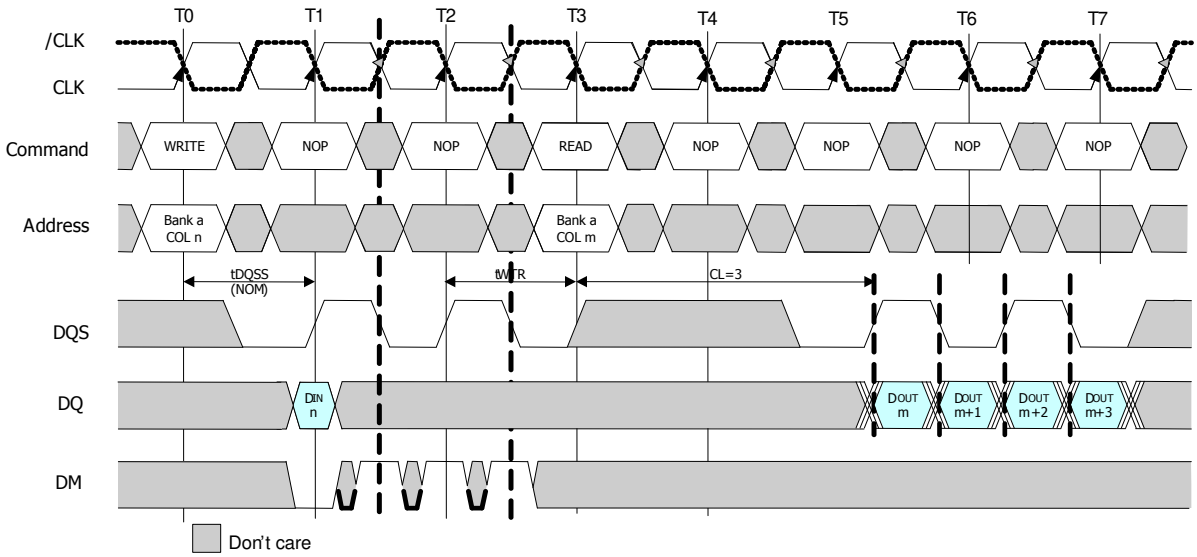
Figure 27 : Write to Read (Interrupting)



Notes:

1. Din n = Data-In from Column n, Dout m = Data-Out from Column m.
2. tWTR is referenced from the first positive CK edge after the last data-in pair.

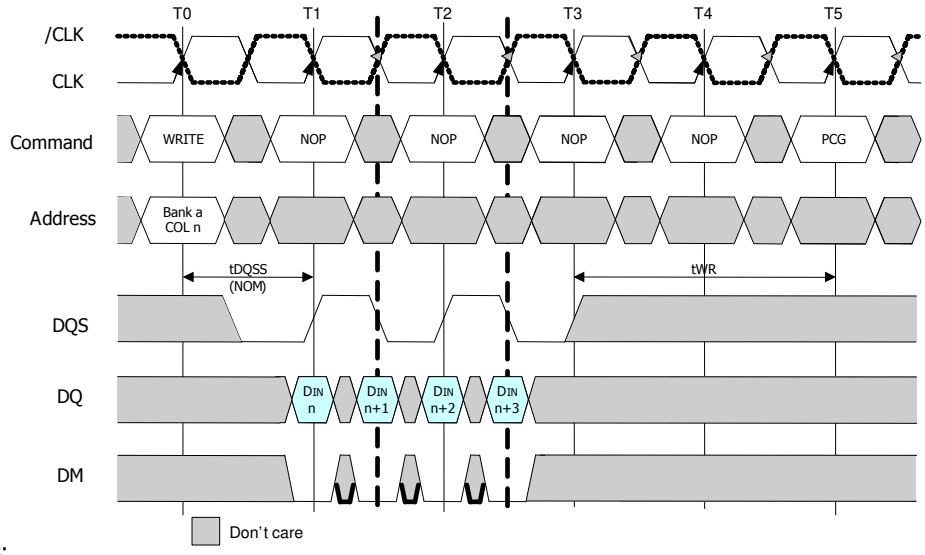
Figure 28 : Write to Read (Odd number of data Interrupting)



Notes:

1. Din n = Data-In from Column n, Dout m = Data-Out from Column m.
2. tWTR is referenced from the first positive CK edge after the last data-in pair.

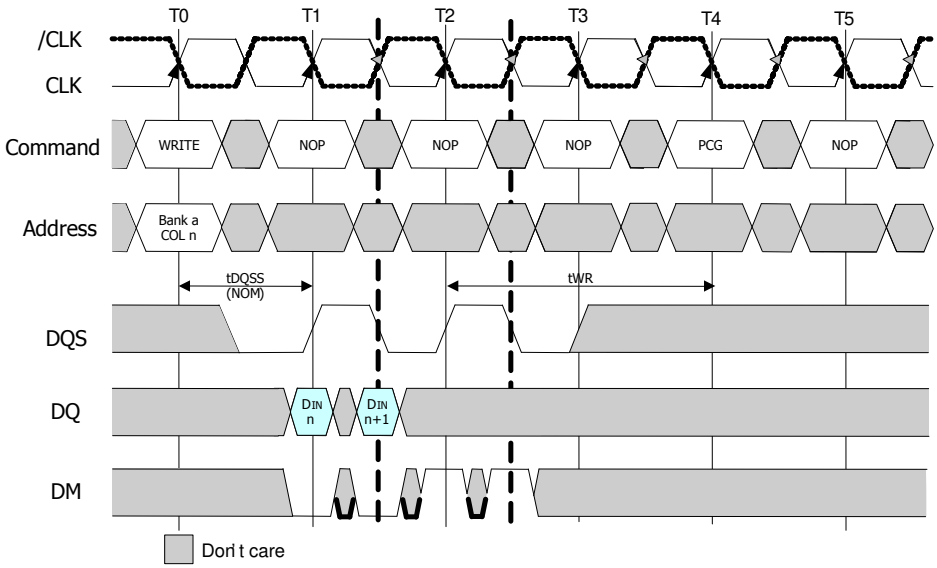
Figure 29 : Write to Precharge (Uninterrupting)



Notes:

1. Din n = Data-In from Column n.
2. tWR is referenced from the first positive CK edge after the last data-in pair.
3. Read and Write command can be directed to different banks, in which case tWR is not required and the Read command could be applied ealier.

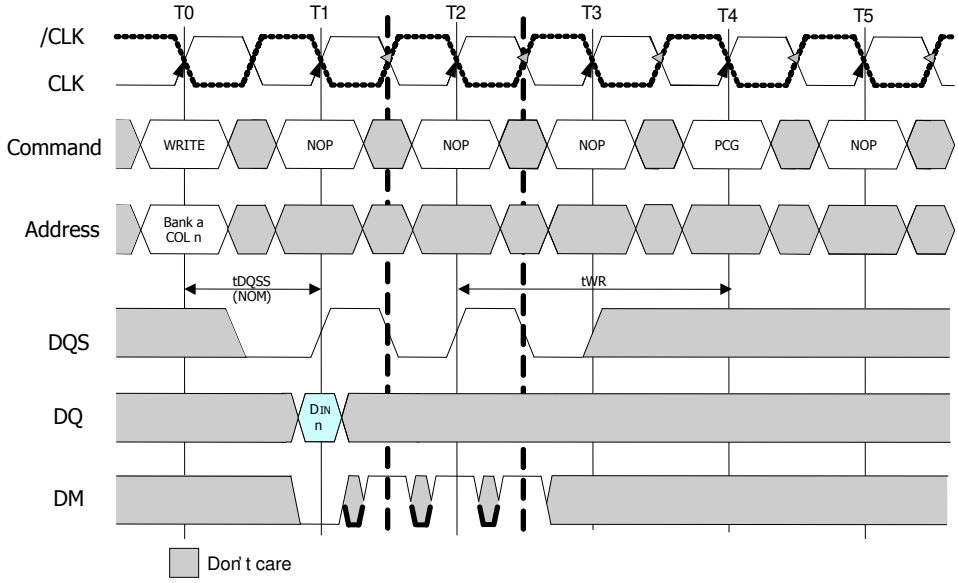
Figure 30 : Write to Precharge (Interrupting)



Notes:

1. Din n = Data-In from Column n.
2. tWR is referenced from the first positive CK edge after the last data-in pair.
3. Read and Write command can be directed to different banks, in which case tWR is not required and the Read command could be applied ealier.

Figure 31 : Write to Precharge (Odd number of data Interrupting)



Notes:

1. Din n = Data-In from Column n.
2. tWR is referenced from the first positive CK edge after the last data-in pair.
3. Read and Write command can be directed to different banks, in which case tWR is not required and the Read command could be applied ealier.

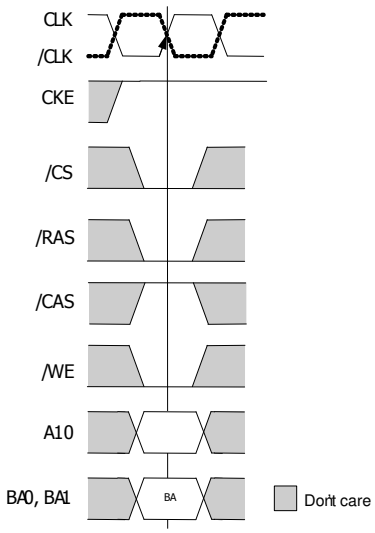
Precharge

The Precharge command is used to deactivate the open row in a particular bank or the open row in all banks. The banks will be available for subsequent row access some specified time (tRP) after the Precharge command issued.

Input A10 determines whether one or all banks are to be precharged. In the case where only one bank is to be precharged (A10=Low), inputs BA0,BA1 select the banks.

When all banks are to be precharged (A10=High), inputs BA0,BA1 are treated as a "Don't Care". Once a bank has been precharged, it is in the idle state and must be actived prior to any Read or Write commands being issued to that bank.

Figure 32 : Precharge command



Notes :

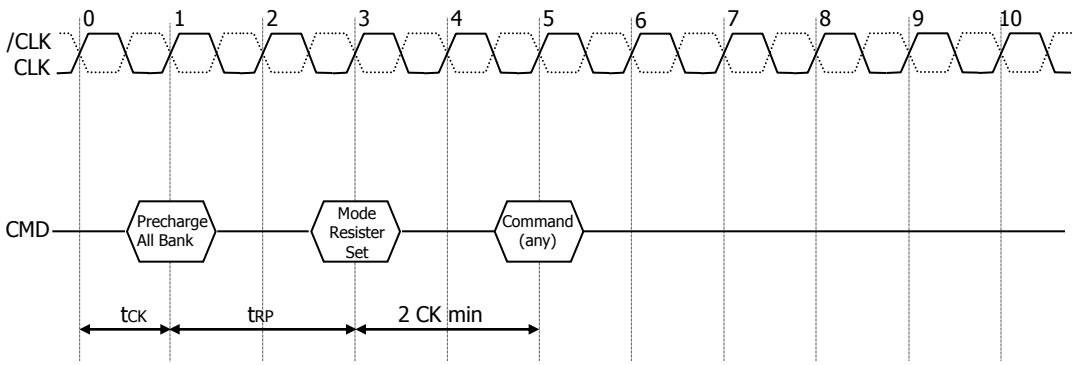
1. BA : Bank address

Mode Register

The mode register contains the specific mode of operation of the Mobile DDR SDRAM. This register includes the selection of a burst length (2, 4, 8, 16), a cas latency(2, 3), a burst type. The mode register set must be done before any activate command after the power up sequence.

Any contents of the mode register be altered by re-programming the mode register through the execution of mode register set command.

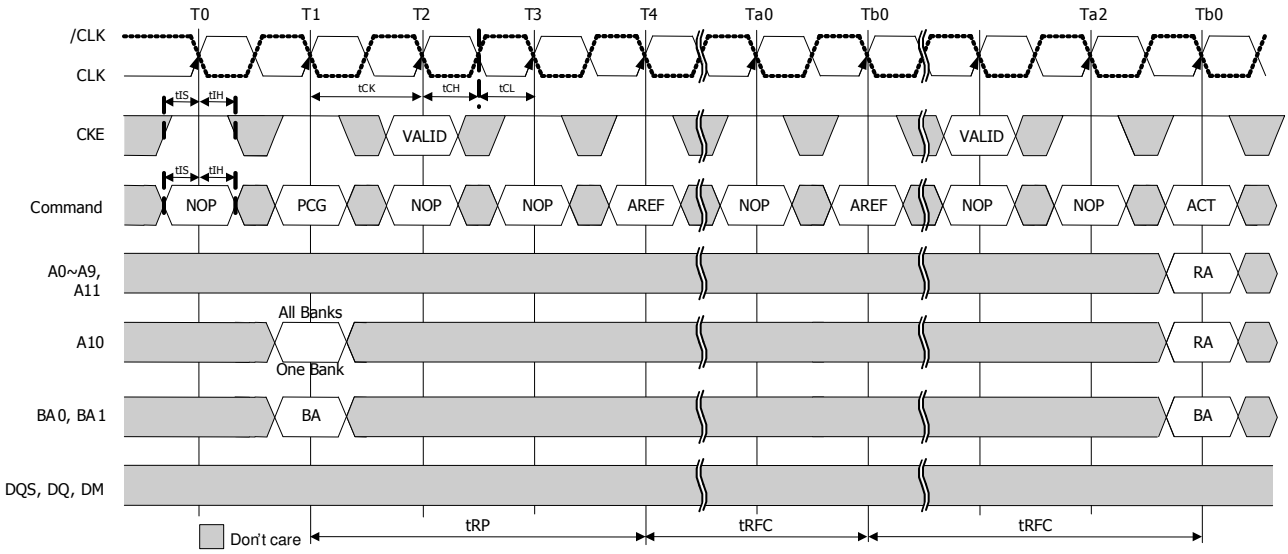
Figure 33 : Mode Resister Set



Auto refresh

The Auto refresh command is used during normal operation of the Mobile DDR. It is non persistent, so must be issued each time a refresh is required. The refresh addressing is generated by the internal refresh controller. The Mobile DDR requires AUTO REFRESH commands at an average periodic interval of tREFI. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given Mobile DDR, and the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 8*tREFI.

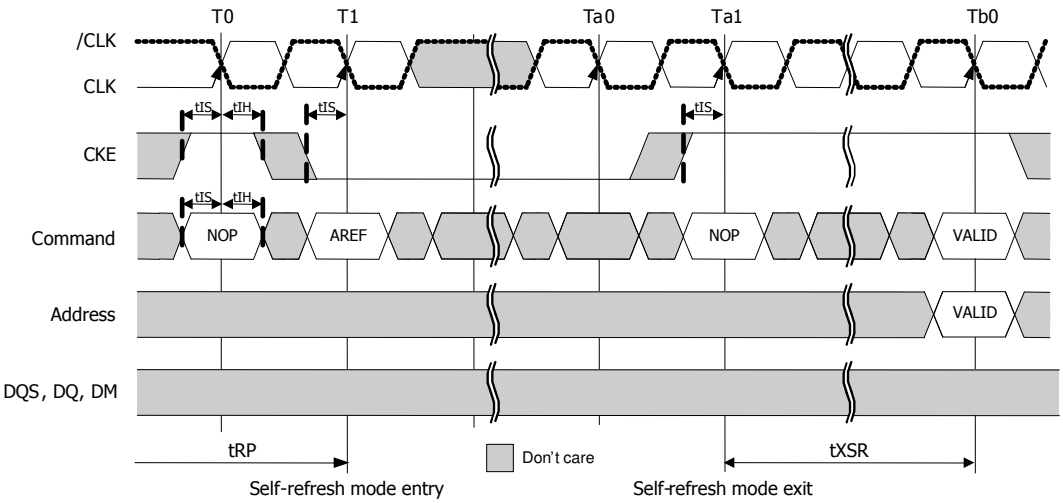
Figure 34 : Auto refresh



Self refresh

This state retains data in the Mobile DDR, even if the rest of the system is powered down (even without external clocking). Note refresh interval timing while in Self Refresh mode is scheduled internally in the Mobile DDR and may vary and may not meet tREFI time. "Don't Care" except CKE, which must remain low. An internal refresh cycle is scheduled on Self Refresh entry. The procedure for exiting Self Refresh mode requires a series of commands. First clock must be stable before CKE going high. NOP commands should be issued for the duration of the refresh exit time (tXSR), because time is required for the completion of any internal refresh in progress. The use of SELF REFRESH mode introduces the possibility that an internally timed event can be missed when CKE is raised for exit from self refresh mode.

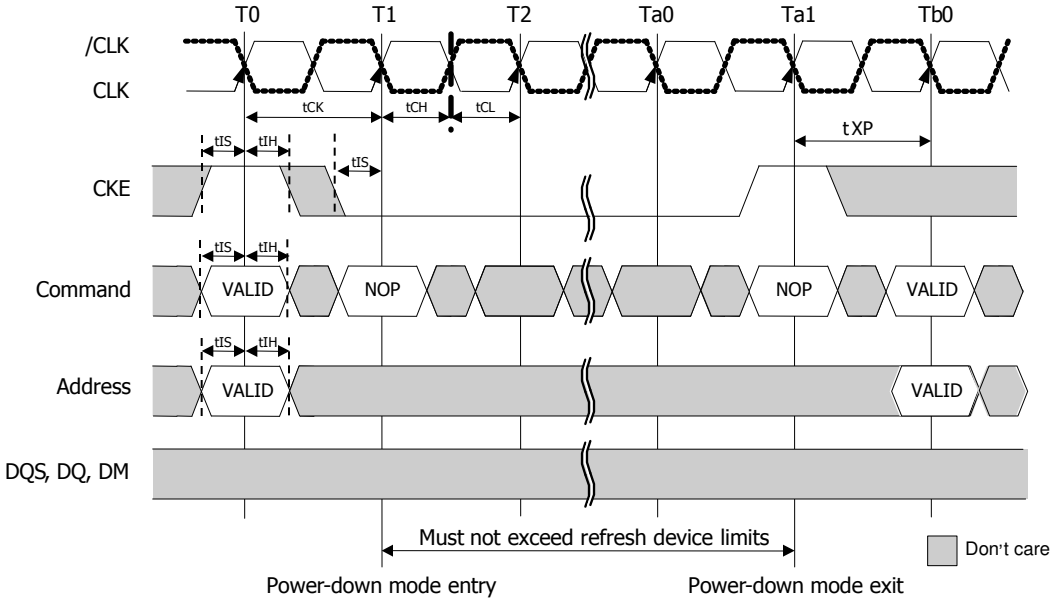
Figure 35 : Self refresh



Power down

Power down occurs if CKE is set low coincident with Device Deselect or NOP command and when no accesses are in progress. If power down occurs when all banks are idle, it is Precharge Power Down. If Power down occurs when one or more banks are Active, it is referred to as Active power down. The device cannot stay in this mode for longer than the refresh requirements of the device, without losing data. The power down state is exited by setting CKE high while issuing a Device Deselect or NOP command. A valid command can be issued after tXP.

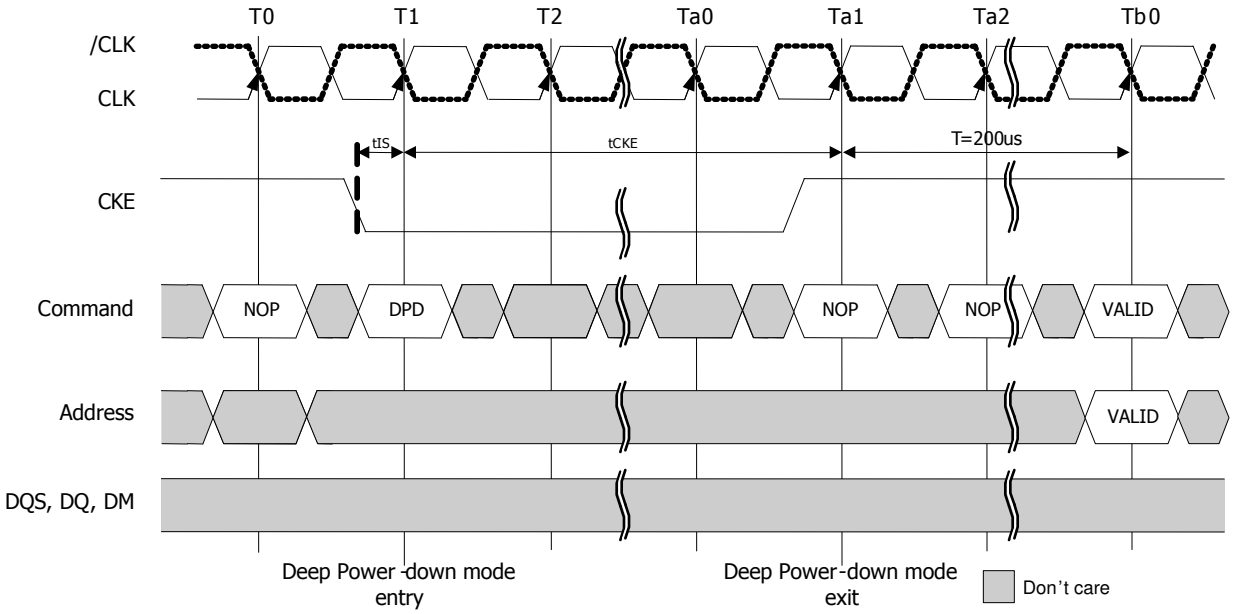
Figure 36 : Power down (Active or Precharge)



Deep Power down

The Deep Power-Down (DPD) mode enables very low standby currents. All internal voltage generators inside the Mobile DDR are stopped and all memory data is lost in this mode. All the information in the Mode Register and the Extended Mode Register is lost. Next Figure, DEEP POWER-DOWN COMMAND shows the DEEP POWER-DOWN command All banks must be in idle state with no activity on the data bus prior to entering the DPD mode. While in this state, CKE must be held in a constant low state. To exit the DPD mode, CKE is taken high after the clock is stable and NOP command must be maintained for at least 200 us.

Figure 37 : Deep Power down



Clock Stop Mode

Clock stop mode is a feature supported by Mobile DDR SDRAM devices. It reduces clock-related power consumption during idle periods of the device.

Conditions: the Mobile DDR SDRAM supports clock stop in case:

- The last access command (ACTIVE, READ, WRITE, PRECHARGE, AUTO REFRESH or MODE REGISTER SET) has executed to completion, including any data-out during read bursts; the number of required clock pulses per access command depends on the device's AC timing parameters and the clock frequency;
- The related timing condition (tRCD, tWR, tRP, tRFC, tMRD) has been met;
- CKE is held HIGH.

When all conditions have been met, the device is either in "idle" or "row active" state, and clock stop mode may be entered with CK held LOW and /CK held HIGH. Clock stop mode is exited when the clock is restarted. NOPs command have to be issued for at least one clock cycle before the next access command may be applied. Additional clock pulses might be required depending on the system characteristics.

Figure37 illustrates the clock stop mode:

- Initially the device is in clock stop mode;
- The clock is restarted with the rising edge of T0 and a NOP on the command inputs;
- With T1 a valid access command is latched; this command is followed by NOP commands in order to allow for clock stop as soon as this access command has completed;
- T*n* is the last clock pulse required by the access command latched with T1.
- The timing condition of this access command is met with the completion of T*n*; therefore Tn is the last clock pulse required by this command and the clock is then stopped.

Figure 38 : Clock Stop Mode

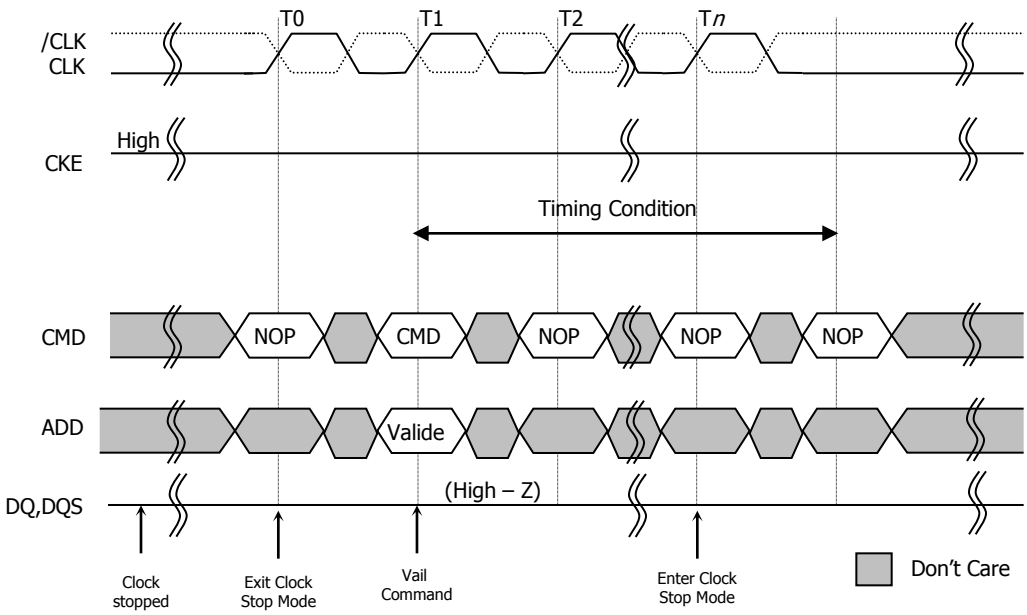
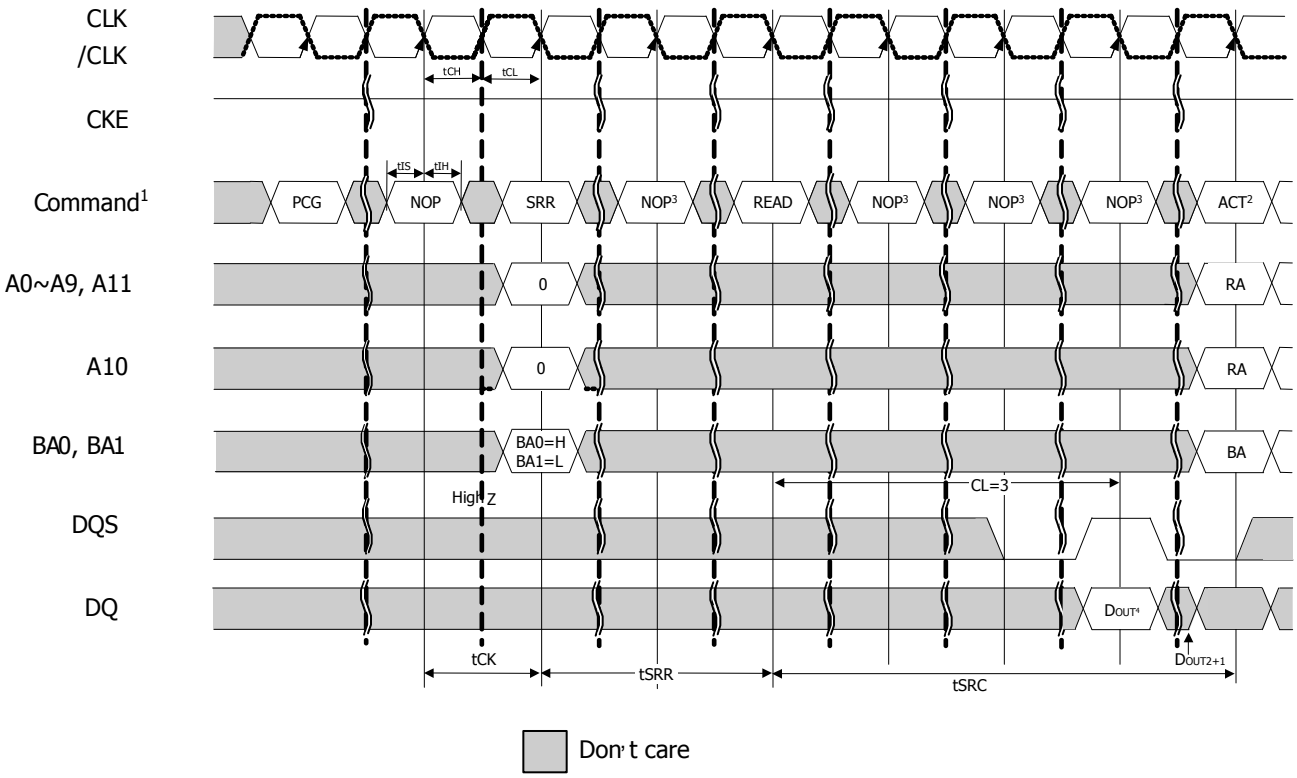


Figure 39 : Status Register Read



Notes:

1. PCG = PRECHARGE command, SRR = Status Register Read command, ACT = ACTIVE command, RA = Row address, BA = Bank address.
2. Other valid commands are possible.
3. NOPs or DESELECTs are required during this time.
4. DOUT1 = Data Out, DOUT2 = dummy data.
5. Data output occurs 3 cycles after Read for CL3, or 2 cycles after Read for CL2.

Ordering Information – VDD = 1.8V

Commercial Range: (0°C to +70°C)

Configuration	Frequency (MHz)	Speed (ns)	Order Part No.	Package
8Mx32	200	5	IS43LR32800G-5BL	90-ball BGA, Lead-free
	166	6	IS43LR32800G-6BL	90-ball BGA, Lead-free

Industrial Range: (-40°C to +85°C)

Configuration	Frequency (MHz)	Speed (ns)	Order Part No.	Package
8Mx32	200	5	IS43LR32800G-5BLI	90-ball BGA, Lead-free
	166	6	IS43LR32800G-6BLI	90-ball BGA, Lead-free

Automotive Range, A1: (-40°C to +85°C)

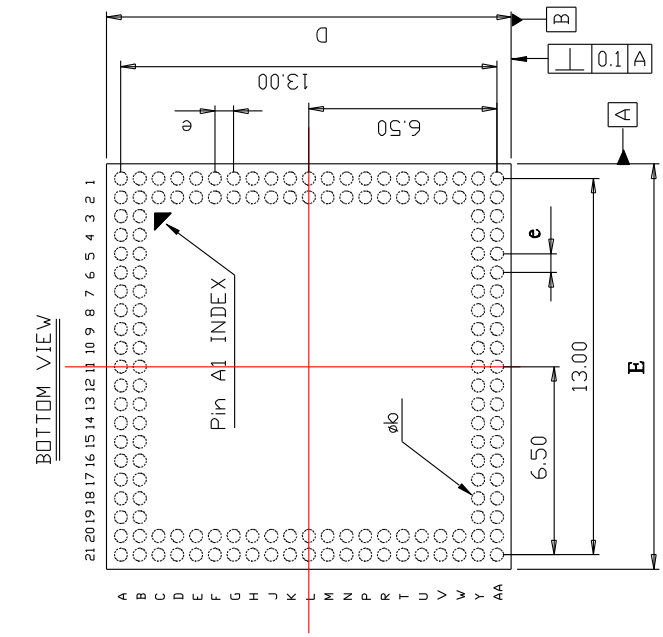
Configuration	Frequency (MHz)	Speed (ns)	Order Part No.	Package
8Mx32	200	5	IS46LR32800G-5BLA1	90-ball BGA, Lead-free
	166	6	IS46LR32800G-6BLA1	90-ball BGA, Lead-free

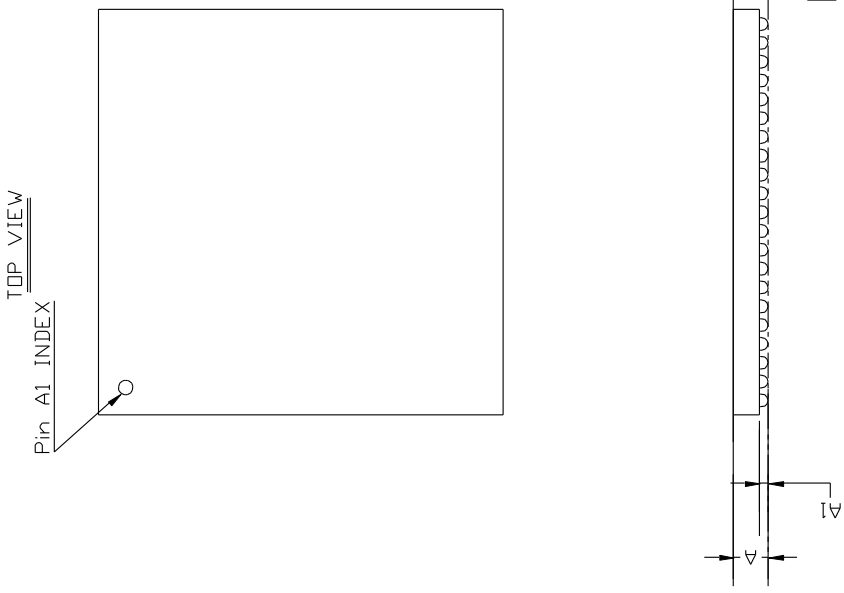
Automotive Range, A2: (-40°C to +105°C)

Configuration	Frequency (MHz)	Speed (ns)	Order Part No.	Package
8Mx32	200	5	IS46LR32800G-5BLA2	90-ball BGA, Lead-free
	166	6	IS46LR32800G-6BLA2	90-ball BGA, Lead-free

Note:
The -6 speed option supports -75 timing specifications

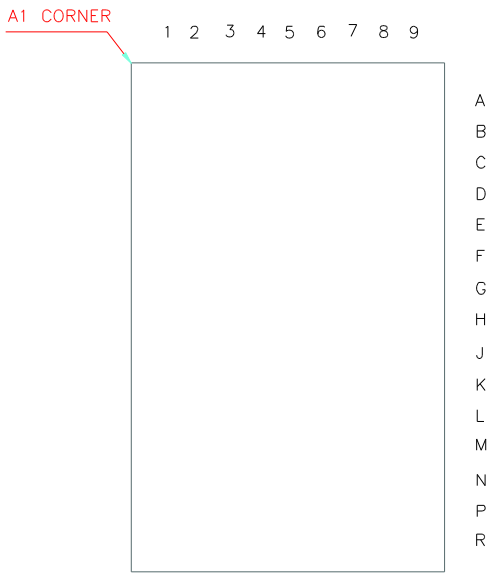
Symbol	Dimension in mm		
	Min	Nom	Max
A	—	—	1.20
A1	0.36	—	0.48
øb	0.40	0.45	0.50
D	13.90	14.00	14.10
E	13.90	14.00	14.10
e	0.60	0.65	0.70



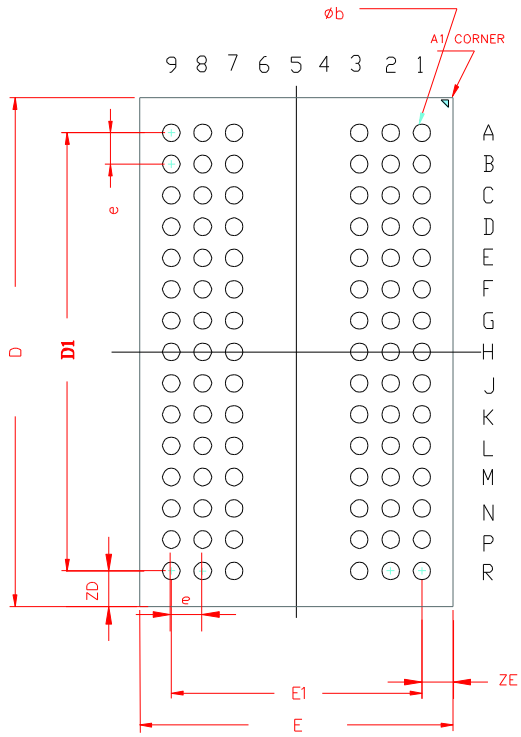


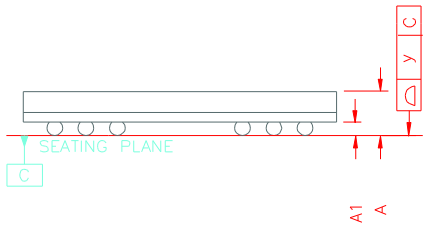
ISSI	TITLE	152L 14x14mm TFBGA Package Outline	REV.	C	DATE	01/25/2013

TOP VIEW



BOTTOM VIEW





SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			0.047
A1	0.25		0.40	0.010		0.016
øb	0.40	0.45	0.50	0.016	0.018	0.020
D	12.90	13.00	13.10	0.508	0.512	0.516
D1	11.20 BSC.			0.441 BSC.		
E	7.90	8.00	8.10	0.311	0.315	0.319
E1	6.40 BSC.			0.252 BSC.		
e	0.80 BSC.			0.315 BSC.		
ZD	0.9 REF.			0.035 REF.		
ZE	0.8 REF.			0.032 REF.		
y	0.10			0.004		

NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207

Ball Pitch :	Ball Diameter :
0.80	0.45

ISSI	TITLE	90L 8x13mm TF-BGA Package Outline	REV.	B	DATE	08/14/2008