IS61C5128AL/AS
IS64C5128AL/AS

512K x 8 HIGH-SPEED CMOS STATIC RAM

MARCH 2008

FEATURES

HIGH SPEED: (IS61/64C5128AL)

- High-speed access time: 10ns, 12 ns
- Low Active Power: 150 mW (typical)
- Low Standby Power: 10 mW (typical) CMOS standby

LOW POWER: (IS61/64C5128AS)

- High-speed access time: 25ns
- Low Active Power: 75 mW (typical)
- Low Standby Power: 1 mW (typical) CMOS standby

- TTL compatible interface levels
- Single 5V ± 10% power supply
- Fully static operation: no clock or refresh required
- Available in 36-pin SOJ (400-mil), 32-pin sTSOP-I, 32-pin SOP, 44-pin TSOP-II and 32-pin TSOP-II packages
- Commercial, Industrial and Automotive temperature ranges available
- Lead-free available

DESCRIPTION

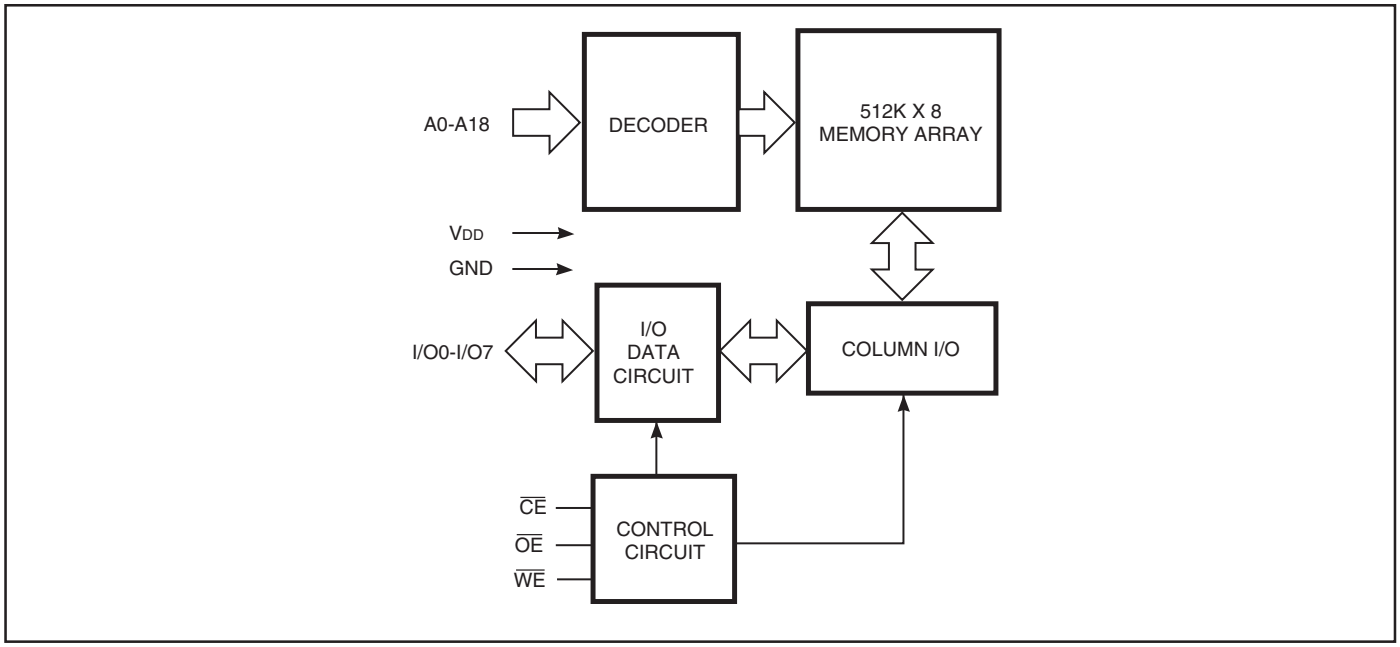
The *ISSI* IS61C5128AL/AS and IS64C5128AL/AS are high-speed, 4,194,304-bit static RAMs organized as 524,288 words by 8 bits. They are fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 12 ns with low power consumption.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, $\overline{CE}$ and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

The IS61C5128AL/AS and IS64C5128AL/AS are packaged in the JEDEC standard 36-pin SOJ (400-mil), 32-pin sTSOP-I, 32-pin SOP, 44-pin TSOP-II and 32-pin TSOP-II packages

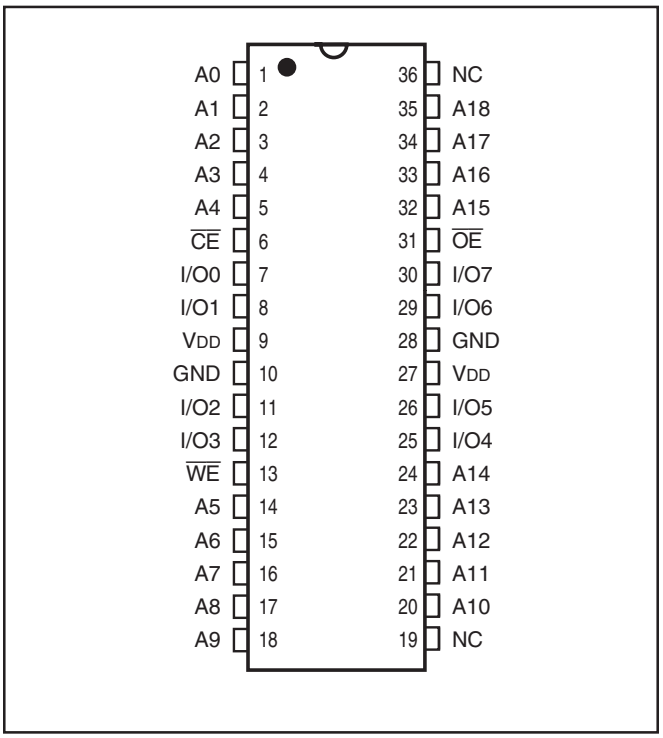
FUNCTIONAL BLOCK DIAGRAM



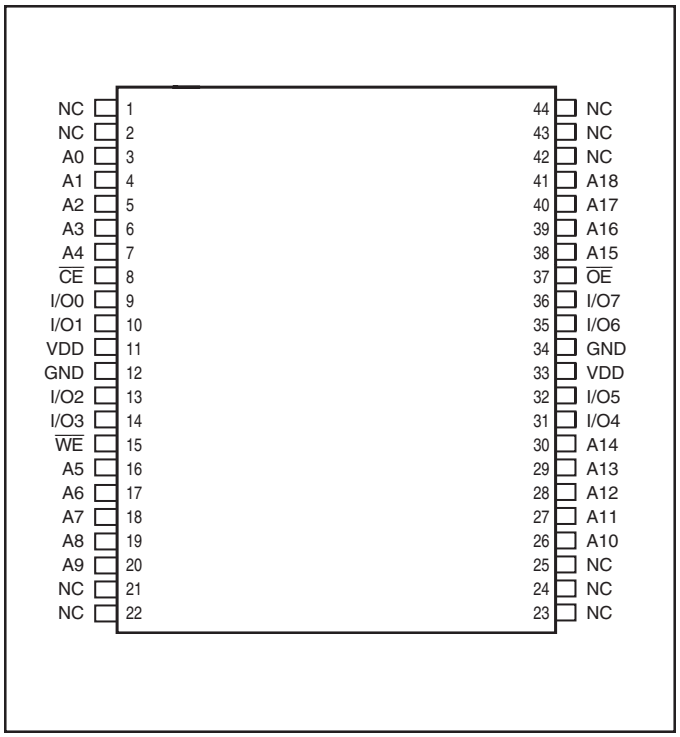
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HIGH SPEED (IS61/64C5128AL) PIN CONFIGURATION

36-Pin SOJ (400-mil)



44-Pin TSOP (Type II)

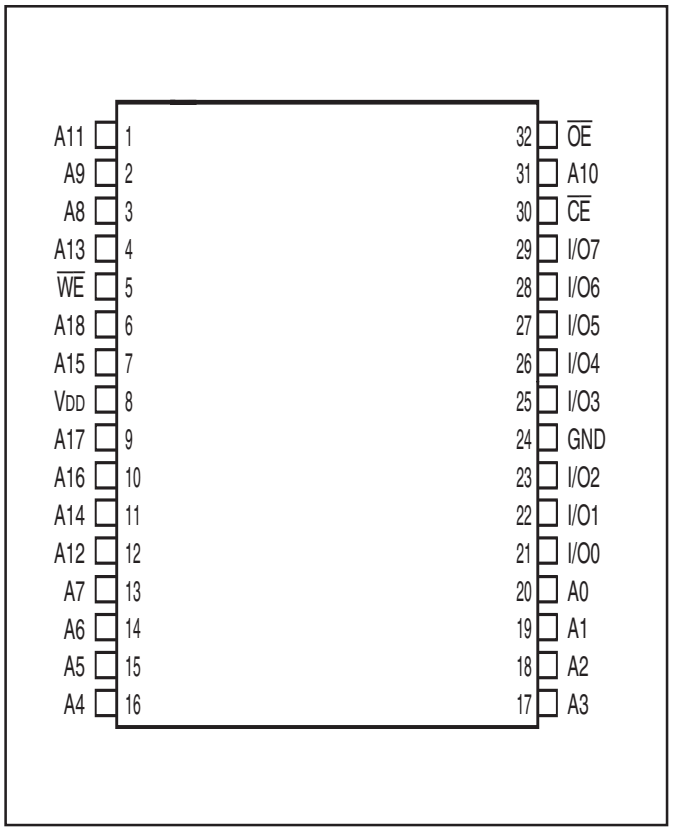


PIN DESCRIPTIONS

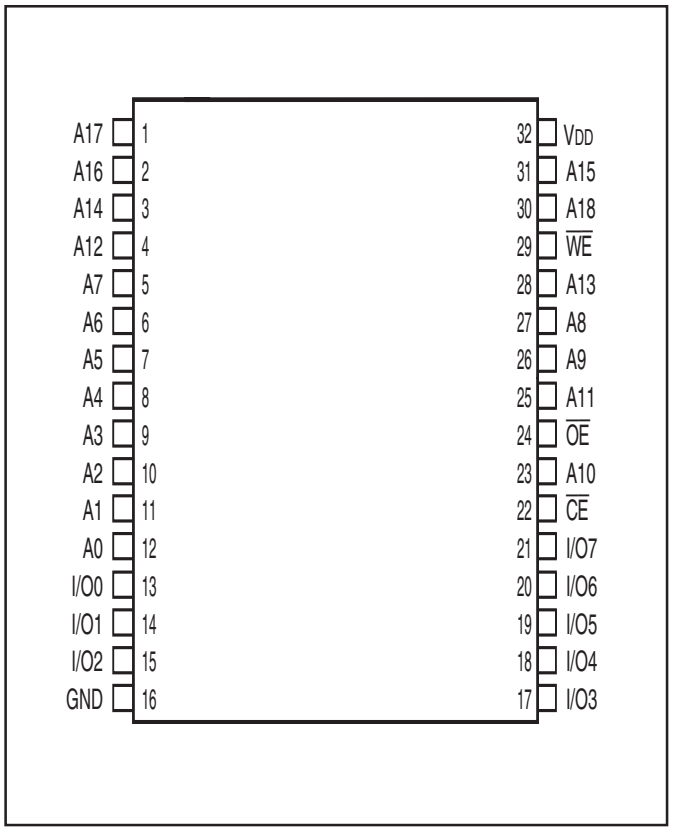
A0-A18	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Bidirectional Ports
V_{DD}	Power
GND	Ground
NC	No Connection

LOW POWER (IS61/64C5128AS) PIN CONFIGURATION

32-pin sTSOP (TYPE I)



32-pin SOP
32-pin TSOP (TYPE II)



PIN DESCRIPTIONS

A0-A18	Address Inputs
$\overline{CE}$	Chip Enable 1 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
VDD	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O0-I/O7	I/O PIN V_{DD} Current
Not Selected	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC1}, I_{CC2}
Read	H	L	L	D_{OUT}	I_{CC1}, I_{CC2}
Write	L	L	X	D_{IN}	I_{CC1}, I_{CC2}

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 5.0V.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –4.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 8.0 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{DD} + 0.5	V
V_{IL}	Input LOW Voltage(1)			–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	Com.	–1	1	µA
			Ind.	–2	2	
			Auto.	–5	5	
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}	Com.	–1	1	µA
		Outputs Disabled	Ind.	–2	2	
			Auto.	–5	5	

Note: 1. V_{IL} = –3.0V for pulse width less than 10 ns.

OPERATING RANGE: HIGH SPEED OPTION (IS61/64C5128AL)

Range	Ambient Temperature	V_{DD}	Speed (ns)
Commercial	0°C to +70°C	5V ± 10%	10
Industrial	-40°C to +85°C	5V ± 10%	10
Automotive	-40°C to +125°C	5V ± 10%	12

OPERATING RANGE: LOW POWER OPTION (IS61/64C5128AS)

Range	Ambient Temperature	V_{DD}	Speed (ns)
Commercial	0°C to +70°C	5V ± 10%	25
Industrial	-40°C to +85°C	5V ± 10%	25
Automotive	-40°C to +125°C	5V ± 10%	25

HIGH SPEED OPTION (IS61/64C5128AL)

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-10 ns Min.	-10 ns Max.	-12 ns Min.	-12 ns Max.	Unit
I_{CC1}	V_{DD} Operating Supply Current	$V_{DD} = V_{DD\ MAX.}$, $\overline{CE} = V_{IL}$ $I_{OUT} = 0$ mA, f = 0	Com. Ind. Auto.	— — —	45 50 55	— — —	45 50 55	mA
I_{CC2}	V_{DD} Dynamic Operating Supply Current	$V_{DD} = V_{DD\ MAX.}$, $\overline{CE} = V_{IL}$ $I_{OUT} = 0$ mA, f = f_{MAX}	Com. Ind. Auto. typ.[2]	— — — 30	50 55 70	— — — 25	45 50 60	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	$V_{DD} = V_{DD\ MAX.}$, $V_{IN} = V_{IH}$ or V_{IL} $\overline{CE} \geq V_{IH}$, f = 0	Com. Ind. Auto.	— — —	15 20 30	— — —	15 20 30	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	$V_{DD} = V_{DD\ MAX.}$, $\overline{CE} \leq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq 0.2V$, f = 0	Com. Ind. Auto. typ.[2]	— — — 2	8 12 20	— — —	8 12 20	mA

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 5V, T_A = 25% and not 100% tested.

LOW POWER OPTION (IS61/64C5128AS)

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-25 ns Min.	-25 ns Max.	Unit
I_{CC}	Average operating Current	$\overline{CE} = V_{IL}$, V_{DD} = Max. I_{OUT} = 0 mA, f = 0	Com. Ind. Auto.	— — —	10 15 20	mA
I_{CC1}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., $\overline{CE} = V_{IL}$ I_{OUT} = 0 mA, f = f_{MAX}	Com. Ind. Auto. typ.[2]	— — — 15	25 30 40	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE} \geq V_{IH}$, f = 0	Com. Ind. Auto.	— — —	1 1.5 2	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CE} \geq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq V_{SS} + 0.2V$, f = 0	Com. Ind. Auto. typ.	— — — 0.2	0.8 0.9 2	mA

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 5V, T_A = 25% and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-10 Min.	-10 Max.	-12 Min.	-12 Max.	-25 Min.	-25 Max.	Unit
t_{RC}	Read Cycle Time	10	—	12	—	25	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	25	ns
t_{OHA}	Output Hold Time	3	—	3	—	3	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	10	—	12	—	25	ns
t_{DOE}	$\overline{OE}$ Access Time	—	5	—	6	—	15	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	5	0	6	0	8	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	2	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	0	5	0	6	0	8	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	2	—	2	—	2	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

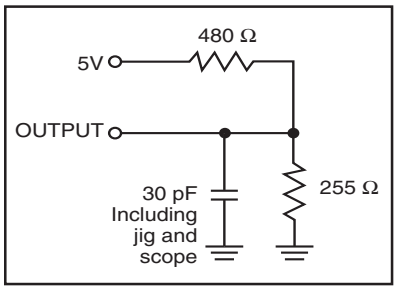


Figure 1

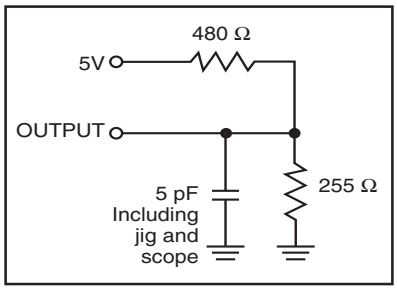
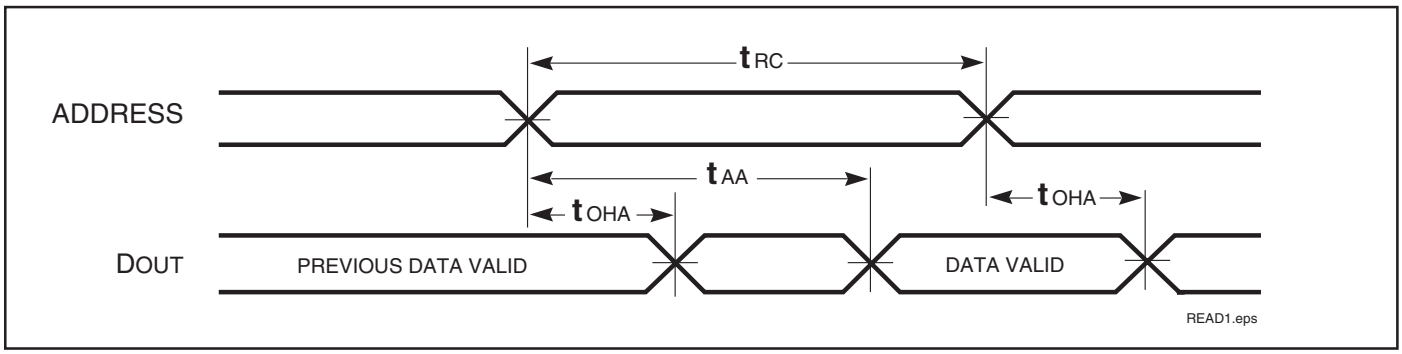


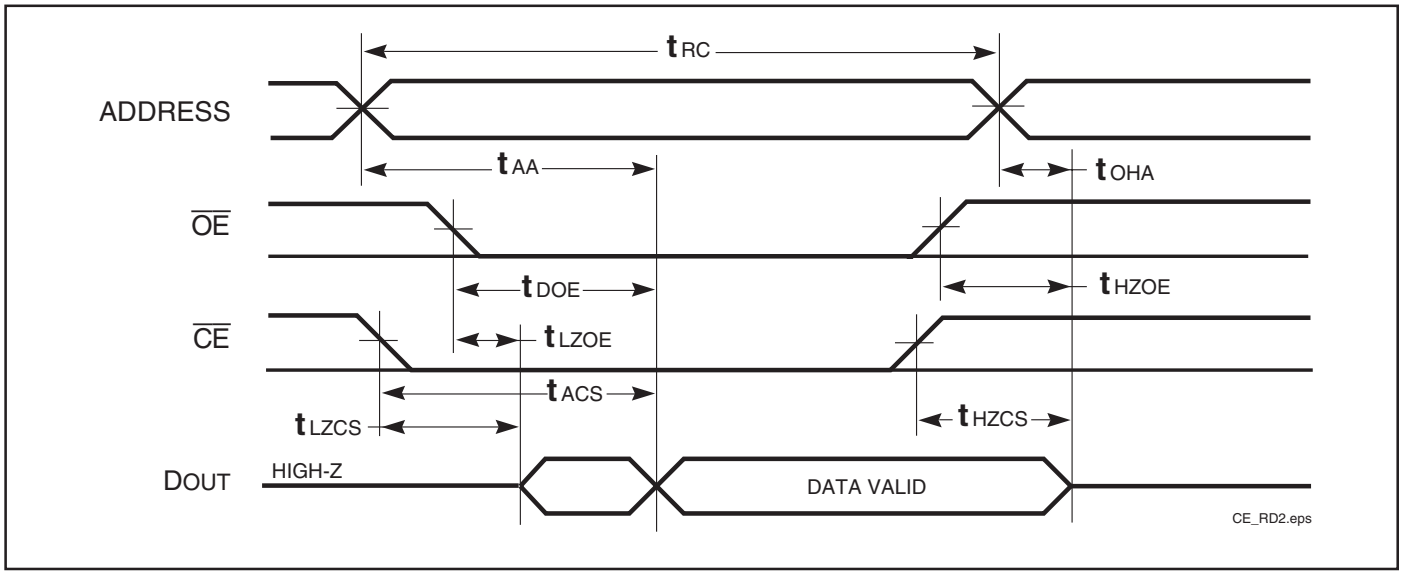
Figure 2

AC WAVEFORMS

READ CYCLE NO. 1[1,2]



READ CYCLE NO. 2[1,3]



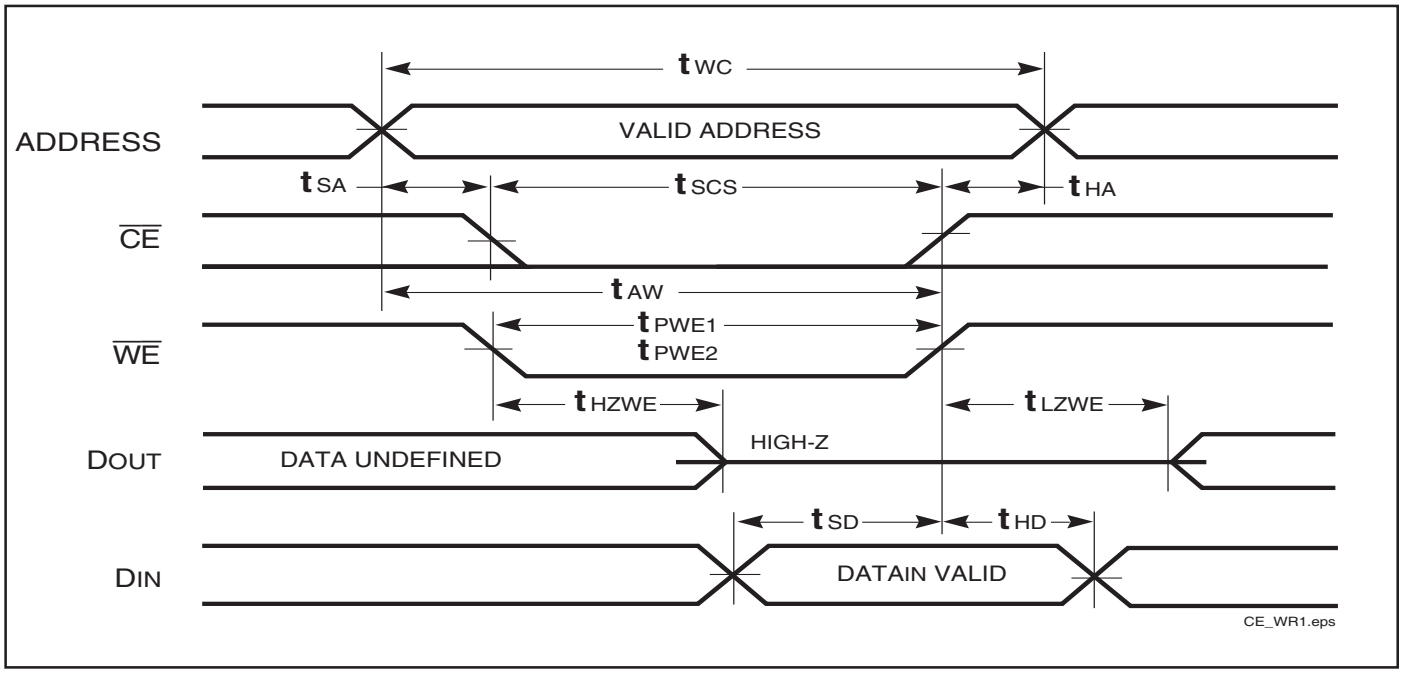
Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

Symbol	Parameter	-10 Min.	-10 Max.	-12 Min.	-12 Max.	-25 Min.	-25 Max.	Unit
t_{WC}	Write Cycle Time	10	—	12	—	25	—	ns
t_{SCE}	$\overline{CE}$ to Write End	7	—	9	—	18	—	ns
t_{AW}	Address Setup Time to Write End	7	—	9	—	18	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ =High)	7	—	9	—	15	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$=Low)	7	—	9	—	15	—	ns
t_{SD}	Data Setup to Write End	6	—	6	—	15	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	6	—	6	—	15	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	3	—	3	—	5	—	ns

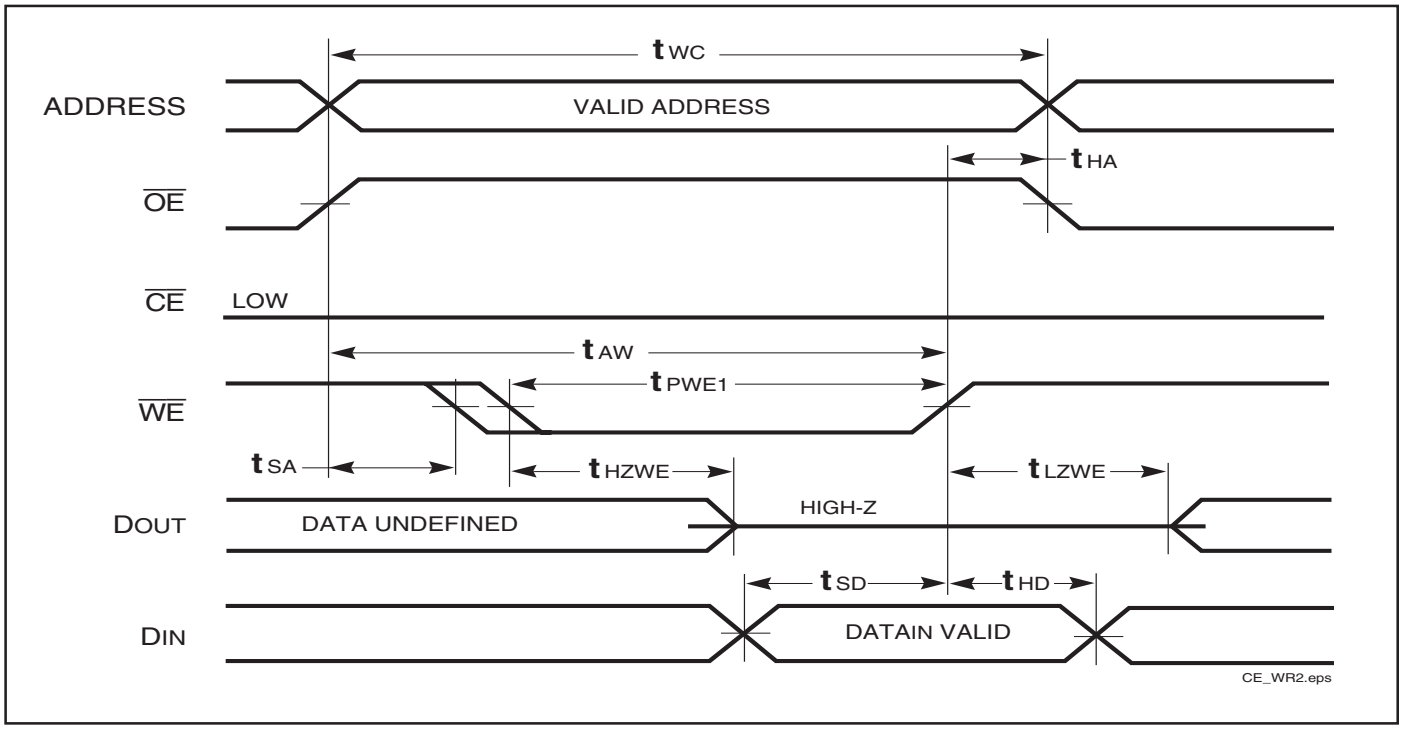
Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS
WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)[1,2]

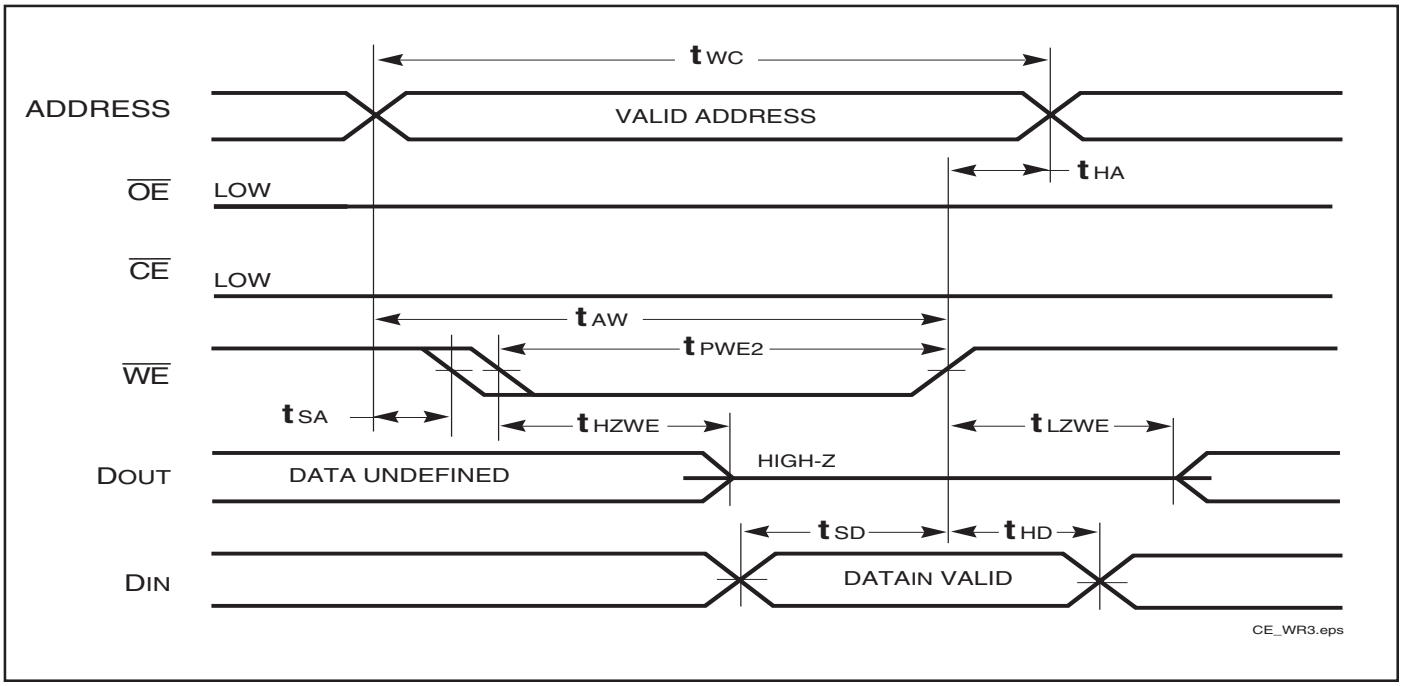


Notes:
1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

WRITE CYCLE NO. 2 ($\overline{OE}$ is HIGH During Write Cycle) [1,2]



WRITE CYCLE NO. 3 ($\overline{OE}$ is LOW During Write Cycle) [1]



Notes:

1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

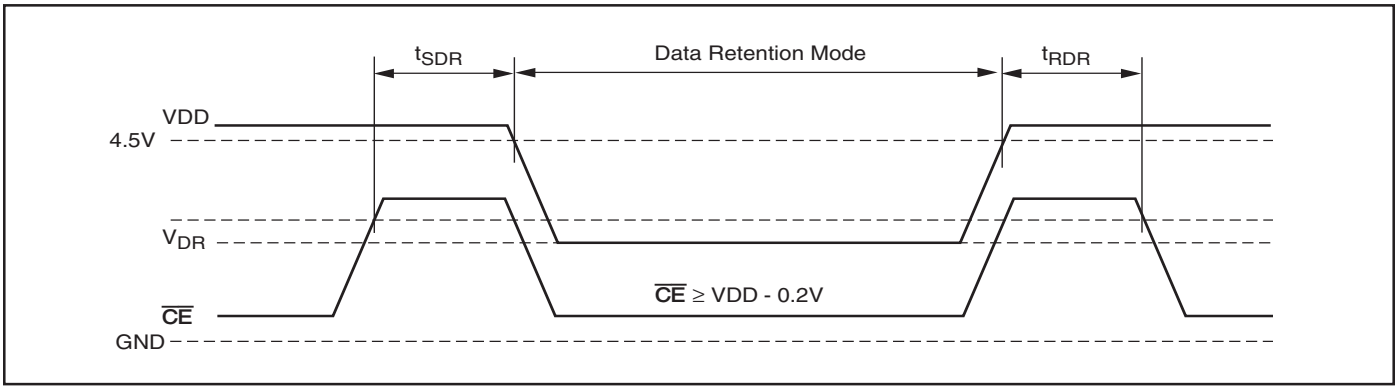
DATA RETENTION SWITCHING CHARACTERISTICS (HIGH SPEED) (IS61/64C5128AL)

Symbol	Parameter	Test Condition		Min.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		2.9	5.5	V
I_{DR}	Data Retention Current	V_{DD} = 2.9V, $\overline{CE} \geq V_{DD} - 0.2V$	Com.	—	8	mA
		$V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq V_{SS} + 0.2V$	Ind.	—	10	
			Auto.	—	15	
			typ. (1)	1		
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}	—	ns

Note:

1. Typical Values are measured at V_{DD} = 5V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



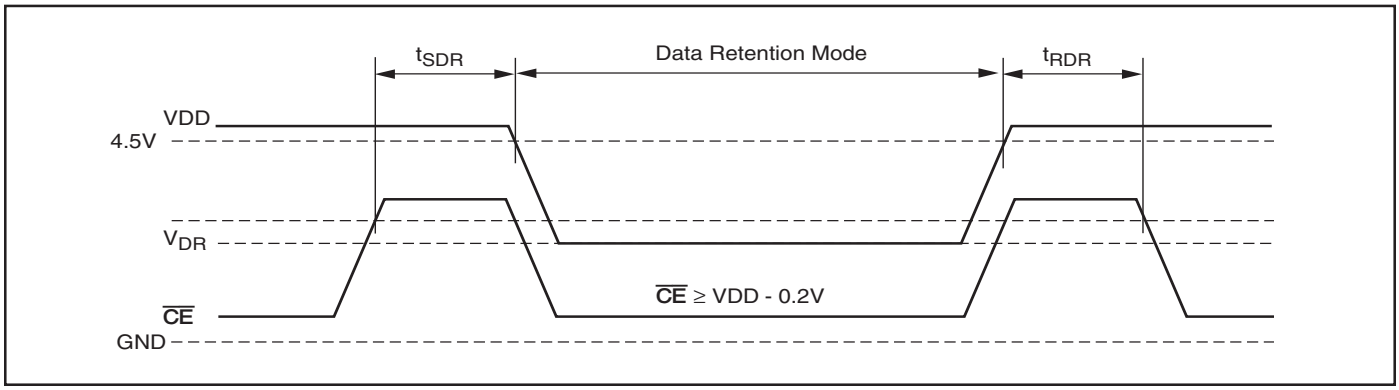
DATA RETENTION SWITCHING CHARACTERISTICS (LOW POWER) (IS61/64C5128AS)

Symbol	Parameter	Test Condition		Min.		Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		2.9		5.5	V
I_{DR}	Data Retention Current	V_{DD} = 2.9V, $\overline{CE} \geq V_{DD} - 0.2V$	Com.	—		0.8	mA
		$V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq V_{SS} + 0.2V$	Ind.	—		0.9	
			Auto.	—		2	
			typ. (1)		0.2		
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0		—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}		—	ns

Note:

1. Typical Values are measured at V_{DD} = 5V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



HIGH SPEED (IS61/64C5128AL)

ORDERING INFORMATION

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
10	IS61C5128AL-10KI	400-mil Plastic SOJ
	IS61C5128AL-10KLI	400-mil Plastic SOJ, Lead-free
	IS61C5128AL-10TI	44-pin TSOP-II
	IS61C5128AL-10TLI	44-pin TSOP-II, Lead-free

Automotive Range: –40°C to +125°C

Speed (ns)	Order Part No.	Package
12	IS64C5128AL-12KA3	400-mil Plastic SOJ
	IS64C5128AL-12TA3	44-pin TSOP-II
	IS64C5128AL-12TLA3	44-pin TSOP-II, Lead-free

LOW POWER (IS61/64C5128AS)

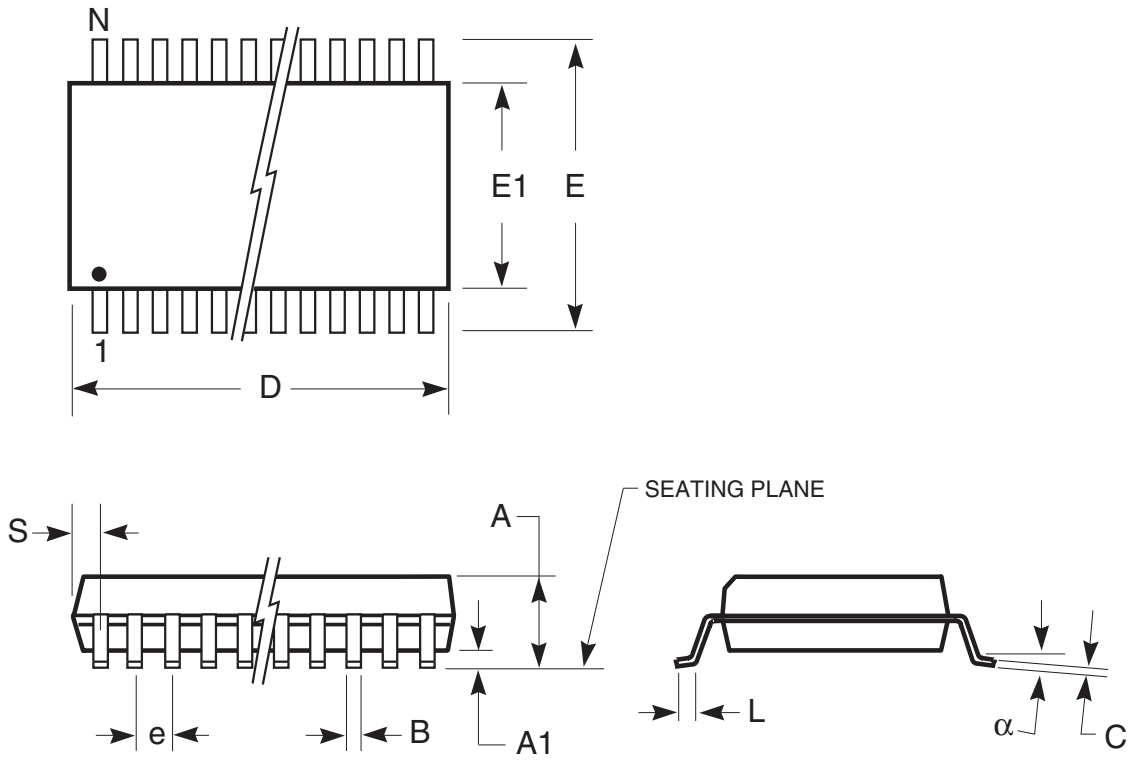
ORDERING INFORMATION

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
25	IS61C5128AS-25QI	450-mil Plastic SOP
	IS61C5128AS-25QLI	450-mil Plastic SOP, Lead-free
	IS61C5128AS-25HI	32-pin STSOP-I
	IS61C5128AS-25HLI	32-pin STSOP-I, Lead-free
	IS61C5128AS-25TI	32-pin TSOP-II
	IS61C5128AS-25TLI	32-pin TSOP-II, Lead-free

PACKAGING INFORMATION

450-mil Plastic SOP
Package Code: Q (32-pin)



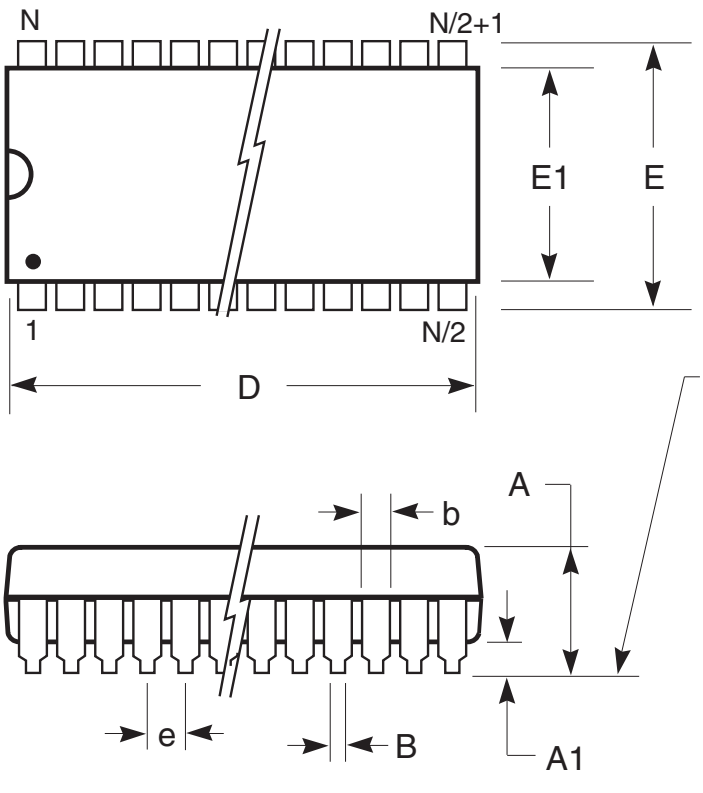
	MILLIMETERS		INCHES	
Symbol	**Min.**	**Max.**	**Min.**	**Max.**
No. Leads		**32**		
A	—	3.00	—	0.118
A1	0.10	—	0.004	—
B	0.36	0.51	0.014	0.020
C	0.15	0.30	0.006	0.012
D	20.14	20.75	0.793	0.817
E	13.87	14.38	0.546	0.566
E1	11.18	11.43	0.440	0.450
e	1.27 BSC		0.050 BSC	
L	0.58	0.99	0.023	0.039
α	0°	10°	0°	10°
S	—	0.86	—	0.034

Notes:
1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

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PACKAGING INFORMATION

400-mil Plastic SOJ
Package Code: K



Notes:
1. Controlling dimension: millimeters.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Reference document: JEDEC MS-027.

	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
No. Leads (N)		28				32				36		
A	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148
A1	0.64	—	0.025	—	0.64	—	0.025	—	0.64	—	0.025	—
A2	2.08	—	0.082	—	2.08	—	0.082	—	2.08	—	0.082	—
B	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020
b	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032
C	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013
D	18.29	18.54	0.720	0.730	20.82	21.08	0.820	0.830	23.37	23.62	0.920	0.930
E	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445
E1	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E2	9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC	
e	1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC	

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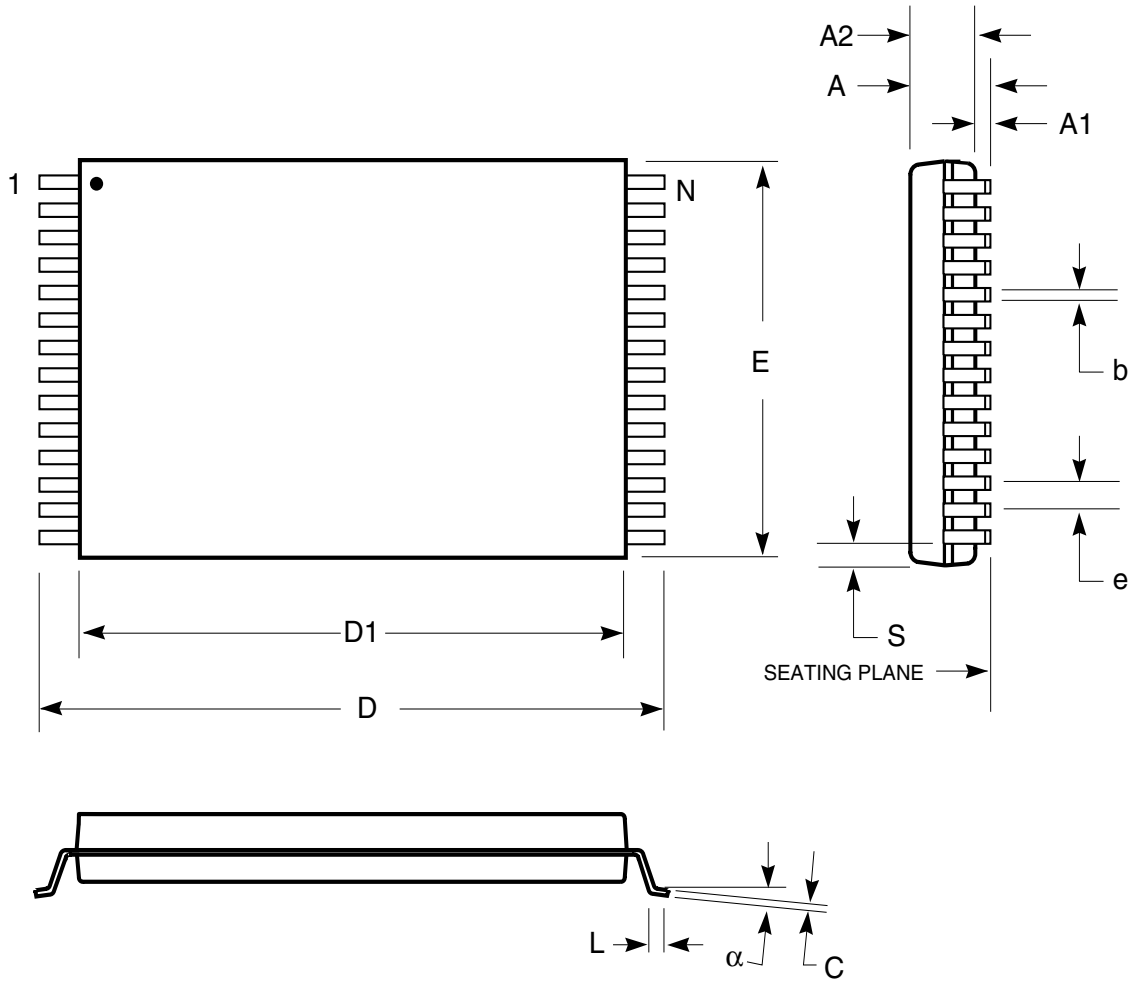
PACKAGING INFORMATION

	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
No. Leads (N)		40				42				44		
A	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148
A1	0.64	—	0.025	—	0.64	—	0.025	—	0.64	—	0.025	—
A2	2.08	—	0.082	—	2.08	—	0.082	—	2.08	—	0.082	—
B	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020
b	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032
C	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013
D	25.91	26.16	1.020	1.030	27.18	27.43	1.070	1.080	28.45	28.70	1.120	1.130
E	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445
E1	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E2	9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC	
e	1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC	

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PACKAGING INFORMATION

Plastic STSOP - 32 pins
Package Code: H (Type I)

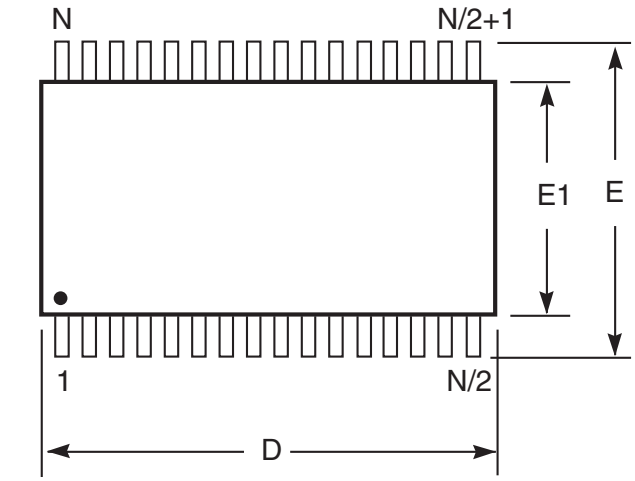


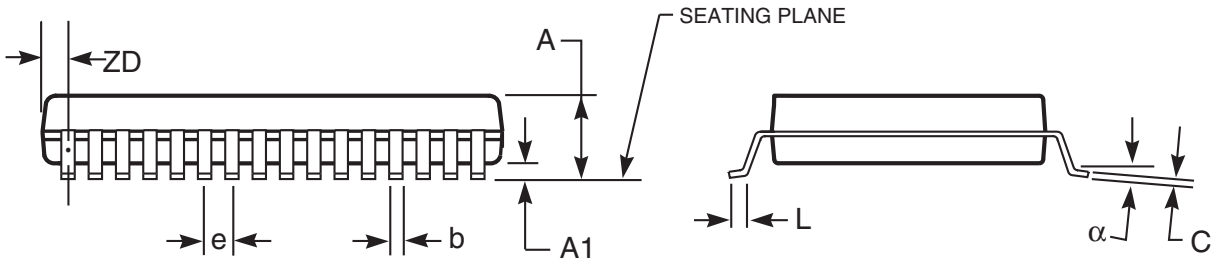
Plastic STSOP (H - Type I)				
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
Ref. Std.				
N		32		
A	—	1.25	—	0.049
A1	0.05	—	0.002	—
A2	0.95	1.05	0.037	0.041
b	0.17	0.23	0.007	0.009
C	0.14	0.16	0.0055	0.0063
D	13.20	13.60	0.520	0.535
D1	11.70	11.90	0.461	0.469
E	7.90	8.10	0.311	0.319
e	0.50 BSC		0.020 BSC	
L	0.30	0.70	0.012	0.028
S	0.28 Typ.		0.011 Typ.	
α	0°	5°	0°	5°

Notes:
1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D1 and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

PACKAGING INFORMATION

Plastic TSOP
Package Code: T (Type II)





Notes:
1. Controlling dimension: millimieters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

Plastic TSOP (T - Type II)

	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Ref. Std.												
No. Leads (N)		**32**				**44**				**50**		
A	—	1.20	—	0.047	—	1.20	—	0.047	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006
b	0.30	0.52	0.012	0.020	0.30	0.45	0.012	0.018	0.30	0.45	0.012	0.018
C	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008
D	20.82	21.08	0.820	0.830	18.31	18.52	0.721	0.729	20.82	21.08	0.820	0.830
E1	10.03	10.29	0.391	0.400	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E	11.56	11.96	0.451	0.466	11.56	11.96	0.455	0.471	11.56	11.96	0.455	0.471
e	1.27 BSC		0.050 BSC		0.80 BSC		0.032 BSC		0.80 BSC		0.031 BSC	
L	0.40	0.60	0.016	0.024	0.41	0.60	0.016	0.024	0.40	0.60	0.016	0.024
ZD	0.95 REF		0.037 REF		0.81 REF		0.032 REF		0.88 REF		0.035 REF	
α	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°

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