AUGUST 2019

1Mx16 HIGH-SPEED ASYNCHRONOUS CMOS STATIC RAM WITH 3.3V/1.8V SUPPLY

FEATURES

- High-speed access time: 8ns, 10ns, 20ns
- High- performance, low power CMOS process
- Multiple center power and ground pins for greater noise immunity
- TTL compatible inputs and outputs
- Single power supply
  - 1.65V-2.2V VDD (IS61WV102416FALL)
  - 2.4V-3.6V VDD (IS61/64WV102416FBLL)
- Packages available :
  - 48 ball mini BGA (6mm x 8mm)
  - 48 pin TSOP (Type I)
  - 54 pin TSOP (Type II)
- Industrial and Automotive temperature support
- Lead-free available
- Data Control for upper and lower bytes

DESCRIPTION

The *ISSI* IS61/64WV102416FALL/BLL are high-speed, 16M bit static RAMs organized as 1024K words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology.

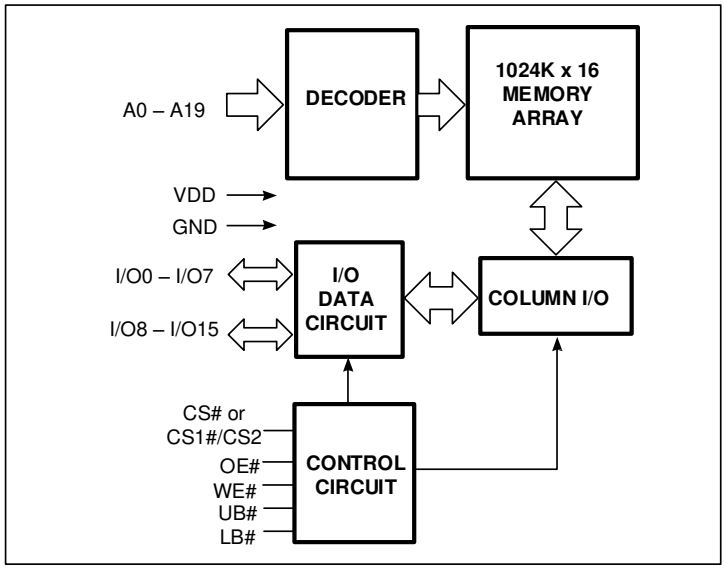
This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When CS# is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels. Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable (WE#) controls both writing and reading of the memory.

A data byte allows Upper Byte (UB#) and Lower Byte (LB#) access.

The devices are packaged in the JEDEC standard 48-Pin TSOP (TYPE I), 48-pin mini BGA (6mm x 8mm), and 54-Pin TSOP (TYPE II) .

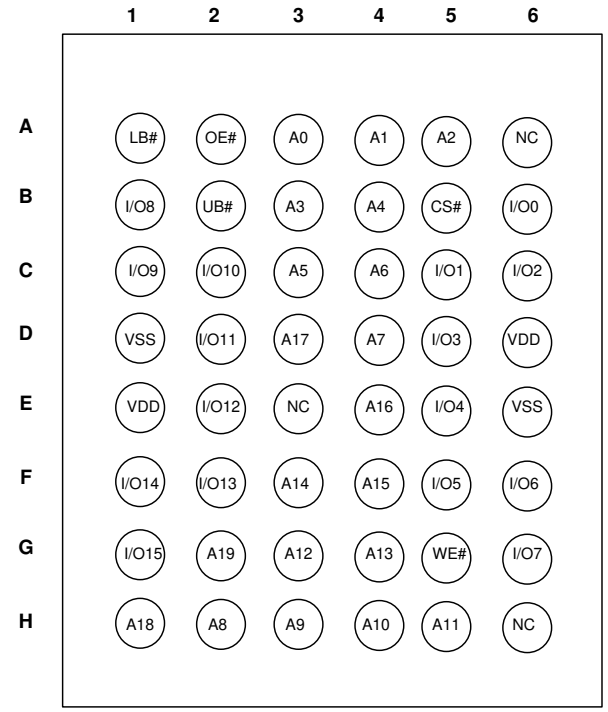
FUNCTIONAL BLOCK DIAGRAM

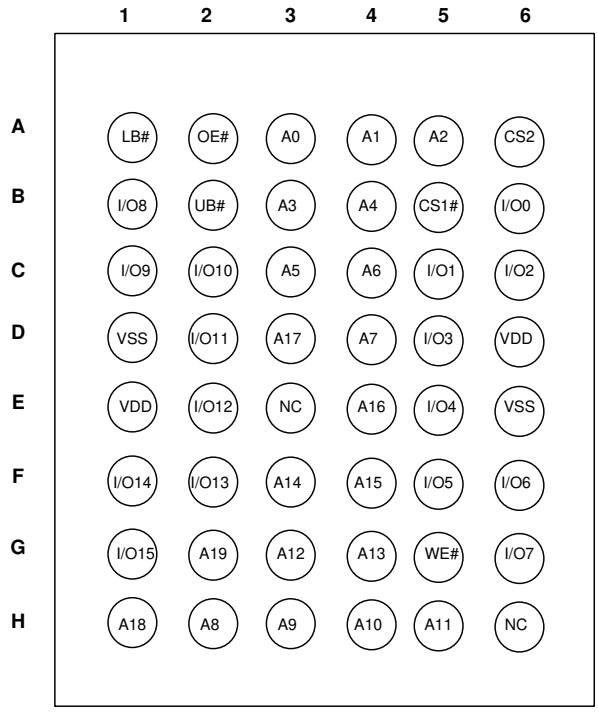


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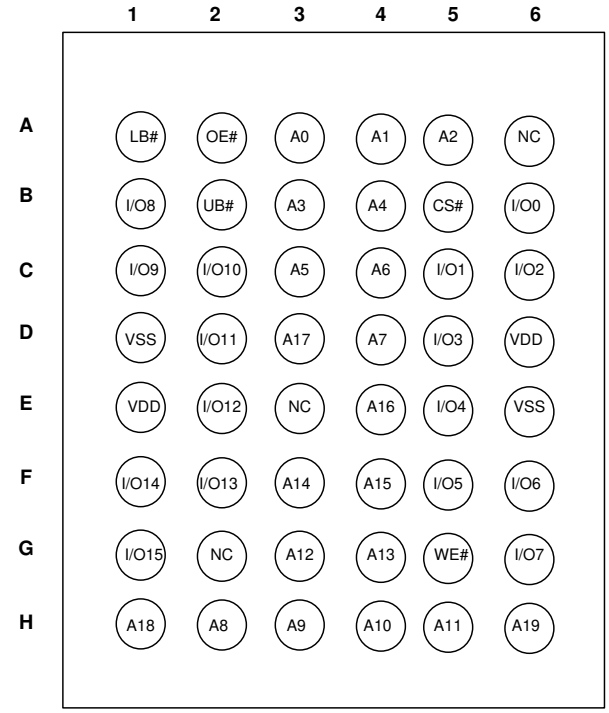
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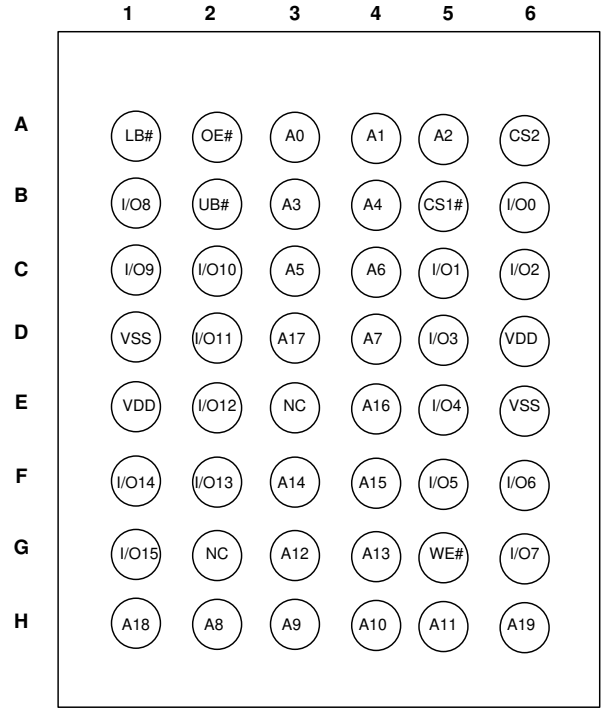
48-Pin mini BGA, 1 Chip Select, A19 on G2 (B), 48-Pin mini BGA, 2 Chip Select, A19 on G2 (B2)



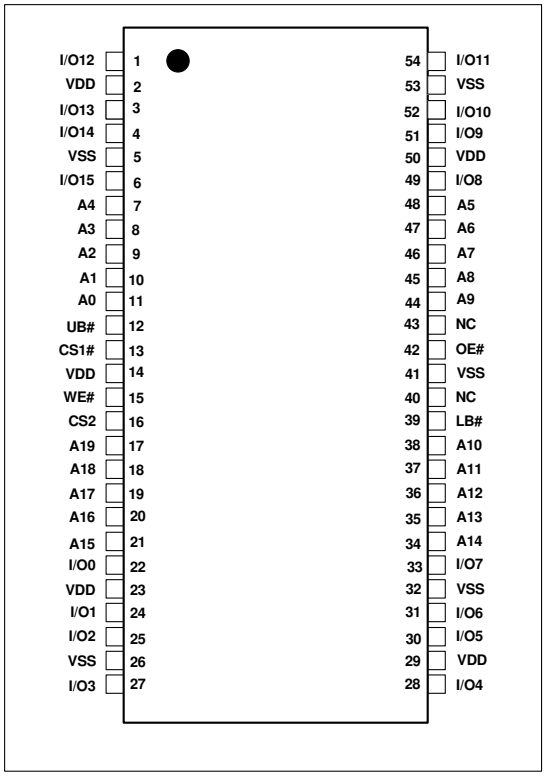


48-Pin mini BGA, 1 Chip Select, A19 on H6 (B3), 48-Pin mini BGA, 2 Chip Select,A19 on H6 (B4)

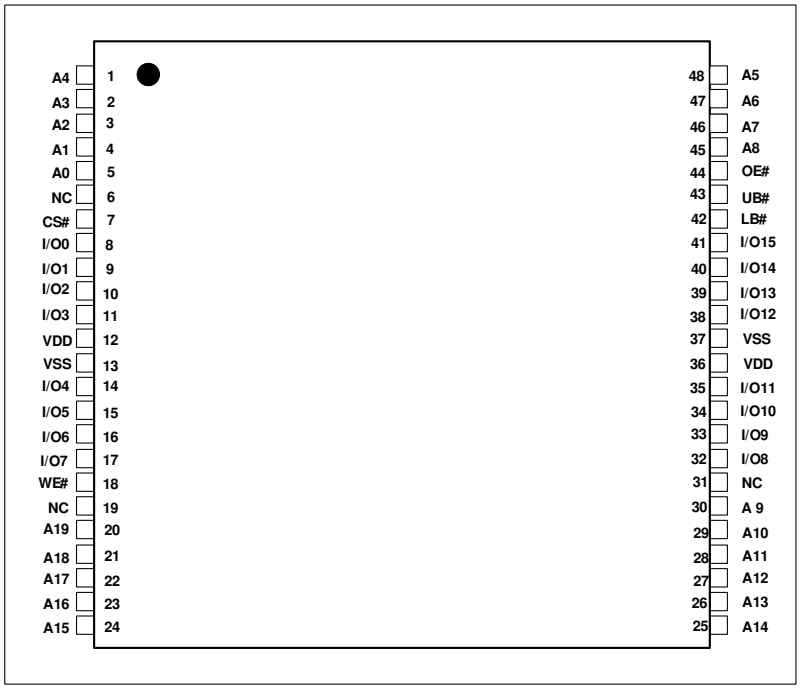




54-Pin TSOP (II)



48-Pin TSOP (I)



Pin Descriptions

A0-A19	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
CS# or CS1#/CS2	Chip Enable Input(s)
OE#	Output Enable Input
WE#	Write Enable Input
LB#	Lower-byte Control (I/O0-I/O7)
UB#	Upper-byte Control (I/O8-I/O15)
NC	No Connection
VDD	Power
VSS	Ground

FUNCTION DESCRIPTION

SRAM is one of random access memories. Each byte or word has an address and can be accessed randomly. SRAM has three different modes supported. Each function is described below with Truth Table.

STANDBY MODE

Device enters standby mode when deselected (CS# HIGH). The input and output pins (I/O0-15) are placed in a high impedance state. CMOS input in this mode will maximize saving power.

WRITE MODE

Write operation issues with Chip selected (CS#) and Write Enable (WE#) input LOW. The input and output pins (I/O0-15) are in data input mode. Output buffers are closed during this time even if OE# is LOW. UB# and LB# enables a byte write feature. By enabling LB# LOW, data from I/O pins (I/O0 through I/O7) are written into the location specified on the address pins. And with UB# being LOW, data from I/O pins (I/O8 through I/O15) are written into the location.

READ MODE

Read operation issues with Chip selected (CS# LOW) and Write Enable (WE#) input HIGH. When OE# is LOW, output buffer turns on to make data output. Any input to I/O pins during READ mode is not permitted. UB# and LB# enables a byte read feature. By enabling LB# LOW, data from memory appears on I/O0-7. And with UB# being LOW, data from memory appears on I/O8-15.

In the READ mode, output buffers can be turned off by pulling OE# HIGH. In this mode, internal device operates as READ but I/Os are in a high impedance state. Since device is in READ mode, active current is used.

TRUTH TABLE

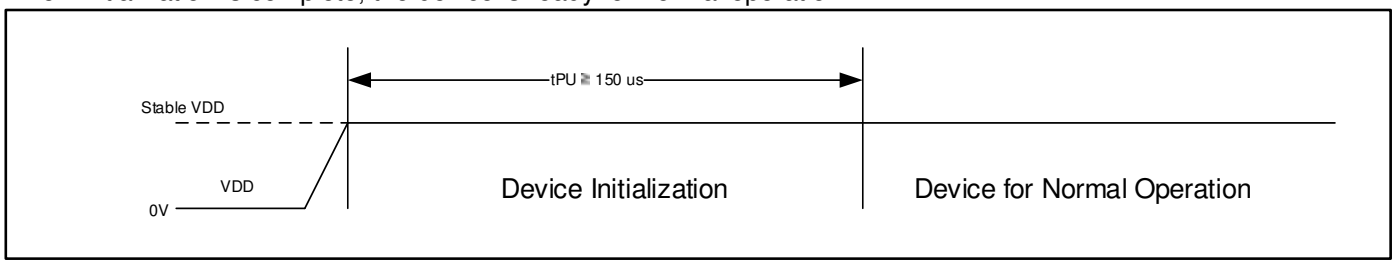
Mode	CS#	WE#	OE#	LB#	UB#	I/O0-I/O7	I/O8-I/O15	VDD Current
Not Selected	H	X	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	L	H	H	L	X	High-Z	High-Z	ICC,ICC1
	L	X	X	H	H	High-Z	High-Z	
Read	L	H	L	L	H	DOUT	High-Z	ICC,ICC1
	L	H	L	H	L	High-Z	DOUT	
	L	H	L	L	L	DOUT	DOUT	
Write	L	L	X	L	H	DIN	High-Z	ICC,ICC1
	L	L	X	H	L	High-Z	DIN	
	L	L	X	L	L	DIN	DIN	

Note:

1. **CS# = H means CS1#=HIGH, and CS2= LOW in Dual Chip Select Device.**

POWER UP INITIALIZATION

The device includes on-chip voltage sensor used to launch POWER-UP initialization process.
When VDD reaches stable level, the device requires 150us of tPU (Power-Up Time) to complete its self-initialization process.
When initialization is complete, the device is ready for normal operation.



ABSOLUTE MAXIMUM RATINGS AND Operating Range

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Value	Unit
Vterm	Terminal Voltage with Respect to VSS	–0.5 to V_{DD} + 0.5V	V
V_{DD}	V_{DD} Related to VSS	–0.3 to 4.0	V
tStg	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN CAPACITANCE (1)

Parameter	Symbol	Test Condition	Max	Units
Input capacitance	C_{IN}	T_A = 25°C, f = 1 MHz, V_{DD} = V_{DD}(typ)	6	pF
DQ capacitance (IO0–IO15)	$C_{I/O}$		8	pF

Note:
1. These parameters are guaranteed by design and tested by a sample basis only.

OPERATING RANGE

Range	Ambient Temperature	IS61WV102416FALL VDD (20ns)	IS61WV102416FBLL VDD (8, 10ns)	IS64WV102416FBLL VDD (10ns)
Industrial	-40°C to +85°C	1.65V – 2.2V	2.4V – 3.6V	–
Automotive (A3)	-40°C to +125°C	–	–	2.4V – 3.6V

AC TEST CONDITIONS (OVER THE OPERATING RANGE)

Parameter	Unit (1.65V~2.2V)	Unit (2.4V~3.6V)
Input Pulse Level	0V to V_{DD}	0V to V_{DD}
Input Rise and Fall Time	1.5 ns	1.5 ns
Output Timing Reference Level	½ V_{DD}	½ V_{DD}
R1 (ohm)	13500	319
R2 (ohm)	10800	353
V_{TM} (V)	1.8V	3.3V
Output Load Conditions	Refer to Figure 1 and 2	

AC TEST LOADS

FIGURE 1

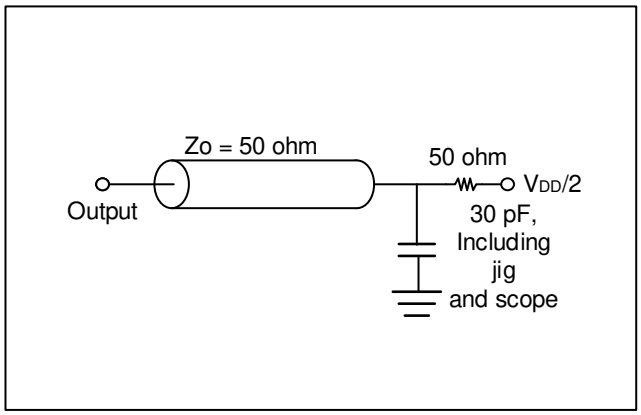
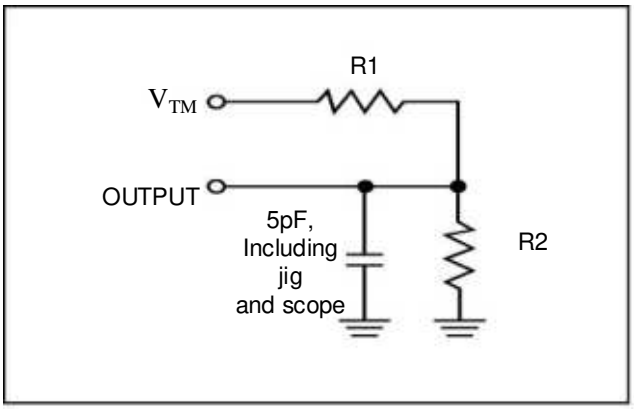


FIGURE 2



DC ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE)

VDD = 1.65V – 2.2V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	—	0.2	V
V_{IH}(1)	Input HIGH Voltage		1.4	V_{DD} + 0.2	V
V_{IL}(1)	Input LOW Voltage		–0.2	0.4	V
I_{LI}	Input Leakage	GND < V_{IN} < V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND < V_{IN} < V_{DD}, Output Disabled	–1	1	µA

Notes:
1. VILL(min) = -1.0V AC (pulse width < 10ns). Not 100% tested.
   VIHH (max) = VDD + 1.0V AC (pulse width < 10ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE)

VDD = 2.4V – 3.6V

Symbol	Parameter		Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	2.4V ~ 2.7V	V_{DD} = Min., I_{OH} = -1.0 mA	2.0	—	V
		2.7V ~ 3.6V	V_{DD} = Min., I_{OH} = -4.0 mA	2.2		
V_{OL}	Output LOW Voltage	2.4V ~ 2.7V	V_{DD} = Min., I_{OL} = 2.0 mA	—	0.4	V
		2.7V ~ 3.6V	V_{DD} = Min., I_{OL} = 8.0 mA	—	0.4	
V_{IH}(1)	Input HIGH Voltage	2.4V ~ 2.7V		2.0	V_{DD} + 0.3	V
		2.7V ~ 3.6V		2.0		
V_{IL}(1)	Input LOW Voltage	2.4V ~ 2.7V		–0.3	0.6	V
		2.7V ~ 3.6V		–0.3	0.8	
I_{LI}	Input Leakage		VSS < V_{IN} < V_{DD}	–2	2	µA
I_{LO}	Output Leakage		VSS < V_{IN} < V_{DD}, Output Disabled	–2	2	µA

Notes:
1. VIL(min) = -0.3V DC ; VIL(min) = -2.0V AC (pulse width 2.0ns). Not 100% tested.
   VIH (max) = VDD + 0.3V DC ; VIH(max) = VDD + 2.0V AC (pulse width 2.0ns). Not 100% tested.

POWER SUPPLY CHARACTERISTICS-II FOR POWER [1] (OVER THE OPERATING RANGE)

Symbol	Parameter	Test Conditions	Grade	-8 Max.	-10 Max.	-20 Max	Unit
ICC	V_{DD} Dynamic Operating Supply Current	V_{DD} = MAX, I_{OUT} = 0 mA, f = f_{MAX}	Com.	90	85	80	mA
			Ind.	100	95	90	
			Auto.	-	135	-	
ICC1	Operating Supply Current	V_{DD} = MAX, I_{OUT} = 0 mA, f = 0	Com.	80	80	80	mA
			Ind.	90	90	90	
			Auto.	-	110	-	
ISB1	TTL Standby Current (TTL Inputs)	V_{DD} = MAX, V_{IN} = V_{IH} or V_{IL} CS# ≥ V_{IH}, f = 0	Com.	40	40	40	mA
			Ind.	50	50	50	
			Auto.	-	60	-	
ISB2	CMOS Standby Current (CMOS Inputs)	V_{DD} = MAX, CS# ≥ V_{DD} - 0.2V V_{IN} ≥ V_{DD} - 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com.	30	30	30	mA
			Ind.	40	40	40	
			Auto.	-	50	-	
			Typ. [2]	10			

Notes:
1. At f = fMAX, address and data inputs are cycling at the maximum frequency, f = 0 means no input line change.
2. Typical values are measured at V_{DD} = 3.0V/1.8V, T_A = 25 °C and not 100% tested.
3. CS#=H means CS1#=HIGH, and CS2=LOW in Dual Chip Select Device

AC CHARACTERISTICS (OVER OPERATING RANGE)

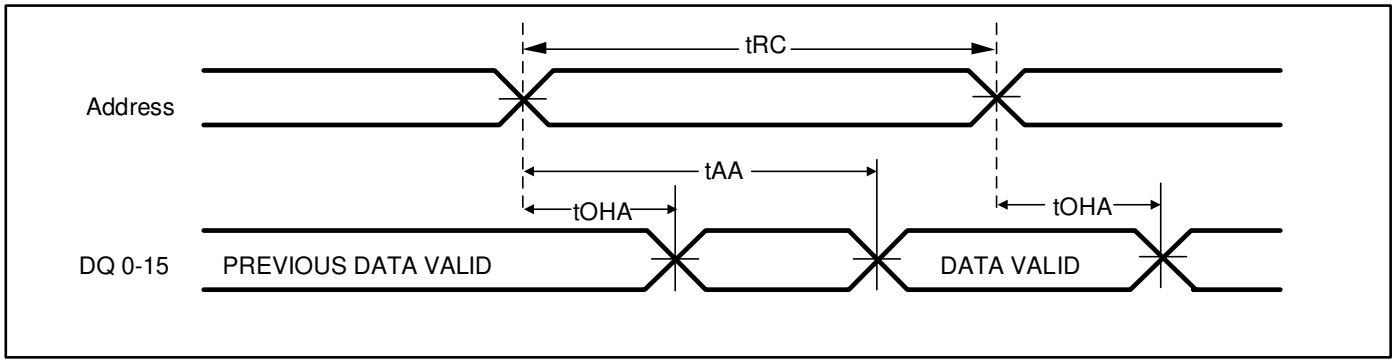
READ CYCLE AC CHARACTERISTICS

Parameter	Symbol	-8[1]		-10[1]		-20[1]		unit	notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	tRC	8	-	10	-	20	-	ns	
Address Access Time	tAA	-	8	-	10	-	20	ns	
Output Hold Time	tOHA	2.5	-	2.5	-	2.5	-	ns	
CS# Access Time	tACE	-	8	-	10	-	20	ns	
OE# Access Time	tDOE	-	5.5	-	6	-	8	ns	
OE# to High-Z Output	tHZOE	0	4	0	5	0	8	ns	2
OE# to Low-Z Output	tLZOE	0	-	0	-	0	-	ns	2
CS# to High-Z Output	tHZCE	0	4	0	5	0	8	ns	2
CS# to Low-Z Output	tLZCE	3	-	3	-	3	-	ns	2
UB#, LB# Access Time	tBA	-	5.5	-	6	-	8	ns	
UB#, LB# to High-Z Output	tHZB	0	4	0	5	0	8	ns	2
UB#, LB# to Low-Z Output	tLZB	0	-	0	-	0	-	ns	2

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of VDD/2, and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. CS#=H means CS1#=HIGH, and CS2=LOW in Dual Chip Select Device

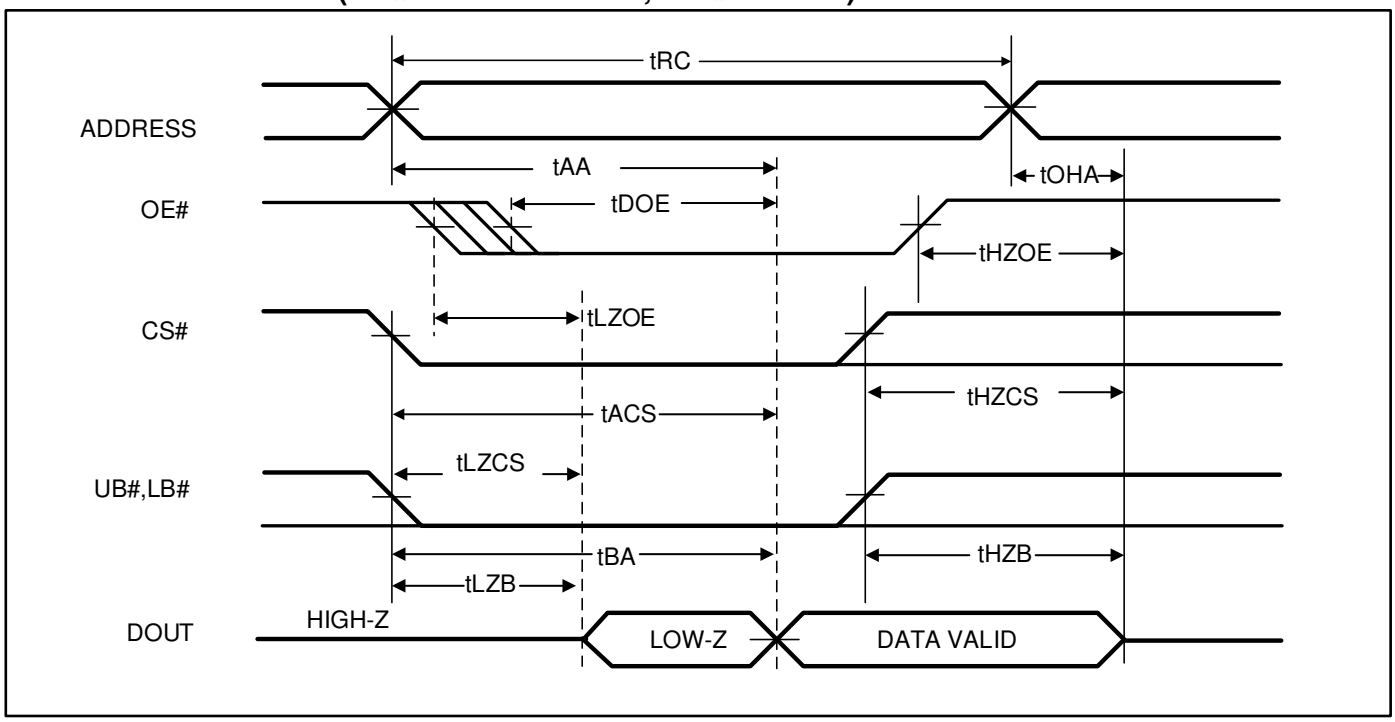
AC WAVEFORMS

READ CYCLE NO. 1[1] (Address Controlled, CS# = OE# = UB# = LB# = LOW, WE# = HIGH)



Notes:
1. The device is continuously selected.

READ CYCLE NO. 2[1] (OE# CONTROLLED, WE# = HIGH)



Notes:
1. Address is valid prior to or coincident with CS# LOW transition.

WRITE CYCLE AC CHARACTERISTICS

Parameter	Symbol	-8[1]		-10[1]		-20[1]		unit	notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	tWC	8	-	10	-	20	-	ns	
CS# to Write End	tSCS	6.5	-	8	-	12	-	ns	
Address Setup Time to Write End	tAW	6.5	-	8	-	12	-	ns	
UB#,LB# to Write End	tPWB	6.5	-	8	-	12	-	ns	
Address Hold from Write End	tHA	0	-	0	-	0	-	ns	
Address Setup Time	tSA	0	-	0	-	0	-	ns	
WE# Pulse Width	tPWE1	6.5	-	8	-	12	-	ns	
WE# Pulse Width (OE# = LOW)	tPWE2	8	-	10	-	17	-	ns	2
Data Setup to Write End	tSD	5	-	6	-	9	-	ns	
Data Hold from Write End	tHD	0	-	0	-	0	-	ns	
WE# LOW to High-Z Output	tHZWE	-	3.5	-	4	-	9	ns	
WE# HIGH to Low-Z Output	tLZWE	2	-	2	-	3	-	ns	

Notes:

1 Test conditions assume signal transition times of 3 ns or less, timing reference levels of VDD/2, and output loading specified in Figure 1.

2 Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

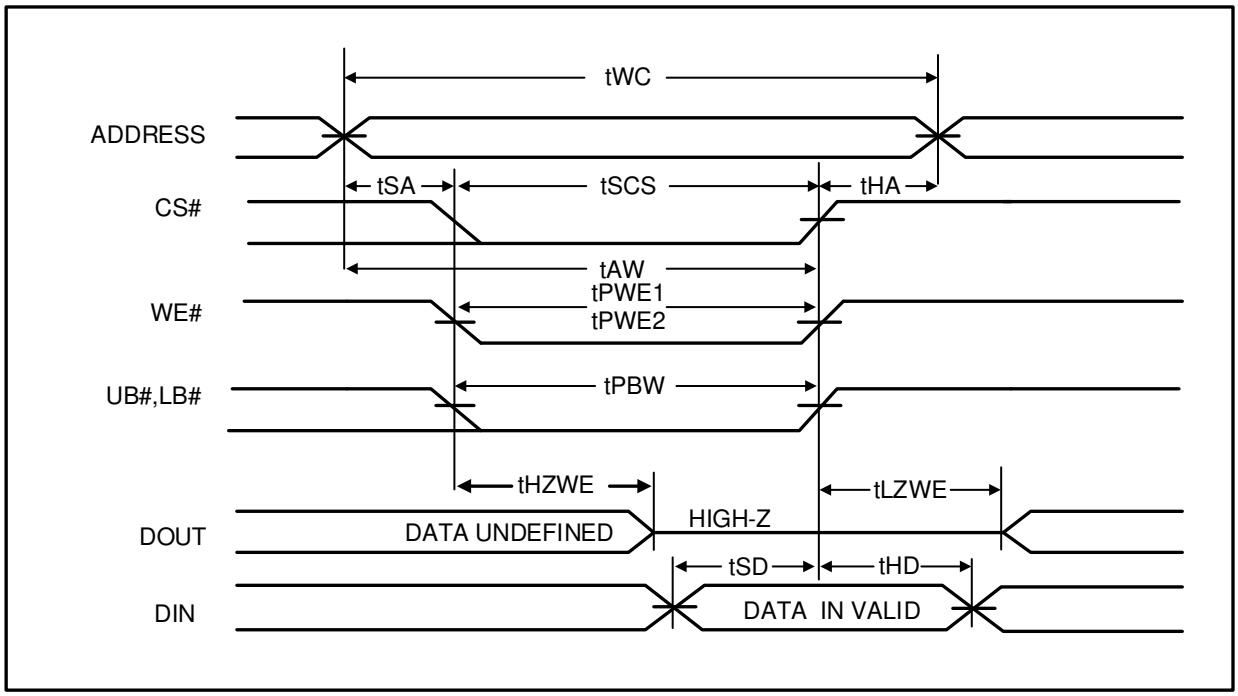
3 The internal write time is defined by the overlap of CS# = LOW, UB# or LB# = LOW, and WE# = LOW. All signals must be in valid states to initiate a Write, but anyone can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

4 CS#=H means CS1#=HIGH, and CS2=LOW in Dual Chip Select Device

5 If OE# is LOW during write cycle, (WE# controlled, CS# = UB# = LB# = LOW), the minimum Write cycle time for write cycle NO.3 is the sum of tHZWE and tSD

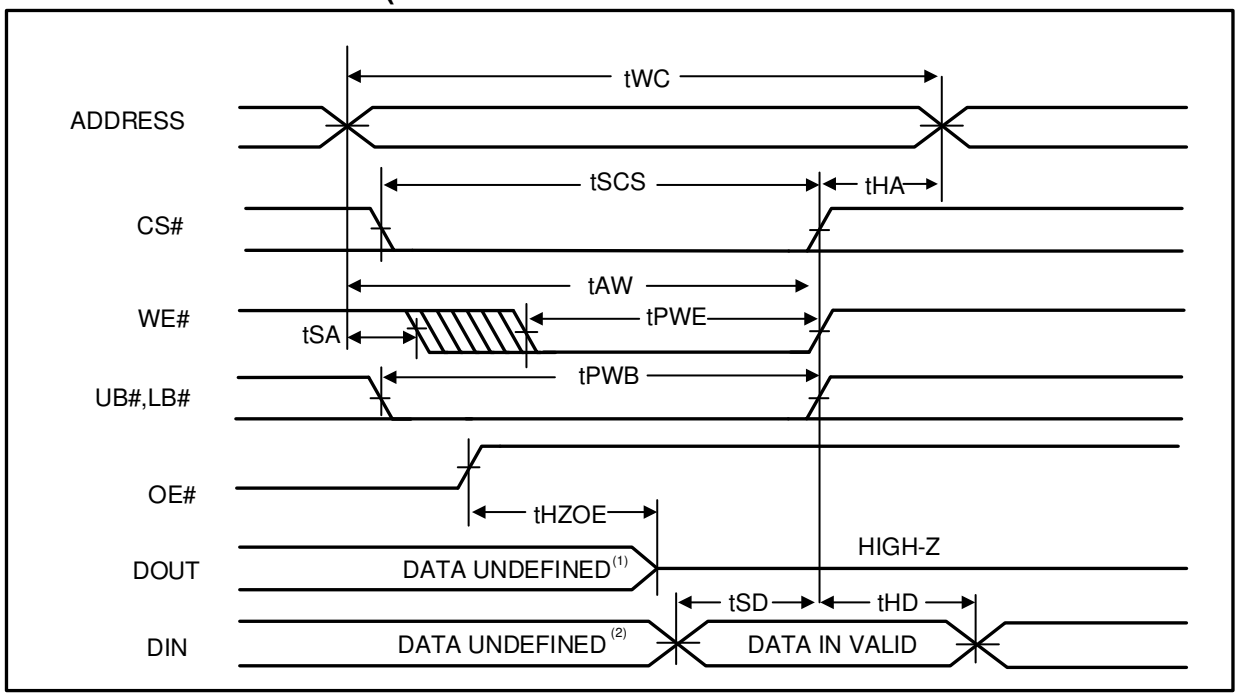
AC WAVEFORMS

WRITE CYCLE NO. 1[1] (CS# CONTROLLED, OE# = HIGH OR LOW)



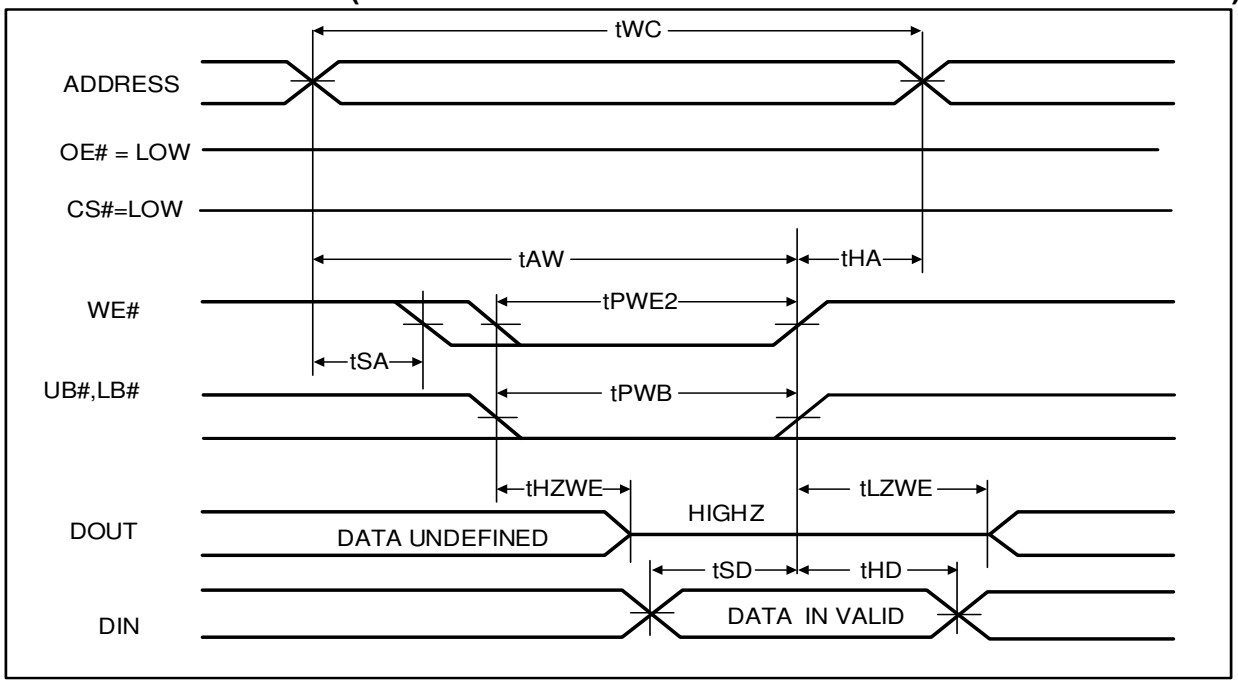
Note:
1. tHZWE is is based on the assumption when tSA=0nS after READ operation. Actual DOUT for tHZWE may not appear if OE# goes high before Write Cycle.

WRITE CYCLE NO. 2[1, 2] (WE# CONTROLLED: OE# IS HIGH DURING WRITE CYCLE)



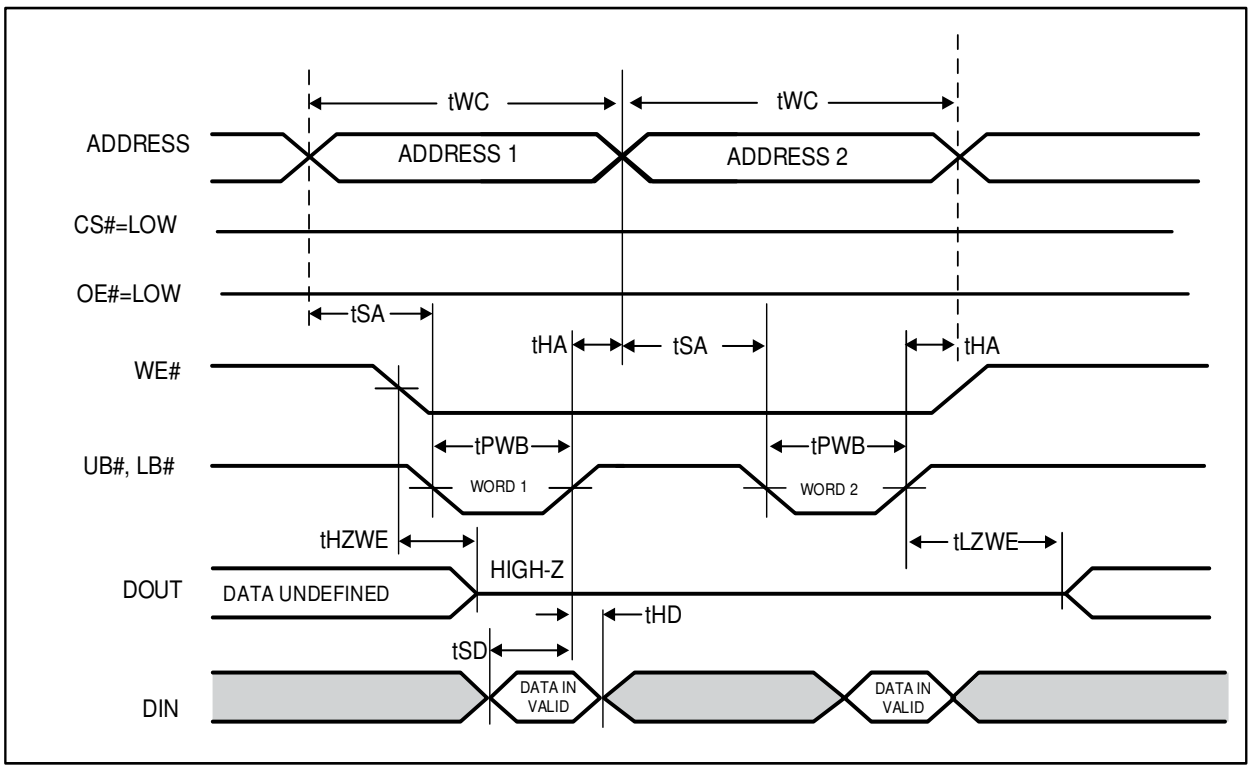
Notes:
1. tHZOE is the time DOUT goes to High-Z after OE# goes high.
2. During this period, the I/Os are in output state. Do not apply input signals.

WRITE CYCLE NO. 3[1] (WE# CONTROLLED: OE# IS LOW DURING WRITE CYCLE)



Note:
1. If OE# is low during write cycle, tHZWE must be met in the application. Do not apply input signal during this period. Data output from the previous READ operation will drive IO BUS.

WRITE CYCLE NO. 4[1, 2, 3] (UB# & LB# Controlled, CS# = OE# = LOW)



Notes:

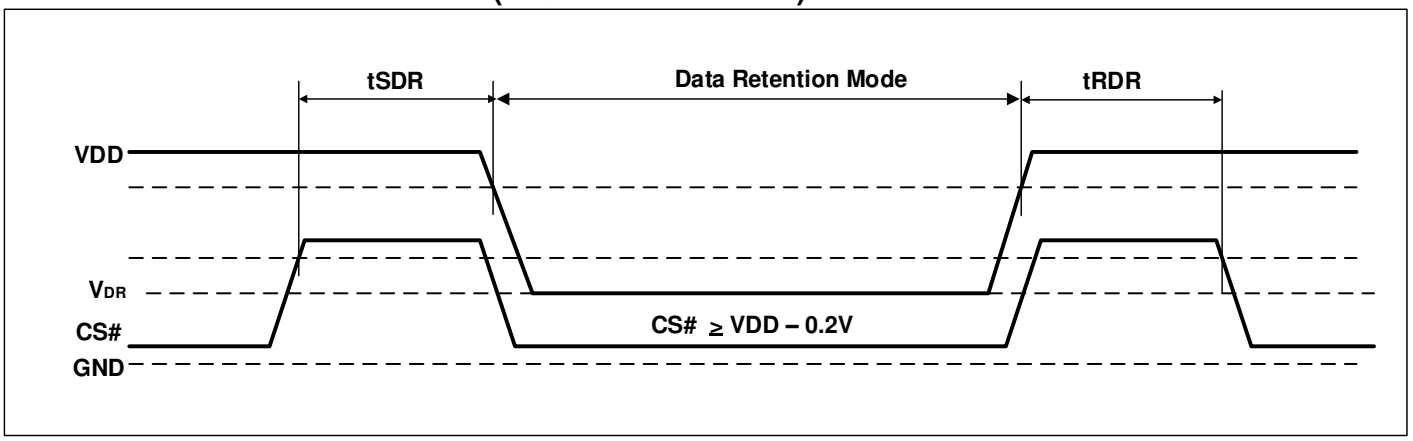
1. If OE# is low during write cycle, tHZWE must be met in the application. Do not apply input signal during this period. Data output from the previous READ operation will drive IO BUS.
2. Due to the restriction of note1, OE# is recommended to be HIGH during write period.
3. WE# stays LOW in this example. If WE# toggles,, tPWE and tHZWE must be considered

DATA RETENTION CHARACTERISTICS

Symbol	Parameter	Test Condition	OPTION	Min.	Typ.(2)	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform	V_{DD} = 2.4V to 3.6V	2.0		3.6	V
			V_{DD} = 1.65V to 2.2V	1.2		3.6	
I_{DR}	Data Retention Current	V_{DD}= V_{DR}(min), CS# ≥ V_{DD} – 0.2V	Com.	-	10	30	mA
			Ind.	-	-	40	
			Auto	-	-	50	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	-	-	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		tRC	-	-	ns

Note:
1. If CS# ≥ VDD–0.2V, all other inputs including UB# and LB# must meet this condition.
2. CS#=H means CS1#=HIGH, and CS2=LOW in Dual Chip Select Device
3. Typical values are measured at V_{DD} = V_{DR} (Min), T_A = 25 °C and not 100% tested.

DATA RETENTION WAVEFORM (CS# CONTROLLED)



ORDERING INFORMATION

Industrial Range: -40°C to +85°C, Voltage Range: 1.65V to 2.2V

Speed (ns)	Order Part No.	Package
20	IS61WV102416FALL-20BLI	mini BGA (6mm x 8mm), Single Chip Select, Lead-free
20	IS61WV102416FALL-20B2LI	mini BGA (6mm x 8mm), Dual Chip Select, Lead-free
20	IS61WV102416FALL-20B3LI	mini BGA (6mm x 8mm), Single Chip Select, Lead-free
20	IS61WV102416FALL-20B4LI	mini BGA (6mm x 8mm), Dual Chip Select, Lead-free
20	IS61WV102416FALL-20TLI	48-pin TSOP (Type I), Lead-free
20	IS61WV102416FALL-20T2LI	54-pin TSOP (Type II), Lead-free

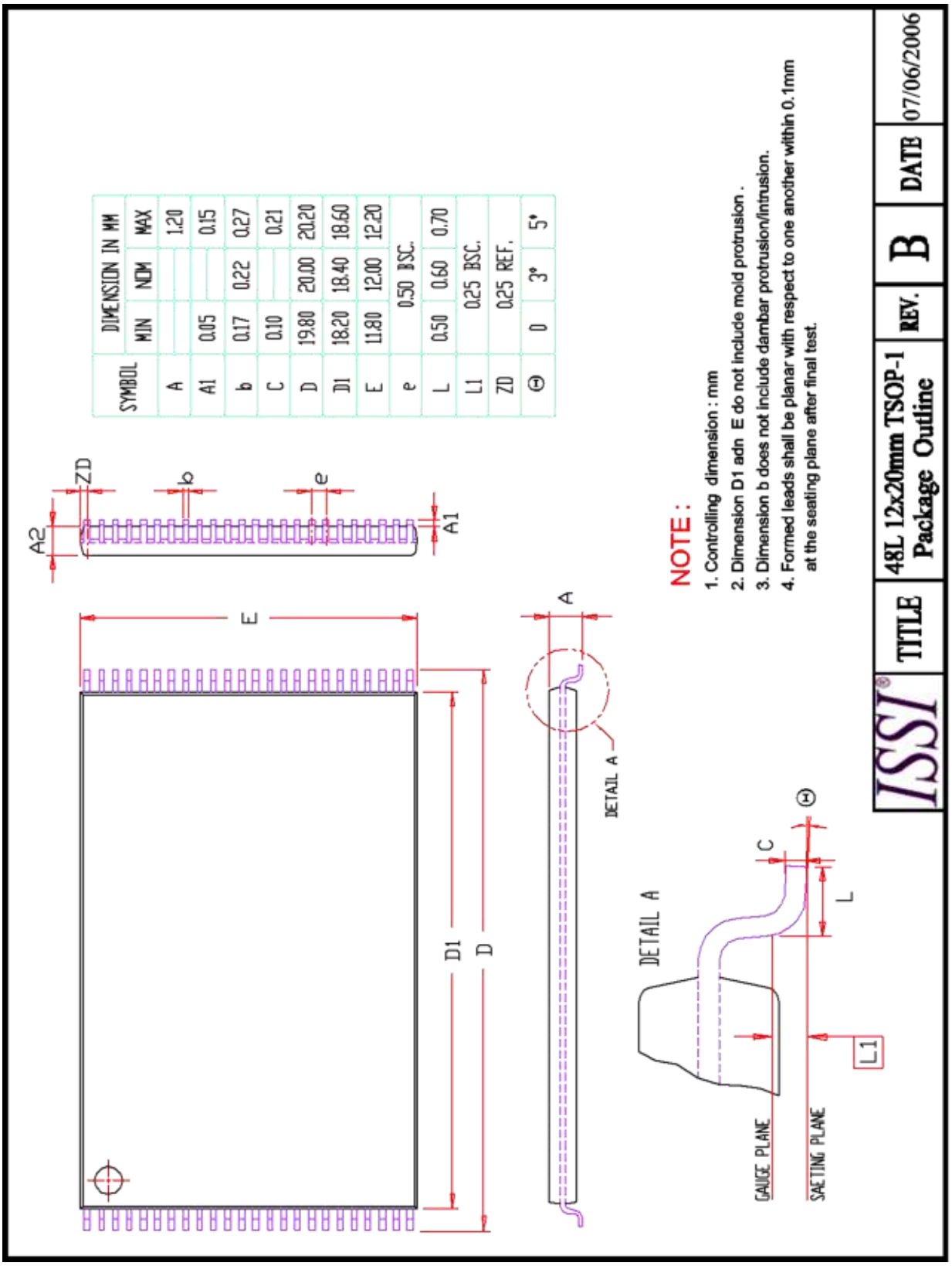
Industrial Range: -40°C to +85°C, Voltage Range: 2.4V to 3.6V

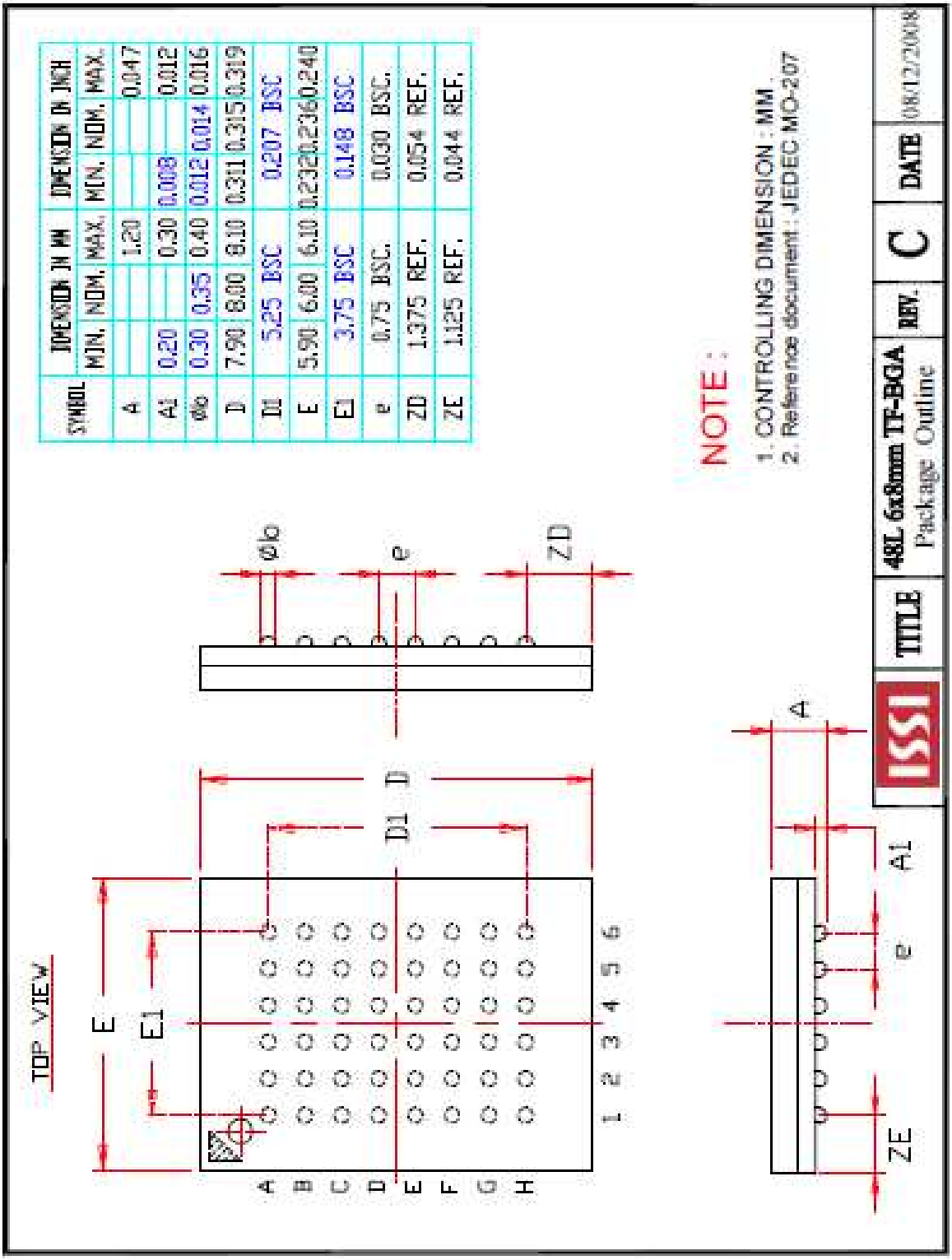
Speed (ns)	Order Part No.	Package
8	IS61WV102416FBLL-8BI	mini BGA (6mm x 8mm), Single Chip Select
8	IS61WV102416FBLL-8BLI	mini BGA (6mm x 8mm), Single Chip Select, Lead-free
8	IS61WV102416FBLL-8B2I	mini BGA (6mm x 8mm), Dual Chip Select
8	IS61WV102416FBLL-8B2LI	mini BGA (6mm x 8mm), Dual Chip Select, Lead-free
8	IS61WV102416FBLL-8B3LI	mini BGA (6mm x 8mm), Single Chip Select, Lead-free
8	IS61WV102416FBLL-8B4LI	mini BGA (6mm x 8mm), Dual Chip Select, Lead-free
8	IS61WV102416FBLL-8TLI	48-pin TSOP (Type I), Lead-free
8	IS61WV102416FBLL-8T2LI	54-pin TSOP (Type II), Lead-free
10	IS61WV102416FBLL-10BI	mini BGA (6mm x 8mm), Single Chip Select
10	IS61WV102416FBLL-10BLI	mini BGA (6mm x 8mm), Single Chip Select, Lead-free
10	IS61WV102416FBLL-10B2I	mini BGA (6mm x 8mm), Dual Chip Select
10	IS61WV102416FBLL-10B2LI	mini BGA (6mm x 8mm), Dual Chip Select, Lead-free
10	IS61WV102416FBLL-10B3LI	mini BGA (6mm x 8mm), Single Chip Select, Lead-free
10	IS61WV102416FBLL-10B4LI	mini BGA (6mm x 8mm), Dual Chip Select, Lead-free
10	IS61WV102416FBLL-10TLI	48-pin TSOP (Type I), Lead-free
10	IS61WV102416FBLL-10T2LI	54-pin TSOP (Type II), Lead-free

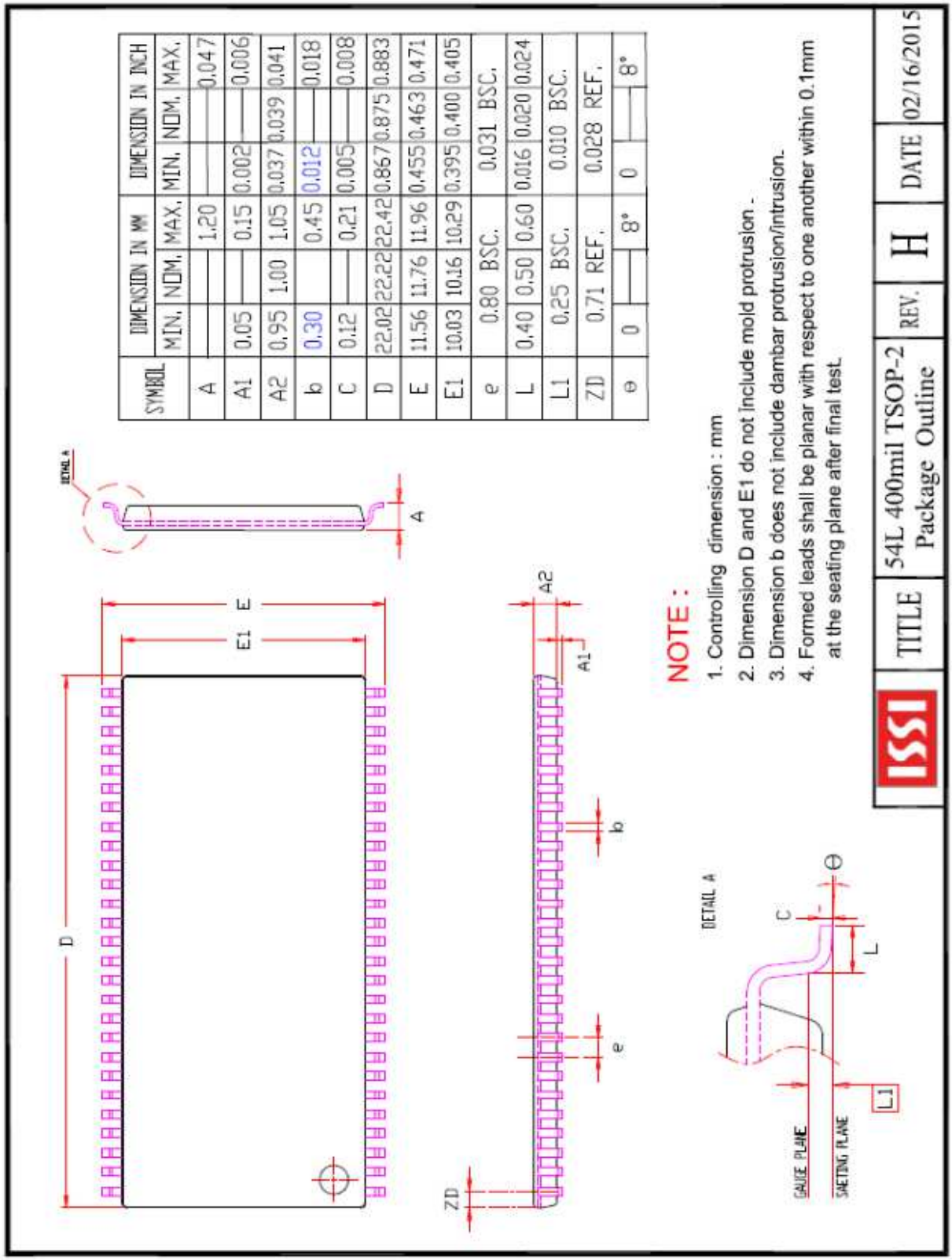
Automotive (A3) Range: –40°C to +125°C, Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
10	IS64WV102416FBLL-10BA3	mini BGA (6mm x 8mm), Single Chip Select
10	IS64WV102416FBLL-10BLA3	mini BGA (6mm x 8mm), Single Chip Select, Lead-free
10	IS64WV102416FBLL-10B2A3	mini BGA (6mm x 8mm), Dual Chip Select
10	IS64WV102416FBLL-10B2LA3	mini BGA (6mm x 8mm), Dual Chip Select, Lead-free
10	IS64WV102416FBLL-10B3LA3	mini BGA (6mm x 8mm), Single Chip Select, Lead-free
10	IS64WV102416FBLL-10B4LA3	mini BGA (6mm x 8mm), Dual Chip Select, Lead-free
10	IS64WV102416FBLL-10CTLA3	48-pin TSOP (Type I), Copper Leadframe, Lead-free
10	IS64WV102416FBLL-10CT2LA3	54-pin TSOP (Type II), Copper Leadframe, Lead-free

PACKAGE INFORMATION




SYMBOL
DIMENSION IN MM
MIN. NOM. MAX.
DIMENSION IN INCH
MIN. NOM. MAX.
A — — 1.20 — — 0.047
A1 0.20 — 0.30 0.008 — 0.012
ϕb 0.30 0.35 0.40 0.012 0.014 0.016
D 7.90 8.00 8.10 0.311 0.315 0.319
D1 5.25 BSC 0.207 BSC
E 5.90 6.00 6.10 0.232 0.236 0.240
E1 3.75 BSC 0.148 BSC
e 0.75 BSC. 0.030 BSC.
ZD 1.375 REF. 0.054 REF.
ZE 1.125 REF. 0.044 REF.
NOTE:
1. CONTROLLING DIMENSION : MM.
2. Reference document : JEDEC MO-207
TOP VIEW
A B C D E F G H
1 2 3 4 5 6
E
E1
D
D1
ϕb
e
ZD
A
A1
e
ZE
ISSI
TITLE
48L 6x8mm TF-BGA
Package Outline
REV.
C
DATE
08/12/2008


SYMBOL
DIMENSION IN MM
MIN. NOM. MAX.
DIMENSION IN INCH
MIN. NOM. MAX.
A — — 1.20 — — 0.047
A1 0.05 — 0.15 0.002 — 0.006
A2 0.95 1.00 1.05 0.037 0.039 0.041
b 0.30 0.45 0.012 0.018
C 0.12 — 0.21 0.005 — 0.008
D 22.02 22.22 22.42 0.867 0.875 0.883
E 11.56 11.76 11.96 0.455 0.463 0.471
E1 10.03 10.16 10.29 0.395 0.400 0.405
e 0.80 BSC. 0.031 BSC.
L 0.40 0.50 0.60 0.016 0.020 0.024
L1 0.25 BSC. 0.010 BSC.
ZD 0.71 REF. 0.028 REF.
θ 0 — 8° 0 — 8°
NOTE :
1. Controlling dimension : mm
2. Dimension D and E1 do not include mold protrusion .
3. Dimension b does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.
ISSI
TITLE
54L 400mil TSOP-2 Package Outline
REV. H
DATE 02/16/2015
DETAIL A
GAUGE PLANE
SEATING PLANE
L1