IS64WV3216BLL
IS61WV3216BLL

32K x 16 HIGH-SPEED CMOS STATIC RAM

JULY 2009

FEATURES

- High-speed access time:
  12 ns: 3.3V ± 10%
  15 ns: 2.5V-3.6V
- CMOS low power operation:
  50 mW (typical) operating
  25 µW (typical) standby
- TTL compatible interface levels
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Automotive Temperature Available
- Lead-free available

DESCRIPTION

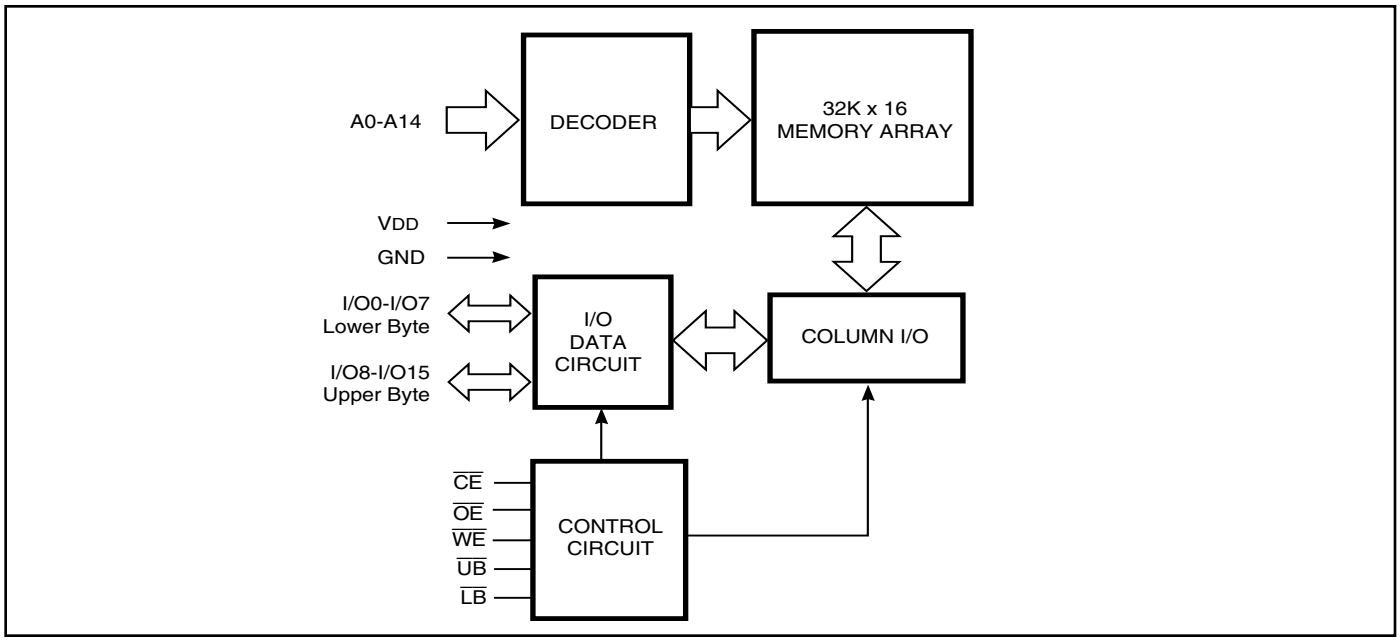
The *ISSI* IS61/64WV3216BLL is a high-speed, 524,288-bit static RAM organized as 32,768 words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 12ns (3.3V ± 10%) and 15ns (2.5V-3.6V) with low power consumption.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, $\overline{CE}$ and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

The IS61/64WV3216BLL is packaged in the JEDEC standard 44-pin TSOP-II, and 48-pin mini BGA (6mm x 8mm).

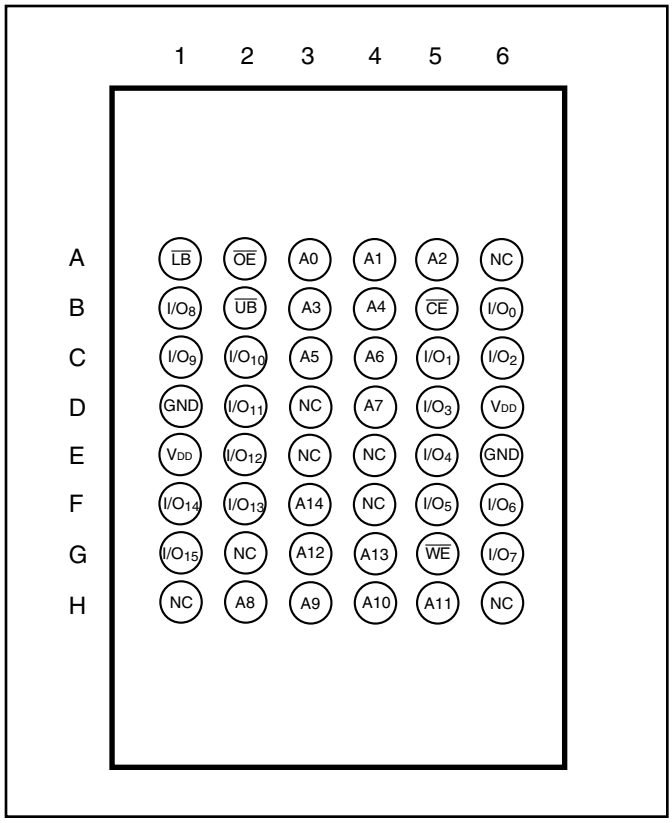
FUNCTIONAL BLOCK DIAGRAM



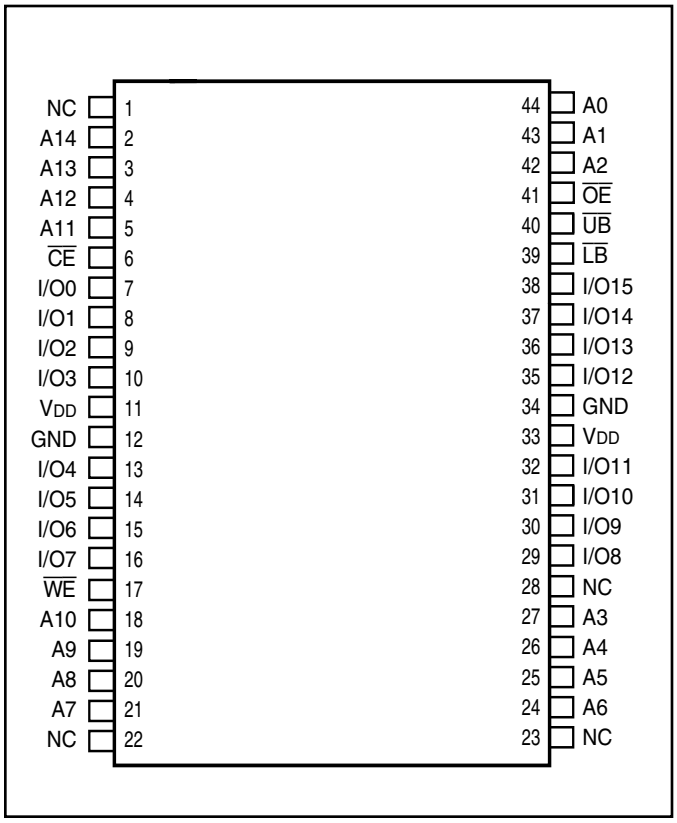
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PIN CONFIGURATIONS

48-Pin mini BGA (6mm x 8mm)



44-Pin TSOP-II



PIN DESCRIPTIONS

A0-A14	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
V_{DD}	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN I/O0-I/O7	I/O PIN I/O8-I/O15	V_{DD} Current
Not Selected	X	H	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	X	X	High-Z	High-Z	I_{CC}
	X	L	X	H	H	High-Z	High-Z	
Read	H	L	L	L	H	D_{OUT}	High-Z	I_{CC}
	H	L	L	H	L	High-Z	D_{OUT}	
	H	L	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	X	L	H	D_{IN}	High-Z	I_{CC}
	L	L	X	H	L	High-Z	D_{IN}	
	L	L	X	L	L	D_{IN}	D_{IN}	

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to V_{DD}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.5	W
V_{DD}	V_{DD} Related to GND	-0.2 to +3.9	V

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE (V_{DD})

Range	Ambient Temperature	V_{DD} (15 ns)	V_{DD} (12 ns)
Commercial	0°C to +70°C	2.5V-3.6V	3.3V $\pm$ 10%
Industrial	–40°C to +85°C	2.5V-3.6V	3.3V $\pm$ 10%
Automotive	–40°C to +125°C	2.5V-3.6V	3.3V $\pm$ 10%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 2.5V-3.6V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –1.0 mA	2.3	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 1.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage[1]		–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	–2	2	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	–2	2	µA

Note:
1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width 2.0 ns). Not 100% tested.
   V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width 2.0 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 3.3V ± 10%

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –4.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 8.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage[1]		–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	–2	2	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	–2	2	µA

Note:
1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width 2.0 ns). Not 100% tested.
   V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width 2.0 ns). Not 100% tested.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions	Options	-12 ns Min.	-12 ns Max.	-15 ns Min.	-15 ns Max.	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX}	COM.	—	35	—	30	mA
			IND.	—	45	—	40	
			AUTO	—	60	—	50	
			typ.[2]	—	20	—	20	
I_{CC1}	Operating Supply Current	V_{DD} = Max., Iout = 0mA, f = 0	COM.	—	5	—	5	mA
			IND.	—	5	—	5	
			AUTO	—	5	—	5	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CE} \geq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq 0.2V$, f = 0	COM.	—	20	—	20	uA
			IND.	—	50	—	50	
			AUTO	—	75	—	75	
			typ.[2]	—	6	—	6	

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD}=2.5V, T_A=25°C. Not 100% tested.

CAPACITANCE[1]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

Parameter	Unit (2.5V-3.6V)	Unit (3.3V ± 10%)
Input Pulse Level	0V to V_{DD} V	0V to V_{DD} V
Input Rise and Fall Times	1.5ns	1.5ns
Input and Output Timing and Reference Level (V_{Ref})	$V_{DD}/2$	$V_{DD}/2$ + 0.05
Output Load	See Figures 1a and 1b	See Figures 1a and 1b

AC TEST LOADS

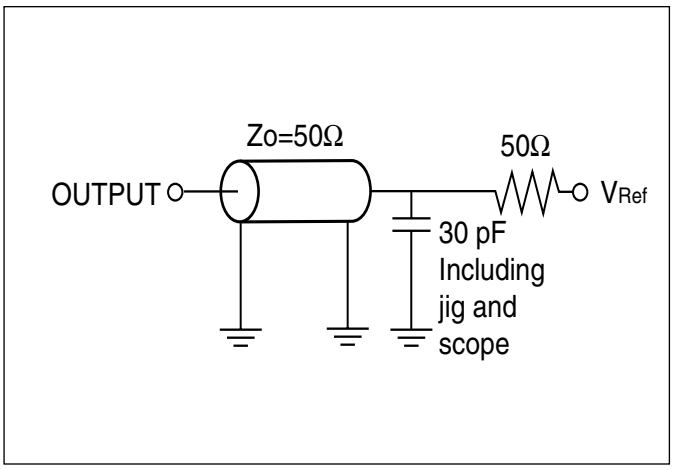


Figure 1a.

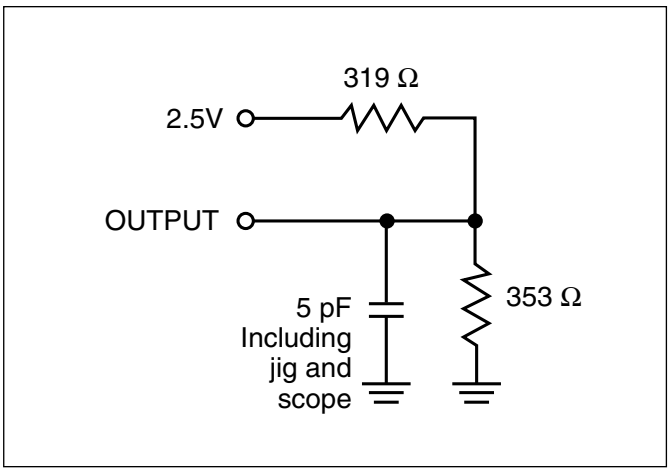


Figure 1b.

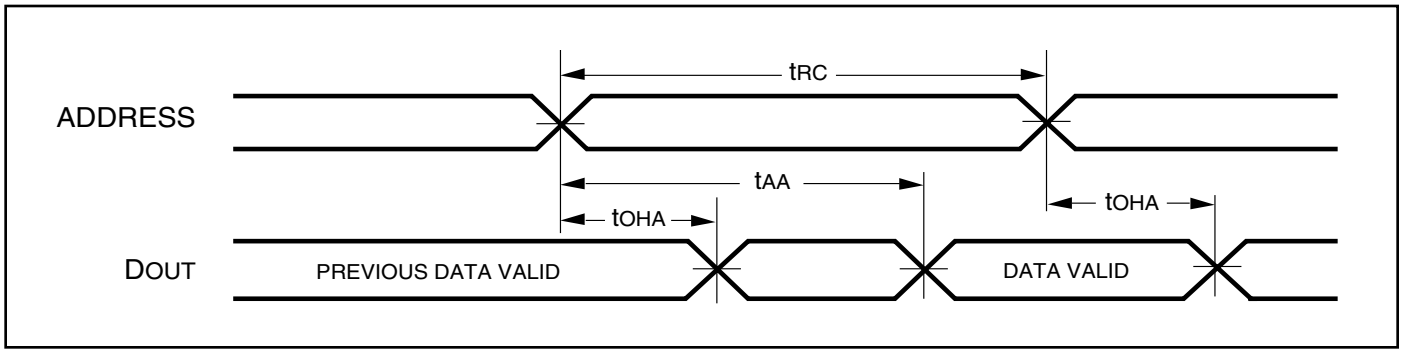
READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-12 ns Min.	-12 ns Max.	-15 ns Min.	-15 ns Max.	Unit
t_{RC}	Read Cycle Time	12	—	15	—	ns
t_{AA}	Address Access Time	—	12	—	15	ns
t_{OHA}	Output Hold Time	3	—	3	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	12	—	15	ns
t_{DOE}	$\overline{OE}$ Access Time	—	6	—	7	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	6	0	6	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	ns
t_{HZCE}[2	$\overline{CE}$ to High-Z Output	0	6	0	6	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output		3 —		3 —	ns
t_{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	6	—	7	ns
t_{HZB}	$\overline{LB}$, $\overline{UB}$ to High-Z Output	0	6	0	6	ns
t_{LZB}	$\overline{LB}$, $\overline{UB}$ to Low-Z Output	0	—	0	—	ns

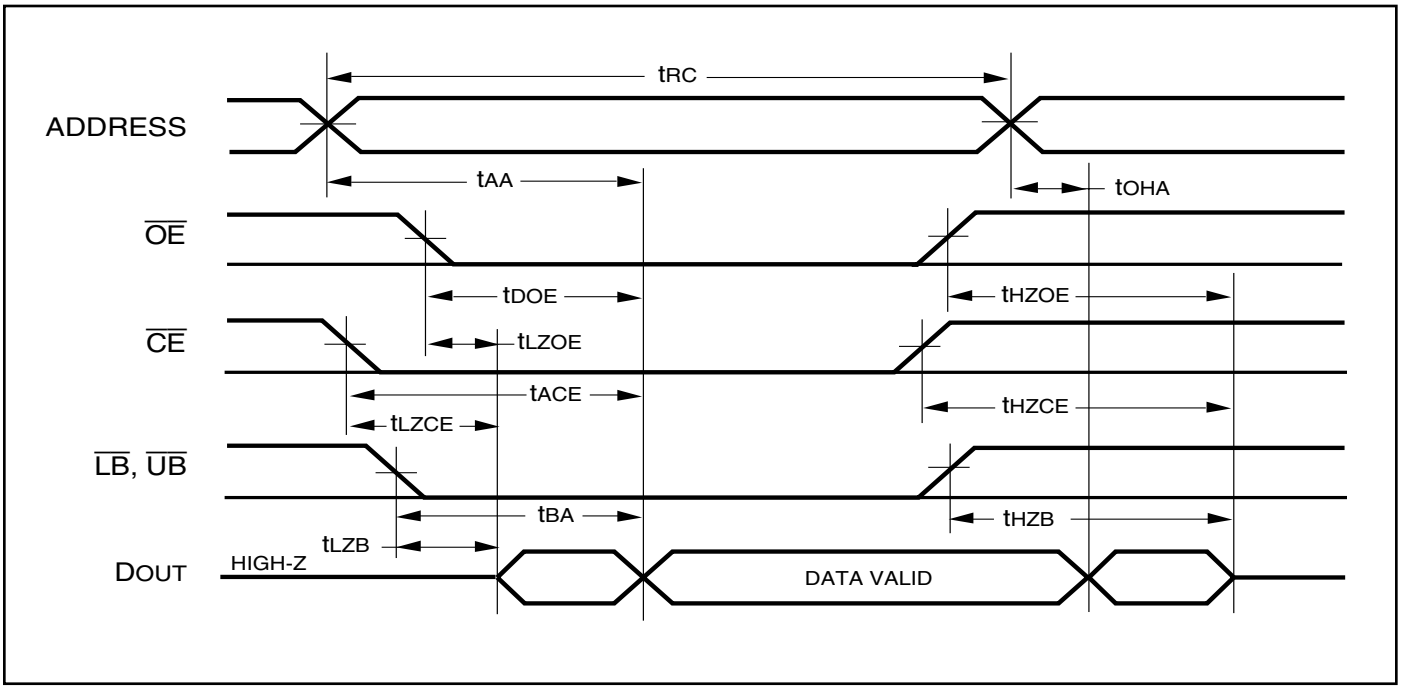
Notes:
1. Test conditions assume signal transition times of 1.5 ns or less, timing reference levels of 1.25V, input pulse levels of 0V to V_{DD} V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL})



READ CYCLE NO. 2[1,3]



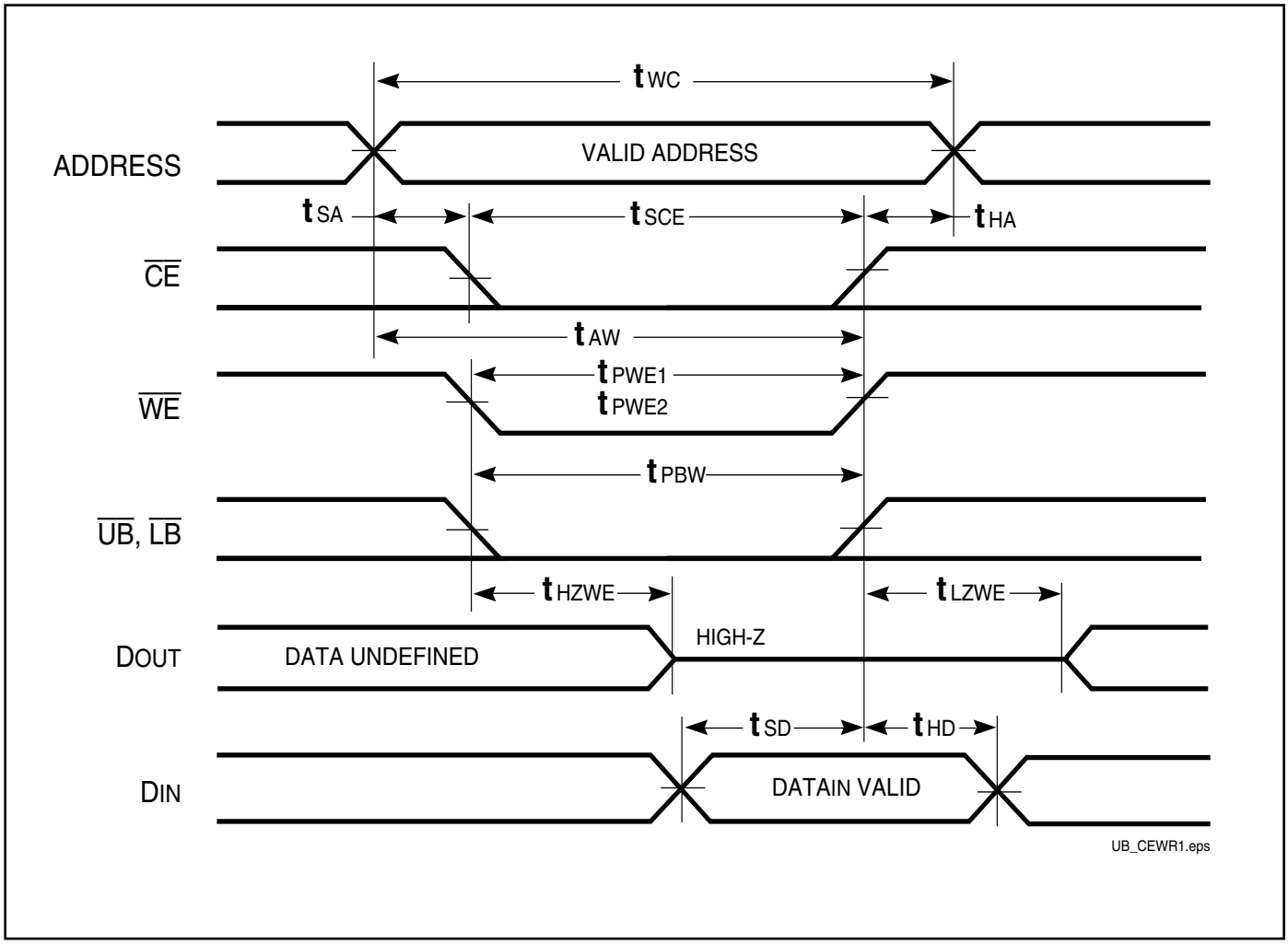
Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{UB}$, or $\overline{LB}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

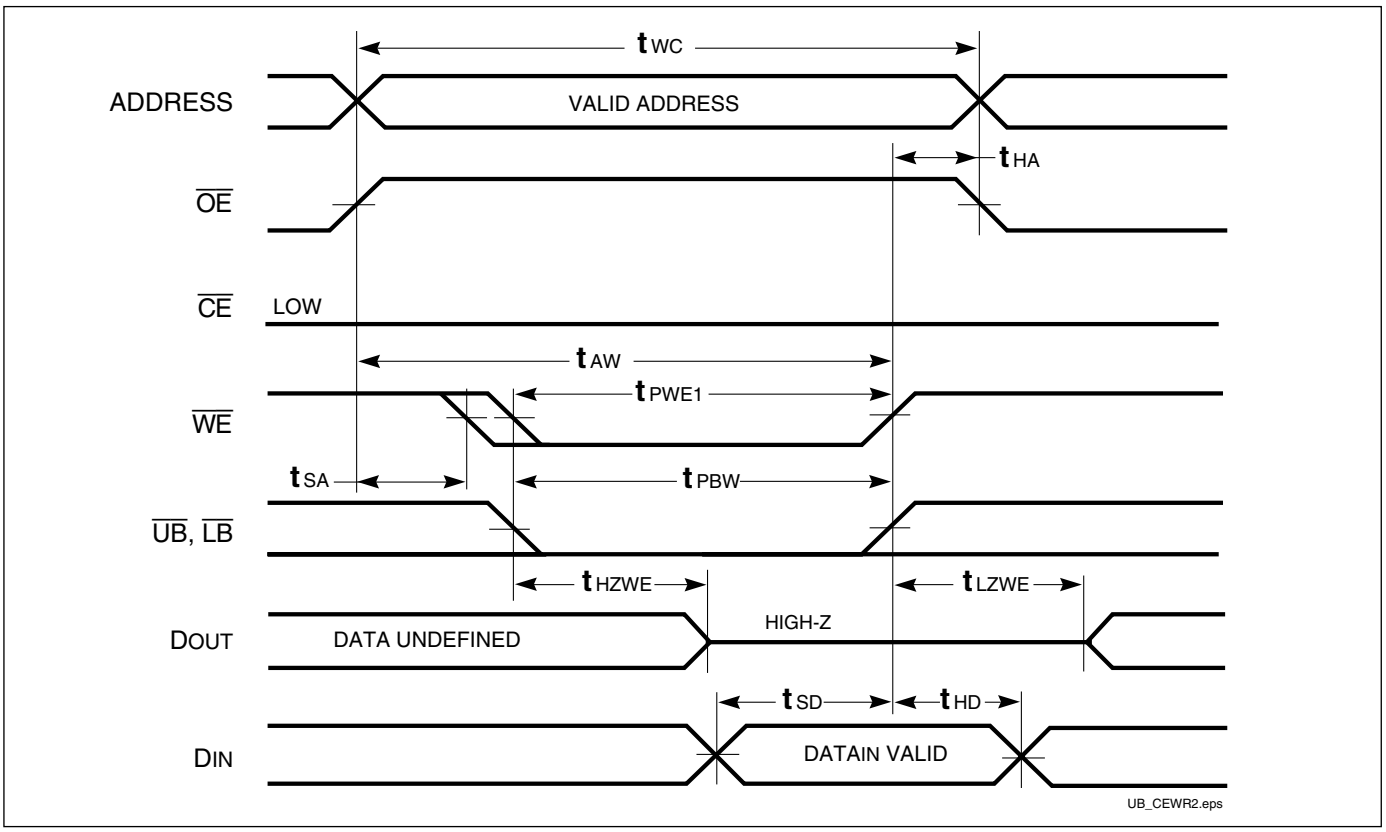
Symbol	Parameter	-12 ns Min.	-12 ns Max.	-15 ns Min.	-15 ns Max.	Unit
t_{WC}	Write Cycle Time	12	—	15	—	ns
t_{SCE}	$\overline{CE}$ to Write End	9	—	10	—	ns
t_{AW}	Address Setup Time to Write End	9	—	10	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	9	—	10	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = HIGH)	9	—	10	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW)	11	—	12	—	ns
t_{SD}	Data Setup to Write End	9	—	9	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	6	—	7	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	3	—	3	—	ns

Notes:
1. Test conditions for IS61WV3216BLL assume signal transition times of 1.5ns or less, timing reference levels of 1.25V, input pulse levels of 0V to V_{DD} V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

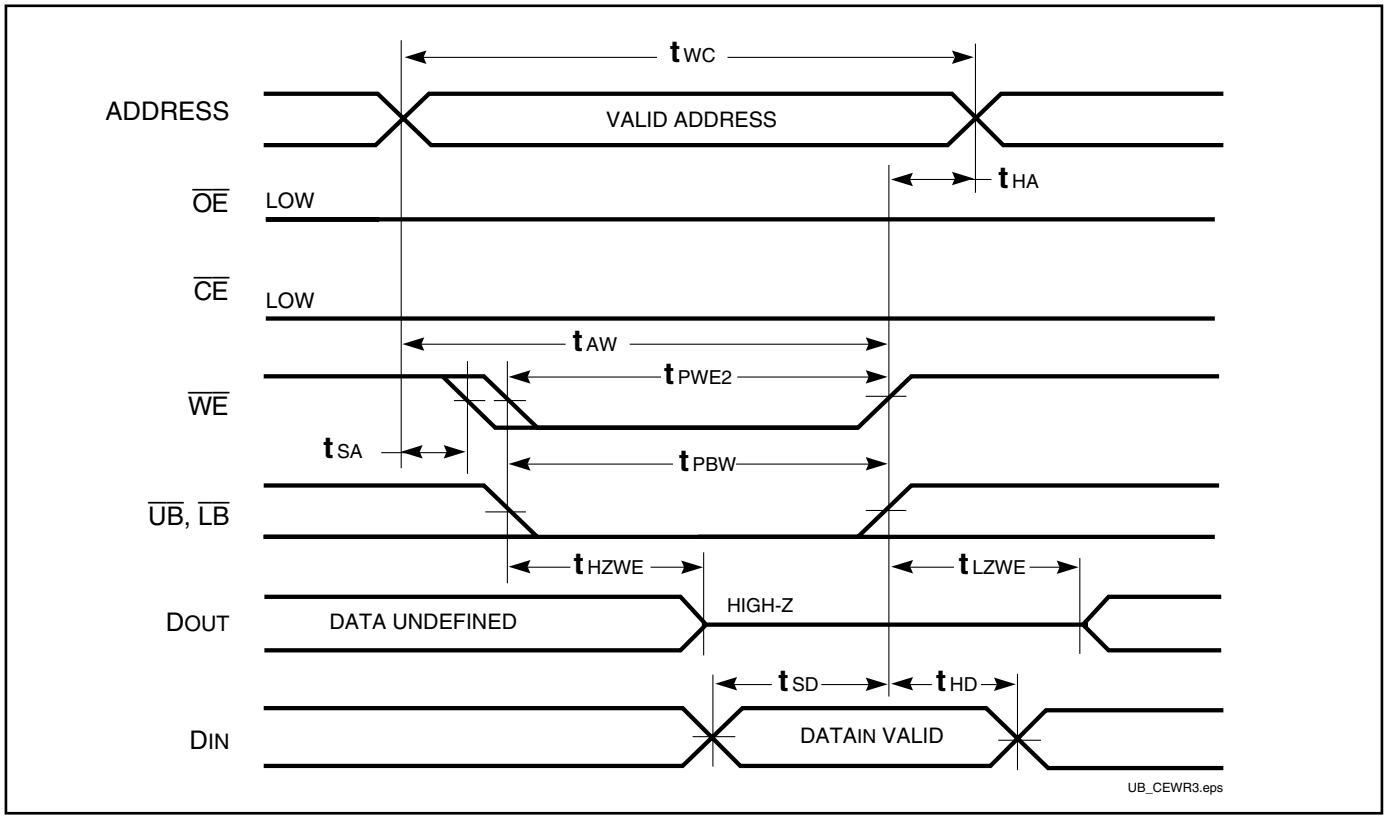
WRITE CYCLE NO. 1[1,2] ($\overline{CE}$ Controlled, $\overline{OE}$ = HIGH or LOW)



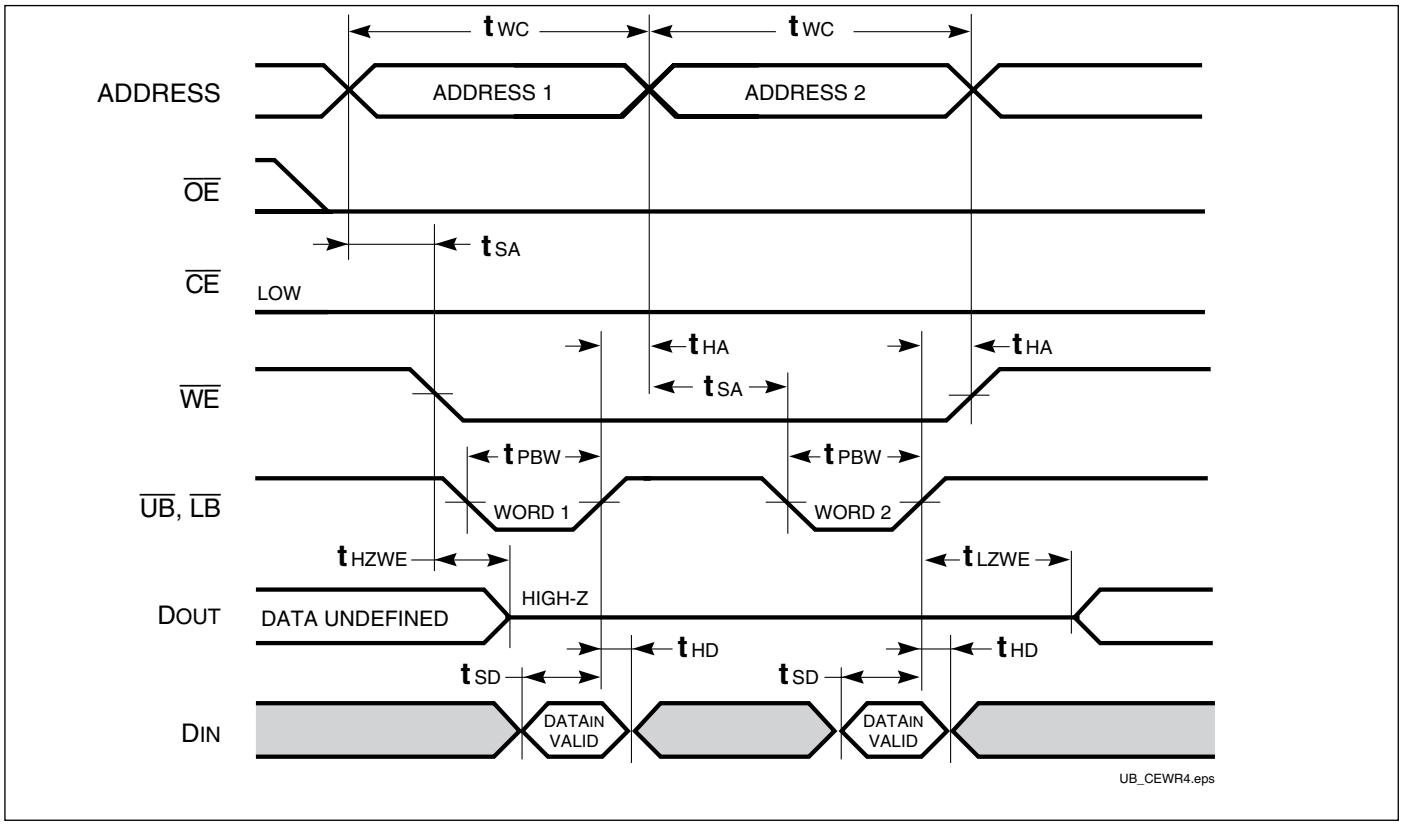
WRITE CYCLE NO. 2[1] ($\overline{WE}$ Controlled, $\overline{OE}$ = HIGH during Write Cycle)



WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)



WRITE CYCLE NO. 4 ($\overline{LB}$, $\overline{UB}$ Controlled, Back-to-Back Write) [1,3]



Notes:
1. The internal Write time is defined by the overlap of $\overline{CE}$ = LOW, $\overline{UB}$ and/or $\overline{LB}$ = LOW, and $\overline{WE}$ = LOW. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The t_{SA}, t_{HA}, t_{SD}, and t_{HD} timing is referenced to the rising or falling edge of the signal that terminates the Write.
2. Tested with $\overline{OE}$ HIGH for a minimum of 4 ns before $\overline{WE}$ = LOW to place the I/O in a HIGH-Z state.
3. $\overline{WE}$ may be held LOW across many address cycles and the $\overline{LB}$, $\overline{UB}$ pins can be used to control the Write function.

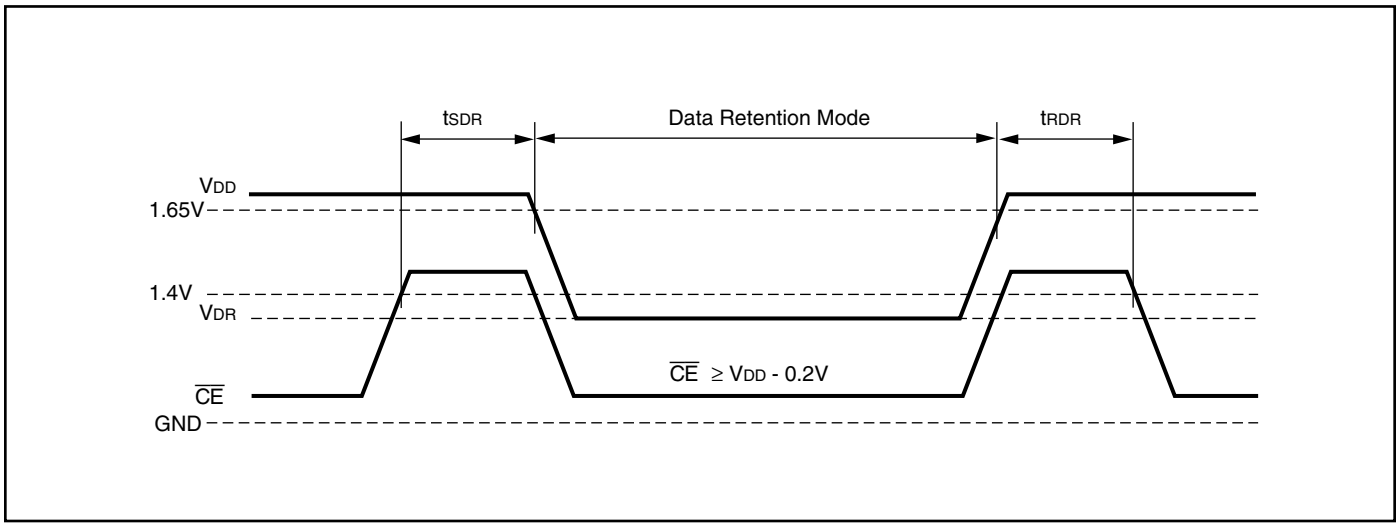
DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Operations	Min.	Typ.(1)	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		1.8	—	3.6	V
I_{DR}	Data Retention Current	V_{DD} = 1.8V, $\overline{CE} \geq V_{DD} - 0.2V$	COM.	—	6	20	µA
			IND.	—	6	50	
			AUTO	—	6	75	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}	—	—	ns

Note:

1. Typical values are measured at V_{DD} = 2.5V, T_A = 25°C. Not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



ORDERING INFORMATION

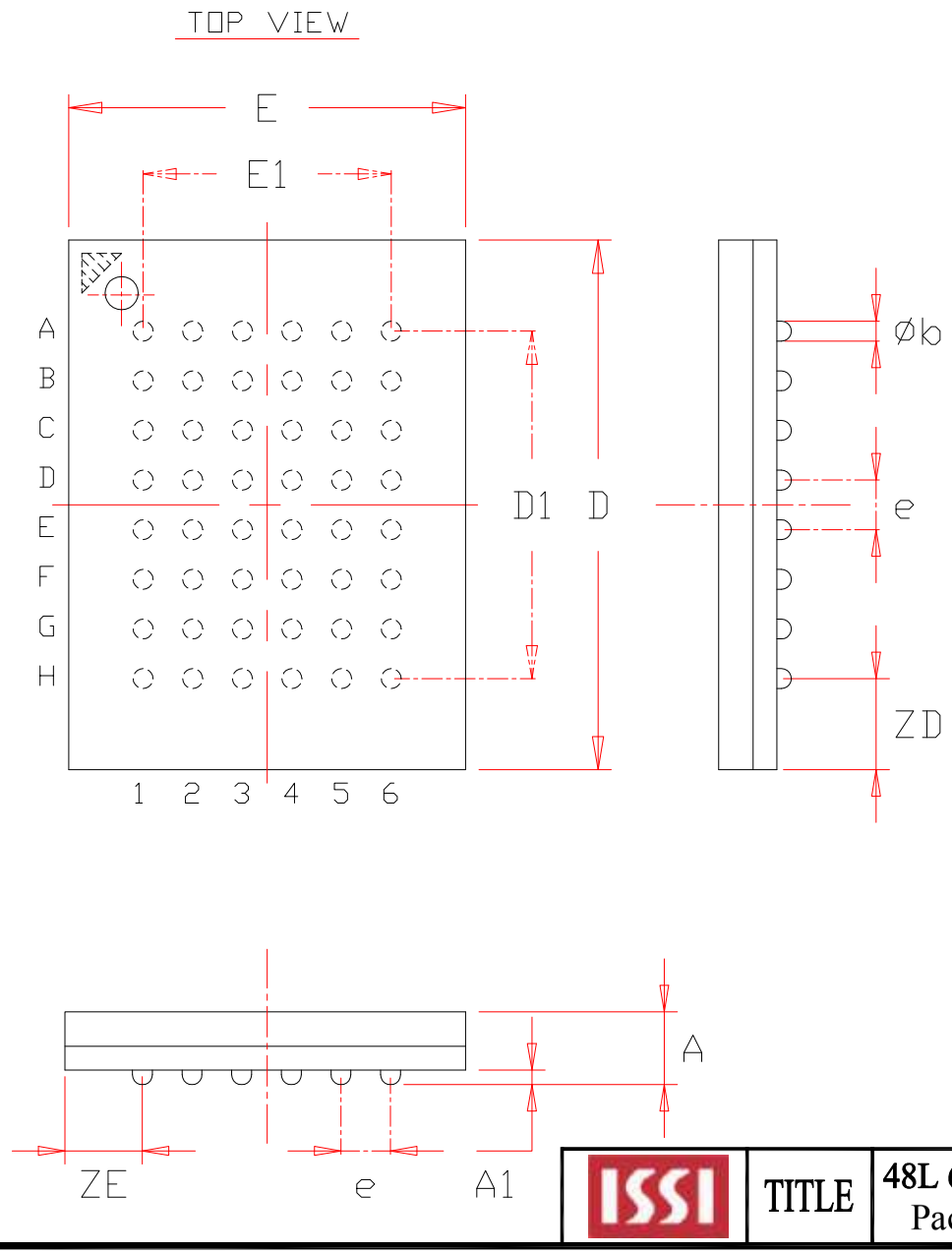
Industrial Temperature Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
12	IS61WV3216BLL-12TI	Plastic TSOP
12	IS61WV3216BLL-12TLI	Plastic TSOP, Lead-free
12	IS61WV3216BLL-12BI	mini BGA (6mm x 8mm)
12	IS61WV3216BLL-12BLI	mini BGA (6mm x 8mm), Lead-free

Temperature Range (A3): –40°C to +125°C

Speed (ns)	Order Part No.	Package
15 (12*)	IS64WV3216BLL-15TA3	Plastic TSOP
15 (12*)	IS64WV3216BLL-15TLA3	Plastic TSOP, Lead-free
15 (12*)	IS64WV3216BLL-15CTLA3	Plastic TSOP, Lead-free, Copper Lead-frame
15 (12*)	IS64WV3216BLL-15BA3	mini BGA (6mm x 8mm)
15 (12*)	IS64WV3216BLL-15BLA3	mini BGA (6mm x 8mm), Lead-free

Note:
1. Speed = 12ns for V_{DD} = 3.3V $\pm$ 10%. Speed = 15ns for V_{DD} = 2.5V- 3.6V.



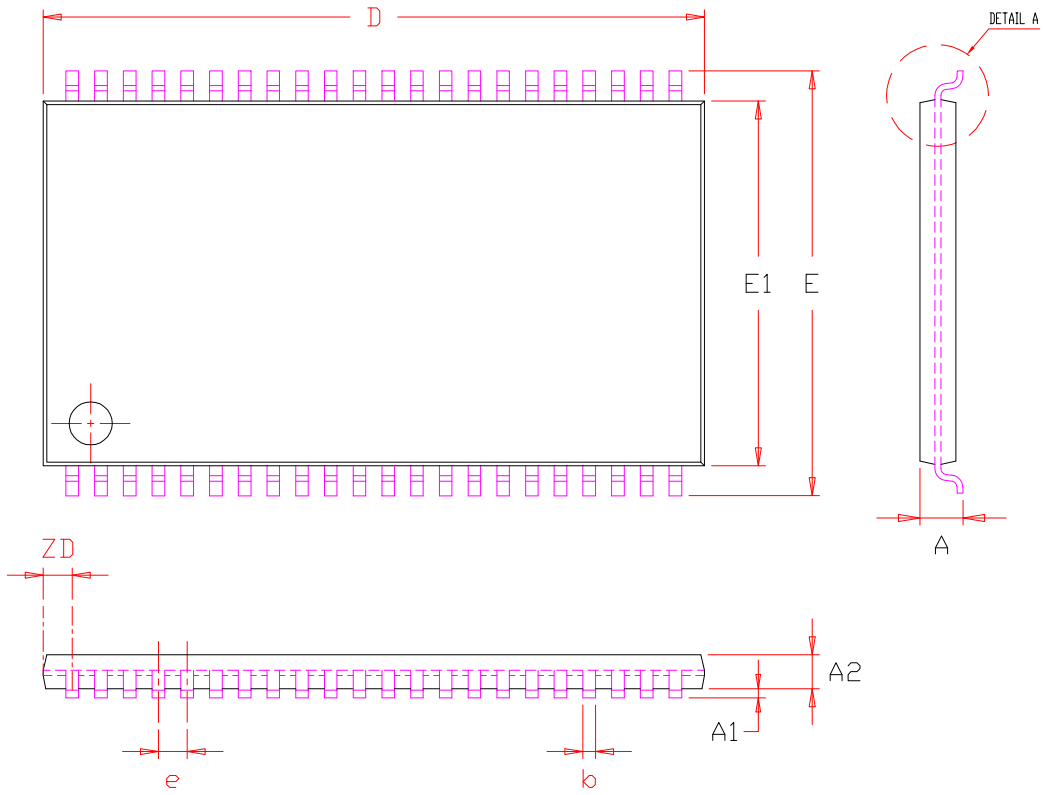
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			0.047
A1	0.20		0.30	0.008		0.012
øb	0.30	0.35	0.40	0.012	0.014	0.016
D	7.90	8.00	8.10	0.311	0.315	0.319
D1	5.25 BSC			0.207 BSC		
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	3.75 BSC			0.148 BSC		
e	0.75 BSC.			0.030 BSC.		
ZD	1.375 REF.			0.054 REF.		
ZE	1.125 REF.			0.044 REF.		

NOTE :

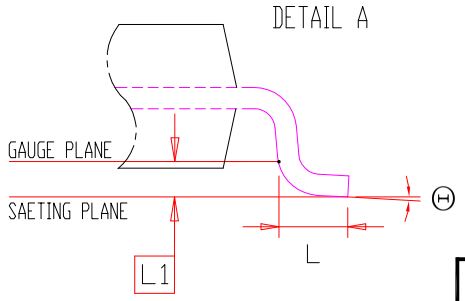
1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207

ISSI	TITLE	48L 6x8mm TF-BGA Package Outline	REV.	C	DATE	08/12/2008

Integrated Silicon Solution, Inc. — www.issi.com — 1-800-379-4774
Rev. B
07/22/09



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00		1.20	0.039		0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30		0.45	0.012		0.018
D	18.28	18.41	18.54	0.720	0.725	0.730
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	0.80 BSC.			0.031 BSC.		
L	0.40		0.69	0.016		0.027
L1	0.25 BSC.			0.010 BSC.		
ZD	0.805 REF.			0.032 REF.		
Θ	0		8°	0		8°



NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

	TITLE	44L 400mil TSOP-2 Package Outline	REV.	F	DATE	06/04/2008