Low Phase Noise, Dual Output Buffer/Driver/ Logic Converter

FEATURES

- **Low Phase Noise Buffer/Driver**
- **Optimized Conversion of Sine Wave Signals to Logic Levels**
- **Three Logic Output Types Available**
  - **LVPECL**
  - **LVDS**
  - **CMOS**
- Additive Jitter 45fs$_{RMS}$ (LTC6957-1)
- Frequency Range Up to 300MHz
- 3.15V to 3.45V Supply Operation
- Low Skew 3ps Typical
- Fully Specified from –40°C to 125°C
- 12-Lead MSOP and 3mm × 3mm DFN Packages

APPLICATIONS

- System Reference Frequency Distribution
- High Speed ADC, DAC, DDS Clock Driver
- Military and Secure Radio
- Low Noise Timing Trigger
- Broadband Wireless Transceiver
- High Speed Data Acquisition
- Medical Imaging
- Test and Measurement

DESCRIPTION

The LTC®6957-1/LTC6957-2/LTC6957-3/LTC6957-4 is a family of very low phase noise, dual output AC signal buffer/driver/logic level translators. The input signal can be a sine wave or any logic level (≤2V$_{P-P}$). There are four members of the family that differ in their output logic signal type as follows:

LTC6957-1: LVPECL Logic Outputs

LTC6957-2: LVDS Logic Outputs

LTC6957-3: CMOS Logic, In-Phase Outputs

LTC6957-4: CMOS Logic, Complementary Outputs

The LTC6957 will buffer and distribute any logic signal with minimal additive noise, however, the part really excels at translating sine wave signals to logic levels. The early amplifier stages have selectable lowpass filtering to minimize the noise while still amplifying the signal to increase its slew rate. This input stage filtering/noise limiting is especially helpful in delivering the lowest possible phase noise signal with slow slewing input signals such as a typical 10MHz sine wave system reference.

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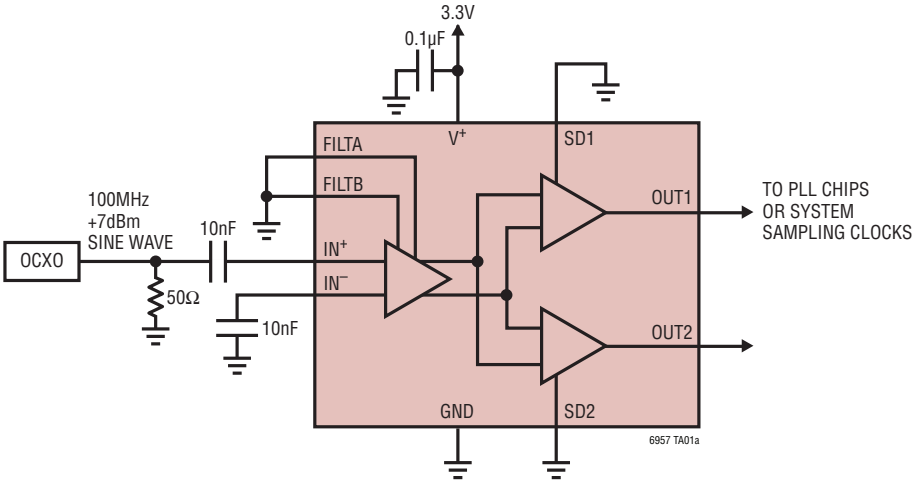
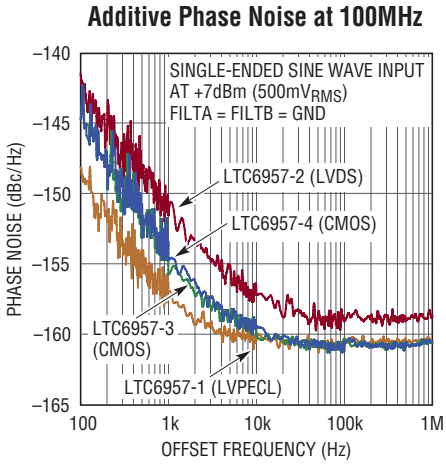
TYPICAL APPLICATION





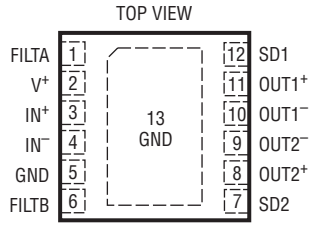
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V^+ or V_{DD}) to GND.....3.6V
Input Current (IN^+, IN^-, FILTA, FILTB, SD1, SD2)
(Note 2) ..... ±10mA
LTC6957-1 Output Current ..... 1mA, –30mA
LTC6957-2 Output Current ..... ±10mA
LTC6957-3, LTC6957-4 Output Current (Note 3).. ±30mA

Specified Temperature Range
LTC6957I .....–40°C to 85°C
LTC6957H.....–40°C to 125°C
Junction Temperature ..... 150°C
Storage Temperature Range .....–65°C to 150°C
Lead Temperature (for MSOP Soldering, 10sec) ... 300°C

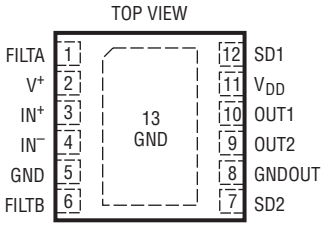
PIN CONFIGURATION

LTC6957-1, LTC6957-2



DD PACKAGE
12-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 58°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

LTC6957-3, LTC6957-4



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12-LEAD (3mm × 3mm) PLASTIC DFN
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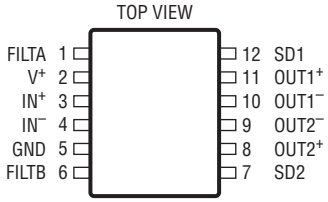
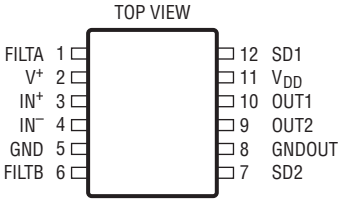
LTC6957-1, LTC6957-2



MS PACKAGE
12-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 145°C/W

LTC6957-3, LTC6957-4



MS PACKAGE
12-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 145°C/W

ORDER INFORMATION

http://www.linear.com/product/LTC6957-1#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6957IDD-1#PBF	LTC6957IDD-1#TRPBF	LFQJ	12-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6957IDD-2#PBF	LTC6957IDD-2#TRPBF	LFQK	12-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6957IDD-3#PBF	LTC6957IDD-3#TRPBF	LFQM	12-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6957IDD-4#PBF	LTC6957IDD-4#TRPBF	LFQN	12-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6957IMS-1#PBF	LTC6957IMS-1#TRPBF	69571	12-Lead Plastic MSOP	–40°C to 85°C
LTC6957HMS-1#PBF	LTC6957HMS-1#TRPBF	69571	12-Lead Plastic MSOP	–40°C to 125°C
LTC6957IMS-2#PBF	LTC6957IMS-2#TRPBF	69572	12-Lead Plastic MSOP	–40°C to 85°C
LTC6957HMS-2#PBF	LTC6957HMS-2#TRPBF	69572	12-Lead Plastic MSOP	–40°C to 125°C
LTC6957IMS-3#PBF	LTC6957IMS-3#TRPBF	69573	12-Lead Plastic MSOP	–40°C to 85°C
LTC6957HMS-3#PBF	LTC6957HMS-3#TRPBF	69573	12-Lead Plastic MSOP	–40°C to 125°C
LTC6957IMS-4#PBF	LTC6957IMS-4#TRPBF	69574	12-Lead Plastic MSOP	–40°C to 85°C
LTC6957HMS-4#PBF	LTC6957HMS-4#TRPBF	69574	12-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS LTC6957-1

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3.3V, SD1 = SD2 = 0.4V, FILTA = FILTB = 0.4V, R_{LOAD} = 50Ω connected to 1.3V, unless otherwise specified. All voltages are with respect to ground.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Inputs (IN^-, IN^+)							
f_{IN}	Input Frequency Range		●			300	MHz
V_{INSE}	Input Signal Level Range, Single-Ended		●	0.2	0.8	2	V_{P-P}
V_{INDIFF}	Input Signal Level Range, Differential		●	0.2	0.8	2	V_{P-P}
t_{MIN}	Minimum Input Pulse Width	High or Low			0.5		ns
V_{INCM}	Self-Bias Voltage, IN^+, IN^-		●	1.8	2.06	2.3	V
R_{IN}	Input Resistance, Differential		●	1.5	2	2.5	kΩ
C_{IN}	Input Capacitance, Differential				0.5		pF
BW_{IN}	Input Section Small Signal Bandwidth (–3dB)	FILTB = L, FILTA = L FILTB = L, FILTA = H FILTB = H, FILTA = L FILTB = H, FILTA = H			1200 500 160 50		MHz MHz MHz MHz
Outputs (LVPECL)							
V_{OH}	Output High Voltage	LTC6957I LTC6957H	● ●	V^+ – 1.22 V^+ – 1.22	V^+ – 0.98 V^+ – 0.98	V^+ – 0.93 V^+ – 0.87	V V
V_{OL}	Output Low Voltage	LTC6957I LTC6957H	● ●	V^+ – 2.1 V^+ – 2.1	V^+ – 1.8 V^+ – 1.8	V^+ – 1.67 V^+ – 1.62	V V
V_{OD}	Output Differential Voltage		●	±660	±810	±965	mV
t_r	Output Rise Time				180		ps
t_f	Output Fall Time				160		ps
t_{PD}	Propagation Delay	FILTB = L, FILTA = L FILTB = L, FILTA = H FILTB = H, FILTA = L FILTB = H, FILTA = H	● ● ● ●	0.35	0.5 0.6 1.1 3.2	0.7 0.8 1.3 4	ns ns ns ns
$\Delta t_{PD}/\Delta T$	Propagation Delay Variation Over Temperature	FILTB = L, FILTA = L FILTB = L, FILTA = H FILTB = H, FILTA = L FILTB = H, FILTA = H	● ● ● ●		0.1 0.1 0.11 0.15		ps/°C ps/°C ps/°C ps/°C
$\Delta t_{PD}/\Delta V$	Propagation Delay Variation vs Supply Voltage	FILTB = L, FILTA = L	●		4	50	ps/V
t_{SKEW}	Output Skew, Differential, CH1 to CH2		●		3	30	ps
t_{MATCH}	Output Matching ($OUTx^+$ to $OUTx^-$)	See Timing Diagram	●		2.5	30	ps
Power							
V^+	V^+ Operating Supply Voltage Range	R_{LOAD} = 50Ω to (V^+– 2V)	●	3.15	3.3	3.45	V
I_S	Supply Current						
	Both Outputs Enabled (SD1 = SD2 = L)	No Output Loads	●		18	22	mA
	One Output Enabled (SD1 = L, SD2 = H or SD1 = H, SD2 = L)	No Output Loads	●		15	19	mA
	Both Outputs Disabled (SD1 = SD2 = H)	No Output Loads	●		0.7	1.2	mA
	Including Output Loads	R_{LOAD} = 50Ω to (V^+– 2V), ×4	●		58	72	mA
t_{ENABLE}	Output Enable Time, Other SDx = L				40		µs
t_{WAKEUP}	Output Enable Time, Other SDx = H				120		µs
$t_{DISABLE}$	Output Disable Time, Other SDx = L				20		µs
t_{SLEEP}	Output Disable Time, Other SDx = H				20		µs

ELECTRICAL CHARACTERISTICS LTC6957-1

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3.3V, SD1 = SD2 = 0.4V, FILTA = FILTB = 0.4V, R_{LOAD} = 50Ω connected to 1.3V, unless otherwise specified. All voltages are with respect to ground.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Logic Inputs							
V_{IH}	High Level SD or FILT Input Voltage		●	V^+ – 0.4			V
V_{IL}	Low Level SD or FILT Input Voltage		●			0.4	V
I_{IN_DIG}	Input Current SD or FILT Pins		●		0.1	±10	µA
Additive Phase Noise and Jitter							
	f_{IN} = 300MHz Sine Wave, 7dBm (FILTA = L, FILTB = L)						
	at 10Hz Offset				–130		dBc/Hz
	at 100Hz Offset				–140		dBc/Hz
	at 1kHz Offset				–150		dBc/Hz
	at 10kHz Offset				–157		dBc/Hz
	at 100kHz Offset				–157.5		dBc/Hz
	>1MHz Offset				–157.5		dBc/Hz
	Jitter (10Hz to 150MHz)				123		fs_{RMS}
	Jitter (12kHz to 20MHz)				45		fs_{RMS}
	f_{IN} = 122.88MHz Sine Wave, 0dBm (FILTA = H, FILTB = L)						
	at 10Hz Offset				–137		dBc/Hz
	at 100Hz Offset				–146		dBc/Hz
	at 1kHz Offset				–154.6		dBc/Hz
	at 10kHz Offset				–157		dBc/Hz
	at 100kHz Offset				–157.2		dBc/Hz
	>1MHz Offset				–157.2		dBc/Hz
	Jitter (10Hz to 61.44MHz)				200		fs_{RMS}
	Jitter (12kHz to 20MHz)				114		fs_{RMS}
	f_{IN} = 100MHz Sine Wave, 10dBm (FILTA = L, FILTB = L)						
	at 10Hz Offset				–138		dBc/Hz
	at 100Hz Offset				–148.1		dBc/Hz
	at 1kHz Offset				–156.8		dBc/Hz
	at 10kHz Offset				–160.6		dBc/Hz
	at 100kHz Offset				–161		dBc/Hz
	>1MHz Offset				–161		dBc/Hz
	Jitter (10Hz to 50MHz)				142		fs_{RMS}
	Jitter (12kHz to 20MHz)				90		fs_{RMS}

ELECTRICAL CHARACTERISTICS LTC6957-2

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3.3V, SD1 = SD2 = 0.4V, FILTA = FILTB = 0.4V, R_{LOAD} = 110Ω differential, unless otherwise specified. All voltages are with respect to ground.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Inputs (IN^-, IN^+)							
f_{IN}	Input Frequency Range		●			300	MHz
V_{INSE}	Input Signal Level Range, Single-Ended		●	0.2	0.8	2	V_{P-P}
V_{INDIFF}	Input Signal Level Range, Differential		●	0.2	0.8	2	V_{P-P}
t_{MIN}	Minimum Input Pulse Width	High or Low			0.5		ns
V_{INCM}	Self-Bias Voltage, IN^+, IN^-		●	1.8	2	2.3	V
R_{IN}	Input Resistance, Differential		●	1.5	2	2.5	kΩ
C_{IN}	Input Capacitance, Differential				0.5		pF
BW_{IN}	Input Section Small Signal Bandwidth	FILTB = L, FILTA = L FILTB = L, FILTA = H FILTB = H, FILTA = L FILTB = H, FILTA = H			1200 500 160 50		MHz MHz MHz MHz
Outputs (LVDS)							
V_{OD}	Output Differential Voltage		●	250	360	450	mV
ΔV_{OD}	Delta V_{OD}		●		0.2	50	mV
V_{OS}	Output Offset Voltage		●	1.125	1.25	1.375	V
ΔV_{OS}	Delta V_{OS}		●		1.5	50	mV
I_{SC}	Short-Circuit Current		●		3.9	6	mA
t_r	Output Rise Time				170		ps
t_f	Output Fall Time				170		ps
t_{PD}	Propagation Delay	FILTB = L, FILTA = L FILTB = L, FILTA = H FILTB = H, FILTA = L FILTB = H, FILTA = H	● ● ● ●	0.65	0.84 0.9 1.35 3.5	1.15 1.3 1.8 4.4	ns ns ns ns
$\Delta t_{PD}/\Delta T$	Propagation Delay Variation Over Temperature	FILTB = L, FILTA = L FILTB = L, FILTA = H FILTB = H, FILTA = L FILTB = H, FILTA = H	● ● ● ●		0.5 0.6 0.7 1.8		ps/°C ps/°C ps/°C ps/°C
$\Delta t_{PD}/\Delta V$	Propagation Delay Variation vs Supply Voltage	FILTB = L, FILTA = L	●		5	60	ps/V
t_{SKEW}	Output Skew, Differential, CH1 to CH2		●		3	50	ps
Power							
V^+	V^+ Operating Supply Voltage Range		●	3.15	3.3	3.45	V
I_S	Supply Current Both Outputs Enabled (SD1 = SD2 = L) One Output Enabled (SD1 = L, SD2 = H or SD1 = H, SD2 = L) Both Outputs Disabled (SD1 = SD2 = H)		 ● ● ●		 38 26 0.7	 45 30 1.2	 mA mA mA
t_{ENABLE}	Output Enable Time, Other SDx = L				300		ns
t_{WAKEUP}	Output Enable Time, Other SDx = H				400		ns
$t_{DISABLE}$	Output Disable Time, Other SDx = L				40		ns
t_{SLEEP}	Output Disable Time, Other SDx = H				50		ns

ELECTRICAL CHARACTERISTICS LTC6957-2

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3.3V, SD1 = SD2 = 0.4V, FILTA = FILTB = 0.4V, R_{LOAD} = 110Ω differential, unless otherwise specified. All voltages are with respect to ground.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Logic Inputs							
V_{IH}	High Level SD or FILT Input Voltage		●	V^+ – 0.4			V
V_{IL}	Low Level SD or FILT Input Voltage		●			0.4	V
I_{IN_DIG}	Input Current SD or FILT Pins		●		0.1	±10	µA
Additive Phase Noise and Jitter							
	f_{IN} = 300MHz Sine Wave, 7dBm (FILTA = L, FILTB = L)						
	10Hz Offset				–124		dBc/Hz
	100Hz Offset				–134		dBc/Hz
	1kHz Offset				–143.5		dBc/Hz
	10kHz Offset				–151.3		dBc/Hz
	100kHz Offset				–154		dBc/Hz
	>1MHz Offset				–154		dBc/Hz
	Jitter (10Hz to 150MHz)				183		fs_{RMS}
	Jitter (12kHz to 20MHz)				67		fs_{RMS}
	f_{IN} = 122.88MHz Sine Wave, 0dBm (FILTA = H, FILTB = L)						
	10Hz Offset				–132.5		dBc/Hz
	100Hz Offset				–142.5		dBc/Hz
	1kHz Offset				–150.7		dBc/Hz
	10kHz Offset				–156		dBc/Hz
	100kHz Offset				–157		dBc/Hz
	>1MHz Offset				–157		dBc/Hz
	Jitter (10Hz to 61.44MHz)				203		fs_{RMS}
	Jitter (12kHz to 20MHz)				116		fs_{RMS}
	f_{IN} = 100MHz Sine Wave, 10dBm (FILTA = L, FILTB = L)						
	10Hz Offset				–132		dBc/Hz
	100Hz Offset				–142		dBc/Hz
	1kHz Offset				–151		dBc/Hz
	10kHz Offset				–157.5		dBc/Hz
	100kHz Offset				–159.5		dBc/Hz
	>1MHz Offset				–159.5		dBc/Hz
	Jitter (10Hz to 50MHz)				169		fs_{RMS}
	Jitter (12kHz to 20MHz)				107		fs_{RMS}

ELECTRICAL CHARACTERISTICS LTC6957-3/LTC6957-4

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. $V^+ = V_{DD}$ = 3.3V, SD1 = SD2 = 0.4V, FILTA = FILTB = 0.4V, R_{LOAD} = 480Ω to $V_{DD}/2$, unless otherwise specified. All voltages are with respect to ground.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Inputs (IN⁻, IN⁺)							
f_{IN}	Input Frequency Range		●			300	MHz
V_{INSE}	Input Signal Level Range, Single-Ended		●	0.2	0.8	2	V_{P-P}
V_{INDIFF}	Input Signal Level Range, Differential		●	0.2	0.8	2	V_{P-P}
t_{MIN}	Minimum Input Pulse Width	High or Low			0.6		ns
V_{INCM}	Self-Bias Voltage, IN^+, IN^-		●	1.8	2	2.3	V
R_{IN}	Input Resistance, Differential		●	1.5	2	2.5	kΩ
C_{IN}	Input Capacitance, Differential				0.5		pF
BW_{IN}	Input Section Small Signal Bandwidth	FILTB = L, FILTA = L FILTB = L, FILTA = H FILTB = H, FILTA = L FILTB = H, FILTA = H			1200 500 160 50		MHz MHz MHz MHz
Outputs (CMOS)							
V_{OH}	Output High Voltage	No Load –3mA Load	● ●	V_{DD} – 0.1 V_{DD} – 0.2			V V
V_{OL}	Output Low Voltage	No Load 3mA Load	● ●			0.1 0.2	V V
t_r	Output Rise Time				320		ps
t_f	Output Fall Time				300		ps
t_{PD}	Propagation Delay	FILTB = L, FILTA = L FILTB = L, FILTA = H FILTB = H, FILTA = L FILTB = H, FILTA = H	● ● ● ●	0.8	0.95 1 1.5 3.6	1.6 1.8 2.4 4.8	ns ns ns ns
$\Delta t_{PD}/\Delta T$	Propagation Delay Variation Over Temperature	FILTB = L, FILTA = L FILTB = L, FILTA = H FILTB = H, FILTA = L FILTB = H, FILTA = H	● ● ● ●		1.7 1.7 2 3		ps/°C ps/°C ps/°C ps/°C
$\Delta t_{PD}/\Delta V$	Propagation Delay Variation vs Supply Voltage	FILTB = FILTA = L, $V^+ = V_{DD}$	●		100	200	ps/V
t_{SKEW}	Output Skew, CH1 to CH2 LTC6957-3 LTC6957-4		 ● ●		 5 120	 35 250	 ps ps
Power							
V^+	V^+ Operating Supply Voltage Range		●	3.15	3.3	3.45	V
V_{DD}	V_{DD} Operating Supply Voltage Range	V_{DD} Must Be ≤V^+	●	2.4	3.3	3.45	V
I_S	Supply Current, Pin 2 Both Outputs Enabled (SD1 = SD2 = L) One Output Enabled (SD1 = L, SD2 = H or SD1 = H, SD2 = L) Both Outputs Disabled (SD1 = SD2 = H)		 ● ● ●		 24 24 0.7	 27.5 27.5 1.2	 mA mA mA
I_{DD}	Supply Current, Pin 11, No Load	Static Dynamic, per Output	● ●		0.001 0.056	0.01 0.07	mA mA/MHz
t_{ENABLE}	Output Enable Time, Other SDx = L				200		ns
t_{WAKEUP}	Output Enable Time, Other SDx = H				300		ns
$t_{DISABLE}$	Output Disable Time, Other SDx = L				20		ns
t_{SLEEP}	Output Disable Time, Other SDx = H				20		ns

ELECTRICAL CHARACTERISTICS LTC6957-3/LTC6957-4

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. $V^+ = V_{DD}$ = 3.3V, SD1 = SD2 = 0.4V, FILTA = FILTB = 0.4V, R_{LOAD} = 480Ω to $V_{DD}/2$, unless otherwise specified. All voltages are with respect to ground.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Logic Inputs							
V_{IH}	High Level SD or Filt Input Voltage		●	V^+ – 0.4			V
V_{IL}	Low Level SD or Filt Input Voltage		●			0.4	V
I_{IN_DIG}	Input Current SD or Filt Pins		●		0.1	±10	µA
Additive Phase Noise and Jitter							
	f_{IN} = 300MHz Sine Wave, 7dBm (FILTA = L, FILTB = L)						
	10Hz Offset				–123		dBc/Hz
	100Hz Offset				–133		dBc/Hz
	1kHz Offset				–143		dBc/Hz
	10kHz Offset				–152		dBc/Hz
	100kHz Offset				–156		dBc/Hz
	>1MHz Offset				–156		dBc/Hz
	Jitter (10Hz to 150MHz)				146		fs_{RMS}
	Jitter (12kHz to 20MHz)				53		fs_{RMS}
	f_{IN} = 122.88MHz Sine Wave, 0dBm (FILTA = H, FILTB = L)						
	10Hz Offset				–132		dBc/Hz
	100Hz Offset				–142		dBc/Hz
	1kHz Offset				–150.6		dBc/Hz
	10kHz Offset				–156.5		dBc/Hz
	100kHz Offset				–157.4		dBc/Hz
	>1MHz Offset				–157.4		dBc/Hz
	Jitter (10Hz to 61.44MHz)				192		fs_{RMS}
	Jitter (12kHz to 20MHz)				109		fs_{RMS}
	f_{IN} = 100MHz Sine Wave, 10dBm (FILTA = L, FILTB = L)						
	10Hz Offset				–135		dBc/Hz
	100Hz Offset				–145		dBc/Hz
	1kHz Offset				–153		dBc/Hz
	10kHz Offset				–159.8		dBc/Hz
	100kHz Offset				–161		dBc/Hz
	>1MHz Offset				–161		dBc/Hz
	Jitter (10Hz to 50MHz)				142		fs_{RMS}
	Jitter (12kHz to 20MHz)				90		fs_{RMS}

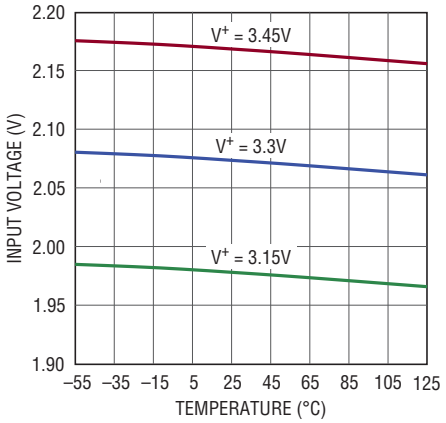
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Input pins IN^+, IN^-, FILTA, FILTB, SD1 and SD2 are protected by steering diodes to either supply. If the inputs go beyond either supply rail, the input current should be limited to less than 10mA. If pushing current into FILTB, the Pin 6 voltage must be limited to 4V. On the logic pins (FILTA, FILTB, SD1 and SD2) the Absolute Maximum input current applies only at the maximum operating supply voltage of 3.45V; 10mA of input current with the absolute maximum supply voltage of 3.6V may create permanent damage from voltage stress.

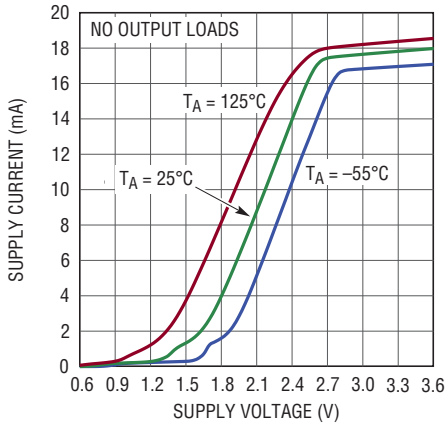
Note 3: With 3.6V Absolute Maximum supply voltage, the LTC6957-3/LTC6957-4 CMOS outputs can sink 30mA while low, and source 30mA while high without damage. However, if overdriven or subject to an inductive load kick outside the supply rails, 30mA can create damaging voltage stress and is not guaranteed unless V_{DD} is limited to 3.15V.

TYPICAL PERFORMANCE CHARACTERISTICS LTC6957-1

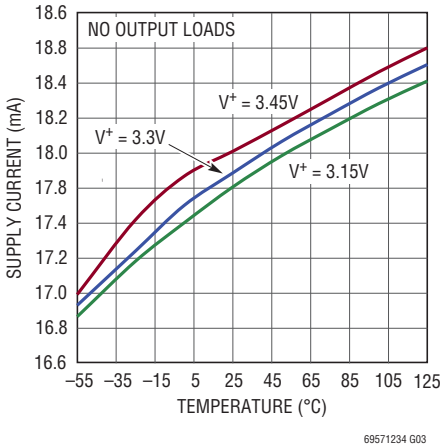
Input Self Bias Voltage vs Temperature



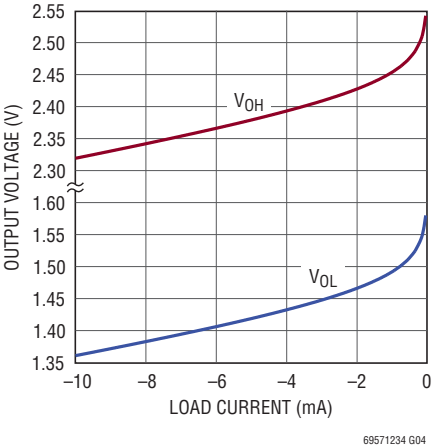
Supply Current vs Supply Voltage



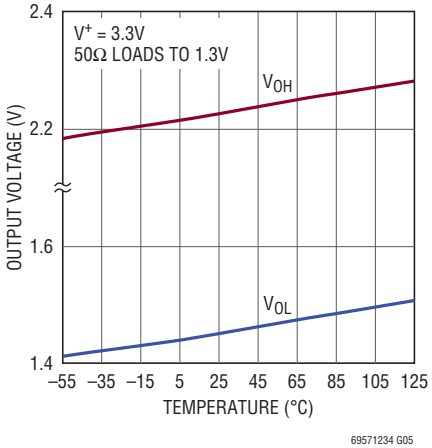
Supply Current vs Temperature



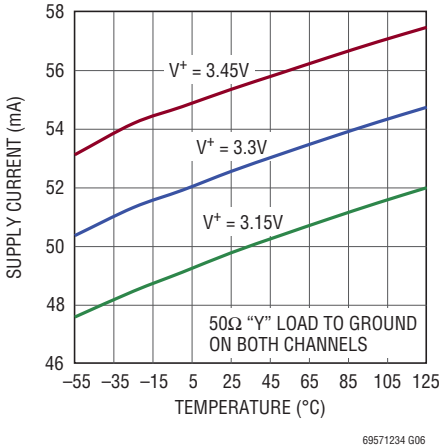
Output Voltage vs Load Current



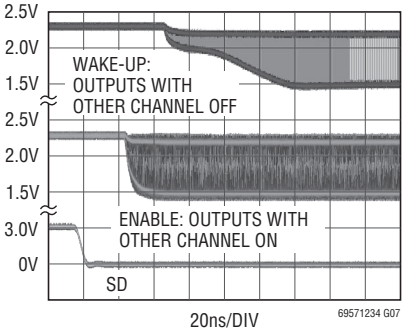
Output Voltage vs Temperature



Supply Current vs Temperature

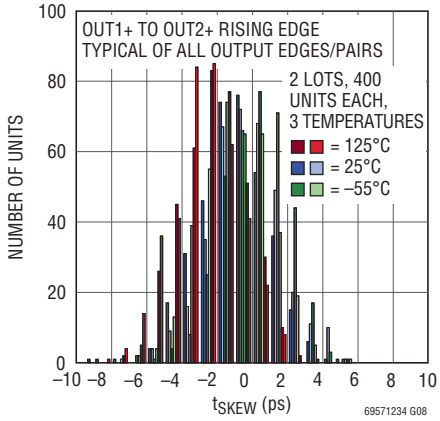


Enable and Wakeup



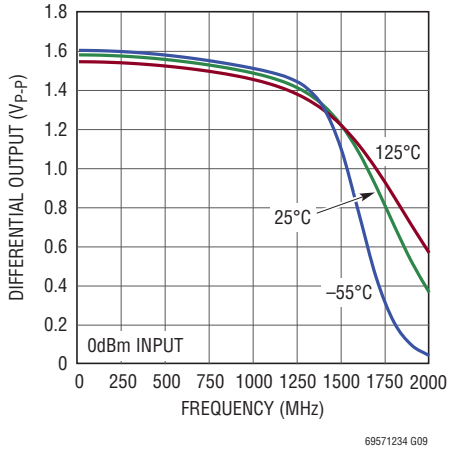
MULTIPLE EXPOSURES, PERSISTENCE MODE
CLOCK I/O = 120MHz
SD DRIVE ~ 140kHz, ASYNCHRONOUS

Typical Distribution of Skew



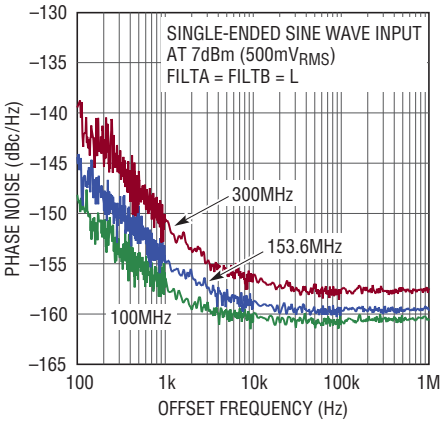
PRODUCTION DATA,
1ps RESOLUTION, ~1-2ps UNCERTAINTY

Differential Output vs Frequency

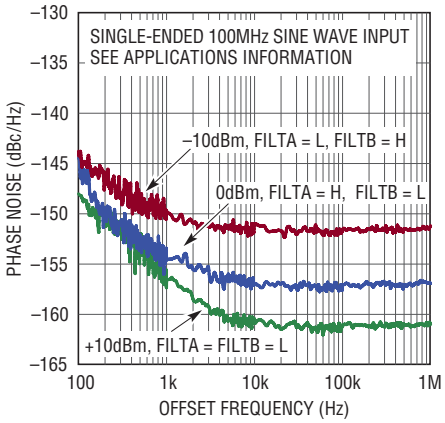


TYPICAL PERFORMANCE CHARACTERISTICS LTC6957-1

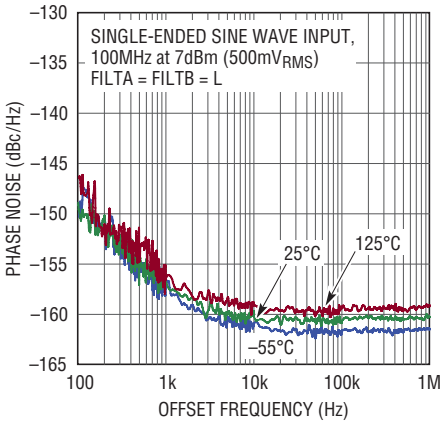
Additive Phase Noise vs Input Frequency



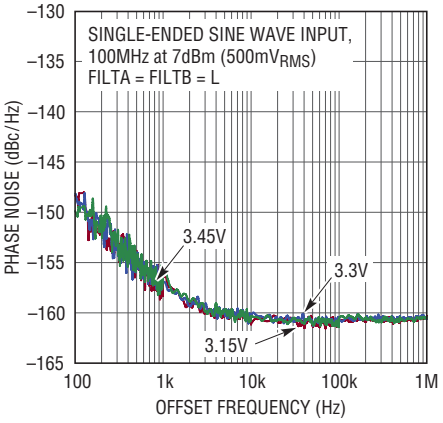
Additive Phase Noise vs Amplitude



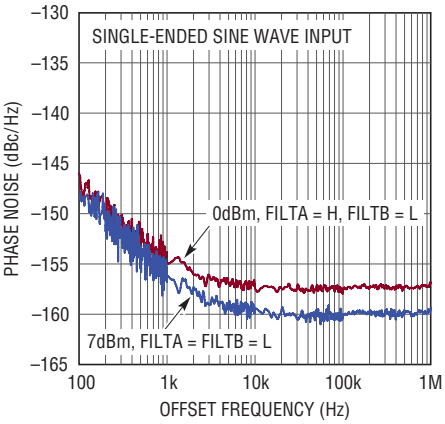
Additive Phase Noise vs Temperature



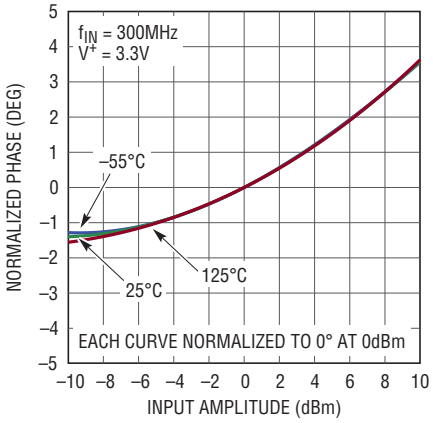
Additive Phase Noise vs Supply Voltage



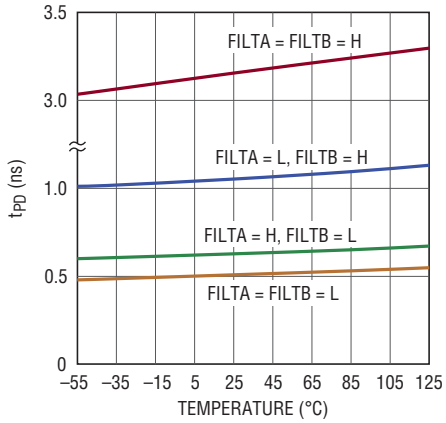
Additive Phase Noise at 122.88MHz



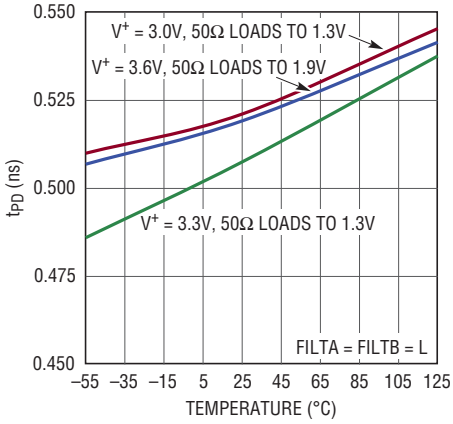
AM to PM Conversion



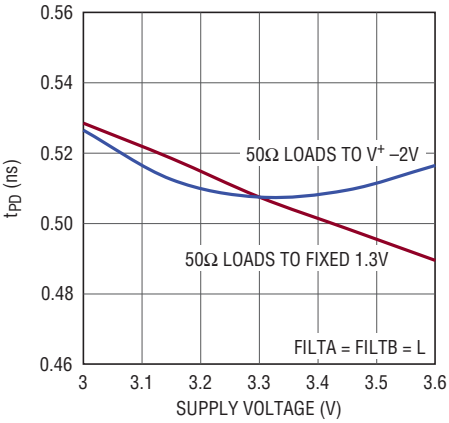
t_{PD} vs Temperature



t_{PD} vs Temperature

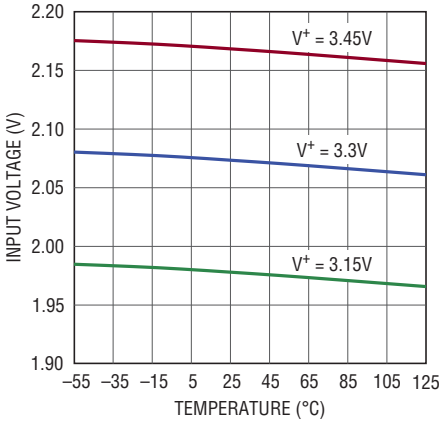


t_{PD} vs Supply Voltage and Termination Voltage

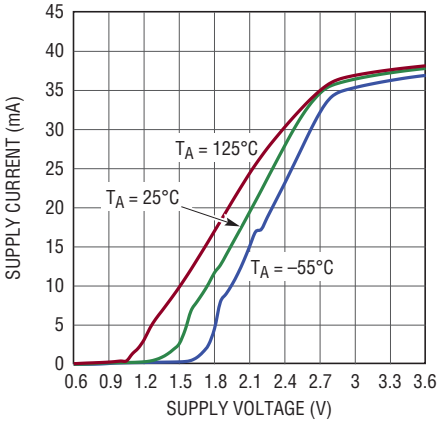


TYPICAL PERFORMANCE CHARACTERISTICS LTC6957-2

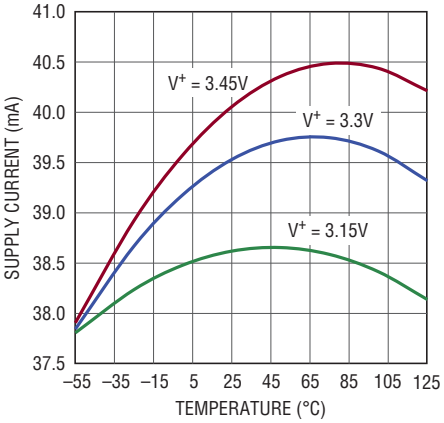
Input Self Bias Voltage vs Temperature



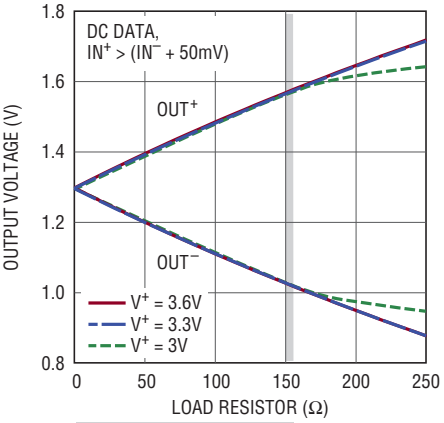
Supply Current vs Supply Voltage



Supply Current vs Temperature

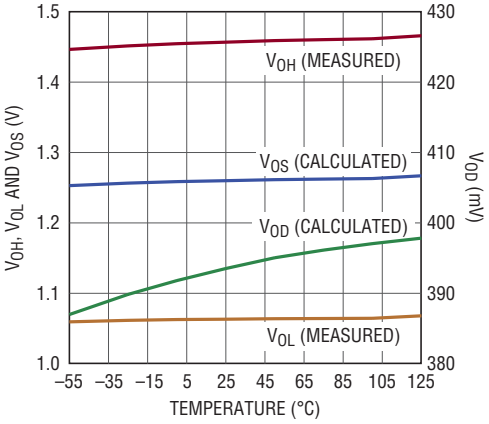


Output Voltages vs Load Resistor

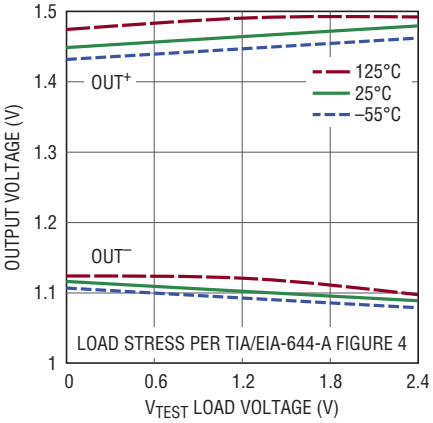


USE OF R_{LOAD} > 150Ω
NOT RECOMMENDED
f_{IN} MAY BE COMPROMISED

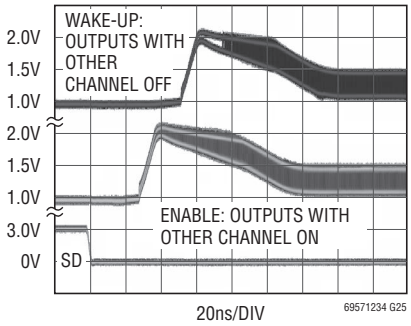
Output Voltages vs Temperature



Output Voltages vs Loading

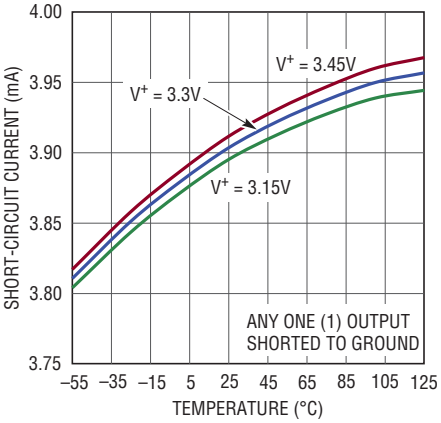


Enable and Wakeup

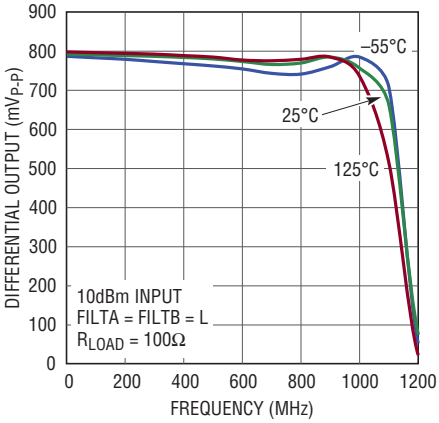


MULTIPLE EXPOSURES, PERSISTENCE MODE
CLOCK I/O = 120MHz
SD DRIVE ~ 140kHz, ASYNCHRONOUS

Output Short-Circuit Current vs Temperature

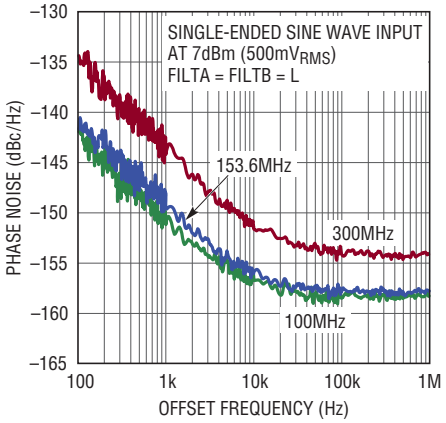


Differential Output vs Frequency

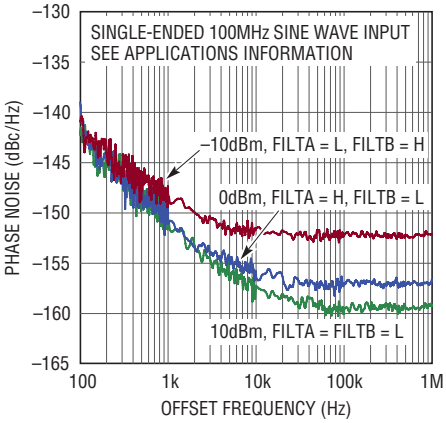


TYPICAL PERFORMANCE CHARACTERISTICS LTC6957-2

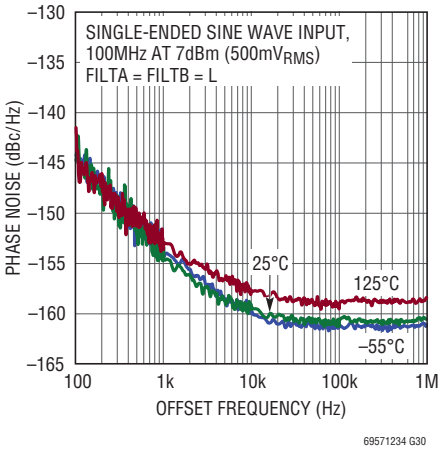
Additive Phase Noise vs Input Frequency



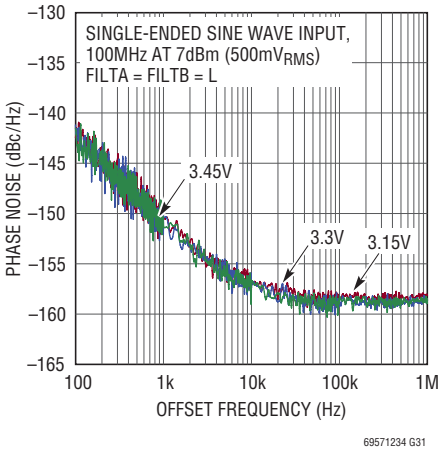
Additive Phase Noise vs Amplitude



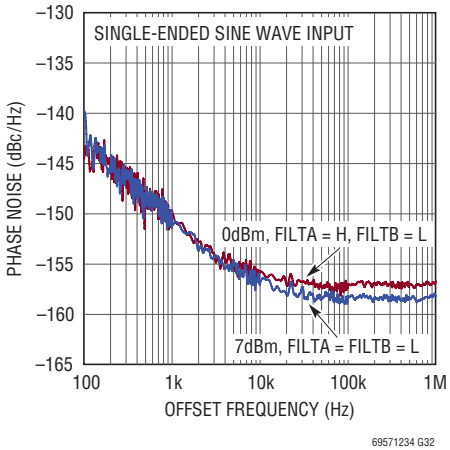
Additive Phase Noise vs Temperature



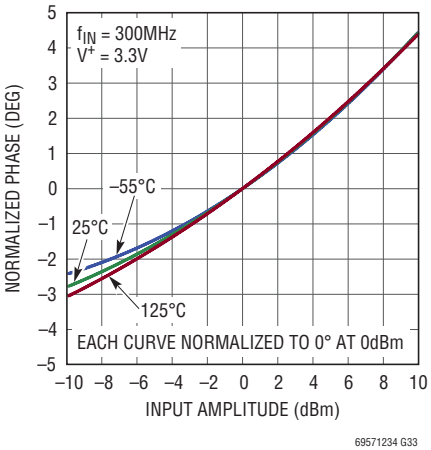
Additive Phase Noise vs Supply Voltage



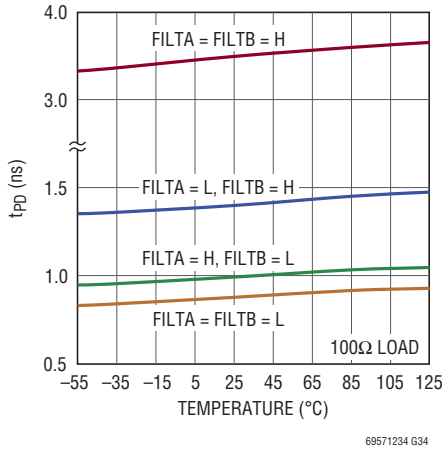
Additive Phase Noise at 122.88MHz



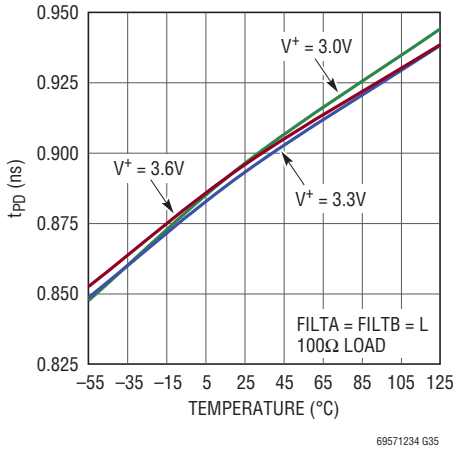
AM to PM Conversion



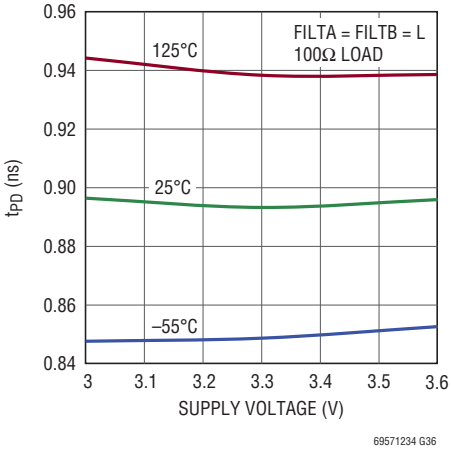
t_{PD} vs Temperature



t_{PD} vs Temperature

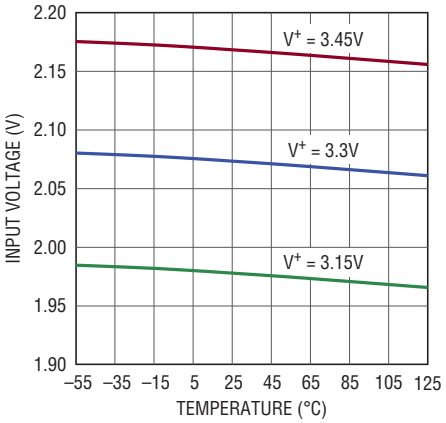


t_{PD} vs Supply Voltage



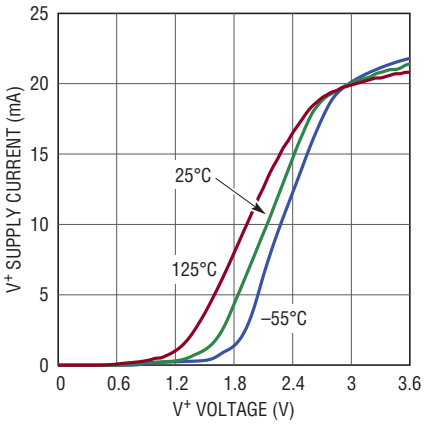
TYPICAL PERFORMANCE CHARACTERISTICS LTC6957-3/LTC6957-4

Input Self Bias Voltage vs Temperature



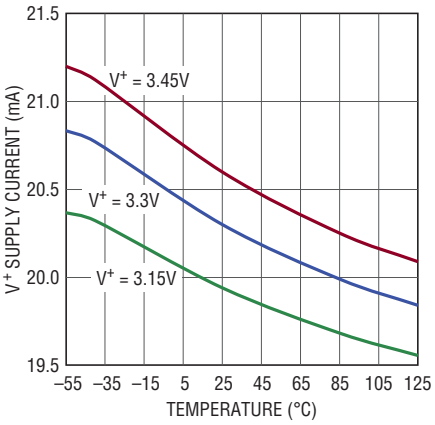
69571234 G37

Supply Current vs Supply Voltage



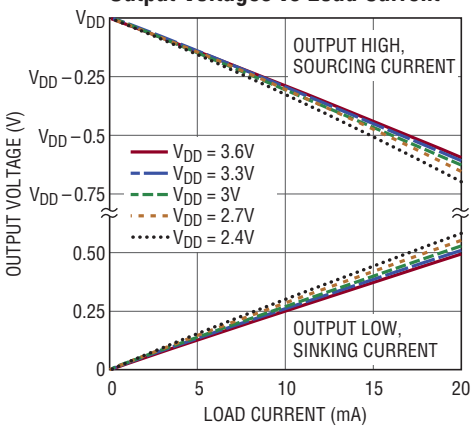
69571234 G38

Supply Current vs Temperature



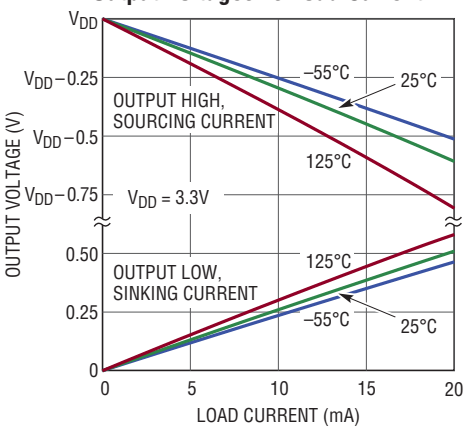
69571234 G39

Output Voltages vs Load Current



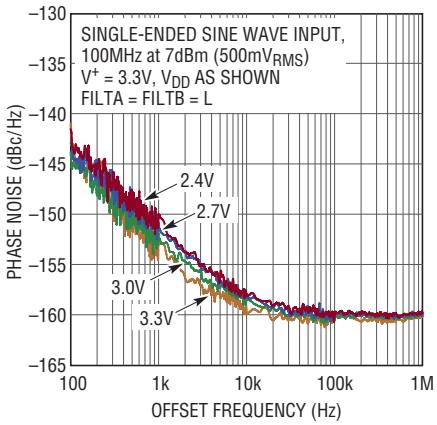
69571234 G40

Output Voltages vs Load Current



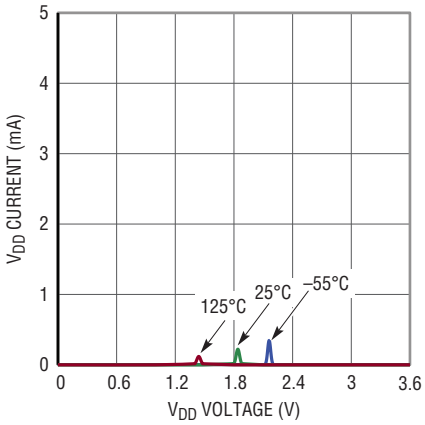
69571234 G41

Additive Phase Noise vs Supply Voltage



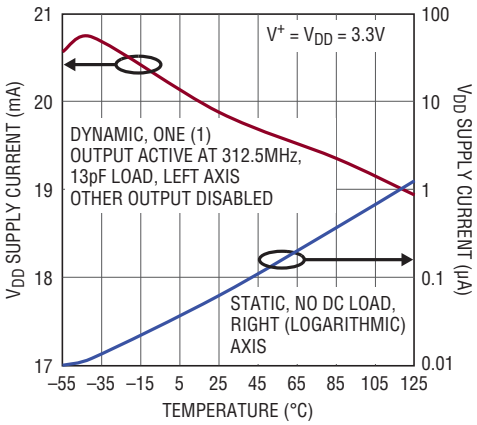
69571234 G42

Supply Current vs Supply Voltage



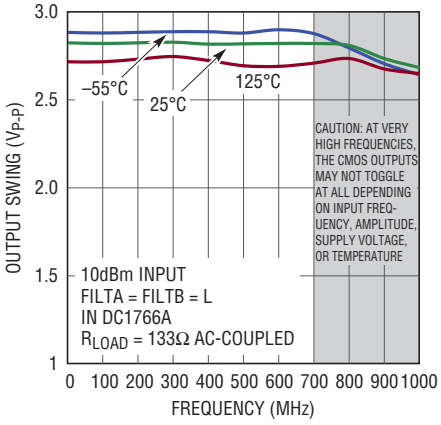
69571234 G43

Supply Current vs Temperature



69571234 G44

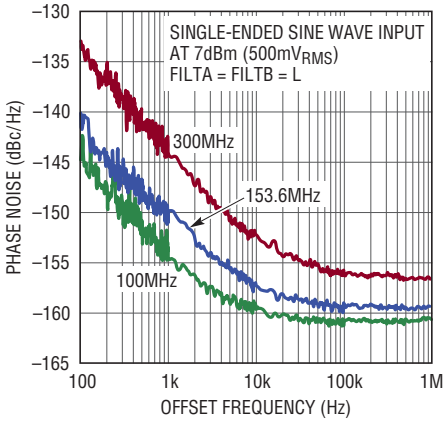
Output Voltage Swing vs Frequency



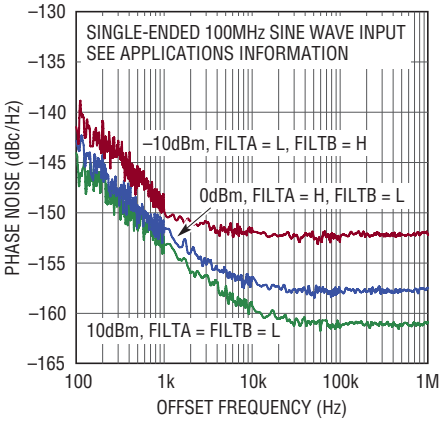
69571234 G45

TYPICAL PERFORMANCE CHARACTERISTICS LTC6957-3/LTC6957-4

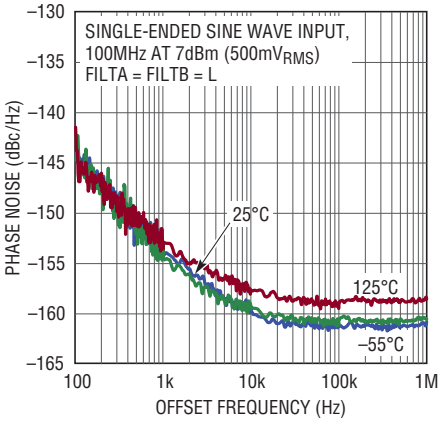
Additive Phase Noise vs Input Frequency



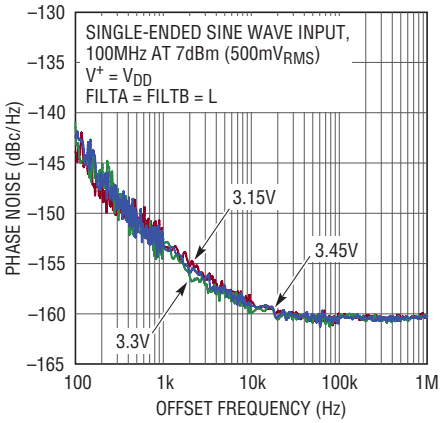
Additive Phase Noise vs Amplitude



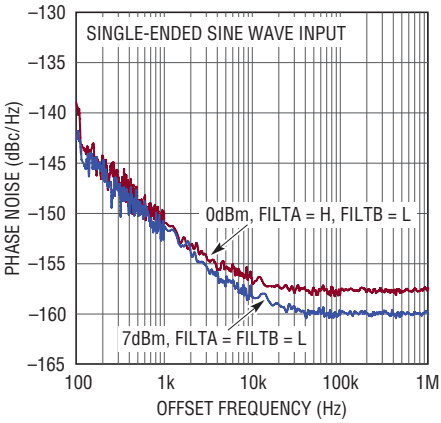
Additive Phase Noise vs Temperature



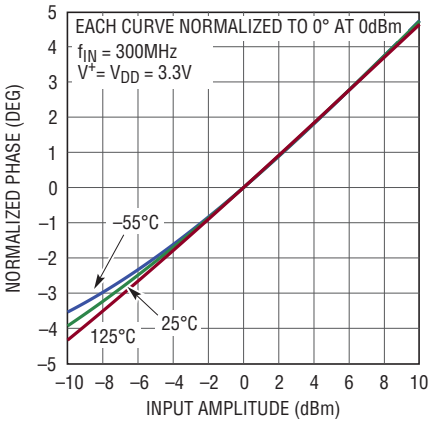
Additive Phase Noise vs Supply Voltage



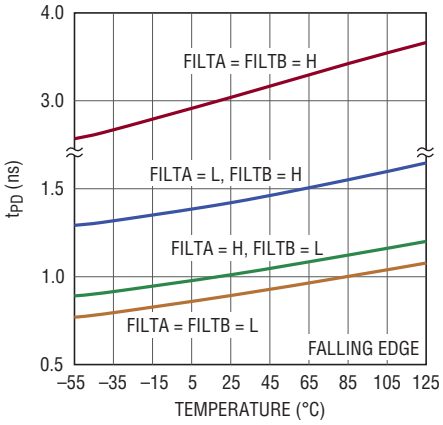
Additive Phase Noise at 122.88MHz



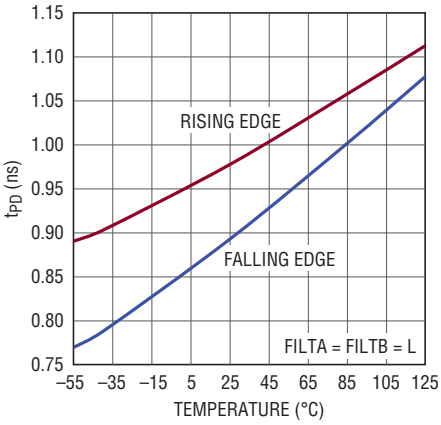
AM to PM Conversion



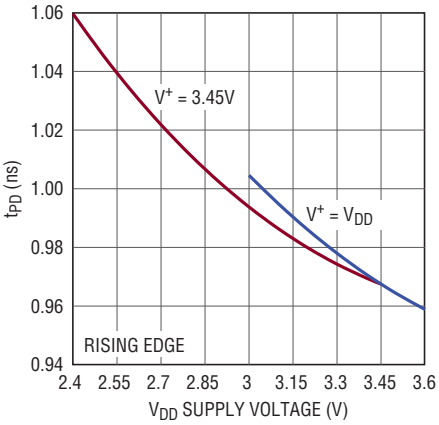
t_{PD} vs Temperature



t_{PD} vs Temperature



t_{PD} vs Supply Voltage



PIN FUNCTIONS

FILTA, FILTB (Pin 1, Pin 6): Input Bandwidth Limiting Control. These CMOS logic inputs control the bandwidth of the early amplifier stages. For slow slewing signals substantially lower phase noise is achieved by using this feature. See the Applications Information section for more details.

V^+ (Pin 2): Supply Voltage (3.15V to 3.45V). This supply must be kept free from noise and ripple. It should be bypassed directly to GND (Pin 5) with a 0.1µF capacitor.

IN^+, IN^- (Pin 3, Pin 4): Input Signal Pins. These inputs are differential, but can also interface with single-ended signals. The input can be a sine wave signal or a CML, LVPECL, TTL or CMOS logic signal. See the Applications Information section for more details.

GND (Pin 5): Ground. Connect to a low inductance ground plane for best performance. The connection to the bypass capacitor for V^+ (Pin 2) should be through a direct, low inductance path.

SD1, SD2 (Pin 12, Pin 7): Output Enable Control. These CMOS logic inputs control the enabling and disabling of their respective OUT1 and OUT2 outputs. When both outputs are disabled, the LTC6957 is placed in a low power shutdown state.

LTC6957-1 Only

$OUT1^-$, $OUT1^+$ (Pin 10, Pin 11): LVPECL Outputs. Differential logic outputs typically terminated by 50Ω connected to a supply 2V below the V^+ supply. Refer to the Applications Information section for more details.

$OUT2^-$, $OUT2^+$ (Pin 9, Pin 8): LVPECL Outputs. Differential logic outputs typically terminated by 50Ω connected to a supply 2V below the V^+ supply. Refer to the Applications Information section for more details.

LTC6957-2 Only

$OUT1^-$, $OUT1^+$ (Pin 10, Pin 11): LVDS Outputs, Mostly TIA/EIA-644-A Compliant. Refer to the Applications Information section for more details.

$OUT2^-$, $OUT2^+$ (Pin 9, Pin 8): LVDS Outputs, Mostly TIA/EIA-644-A Compliant. Refer to the Applications Information section for more details.

LTC6957-3/LTC6957-4 Only

OUT1, OUT2 (Pin 10, Pin 9): CMOS Outputs. Refer to the Applications Information section for more details.

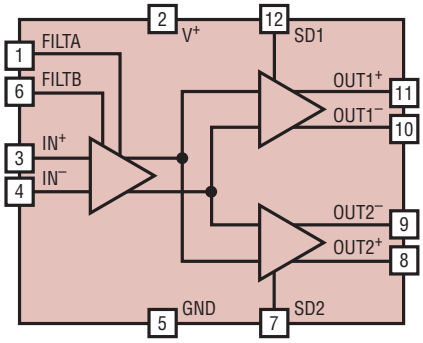
V_{DD} (Pin 11): Output Supply Voltage (2.4V to 3.45V). For best performance connect this to the same supply as V^+ (Pin 2). If the output needs to be a lower logic rail, this supply can be separately connected, but this voltage must be less than or equal to that on Pin 2 for proper operation. This supply must also be kept free from noise and ripple. It should be bypassed directly to the GNDOUT pin (Pin 8) with a 0.1µF capacitor.

GNDOUT (Pin 8): Output Logic Ground. Tie to a low inductance ground plane for best performance. The connection to the bypass capacitor for V_{DD} (Pin 11) should be through a direct, low inductance path.

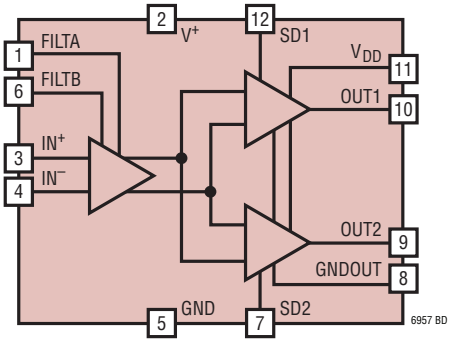
LTC6957-xDD Only

Exposed Pad (Pin 13): Always tie the underlying DFN exposed pad to GND (Pin 5). To achieve the rated θ_{JA} of the DD package, there should be good thermal contact to the PCB.

BLOCK DIAGRAMS

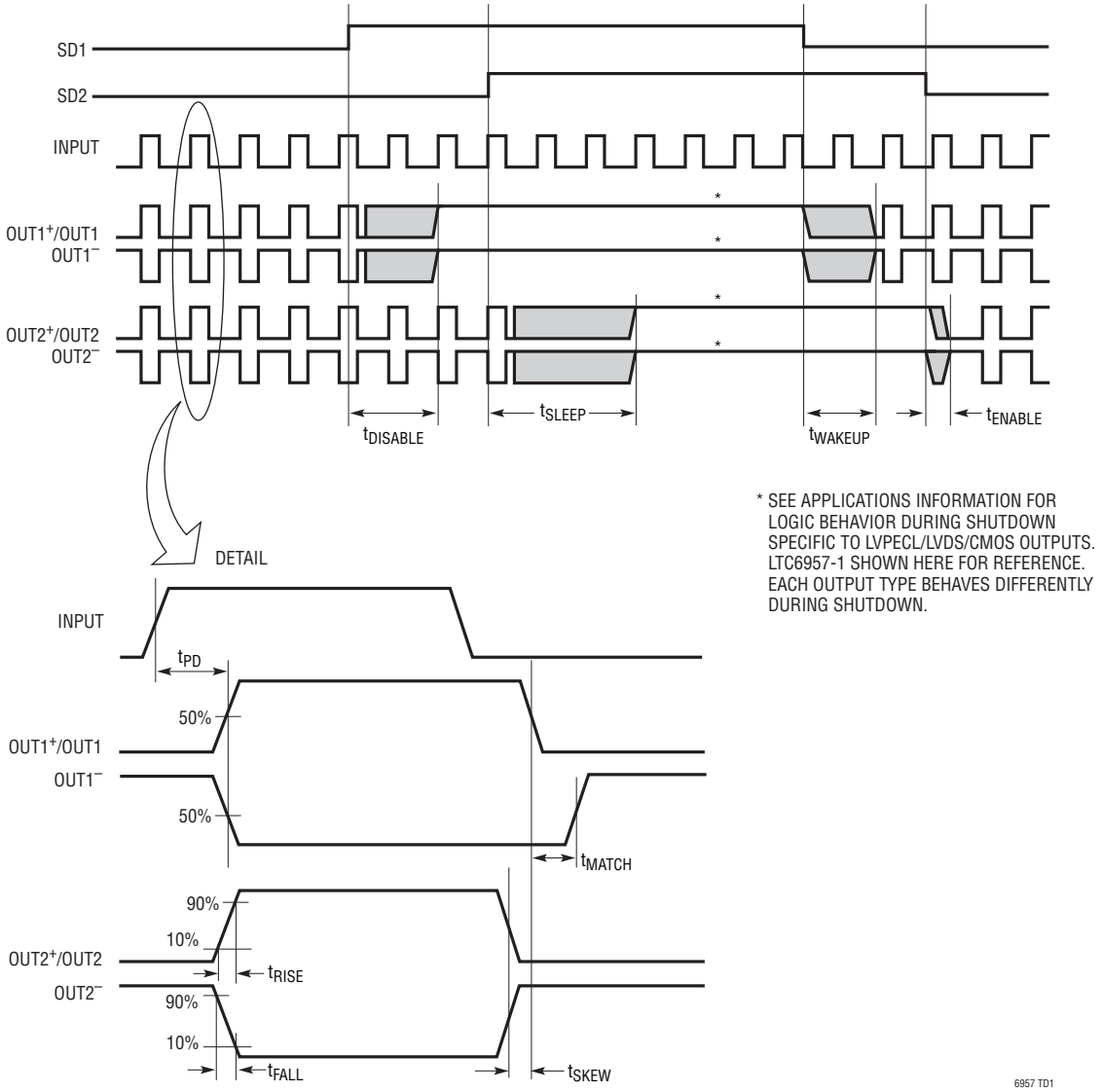


LTC6957-1 and LTC6957-2



LTC6957-3 and LTC6957-4

TIMING DIAGRAM



* SEE APPLICATIONS INFORMATION FOR LOGIC BEHAVIOR DURING SHUTDOWN SPECIFIC TO LVPECL/LVDS/CMOS OUTPUTS. LTC6957-1 SHOWN HERE FOR REFERENCE. EACH OUTPUT TYPE BEHAVES DIFFERENTLY DURING SHUTDOWN.

APPLICATIONS INFORMATION

General Considerations

The LTC6957-1/LTC6957-2/LTC6957-3/LTC6957-4 are low noise, dual output clock buffers that are designed for demanding, low phase noise applications. Properly applied, they can preserve phase noise performance in situations where alternative solutions would degrade the phase noise significantly. They are also useful as logic converters.

However, no buffer device is capable of removing or reducing phase noise present on an input signal. As with most low phase noise circuits, improper application of the LTC6957-1/LTC6957-2/LTC6957-3/LTC6957-4 can result in an increase in the phase noise through a variety of mechanisms. The information below will, hopefully, allow a designer to avoid such an outcome.

The LTC6957 is designed to be used with high performance clock signals destined for driving the encode inputs of ADCs or mixer inputs. Such clocks should not be treated as digital signals. The beauty of digital logic is that there is noise margin both in the voltage and the timing, before any deleterious effects are noticed. In contrast, high performance clock signals have no margin for error in the timing before the system performance is degraded. Users are encouraged to keep this distinction in mind while designing the entire clocking signal chain before, during, and after the LTC6957.

Input Interfacing

The input stage is the same for all versions of the LTC6957 and is designed for low noise and ease of interfacing to sine-wave and small amplitude signals. Other logic types can interface directly, or with little effort since they present a smaller challenge for noise preservation.

Figure 1 shows a simplified schematic of the LTC6957 input stage. The diodes are all for protection, both during ESD events and to protect the low noise NPN devices from being damaged by input overdrive.

The resistors are to bias the input stage at an optimal DC level, but they are too large to leave floating without increasing the noise. Therefore, for low noise use, always connect both inputs to a low AC impedance. A capacitor to ground/return is imperative on the unused input in single-ended applications.

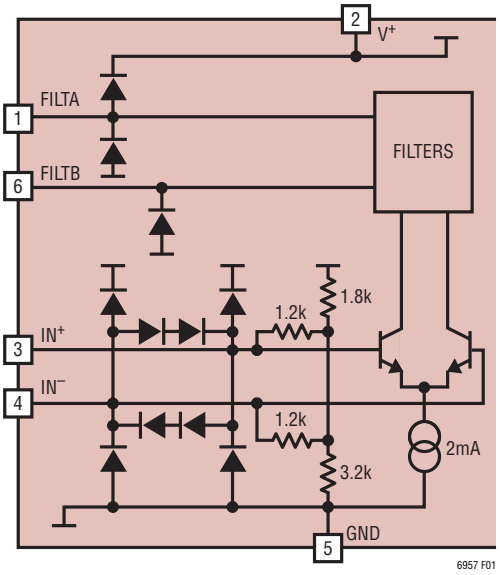


Figure 1

APPLICATIONS INFORMATION

Figure 2a shows how to interface single-ended LVPECL logic to the LTC6957, while Figure 2b shows how to drive the LTC6957 with differential LVPECL signals. The capacitors shown are 10nF and can be inexpensive ceramics, preferably in small SMT cases. For use above 100MHz, lower value capacitors may be desired to avoid series resonance, which could increase the noise in Figure 2a even though the capacitor is just on the DC input. This comment applies to all capacitors hooked to the inputs throughout this data sheet.

In Figure 2a, the R_{TERM} implementation is up to the user and is to terminate the transmission line. If it is connected to a V_{TT} that is passively generated and heavily bypassed to ground, the 10nF to ground shown on the inverting LTC6957 input is the appropriate connection to use. However, if the termination goes to an actively generated V_{TT} voltage, lower noise may be achieved by connecting the capacitor on the inverting input to that V_{TT} rather than ground.

In Figure 2b, both inputs to the LTC6957 are driven, increasing the differential input signal size and minimizing noise from any common mode source such as V_{TT}, both of which improve the achievable phase noise.

A variety of termination techniques can be used, and as long as the two sides use the same termination, the configuration used won't matter much. In Figure 2b, the R_{TERM}s are shown in a "Y" configuration that creates a passive V_{TT} at the common point. Most 3.3V LVPECL devices have differential outputs and can be terminated with three 50Ω resistors as shown.

Figure 3 shows a 50Ω RF signal source interface to the LTC6957. For a pure tone (sine wave) input, Figure 3 can handle up to 10dBm maximum. A broadband 50Ω match as shown should suffice for most applications, though for small amplitude input signals a narrow band reactive matching network may offer incremental improvements in performance.

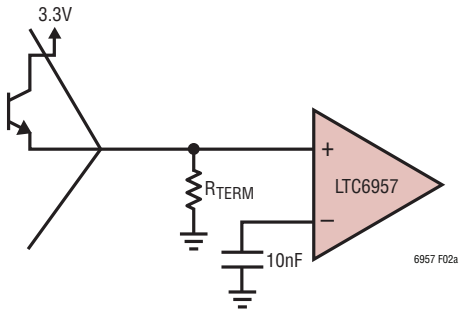


Figure 2a. Single-Ended LVPECL Input

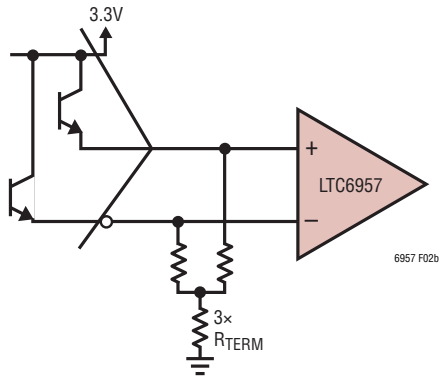


Figure 2b. Differential LVPECL Input

Figure 2

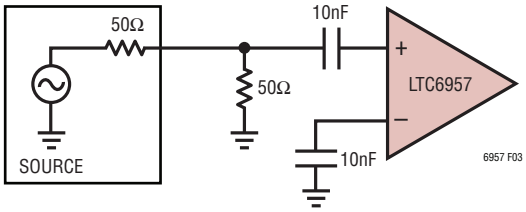


Figure 3. Single-Ended 50Ω Input Source

APPLICATIONS INFORMATION

Figure 4 shows the interface between current mode logic (CML) signals and the LTC6957 inputs. The specifics of terminating will be dependent on the particular CML driver used; Figure 4 shows terminations only at the load end of the line, but the same LTC6957 interface is appropriate for applications with the source end of the line also terminated. In Figure 4a, a differential signal interface to the LTC6957 is shown, which must be AC-coupled due to the DC input levels required at the LTC6957.

Figure 4b shows a single-ended CML signal driving the LTC6957. This is not commonly used because of noise and immunity weaknesses compared to the differential CML case. Because the signal is created by a current pulled through the termination resistor, the signal is inherently referenced to the supply voltage to which R_{TERM} is tied. For that reason, the other LTC6957 should be AC-referenced to that supply voltage as shown.

The polarity change shown here is for graphic clarity only, and can be reversed by swapping the LTC6957 input terminals.

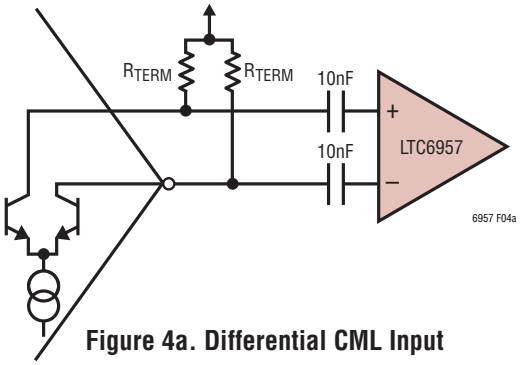


Figure 4a. Differential CML Input

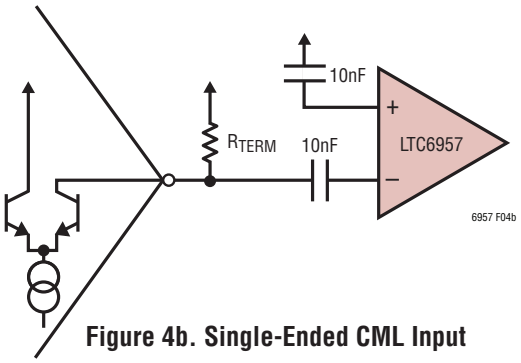


Figure 4b. Single-Ended CML Input

Figure 4

APPLICATIONS INFORMATION

Figure 5 shows the LTC6957 being driven by an LVDS (EIA-644-A) signal pair. This is simply a matter of differentially terminating the pair and AC-coupling as shown into the LTC6957 whose DC common mode voltage is incompatible with the LVDS standard.

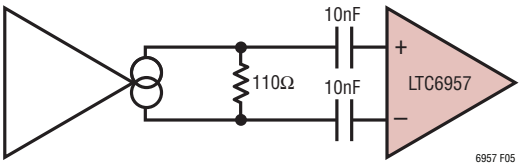


Figure 5. LVDS Input

The choice of 110Ω versus 100Ω termination is arbitrary (the EIA-644-A standard allows 90Ω to 132Ω) and should be made to match the differential impedance of the trace pair. The termination and AC-coupling elements should be located as close as possible to the LTC6957.

If DC-coupling is desired, for example to control the LTC6957 output phasing during times the LVDS input clocks will be halted, a pair of 3k resistors can parallel the two capacitors in Figure 5. An EIA/TIA-644-A compliant driver can drive this load, which is less load stress than specification 4.1.1. The differential voltage into the LTC6957 when clocked (>100kHz) will be full LVDS levels. When the clocks stop, the DC differential voltage created by the resistors and the 1.2k internal resistors (Figure 1) will be 100mV, still sufficient to assure the desired LTC6957 output polarity. Choosing the smallest capacitors needed for phase noise performance will minimize the settling transients when the clocks restart.

Interfacing with CMOS Logic

The logic families discussed and illustrated to this point are generally a better choice for routing and distributing low phase-noise reference/clock signals than is CMOS logic. All of the logic types shown so far are well suited for use with low impedance terminations. Most of the time there is a differential signal when using LVPECL or CML, and LVDS always has a differential signal. Differential signals provide lots of margin for error when it comes to picking up noise and interference that can corrupt a reference clock.

CMOS on the other hand cannot drive 50Ω loads, is usually routed single-ended, and by its nature is coupled to the potentially noisy supply voltage half the time.

The LTC6957-3/LTC6957-4 provide CMOS outputs, so it may seem surprising to read herein that CMOS is a poor choice for low phase noise applications. However, these devices should prove useful for designers that recognize the challenges and limitations of using CMOS signals for low phase noise applications. See the CMOS Outputs of the LTC6957-3/LTC6957-4 section for further information.

The best method for driving the LTC6957 with CMOS signals would be to provide differential drive, but if that is not available, there are few ways to create a differential CMOS signal without running the risk of corrupting the skew or creating other problems. Therefore, single-ended CMOS signals are the norm and care must be taken when using this to drive the LTC6957.

The primary concern is that all routing should be terminated to minimize reflections. With CMOS logic there is usually plenty of signal (more than the LTC6957 can handle without attenuation) and the amplitude of the LTC6957 input signal will generally be of secondary importance compared to avoiding the deleterious effects of signal reflections. The primary concern about terminations is that the input waveform presented to the LTC6957 should have full speed slewing at the all important transitions. If a rising edge is slowed by the destructive addition of the ringing/settling of a prior edge reflection, or even the start of the current edge, the phase noise performance will suffer. This is true for all logic types, but is particularly problematic when using CMOS because of the fast slew rates and because it does not naturally lend itself to clean terminations.

Point-to-point routing is best, and care should be taken to avoid daisy-chain routing, because the terminated end may be the only point along the line that sees clean transitions. Earlier loads may even see a dwell in the transition region which will greatly degrade phase noise performance.

APPLICATIONS INFORMATION

Figure 6 shows a suggested CMOS to LTC6957 interface. The transmission line shown is the PCB trace and the component values are for a characteristic impedance of 50Ω, though they could be scaled up or down for other values of Z0. The R1/R2 divider at the CMOS output cuts the Thevenin voltage in half when the Z_{OUT} of the driver is included. More importantly, it drives the transmission line with a Thevenin driving resistance of 50Ω, matching the Z0 of the line. On the other end of the line, a 50Ω load is presented, minimizing reflections. This results in a second 2:1 attenuation in voltage, so the LTC6957 input will be approximately $800mV_{P-P}$ with 3V CMOS; $1.25V_{P-P}$ with 5V and $600mV_{P-P}$ with 2.5V. All of these levels are less than the maximum input swing of $2V_{P-P}$ yet with clean edges and fast slew rates should be able to realize the full phase noise performance of the LTC6957.

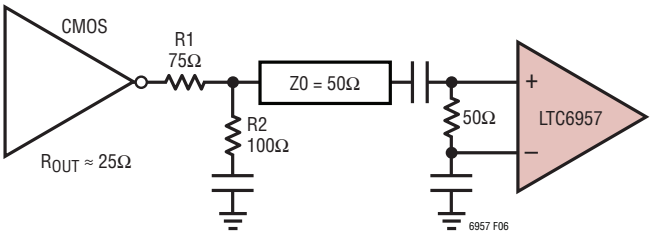


Figure 6. CMOS Input

The various capacitors are for AC-coupling and should have Z << 50Ω at the operating frequency. The capacitors allow the LTC6957 to set its own DC input bias level, and reduce the DC current drain, which at 12.4mA (for the case of a driver powered from 3.3V) is significant. This current drain can be reduced (with some potential for a noise penalty) by increasing the attenuation at the R1/R2 network, taking care to keep the Thevenin impedance equal to the Z0 of the trace.

When using CMOS logic, it is important to consider how all of the output drivers, in the same IC, are being used. For best performance, the entire IC should be devoted to driving the LTC6957, or if other gates in the same package must be put to use, they should only carry the same timing signal (such as for fan-out) or be multiplexed in time so that only one timing signal is being processed at a time, such as for multiplexing selective shutdowns of different segments of a system. Otherwise performance is likely to suffer with spurs or other interference in the phase noise spectrum related to the other signals processed in the driver.

Input Resistors

The LTC6957 input resistors, seen in Figure 1, are present at all times, including during shutdown. Although they constitute a large portion of the shutdown current, this behavior prevents the shutdown and wake-up cycling of the LTC6957 from “kicking back” into prior stages, which could create large transients that could take a while to settle. Particularly in the common case of AC-coupling where the coupling cap charge is preserved.

Input Filtering

The LTC6957 includes input filtering with three narrowband settings in addition to the full bandwidth limitation of the circuit design.

Table 1

FILTA	FILTB	BANDWIDTH
Low	Low	1200MHz (Full Bandwidth)
High	Low	500MHz (–3dB)
Low	High	160MHz (–3dB)
High	High	50MHz (–3dB)

For slow slewing signals (i.e., <100MHz sine wave signals) substantially lower phase noise can be achieved by using this feature. Bandwidth limiting is useful because it limits the impact of all of the spectral energy that will alias down to (on top of) the fundamental frequency.

The best filter setting to use for a given application will depend on the clock frequency, amplitude, and waveform shape, with the single biggest determinant being the slew rate at the input of the LTC6957. Any amplifier noise will add phase noise inversely proportional to its input slew rate, just from the dV/dt changing voltage noise to time base noise. But a fast slew rate may not be possible with other design constraints, such as the use of sine waves for EMI/RFI reasons, signal losses, etc. A limiting amplifier such as the LTC6957 should have enough bandwidth to preserve the slew rate of the input. But any additional bandwidth will provide no improvement in phase noise due to slew rate preservation, while incurring a phase noise penalty from noise aliasing.

APPLICATIONS INFORMATION

Table 2 has the slew rate ranges most suitable for the four different filter settings.

Table 2

FILTA	FILTB	INPUT SLEW RATE (V/µs)
Low	Low	>400
High	Low	125 to 400
Low	High	40 to 125
High	High	<40

Another way to look at this is to consider the case of sine waves, for which the frequency ranges will depend on input amplitudes, as illustrated in Table 3.

Table 3

	FREQUENCY RANGE			
INPUT AMPLITUDE (dBm)	FILTA = L, FILTB = L (MHz)	FILTA = H, FILTB = L (MHz)	FILTA = L, FILTB = H (MHz)	FILTA = H, FILTB = H (MHz)
10	>63	20 to 63	6.3 to 20	<6.3
5	>112	35 to 112	11 to 35	<11
0	>200	63 to 200	20 to 63	<20
–5		>112	35 to 112	<35
–10		>200	63 to 200	<63

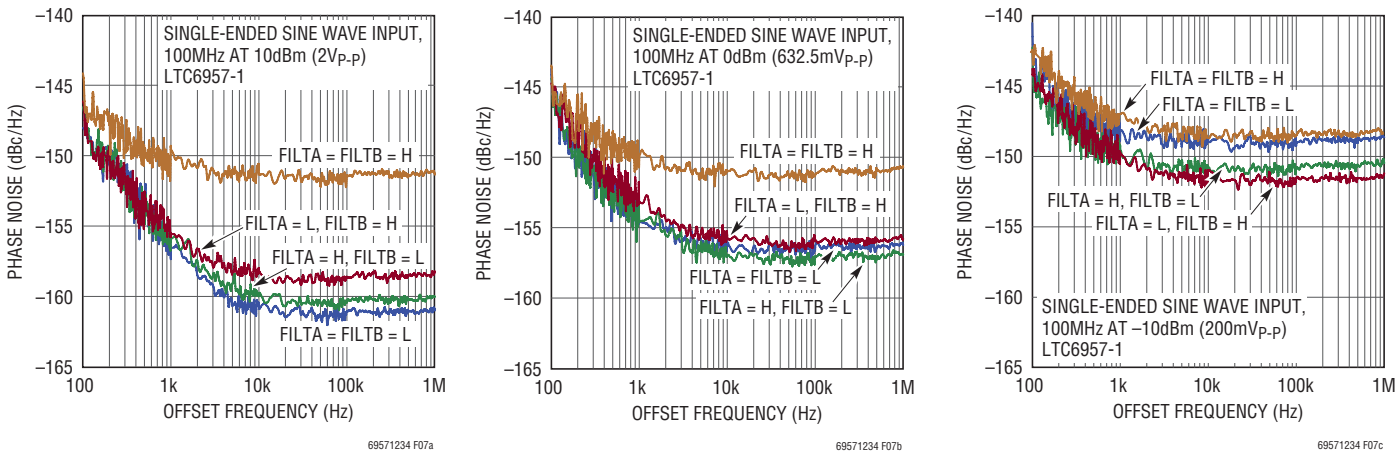
Figure 7 has LTC6957-1 100MHz additive phase noise measurements that illustrate the trade-offs between filter settings at various input slew rates. Each of the three charts has all four filter settings, and one input amplitude; Figure 7a has a +10dBm input, Figure 7b has a 0dBm input, and Figure 7c has a –10dBm input. The four filter settings are shown in the same colors throughout.

With +10dBm at 100MHz, the input slew rate is 628V/µs and Table 2 indicates the best filter setting to use is FILTA = FILTB = L, which is seen to be the case in Figure 7a.

The noise at the next filter setting is only slightly higher, but for the maximum filtering case there is a full 10dB of additional noise.

With 0dBm at 100MHz, the input slew rate is 198V/µs and Table 2 indicates the best filter setting to use is FILTA = H, FILTB = L. Again this is seen to be the case in Figure 7b. As the input was decreased 10dB from Figure 7a to Figure 7b, the blue trace rose 5dB while the green trace only rose 3dB.

With –10dBm at 100MHz, the input slew rate is 63V/µs and Table 2 indicates the best filter setting to use is FILTA = L, FILTB = H. Again this is seen to be the case in Figure 7c. As the input was decreased 10dB from Figure 7a to Figure 7b, and again to Figure 7c, the red trace rose just 3dB then another 4dB, while the green and blue traces rose much faster.



(a) (b) (c)

Figure 7. 100MHz Additive Phase Noise with Varying Input Amplitudes

APPLICATIONS INFORMATION

One important observation to take away from Figures 7a to 7c is that while the worst filter settings for a given set of conditions should certainly be avoided, it doesn't matter nearly as much if the optimal or next to optimal filter setting is used, because they are always fairly comparable in terms of phase noise. So if a design will have an octave or two range of amplitudes or frequencies, it is sufficient to choose the filter setting whose range most closely matches the application's range when using Tables 2 or 3 and the noise penalty will not be severe anywhere in the range.

Evidently, the input filtering will not significantly help with large and fast slewing input signals to the LTC6957. As seen in Figure 1, the input has a differential pair before the filters, so the limiting will already have happened before the filter. Fortunately, with large input signals, performance is typically better than with smaller input signals because phase noise is a signal-to-noise phenomenon.

Input Drive and Output Skew

All versions of the LTC6957 have very good output skew; the specification limits consist almost entirely of test margins. Even laboratory verification of the skew between different outputs is a challenging exercise, given the need to measure within ±1ps. With electromagnetic propagation velocity in FR-4 being well known as 6" per nanosecond, the skew of the LTC6957 will be impacted by PCB trace routing length differences of just 6mils.

The LTC6957 t_{PD} and t_{SKEW} are specified for a 100mV step with 50mV of overdrive. This is common for high speed comparators, though it may not reflect the typical application usage of parts such as the LTC6957. The propagation delay of the LTC6957 will increase with less overdrive and decrease with more overdrive, as would that of a high speed comparator. To a lesser extent, having the same overdrive but a larger signal (for instance a differential input step of –200mV to 50mV) will increase propagation delay, though this effect is smaller and can usually be ignored.

A consequence of this behavior may be a perceived mismatch between the propagation delay for rising versus falling edges when driven with an AC-coupled input whose duty cycle is not exactly 50%. The LTC6957 inputs are internally DC-coupled, and as shown in Figure 1, biasing is provided at ~64% of the supply voltage. AC-coupled input signals with a duty cycle of exactly 50% will see symmetric levels of overdrive for the two signal directions. If, for example, the input signal is a $100mV_{P-P}$ square wave with a duty-cycle of 48%, meaning it is high 48% of the time and low 52% of the time, the DC average will be 48mV above the low voltage level. This means the rising edge has 52mV of overdrive, and the falling edge has 48mV of overdrive.

As a result of this, the rising edge t_{PD} will be faster than the falling edge t_{PD}. Fortunately, this will make the output duty cycle closer to 50% than the input duty cycle. Figure 8 is from measurements on the LTC6957-2, with a 2V to 2.1V square wave on IN^-, and with IN^+ set to various DC voltages between those two levels. The X-axis is the overdrive level for the $t_{PD}+$ data, and is 100mV minus the overdrive level for the $t_{PD}-$ data, to illustrate the level of t_{PD} changes that can unexpectedly occur with AC-coupling. The lines are dashed where the measurement uncertainty becomes large, when single digit millivolts and picoseconds are being measured[1]. As can be seen, the $t_{PD}+/t_{PD}-$ mismatch is very good at 50mV where the two overdrive levels are the same.

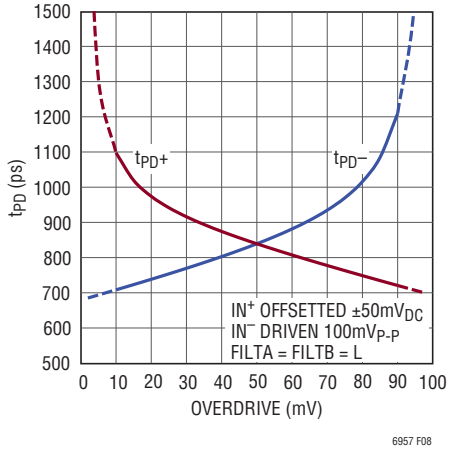


Figure 8. LTC6957-2 Propagation Delay vs Overdrive

[1] Below 2mV to 3mV, the input offset and the small input hysteresis play a role too. Fortunately, neither is large enough to be a concern in normal operation.

APPLICATIONS INFORMATION

This data is shown for the LTC6957-2, but the effect is due to the input stage that is common to all versions, so any other version will have the same general behavior.

The LTC6957-3 and LTC6957-4 CMOS outputs may have additional t_{PD}+ vs t_{PD}– discrepancies due to differences between the NMOS and PMOS output devices, particularly when driving heavy loads. These are independent of input overdrive, but can change with supply voltage and temperature, and can vary part to part. The complementary outputs of the LTC6957-4 will therefore be higher skew than the like edges of the LTC6957-3. Both the LTC6957-3 and LTC6957-4 will have large (120ps typ) t_{PD}^{+} to t_{PD}^{-} discrepancies compared to LVPECL or LVDS outputs.

LVPECL Outputs of the LTC6957-1

Figure 9 shows a simplified schematic of the LTC6957-1 LVPECL output stage. As with most ECL outputs, there are no internal pull-down devices so the user must provide both termination and biasing external to the device. Note that only the current source is cut off during shutdown. The bases of the output NPNs are still tied to the pull-up resistors, so both outputs will be pulled high in shutdown, and it is the user's responsibility to disconnect the external loading if power reduction is to be realized.

The simplest way to terminate and bias the LTC6957-1 outputs is to route the differential output to the differential receiver and terminate the lines at that point with the three resistor network shown in Figure 9. The differential termination will be 100Ω, while the common mode termination will be 75Ω which could result in additional common mode susceptibility. A bypass capacitor on the midpoint of the Y can be used to improve this.

If the common mode termination impedance is not an issue, the three resistor Y configuration can be changed to a three resistor delta configuration, which is a simpler layout in most cases.

During transitions to and from shutdown, the LTC6957-1 outputs are not guaranteed to comply with the specified output levels for any length of time after the rising edge of SD1/SD2, nor for any time before sufficient t_{WAKEUP}/t_{ENABLE} subsequent to the falling edge of SD1/SD2. The output common mode and differential voltage could have a slow settling time compared to the signal frequency, and a long string of runt pulses could be seen. The LTC6957-1 shutdown capability should be used as a slow on/off control, not a logic gating/enable control.

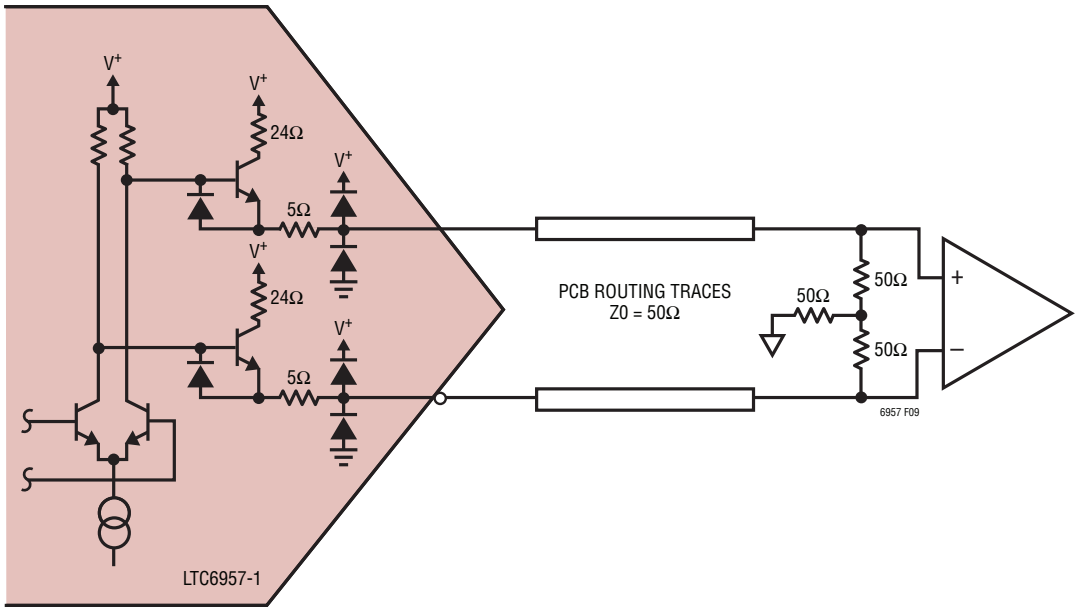


Figure 9. LTC6957-1 LVPECL Outputs

APPLICATIONS INFORMATION

Power Supplies for LVPECL Operation

The LTC6957-1 can operate from 3.15V to 3.45V total supply voltage difference, irrespective of the absolute level of those voltages. The convention in LVPECL is that the negative supply is ground, while in ECL the positive supply may be ground or 2.0V. The LTC6957-1 can work in all of these situations provided the total supply voltage difference is within the 3.15V to 3.45V range. No special supply sequencing will be needed. With a 2V rail the output terminations go to ground, while, with the positive supply grounded, the outputs can tolerate short circuits to ground. However, the four CMOS logic input signals will need to be driven with respect to whatever absolute levels of supply voltages are used. If FILTA, FILTB, SD1, and SD2 are fixed, they can be tied to the appropriate rail and this is not a problem. Interface logic levels could get tricky if they need to be programmed in-system.

In any voltage configuration, be aware that the LVPECL output stage depends on the external load to complete its biasing and, as such, is susceptible to phase modulation as the supply voltage changes. The LTC6957-1 is generally less sensitive to variations in the supply voltage if the termination voltage tracks the supply rather than ground.

With all four outputs terminated or otherwise driving heavy loads, the LTC6957-1 power consumption and temperature rise may be an issue.

Fortunately, the data sheet specification for supply current with output loads does not need to be multiplied by the entire supply voltage to calculate on-chip power dissipation because most of that current flows through the loads which will dissipate a significant portion of the total system power.

Typically, the internal power consumption will be (20mA • 3.3V =) 66mW, while the on-chip power dissipation from the output loading will be less than half that number. With a total power dissipation on-chip of 90mW, the temperature rise in the MS-12 package will be 13°C given the θ_{JA} of that package. For use to 125°C ambient (H-grade) designers should be sure to check the temperature rise using their specific output loading and supply levels. The Absolute Maximum rating for Junction Temperature is 150°C, and must be avoided to prevent damaging the device, and as stated in Note 1: "Exposure to any Absolute Maximum Rating condition for extended periods of time may affect device reliability and lifetime."

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LVDS Outputs of the LTC6957-2

Figure 10 shows a simplified schematic of the LTC6957-2 LVDS output stage. The TIA/EIA-644-A standard specifies the generator electrical requirements for this type of interface, and the LTC6957-2 has been verified against that standard using the following test methods:

SPECIFICATION	LEVEL OF TESTING
4.1.1	100% Production Tested
4.1.2	100% Production Tested
4.1.3	100% Production Tested
4.1.4	100% Production Tested*
4.1.5	Lab Verification of Design Only
6a	100% Production Tested
6b	100% Production Tested
6c	100% Production Tested

*The t_{RISE}/t_{FALL} of the LTC6957-2 are not compliant with the standard so as to preserve full phase noise performance. To slow the edge rates, add differential capacitance across the outputs. 2.7pF is sufficient to meet the standard.

The TIA/EIA-644-A standard does not cover driver characteristics during shutdown nor the transitions to and from shutdown. The LTC6957-2 outputs are not guaranteed to comply with the standard for any length of time after the rising edge of SD1/SD2, nor for any time before sufficient t_{WAKEUP}/t_{ENABLE} subsequent to the falling edge of SD1/SD2. The output common mode voltage (V_{OS} in 644-A parlance) could have a slow settling time compared to the signal frequency, and a long string of runt pulses could be seen. The LTC6957-2 shutdown capability should be used as a slow, power-saving on/off control, not a logic gating/enable control.

Power Supplies for LVDS Operation

The LTC6957-2 has a single supply that should be within the 3.15V to 3.45V range.

The LTC6957-2 power supply voltage can corrupt the spectral purity of the clock signal, though to a lesser degree than with any of the other options. See the Typical Performance Characteristic chart t_{PD} vs Supply Voltage.

When using both LVDS channels, the LTC6957-2 power consumption can exceed 120mW, which results in a junction-to-ambient rise of 17.4°C in the MS-12 package, more when operated at 3.45V. Again, it is up to the user to always avoid junction temperatures above the Absolute Maximum rating, and to stay comfortably below it for any extended periods of time.

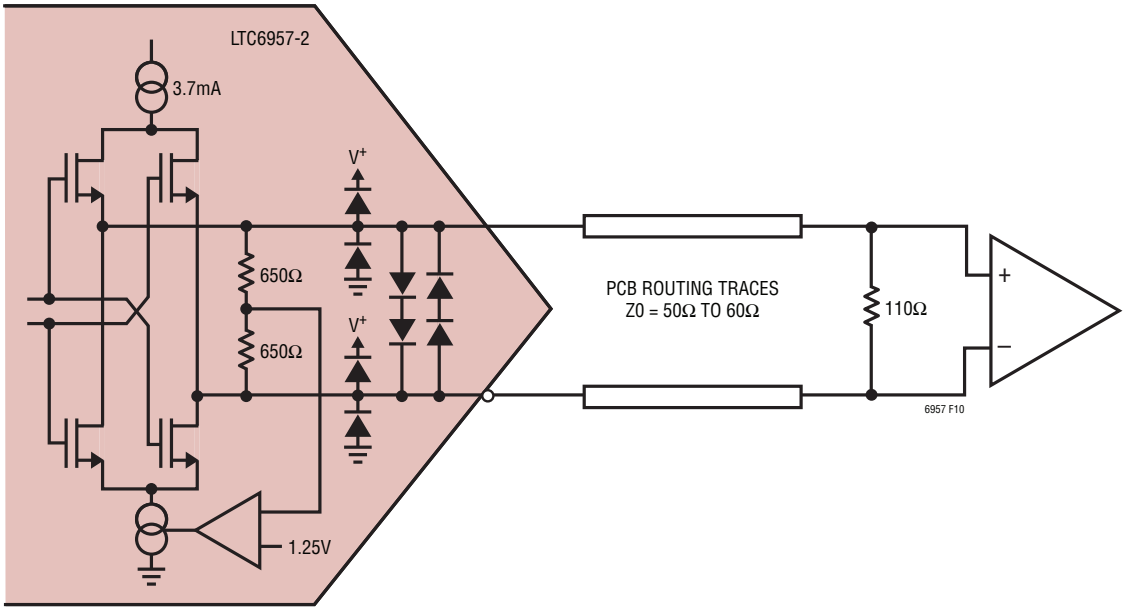

Figure 10. LTC6957-2 LVDS Outputs

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CMOS Outputs of the LTC6957-3/LTC6957-4

Figure 11 shows a simplified schematic of the LTC6957-3/LTC6957-4 CMOS output stage. The LTC6957-3 outputs are driven synchronously in-phase, while the LTC6957-4 outputs are driven differentially out-of-phase.

Although the LTC6957-3/LTC6957-4 are specified for a resistive load, the outputs can drive capacitive loads as well. With more than a few picoFarads of load, the rise and fall times will be degraded in direct proportion to the load capacitance.

During shutdown, the LTC6957-3 outputs will both be set to a logic low.

During shutdown, the LTC6957-4 OUT1 will be set to a logic low, while OUT2 will be set to a logic high.

During transitions to and from shutdown, the LTC6967-3/LTC6957-4 outputs may not comply with the specified output levels for any length of time after the rising edge of SD1/SD2, nor for any time before sufficient t_{WAKEUP}/t_{ENABLE} subsequent to the falling edge of SD1/SD2. The outputs may have one or two errant transitions resulting in runt pulses being seen. The LTC6957-3/LTC6957-4 shutdown capability should be used as a slow, power-saving on/off control, not a logic gating/enable control, and because they can not be put in a high impedance (3-state) condition, the shutdown functionality is not usable as a way to multiplex multiple outputs or devices.

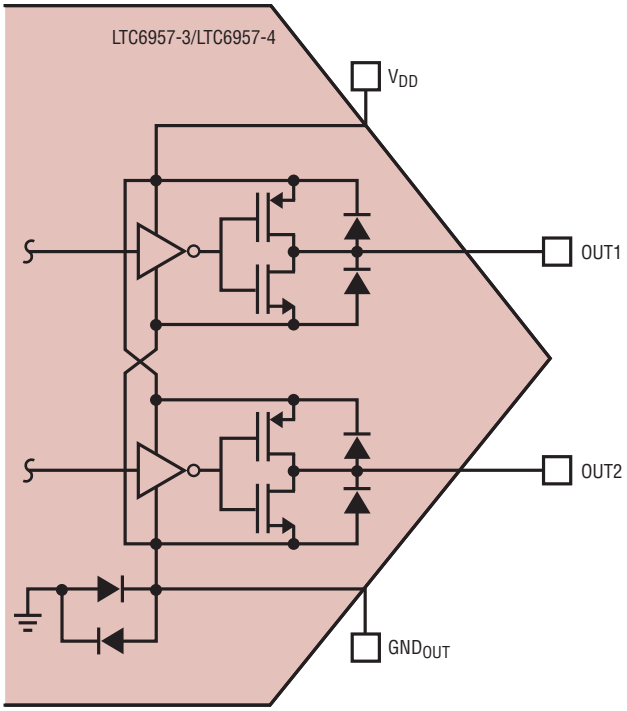

Figure 11. LTC6957-3/LTC6957-4 CMOS Outputs

Power Supplies for CMOS Operation

The LTC6957-3/LTC6957-4 operate with V^+ from 3.15V to 3.45V only. If the LTC6957-3/LTC6957-4 are used to drive CMOS logic at a lower voltage rail, the output stage can be powered (Pin 11) by a lower voltage, down to $2.4V_{MIN}$. Note that significant degradation of the spectral purity could occur if the output supply, V_{DD}, is not clean, either because of additional broadband noise or discrete spectral tones. The nature of a CMOS logic gate forms an AM modulator of low frequency disturbances on the power/ground that modulate the signal propagating through the CMOS gate. Numerous common phenomena can serve to convert the AM to PM/FM and, even if the conversion efficiency is low, corrupt the phase noise to unacceptable levels in demanding applications.

If two separate supplies are used, the only supply sequencing issue to be aware of is that if the V_{DD} comes up first, the OUT1/OUT2 CMOS outputs will be high impedance until $V^+ > \sim 1V$. Note that the four CMOS control inputs are all referenced to V^+, not the output supply. Also note that during operation the output supply should be equal to or less than V^+. The LTC6957-3/LTC6957-4 will function with V_{DD} several hundred millivolts above the V^+ supply, but depending on the load, this margin for error can largely be consumed by transient load steps.

When driving capacitive loads at high frequencies, the LTC6957-3/LTC6957-4 V_{DD} power consumption can jump considerably over the quiescent power taken from V^+. The Dynamic current specification is with no load and adds directly to the current needed to repetitively charge and discharge a capacitive load.

With 24mA drawn from V^+ at 3.3V, and another 20mA to 30mA drawn from V_{DD} (easy to do with two outputs active at 300MHz), the total power consumption can be 145mW to 178mW, resulting in a junction-to-ambient rise

APPLICATIONS INFORMATION

of 21°C to 26°C in the MS-12 package. For use to 125°C ambient (H-grade) designers should be sure to check the temperature rise using their specific output frequency, loading, and supply voltages. The Absolute Maximum rating for Junction Temperature is 150°C, which must be avoided to prevent damaging the device, and as stated in Note 1: "Exposure to any Absolute Maximum Rating condition for extended periods of time may affect device reliability and lifetime."

Low Phase Noise Design Considerations

Phase noise is a frequency domain representation of the random variation in phase of a periodic signal. It is characterized as the power at a given offset frequency relative to the power of the fundamental frequency. Phase noise is specified in dBc/Hz, decibels relative to the carrier in a 1Hz bandwidth. It is essentially a frequency dependent signal-to-noise ratio.

Designing for low phase noise is challenging, even with a solid understanding of phase noise. Any designer attempting such a task will find a good working understanding of what phase noise is, and how it behaves, to be the most important tool to achieve success. One of the most intuitive explanations is found in Chapter 3, “The Relationship Between Phase Jitter and Noise Density,” of W.P. Robins’ 1982 text, “Phase Noise in Signal Sources.”

With a solid base of understanding, the designer will now see that the entire clocking chain is full of potential phase modulators. The noise of an amplifier is usually thought of as an additive term, but for phase noise the bias noise, to the extent that the amplifier bandwidth is dependent on the bias level, is not an additive term but a modulating term. The LTC6957 is a monolithic clock limiting amplifier carefully designed so that users do not have to worry about such details.

However, users of the LTC6957 still need to pay attention to external considerations that can result in corruption of the good phase noise performance available from all the components used.

Timing jitter is a term used to describe the integration of phase noise over a specified bandwidth which is presented as a time domain specification.

Unfortunately, the term “low jitter” has become so overused that it is rendered virtually meaningless. High speed communication links doing de-serialization and the like can require jitter on the order of 30ps to 50ps. This is lower jitter than required for a clock on a micro-controller, but for high frequency sampling, even 1ps can severely impact the dynamic range achievable. Therefore, it is best to ignore the term “low jitter” and look for measured values of jitter, and preferably phase noise. To analyze and measure true low noise components, most instruments measure phase noise (in dBc/Hz) rather than jitter.

A second consideration when designing for low phase noise is that any clock signal is an analog signal and should be thought of and routed as such. They should not be run through large FPGAs with lots of activities at multiple frequencies, they should not be routed through PCB traces alongside digital data lines, and they should not be routed through clock fan-out devices that have features such as zero delay or programmable skew. The specifics of the PCB traces and what surrounds them should be analyzed as if the clock signals were among your most sensitive analog signals, because in demanding applications that is what your clock signals are. Note that signal integrity software intended for analyzing crosstalk in digital systems may only give yes or no answers and that clocking performance can be compromised at levels 40dB to 60dB below what is required to get that “yes” answer.

Common pitfalls with clock signals are the same as for sensitive analog signals: routing near or alongside digital traces of any kind, crossing digital traces on an adjacent layer within a sandwich of ground planes, using digital power planes as part of layer sandwiches, and assuming all of these are sufficiently mitigated by using differential clock signaling.

The way to address these issues is also the same as for sensitive analog signals: routing away from digital traces wherever possible; routing with shielding of ground, either planes, adjacent traces, or both; making realistic assumptions of common mode rejections (30dB to 40dB at most); and keeping a critical eye out for unintended couplers during the design and debug phases.

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Even if the world's cleanest reference clock were used to feed the LTC6957, simply routing it through a poorly designed system would result in compromised spectral performance. This often catches designers by surprise because the mechanisms above are typically additive and linear, which result in filtering and additional spectral components, but don't by themselves create phase modulation. Unfortunately, any limiter, including the LTC6957, will, through its nonlinear action, transform additive terms into phase modulation. When a small tone is added to a large pure tone, the larger tone will appear to have its amplitude and phase modulated at a rate equal to the difference of the two frequencies. Pass this through a limiter and only the phase modulation remains.

In large complex systems, it may be impractical to eliminate all potential corrupting of the clock signals. In such a case, a narrow band filter placed at the inputs of the LTC6957 can remove the unwanted spectral components that are far enough away from the fundamental.

Close-in spectral anomalies will likely be impervious to such filtering. Therefore, it is doubly important to keep an eye out for modulating mechanisms. If the clock is routed through CMOS logic gates, the power supply used for that gate will AM modulate the signal at the very least. The modulation could manifest itself as sideband tones if the power supply has repetitive disturbances, common with switching power supplies, or it could manifest itself as random noise if the noise of a linear regulator is too high.

Another source of corruption in large systems or laboratory measurements is the use of flexible cabling, which can have a low level piezoelectric effect that modulates the electrical length in response to mechanical vibration. Rigid or semi-rigid cabling and PCB routing can be used to eliminate this source of signal corruption.

AM to PM Conversion at the LTC6957 Inputs

The LTC6957 input stage has some AM to PM conversion, but as seen in the Typical Performance Characteristics section, even at 300MHz this is less than 0.5°/dB. One source of AM to PM conversion at the LTC6957 input is the optional lowpass filtering, because the upper sideband and the lower sideband will be attenuated by slightly different amounts. This difference is quite small for low offset frequencies, but the difference grows both as the frequency of the modulation increases, and as the carrier frequency approaches the filter cutoff frequency where the filter has a steeper roll-off.

Therefore, if small amounts of AM are known to be present and an unacceptable level of PM is seen at the LTC6957 output, it may be helpful to change the input filter setting to a higher cutoff frequency.

Cross Talk from Loading at the LTC6957 Outputs

Another mechanism to be aware of in the LTC6957 is cross-modulation of the outputs. Except for the CMOS LTC6957-3/LTC6957-4, there is minimal direct AM or PM modulation of the outputs by the power supply. In the CMOS case, the V_{DD} power supply will directly AM modulate the outputs, with a small amount of AM to PM conversion.

The thing to be aware of here is that there can be load-induced disturbances internal to the LTC6957 that can modulate the other output. For instance, hooking up one output to an ADC encode input and the second output to the FPGA that performs the first DSP on the ADC outputs, can result in considerable kickback of FPGA generated signals into the LTC6957. If this cross-modulates over to the other output, all kinds of deleterious effects may be seen including tones, images, etc.

The CMOS LTC6957-3/LTC6957-4 are more susceptible to this than the LVPECL and LVDS (LTC6957-1/LTC6957-2). To prevent this, a buffer can be placed between the LTC6957 and the FPGA, even one that compromises the full jitter performance considerably. Because it is the ADC that is doing the sampling—the FPGA clock input has enough margin for error to qualify as a digital signal.

APPLICATIONS INFORMATION

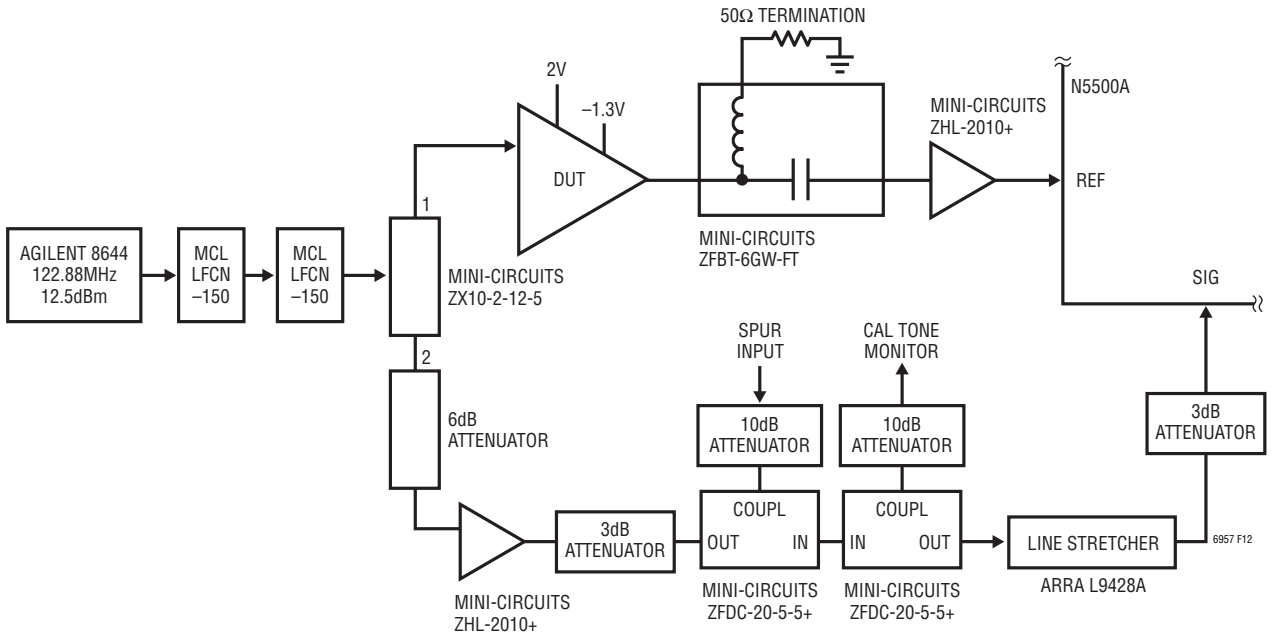


Figure 12. Setup for LTC6957-1 Phase Noise Measurement Using Agilent E5505

Phase Noise Measurement

Additive (also called residual) phase noise can be particularly challenging to measure. Figure 12 shows a typical laboratory set-up for testing the LTC6957-1 phase noise. The LTC6957-1 has the lowest broadband phase noise of the various dash numbers (equal to that of the LTC6957-3/LTC6957-4) and the lowest close-in noise with a corner frequency below 2kHz, so it presents the most challenging case.

The various components and their role will be discussed as this will illustrate both the care that must be taken to realize the full performance of the LTC6957, and the demanding nature of making phase noise measurements.

The signal starts with a 122.88MHz CW tone from the Agilent 8644 synthesizer at a fairly high power level of 12.5dBm. Two series LPFs at 150MHz cut out all the high frequency noise components that would otherwise contribute noise because of the aliasing caused by the limiting action of the LTC6957. A signal splitter then separates the signal in two; one path will propagate through the DUT and the other won't, a common method used for measuring residual phase noise.

In theory, all the phase noise in the signal source will be rejected with the reading reflecting only the difference in noise between the two paths. However, the rejection is not perfect, particularly at very high offset frequencies where the phase difference between the two paths progressively increases, thus the successive lowpass filters on the signal source.

The Agilent 5505 measurement system uses the N5500A front end, which includes a mixer to compare the signal and reference phases. For amplifier noise, it is appropriate to feed the DUT path to the signal input, but for clock buffers that create fast clock edges, it is usually advantageous to use the reference input, which seems to be sensitive only to the edges and not noise throughout the period. This is a reasonable thing to do because the LTC6957 is designed to drive ADC encode inputs or mixer ports which have the same qualitative properties.

Both the signal and reference inputs to the test set need to be fairly large (15dBm to 20dBm) to realize the best noise floor, so both signal paths include Mini-Circuits ZHL-2010+ low noise amplifiers to boost the signal. The LTC6957-1 was operated from 2V/–1.3V supplies so it

APPLICATIONS INFORMATION

could drive a 50Ω load to ground directly, but this creates a DC offset (the signal is always positive) that the amplifier cannot take, so a bias tee was included in the DUT signal path.

Only the 122.88MHz sine wave will be in the path without the DUT, going to the N5500A signal port, until the first coupler. This coupler allows a spur input to be injected, while a second coupler allows the size of the spur, relative to the carrier, to be measured. More on that in a minute. The three attenuators in this signal path work with the ZHL-2010+ to manage the dynamic range, while the attenuators on the coupling ports keep these terminals from degrading the measured noise.

Finally, an ARRA L9428A line stretcher is used to adjust for quadrature. One last attenuator helps with impedance matching between the N5500A input and the line stretcher output port. The E5505A can automatically adjust the signal source phase/frequency for quadrature when measuring VCOs or synthesizers, but for additive noise this adjustment is manual because the adjustment must be made after the signal is split into the two paths. The line stretcher has a range of just 166ps, but with 122.88MHz, up to 20ns of adjustment may be needed (1/4 cycle). Not shown is the various short lengths of SMA cables and barrel couplers that can also be added or subtracted to adjust the relative phase of the two signal paths.

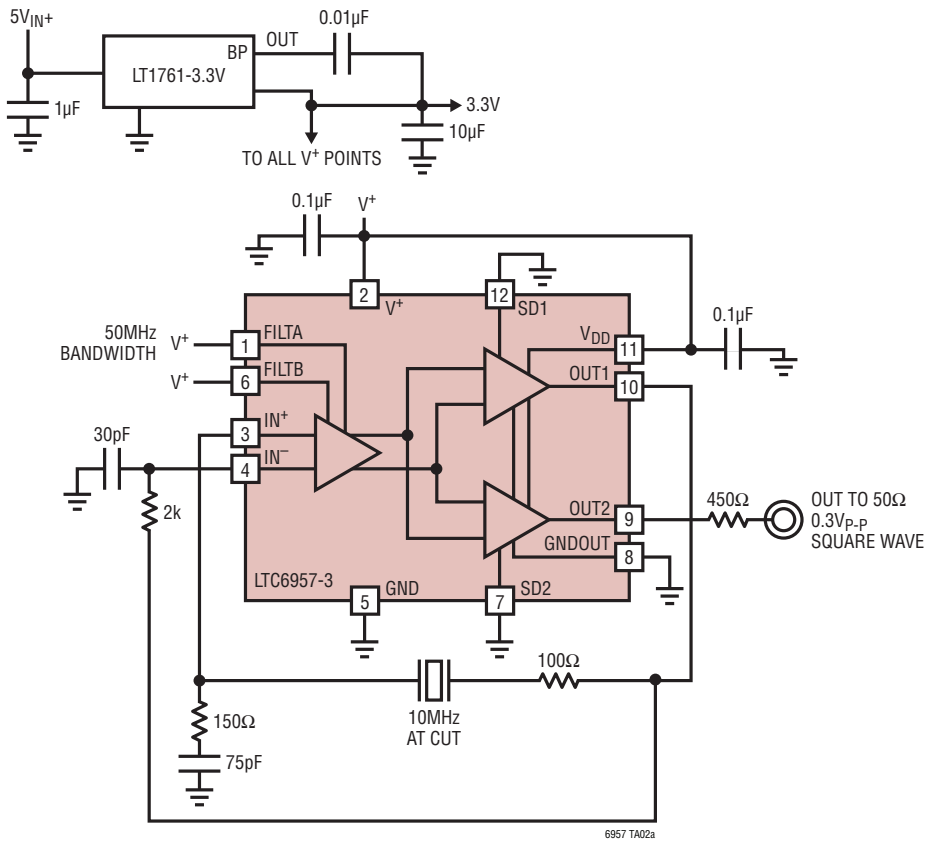
To calibrate E5505/N5500 measurements, the gain of the mixer must be known. The surest way to measure it at the actual frequencies being used is to inject a calibration tone. For a 10kHz offset, a 122.89MHz low level (–10dBm) signal is fed into the first coupler port. The requirements for this signal are not demanding, so a general purpose synthesizer that can be frequency locked, such as the HP8657B, can be used.

The E5505 measures the amplitude of the resulting 10kHz mixer output, but to put that in context (so that it can later calculate results in dBc) it needs to know the size of the injected spur relative to the carrier. Therefore, that relative difference is measured using a spectrum analyzer connected to the attenuator on the second coupler.

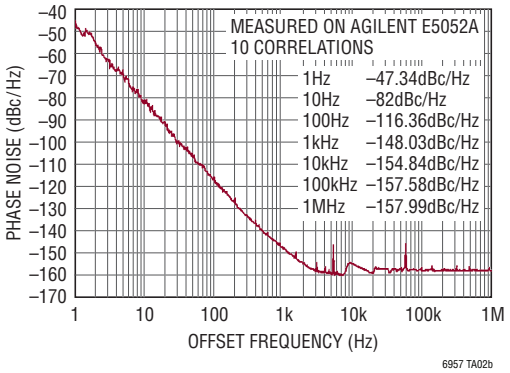
Hopefully the above discussion conveys the meticulous effort needed to measure additive phase noise of a single device, at a single operating frequency. While the circuitry in Figure 12 can be used to measure the entire spectrum of phase noise (all offset frequencies) as well as the phase noise at other clock frequencies, every clock frequency will require manual adjusting for quadrature. The input LPFs will either need to be changed to match the new clock frequency, or possibly amplitudes at various places will have to be adjusted to account for the frequency roll-off therein.

TYPICAL APPLICATIONS

Crystal Oscillator



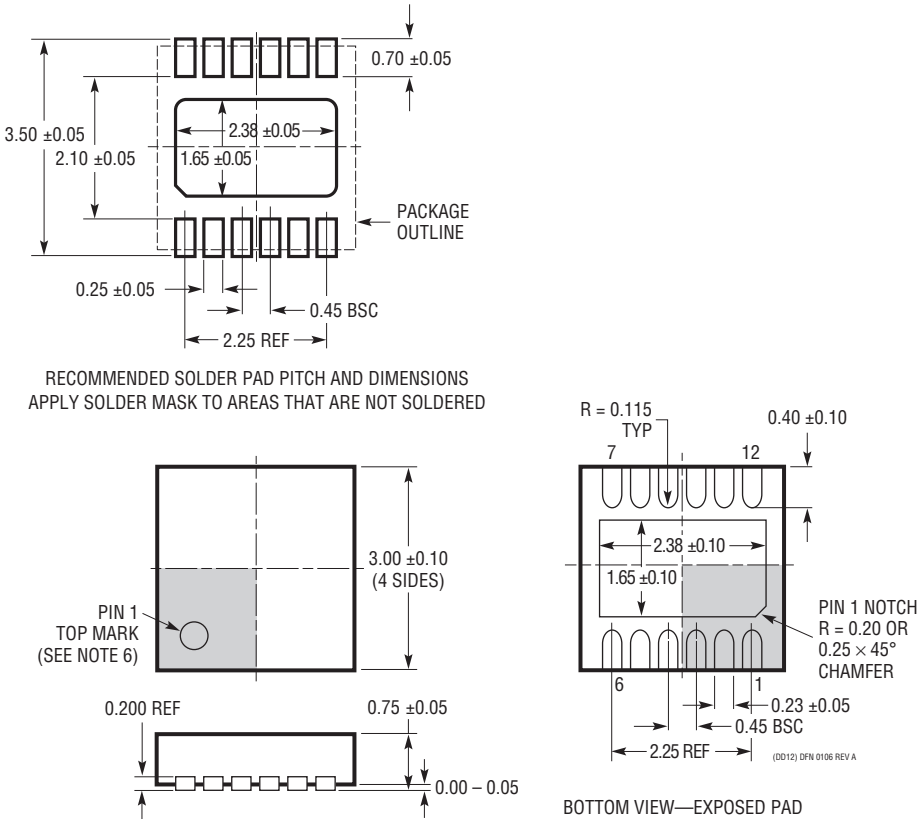
Total Phase Noise of 10MHz Crystal Oscillator



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC6957-1#packaging for the most recent package drawings.

DD Package
12-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1725 Rev A)

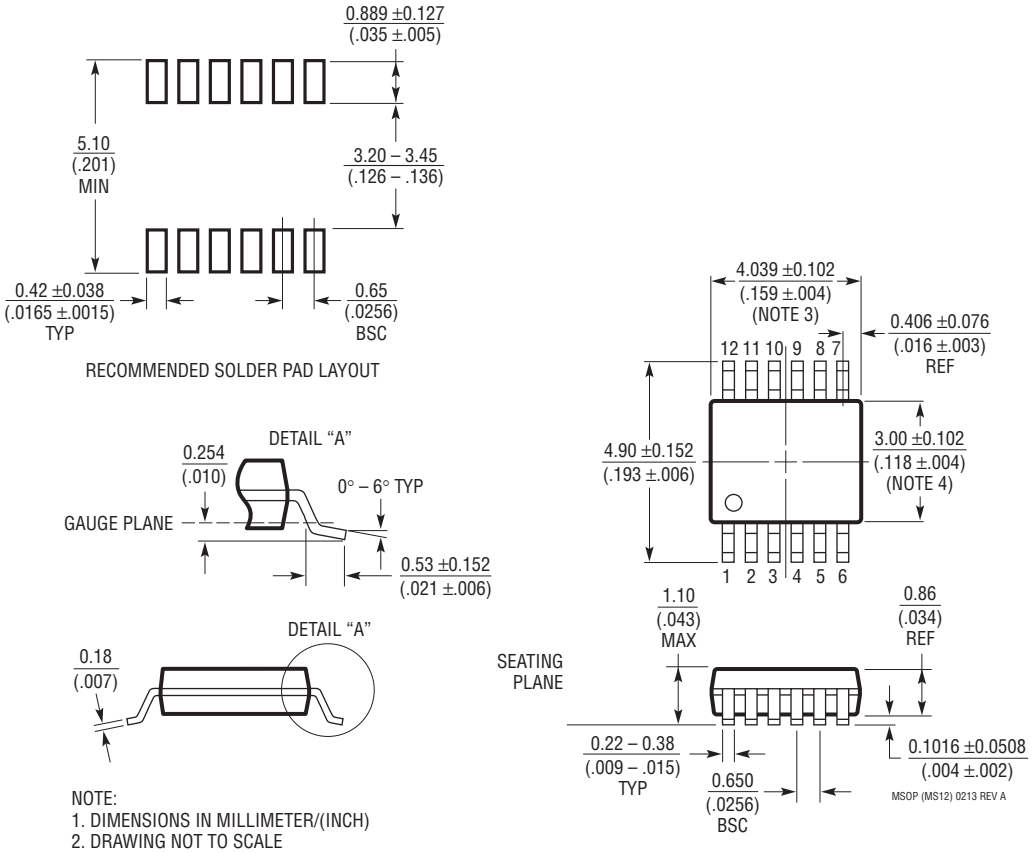


NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD AND TIE BARS SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC6957-1#packaging for the most recent package drawings.

MS Package
12-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1668 Rev A)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/15	Corrected connections and part values in the Typical Applications schematic.	36
B	12/17	Corrected the Timing Diagram and added clarification text.	18

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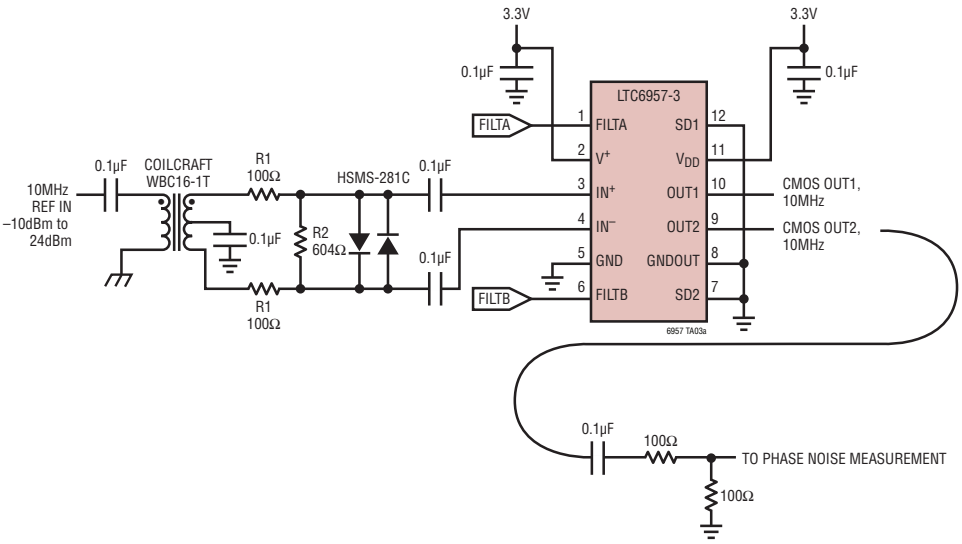
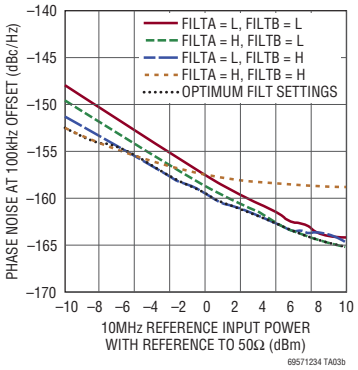
TYPICAL APPLICATION

10MHz Frequency Reference Input Stage with Dual CMOS Outputs



Additive Phase Noise vs Input Amplitude



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC6945	Ultralow Noise and Spurious Integer-N Synthesizer	350MHz to 6GHz, –226dBc/Hz Normalized In-Band Phase Noise Floor, –157dBc/Hz Wideband Output Phase Noise Floor
LTC6946-x	Ultralow Noise and Spurious Integer-N Synthesizer with Integrated VCO	370MHz to 6.4GHz, –226dBc/Hz Normalized In-Band Phase Noise Floor, –157dBc/Hz Wideband Output Phase Noise Floor
LTC6947	Ultralow Noise and Spurious Fractional-N Synthesizer	350MHz to 6GHz, –226dBc/Hz Normalized In-Band Phase Noise Floor, –157dBc/Hz Wideband Output Phase Noise Floor, Integer-N Spurious Performance
LTC6948-x	Ultralow Noise and Spurious Fractional-N Synthesizer with Integrated VCO	370MHz to 6.4GHz, –226dBc/Hz Normalized In-Band Phase Noise Floor, –157dBc/Hz Wideband Output Phase Noise Floor, Integer-N Spurious Performance
LTC6950	1.4GHz Low Phase Noise, Low Jitter PLL with Clock Distribution	Four Independent LVPECL Outputs with 18fs$_{RMS}$ Additive Jitter (12kHz to 20MHz)
LTC6954-x	Low Phase Noise, Triple Output Clock Distribution Divider/Driver	LVPECL, LVDS and CMOS Outputs with < 20fs$_{RMS}$ Additive Jitter (12kHz to 20MHz)

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