ATWILC1000B-MUT

ATWILC1000B-MUT IEEE® 802.11 b/g/n Link Controller SoC

Introduction

The ATWILC1000B is a single chip IEEE® 802.11 b/g/n Radio/Baseband/MAC link controller optimized for low-power mobile applications. The ATWILC1000B supports single stream 1x1 802.11n mode providing up to 72 Mbps PHY rate. The ATWILC1000B features a fully integrated Power Amplifier (PA), Low Noise Amplifier (LNA), Switch, and Power Management. The ATWILC1000B offers very low-power consumption while simultaneously providing high performance and minimal bill of materials.

The ATWILC1000B provides Serial Peripheral Interface (SPI) and Secure Digital Input Output (SDIO) to interface with the host controller. The clock source for the ATWILC1000B is provided by an external crystal at 26 MHz. The ATWILC1000B is available in both QFN and Wafer Level Chip Scale Package (WLCSP) packaging.

Features

- IEEE 802.1 b/g/n 20 MHz (1x1) Solution
- Single Spatial Stream in 2.4 GHz ISM Band
- Integrated PA and T/R Switch
- Superior Sensitivity and Range via Advanced PHY Signal Processing
- Advanced Equalization and Channel Estimation
- Advanced Carrier and Timing Synchronization
- Wi-Fi Direct® and Soft-AP Support
- Supports IEEE 802.11 WEP, WPA, WPA2 and WPA2-Enterprise Security
- Superior MAC Throughput via Hardware Accelerated Two-Level A-MSDU/A-MPDU Frame Aggregation and Block Acknowledgment
- On-Chip Memory Management Engine to Reduce Host Load
- SPI and SDIO Host Interfaces
- Operating Conditions:
  - Operating temperature: −40°C to +85°C
  - Input/Output supply voltage(VDDIO): 1.62V to 3.6V
  - Power supply (VBATT): 3.0V to 4.2V
- Power Save Modes:
  - <1 µA Deep Power-Down mode typical at 3.3V I/O
  - 380 µA Doze mode with chip settings preserved (used for beacon monitoring)
  - On-chip low-power sleep oscillator
  - Fast host wake up from Doze mode by a pin or host I/O transaction

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1. Ordering Information and IC Marking

The following table provides the ordering details of the ATWILC1000B IC.

Table 1-1. Ordering Details

Ordering Code[1]	Package Type	IC Marking
ATWILC1000B-MU-ABCD	5 x 5 QFN in Tape and Reel	ATWILC1000B
ATWILC1000B-UU-ABCD	3.24 x 3.24 mm WLCSP in Tape and Reel	ATWILC1000B

Note:

1. ABCD interprets as:
   "A" can be "Y" indicating Tray, or "T" indicating Tape and Reel.

   "BCD" equals to "042" for part assigned with MAC ID and blank for part with no MAC ID.

   The following table lists possible combinations for ordering the ATWILC1000B-MU and ATWILC1000B-UU.

Ordering Code	Description
ATWILC1000B-MU-T	No MAC ID and ship in Tape and Reel
ATWILC1000B-MU-Y	No MAC ID and ship in Tray
ATWILC1000B-MU-Y042	MAC ID assigned and ship in Tray
ATWILC1000B-MU-T042	MAC ID assigned and ship in Tape and Reel
ATWILC1000B-UU-T	No MAC ID and ship in Tape and Reel
ATWILC1000B-UU-Y	No MAC ID and ship in Tray
ATWILC1000B-UU-Y042	MAC ID assigned and ship in Tray
ATWILC1000B-UU-T042	MAC ID assigned and ship in Tape and Reel

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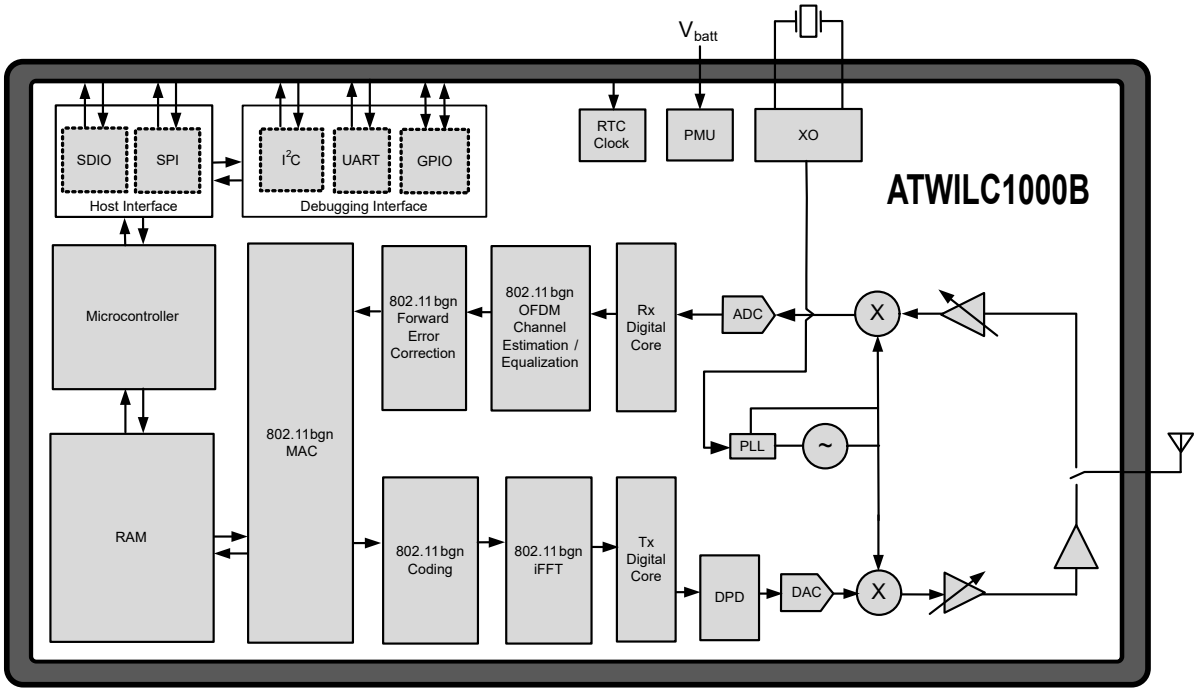
2. Functional Overview

2.1 Block Diagram

The following figure provides a basic overview of the ATWILC1000B IC.

Figure 2-1. ATWILC1000B Block Diagram



2.2 Pin Description

The ATWILC1000B is offered in an exposed pad 40-pin QFN package. This package has an exposed paddle that must be connected to the system board ground. The QFN package pin assignment and the WLCSP package pin assignment are shown in the following figures. The color shading is used to indicate the pin type as follows:

- Green – Power
- Red – Analog
- Blue – Digital I/O
- Yellow – Digital input
- Grey – Unconnected or reserved

Figure 2-2. QFN Package Pin Assignment

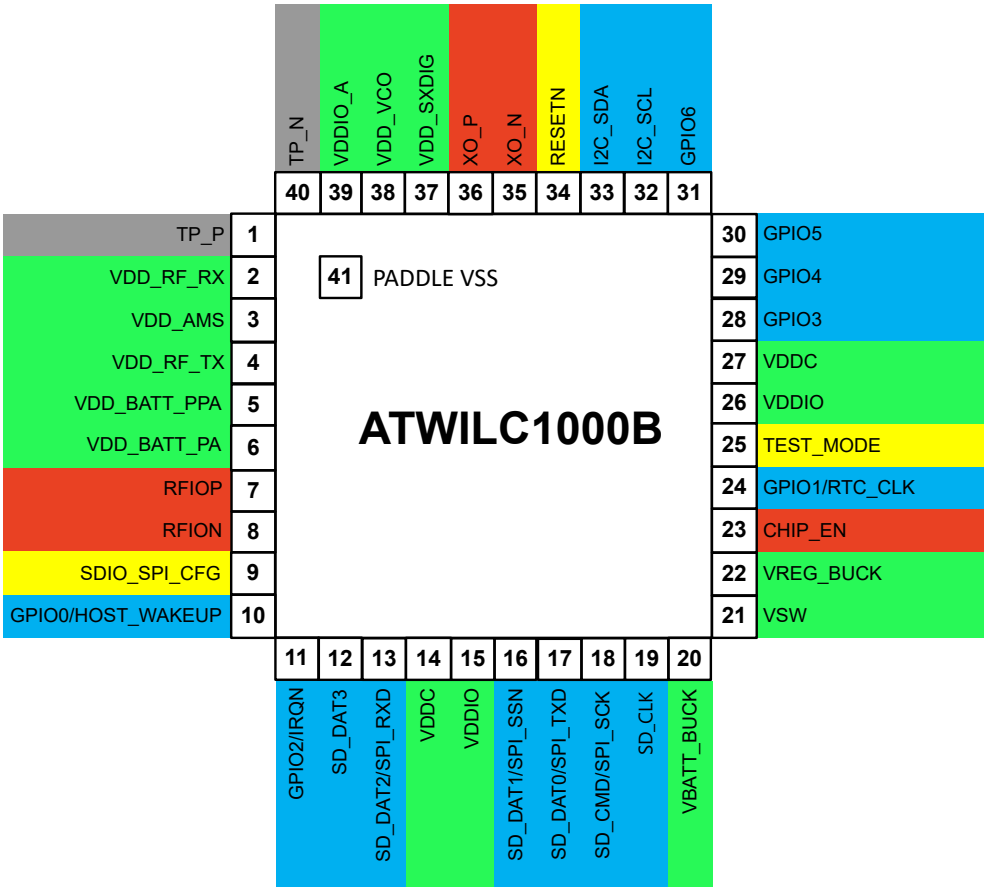
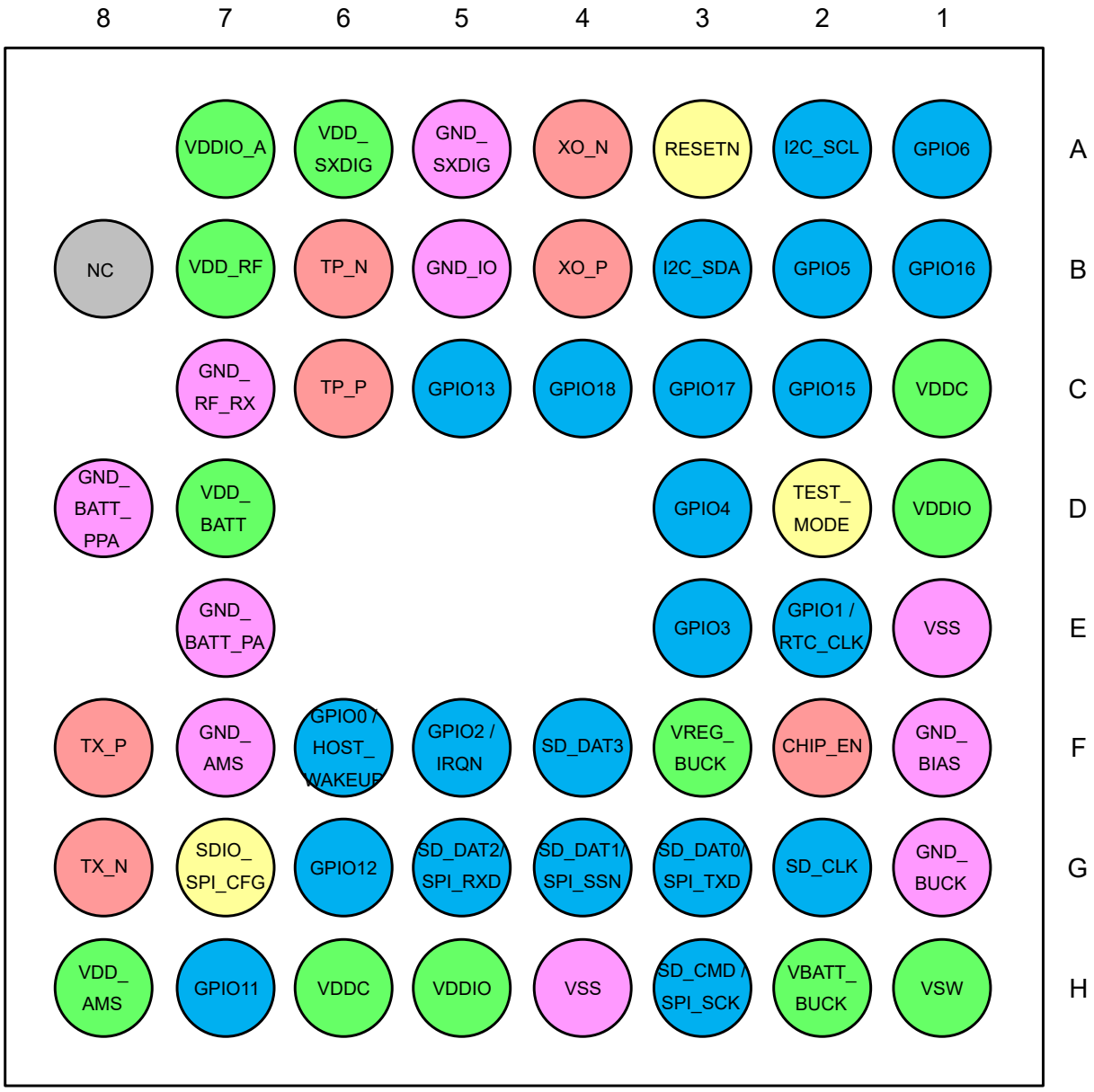


Figure 2-3. WLCSP Package Pin Assignment



The ATWILC1000B pins are described in the following table.

Table 2-1. Pin Description

QFN Pin Number	WLCSP Pin Number	Pin Name	Pin Type	Description
1	C6	TP_P	Analog	Test Pin/No Connect
2	B7	VDD_RF_RX	Power	Tuner RF Supply (see Section 7.1 Power Architecture)
3	H8	VDD_AMS	Power	Tuner BB Supply (see Section 7.1 Power Architecture)

.....continued

QFN Pin Number	WLCSP Pin Number	Pin Name	Pin Type	Description
4	—	VDD_RF_TX	Power	Tuner RF Supply (see Section 7.1 Power Architecture)
5	—	VDD_BATT_PPA	Power	PA 1ST Stage Supply (see Section 7.1 Power Architecture)
6	D7	VDD_BATT_PA	Power	PA 2ND Stage Supply (see Section 7.1 Power Architecture)
7	—	RFIOP	Analog	Positive RF Differential I/O
8	—	RFION	Analog	Negative RF Differential I/O
9	G7	SDIO_SPI_CFG	Digital Input	• Tie to VDDIO through a 1 MΩ resistor to enable the SPI interface • Tie to GND to enable the SDIO interface
10	F6	GPIO0/ HOST_WAKE	Digital I/O, Programmable Pull-up	• GPIO0/Host wake control • Used to wake-up the device from Doze mode. Current firmware implementation makes use of IRQ/SDIO Interface to wake-up the Host (2)
11	F5	GPIO2/IRQN	Digital I/O, Programmable Pull-up	• GPIO2(2)/ATWILC1000B device interrupt output • Connect to a host interrupt pin
12	F4	SD_DAT3	Digital I/O, Programmable Pull-up	SDIO Data Line 3 from the ATWILC1000B when device is configured for SDIO
13	G5	SD_DAT2/ SPI_RXD	Digital I/O, Programmable Pull-up	• SDIO Data Line 2 signal from ATWILC1000B when device is configured for SDIO • SPI MOSI (Master Out Slave In) pin when device is configured for SPI
14	C1	VDDC	Power	Digital Core Power Supply (see Section 7.1 Power Architecture)
15	D1	VDDIO	Power	Digital I/O Power Supply (see Section 7.1 Power Architecture)
16	G4	SD_DAT1/ SPI_SSN	Digital I/O, Programmable Pull-up	• SDIO Data Line 1 from ATWILC1000B when device is configured for SDIO (active-low) • SPI slave select from the ATWILC1000B when device is configured for SPI
17	G3	SD_DAT0/ SPI_TXD	Digital I/O, Programmable Pull-up	• SDIO Data Line 0 from the ATWILC1000B when device is configured for SDIO • SPI MISO (Master In Slave Out) pin from ATWILC1000 when device is configured for SPI

.....continued

QFN Pin Number	WLCSP Pin Number	Pin Name	Pin Type	Description
18	H3	SD_CMD/ SPI_SCK	Digital I/O, Programmable Pull-up	• SDIO CMD line from ATWILC1000B when device is configured for SDIO • SPI Clock from ATWILC1000 when device is configured for SPI
19	G2	SD_CLK	Digital I/O, Programmable Pull-up	SDIO clock line for the ATWILC1000B when device is configured for SDIO
20	H2	VBATT_BUCK	Power	Battery Supply for DC/DC Converter (see Section 7.1 Power Architecture)
21	H1	VSW	Power	Switching output of DC/DC Converter (see Section 7.1 Power Architecture)
22	F3	VREG_BUCK	Power	• Core Power from DC/DC Converter (see Section 7.1 Power Architecture) • Decouple with 10 µF and 0.01 µF capacitor to GND and place these capacitors as recommended in Section 10.1.3 Power Management Unit
23	F2	CHIP_EN	Analog	• Device enable • High level enables device, low level places device in Power-Down mode • Connect to a host output that has default low at power-up; if the host output is tristated, add a 1 MΩ pull-down resistor to ensure a low level at power-up
24	E2	GPIO1/RTC_CLK	Digital I/O, Programmable Pull-up	GPIO1/32kHz Clock Input
25	D2	TEST_MODE	Digital Input	Test Mode – User must tie this pin to GND
26	H5	VDDIO	Power	Digital I/O Power Supply (see Section 7.1 Power Architecture)
27	H6	VDDC	Power	Digital Core Power Supply (see Section 7.1 Power Architecture)
28	E3	GPIO3	Digital I/O, Programmable Pull-up	• GPIO3(1)/UART_RxD • By default, acts as a UART receive input to ATWILC1000B • Used only for development debug purposes; It is recommended to add test point for this pin
29	D3	GPIO4	Digital I/O, Programmable Pull-up	GPIO4(2)

.....continued

QFN Pin Number	WLCSP Pin Number	Pin Name	Pin Type	Description
30	B2	GPIO5	Digital I/O, Programmable Pull-up	• GPIO5(2)/UART_TxD • By default, acts as a UART transmit output from ATWILC1000B • Used only for development debug purposes; It is recommended to add test point for this pin
31	A1	GPIO6	Digital I/O, Programmable Pull-up	GPIO6(2)
32	A2	I2C_SCL	Digital I/O, Programmable Pull-up	• I^2C slave clock • Used only for development debug purposes; It is recommended to add test point for this pin
33	B3	I2C_SDA	Digital I/O, Programmable Pull-up	• I^2C slave data • Used only for development debug purposes; It is recommended to add test point for this pin
34	A3	RESETN	Digital Input	• Active-low hard Reset • Assert low to place the device in Reset state • Assert high to put the device in Normal state and move it out of Reset state • Connect to a host output that has default low at power-up; if the host output is tri-stated, add a 1 MΩ pull-down resistor to ensure a low level at power-up
35	A4	XO_N	Analog	Crystal Oscillator N
36	B4	XO_P	Analog	Crystal Oscillator P
37	A6	VDD_SXDIG	Power	SX Power Supply (see Section 7.1 Power Architecture)
38	—	VDD_VCO	Power	VCO Power Supply (see Section 7.1 Power Architecture)
39	A7	VDDIO_A	Power	Tuner VDDIO Power Supply (see Section 7.1 Power Architecture)
40	B6	TP_N	Analog	Test Pin/No Connect
41(1)	—	PADDLE VSS	Ground	Connect to System Board Ground
—	A5	GND_SXDIG	Ground	SX Ground, Connect to System Board Ground
—	B1	GPIO16	Digital I/O, Programmable Pull-up	GPIO16(2)
—	B5	GND_IO	Ground	I/O Ground, Connect to System Board Ground
—	B8	NC	None	Reserved/No Connect
—	C2	GPIO15	Digital I/O, Programmable Pull-up	GPIO15(2)

.....continued

QFN Pin Number	WLCSP Pin Number	Pin Name	Pin Type	Description
—	C3	GPIO17	Digital I/O, Programmable Pull-up	GPIO17(2)
—	C4	GPIO18	Digital I/O, Programmable Pull-up	GPIO18(2)
—	C5	GPIO13	Digital I/O, Programmable Pull-up	GPIO13(2)
—	C7	GND_RF_RX	Ground	RF Rx Ground, Connect to System Board Ground
—	D8	GND_BATT_PPA	Ground	PA 2nd Stage Ground, Connect to System Board Ground
—	E1	VSS	Ground	Connect to System Board Ground
—	E7	GND_BATT_PA	Ground	PA 1st Stage Ground, Connect to System Board Ground
—	F1	GND_BIAS	Ground	Bias Ground, Connect to System Board Ground
—	F7	GND_AMS	Ground	AMS Ground, Connect to System Board Ground
—	F8	TX_P	Analog	Positive RF Differential I/O
—	G1	GND_BUCK	Ground	DC/DC Converter Ground, Connect to System Board Ground
—	G6	GPIO12	Digital I/O, Programmable Pull-up	GPIO12(2)
—	G8	TX_N	Analog	Negative RF Differential I/O
—	H4	VSS	Ground	Connect to System Board Ground
—	H7	GPIO11	Digital I/O, Programmable Pull-up	GPIO11(2)

Notes:

1. Applies to QFN package only. Pin 41, PADDLE_VSS must be soldered to GND for good RF grounding and good power dissipation.
2. Use of the GPIO functionality is not supported by the ATWILC1000B firmware. The data sheet will be updated once the support for this feature is added.

2.3 Package Description

The ATWILC1000B QFN package information is provided in the following table and the package view is shown in 11. Package Drawing Outline.

Table 2-2. QFN Package Information

Parameter	Value	Unit	Tolerance
Package size	5 x 5	mm	±0.1 mm
QFN pad count	40	—	—

.....continued			
Parameter	**Value**	**Unit**	**Tolerance**
Total thickness	0.85	mm	+0.15/-0.05 mm
QFN pad pitch	0.40		—
Pad width	0.20		±0.05 mm
Exposed pad size	3.7 x 3.7		—

The ATWILC1000B WLCSP package information is provided in the following table and the package view is shown in the 11. Package Drawing Outline.

Table 2-3. WLCSP Package Information

Parameter	Value	Unit	Tolerance
Package size	3.24 x 3.24	mm	±0.3 mm
Total thickness	0.56		±0.3 mm
I/O Pitch	0.35		—
Ball diameter	0.20		±0.3 mm

3. Clocking

3.1 Crystal Oscillator

The following table provides the crystal oscillator parameters of the ATWILC1000B.

Table 3-1. Crystal Oscillator Parameters

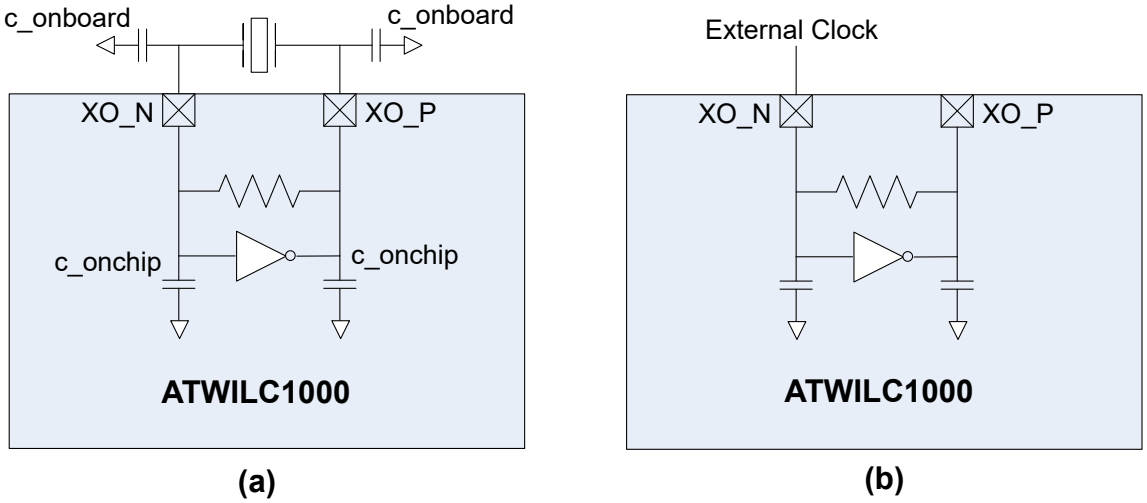
Parameter	Min.	Typ.	Max.	Unit
Crystal resonant frequency	–	26	–	MHz
Crystal equivalent series resistance	–	50	150	Ω
Stability – Initial offset(1)	-100	–	100	ppm
Stability - Temperature and aging	-25	–	25	

Note:

1. To ensure ±25 ppm under operating conditions, frequency offset calibration is required.

The following block diagram in figure "XO Connections - (a)" shows how the internal Crystal Oscillator (XO) is connected to the external crystal. The XO has 5 pF internal capacitance, (denoted as c_onchip in the following figure) on each terminal XO_P and XO_N. To bypass the crystal oscillator with an external reference, an external signal capable of driving 5 pF can be applied to the XO_N terminal as shown in following figure "XO Connections - (b)". The XO has 5 pF internal capacitance on each terminal XO_P and XO_N. This internal capacitance must be accounted for when calculating the external loading capacitance, c_onboard, for the XTAL.

Figure 3-1. XO Connections: (a) The Crystal Oscillator is Used, (b) The Crystal Oscillator is Bypassed



The following table specifies the electrical and performance requirements for the external clock.

Table 3-2. Bypass Clock Specification

Parameter	Min.	Typ.	Max.	Unit	Comments
Oscillation frequency	–	26	–	MHz	Must drive 5 pF load at desired frequency
Voltage swing	0.5	–	1.2	V_{PP}	Must be AC coupled

.....continued					
Parameter	**Min.**	**Typ.**	**Max.**	**Unit**	**Comments**
Stability – Temperature and aging	-25	–	+25	ppm	–
Phase noise	–	–	-130	dBc/Hz	At 10 kHz offset
Jitter (RMS)	–	–	<1	psec	Based on integrated phase noise spectrum from 1 kHz to 1 MHz

3.2 Low-Power Oscillator

The ATWILC1000B has an internally-generated 32 kHz clock to provide timing information for various sleep functions. Alternatively, the ATWILC1000B allows for an external 32 kHz clock to be used for this purpose, which is provided through pin 24 (RTC_CLK). Software selects whether the internal clock or external clock is used.
Note: The current software implementation does not require a 32.768 kHz clock.

The internal low-power clock is ring oscillator-based and has accuracy within 10,000 ppm. When using the internal low-power clock, the advance wake-up time in the Beacon Monitoring mode has to be increased by about 1% of the sleep time to compensate for the oscillator inaccuracy. For example, for the DTIM interval value of 1, wake-up time has to be increased by 1 ms.

4. CPU and Memory Subsystem

4.1 Processor

The ATWILC1000B has a Cortus APS3 32-bit processor. This processor performs many of the MAC functions, including but not limited to: association, authentication, power management, security key management, and MSDU aggregation/de-aggregation. In addition, the processor provides flexibility for various modes of operation, such as STA and AP modes.

4.2 Memory Subsystem

The APS3 core uses a 128 KB instruction/boot ROM along with a 160 KB instruction RAM and a 64 KB data RAM. In addition, the device uses a 128 KB shared RAM, accessible by the processor and MAC, which allows the APS3 core to perform various data management tasks on the TX and RX data packets.

4.3 Nonvolatile Memory (eFuse)

The ATWILC1000B IC has 768 bits of nonvolatile eFuse memory that can be read by the CPU after a device Reset. The eFuse is partitioned into six 128-bit banks (Bank 0 – Bank 5). Each bank has the same bit map (see the following figure). The purpose of the first 108 bits in each bank is fixed and the remaining 20 bits are general-purpose software-dependent bits, or reserved for future use.

Note: Bank 2 must not be used if the IQ Amp Used, IQ Amp Correction, IQ Pha Used and IQ Pha Correction bit fields are programmed. If it is necessary to update these bit fields, Bank 2 must not be programmed with any values and must be skipped by programming only the Bank 2 Bank Invalid bit.

This nonvolatile one-time-programmable (OTP) memory can be used for storing the following customer-specific parameters:

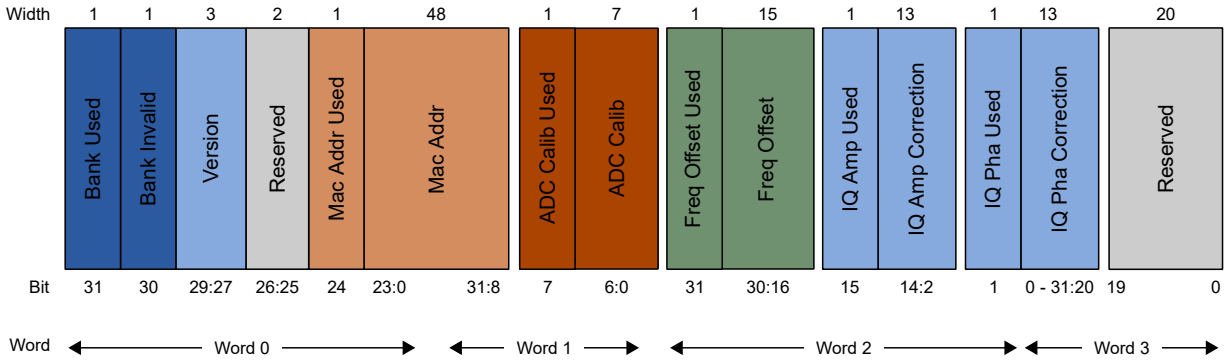
- MAC address
- Calibration information (TX power, crystal frequency offset and so on)
- Other software-specific configuration parameters

Each bank can be programmed independently, which allows for several updates of the device parameters following the initial programming. For example, if the MAC address is currently programmed in Bank 1 and the MAC address has to be changed, the following steps should be performed:

1. Invalidate the contents of Bank 1 by programming the Bank Invalid bit field of Bank 1.
2. If the IQ Amp Used, IQ Amp Correction, IQ Pha Used and IQ Pha Correction bit fields are programmed, skip Bank 2 by programming only the Bank Invalid bit of Bank 2 (see the note above).
3. Program Bank 3 with the new MAC address along with the values of ADC Calib (if used in Bank 1), Frequency Offset (from Bank 1), IQ Amp Correction (from Bank 1) and IQ Pha Correction (from Bank 1). The Used bit field for each corresponding value bit field should also be programmed.
4. Validate the contents of Bank 3 by programming the Bank Used bit field of Bank 3.

Each bit field (i.e., MAC Addr, ADC Calib, Freq Offset, IQ Amp Correction and IQ Pha Correction) has its corresponding Used bit field. Each Used bit field is used to indicate to the firmware that the value in the related bit field is valid. A value of '0' in the Used bit field indicates that the following bit field is invalid and a value of '1' programmed to the Used bit field indicates that the corresponding bit field is valid and can be used by the firmware. By default, ATWILC1000B devices are programmed with the IQ Amp and IQ Phase fields in Bank 0. In IC variants where the MAC address is assigned, the MAC address bit field will be programmed in Bank 0. For more information on IC marking, refer to Section 1. Ordering Information and IC Marking.

Figure 4-1. Bit Map for ATWILC1000B eFuse Bank



Note:

1. The bit map has been updated with the IQ Amp Correction and IQ Pha Correction bit fields from firmware version 15.3 for WILC Linux and 4.5 for WILC RTOS onwards. Earlier, these bit fields were reserved for future use. For customers using firmware older than 15.3 for WILC Linux and 4.5 for WILC RTOS, the IQ Amp Correction and IQ Pha Correction bit fields will not be used by the firmware.

The matrix table below provides details on how different versions of the firmware handle the IQ Amp Used, IQ Amp Correction, IQ Pha Used and IQ Pha Correction bit fields during Initialization.

Firmware Version	IQ Amp Used and IQ Pha Used Bit Status	
	Device with IQ Amp Used and IQ Pha Used Bit Fields with Value as '1'	**Device with IQ Amp Used and IQ Pha Used Bit Fields with Value as '0'**
15.3 or later for WILC Linux 4.5 or later for WILC RTOS	The firmware loads the IQ calibration values from the IQ Amp Correction and IQ Pha Correction bit fields of the corresponding eFuse bank and proceeds with Initialization.	The firmware ignores the values in the IQ Amp Correction and IQ Pha Correction bit fields and proceeds with Initialization.
Prior to 15.3 for WILC Linux Prior to 4.5 for WILC RTOS	The firmware does not check for the IQ Amp Used and IQ Pha Used bit fields and proceeds with Initialization.	

5. WLAN Subsystem

The WLAN subsystem is composed of the Media Access Controller (MAC) and the Physical Layer (PHY). The following two subsections describe the MAC and PHY in detail.

5.1 MAC

5.1.1 Features

The ATWILC1000B IEEE802.11 MAC supports the following functions:

- IEEE 802.11b/g/n
- IEEE 802.11e WMM QoS EDCA/PCF Multiple Access Categories Traffic Scheduling
- Advanced IEEE 802.11n Features:
  - Transmission and reception of aggregated MPDUs (A-MPDU)
  - Transmission and reception of aggregated MSDUs (A-MSDU)
  - Immediate Block Acknowledgment
  - Reduced Interframe Spacing (RIFS)
- Support for IEEE 802.11i and WFA Security with Key Management
  - WEP 64/128
  - WPA-TKIP
  - 128-bit WPA2 CCMP (AES)
- Support for WAPI Security
- Advanced Power Management
  - Standard 802.11 Power Save mode
  - Wi-Fi Alliance® WMM-PS (U-APSD)
- RTS-CTS and CTS-Self Support
- Supports Either STA or AP Mode in the Infrastructure Basic Service Set Mode
- Supports Independent Basic Service Set (IBSS)

5.1.2 Description

The ATWILC1000B MAC is designed to operate at low power while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated datapath engines, hardwired control logic, and a low-power, high-efficiency microprocessor. The combination of dedicated logic with a programmable processor provides optimal power efficiency and real-time response while providing the flexibility to accommodate evolving standards and future feature enhancements.

Dedicated datapath engines with heavy computational are used to implement datapath functions. For example, an FCS engine checks the CRC of the transmitting and receiving packets, and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP, WPA2 CCMP-AES, and WAPI security requirements.

Control functions which have real-time requirements are implemented using hardwired control logic modules. These logic modules offer real-time response while maintaining configurability via the processor. Examples of hardwired control logic modules are: the channel access control module (implements EDCA/HCCA, Beacon TX control, interframe spacing, and so on.), protocol timer module (responsible for the Network Access Vector, back-off timing, timing synchronization function, and slot management), MPDU handling module, aggregation/deaggregation module, block ACK controller (implements the protocol requirements for burst block communication), and TX/RX control FSMs (coordinate data movement between PHY-MAC interface, cipher engine, and the DMA interface to the TX/RX FIFOs).

The MAC functions that are implemented in software on the microprocessor have the following characteristics:

- Functions with high memory requirements or complex data structures. Examples are association table management and power save queuing.
- Functions with low computational load or without critical real-time requirements. Examples are authentication and association.

- Functions which need flexibility and upgradeability. Examples are beacon frame processing and QoS scheduling.

5.2 PHY

5.2.1 Features

The ATWILC1000B IEEE 802.11 PHY supports the following functions:

- Single Antenna 1x1 Stream in 20 MHz Channels
- Supports IEEE 802.11b DSSS-CCK Modulation: 1, 2, 5.5 and 11 Mbps
- Supports IEEE 802.11g OFDM Modulation: 6, 9, 12,18, 24, 36, 48 and 54 Mbps
- Supports IEEE 802.11n HT Modulations MCS0-7, 20 MHz, 800 and 400 ns guard interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0 and 72.2 Mbps(1)
- IEEE 802.11n Mixed Mode Operation
- Per Packet TX Power Control
- Advanced Channel Estimation/Equalization, Automatic Gain Control, CCA, Carrier/Symbol Recovery and Frame Detection

Note:

1. Short GI is currently not supported by Firmware. The data sheet will be updated when the feature is supported.

5.2.2 Description

The ATWILC1000B WLAN PHY is designed to achieve reliable and power-efficient physical layer communication specified by IEEE 802.11 b/g/n in Single Stream mode with 20 MHz bandwidth. Advanced algorithms are used to achieve maximum throughput in a real-world communication environment with impairments and interference. The PHY implements all the required functions such as FFT, filtering, FEC (Viterbi decoder), frequency and timing acquisition and tracking, channel estimation and equalization, carrier sensing and clear channel assessment, as well as the automatic gain control.

5.3 Radio

This section describes the properties and characteristics of the ATWILC1000B and Wi-Fi radio transmit and receive performance capabilities of the device. The performance measurements are taken at the RF pin assuming 50Ω impedance; the RF performance is assured for room temperature of 25°C with a derating of 2-3 dB at boundary conditions.

Measurements were taken under typical conditions: VBATT at 3.3V, VDDIO at 3.3V and temperature at +25ºC.

Table 5-1. Features and Properties

Feature	Description
Part Number	ATWILC1000B
WLAN Standard	IEEE 802.11b/g/n, Wi-Fi compliant
Host Interface	SPI, SDIO
Dimension	See 11. Package Drawing Outline
Frequency range	2.412 GHz ~ 2.484 GHz (2.4 GHz ISM band)
Number of channels	11 for North America, 13 for Europe, 14 for Japan
Modulation	802.11b: DQPSK, DBPSK, CCK 802.11g/n: OFDM/64-QAM,16-QAM, QPSK, BPSK

.....continued

Feature	Description
Data rate	802.11b: 1, 2, 5.5, 11 Mbps 802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps
Data rate (20 MHz, short GI, 400 ns)(1)	802.11n: 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65, 72.2 Mbps
Operating temperature(2)	-40°C to 85°C
Storage temperature	-40°C to 125°C
Humidity	Operating humidity: 10% to 95% non-condensing Storage humidity: 5% to 95% non-condensing

Notes:

1. Short GI is currently not supported by Firmware. The data sheet will be updated when the feature is supported.
2. RF performance is assured at room temperature of 25°C with a 2-3 db change at boundary conditions.

6. External Interfaces

The ATWILC1000B external interfaces include:

- I^2C for debug
- SPI and SDIO for control and data transfer
- UART for debug
- General Purpose Input/Output (GPIO) pins(1)

Note: Usage of the GPIO functionality is not supported by the ATWILC1000B firmware. The data sheet will be updated once the support for this feature is added.

6.1 Interfacing with the Host Microcontroller

This section describes how to interface the ATWILC1000B device with the host microcontroller. The interface is comprised of a slave SPI/SDIO and additional control signals, as shown in the following figure. Additional control signals are connected to the GPIO/IRQ interface of the microcontroller.

Figure 6-1. Interfacing with the Host Microcontroller

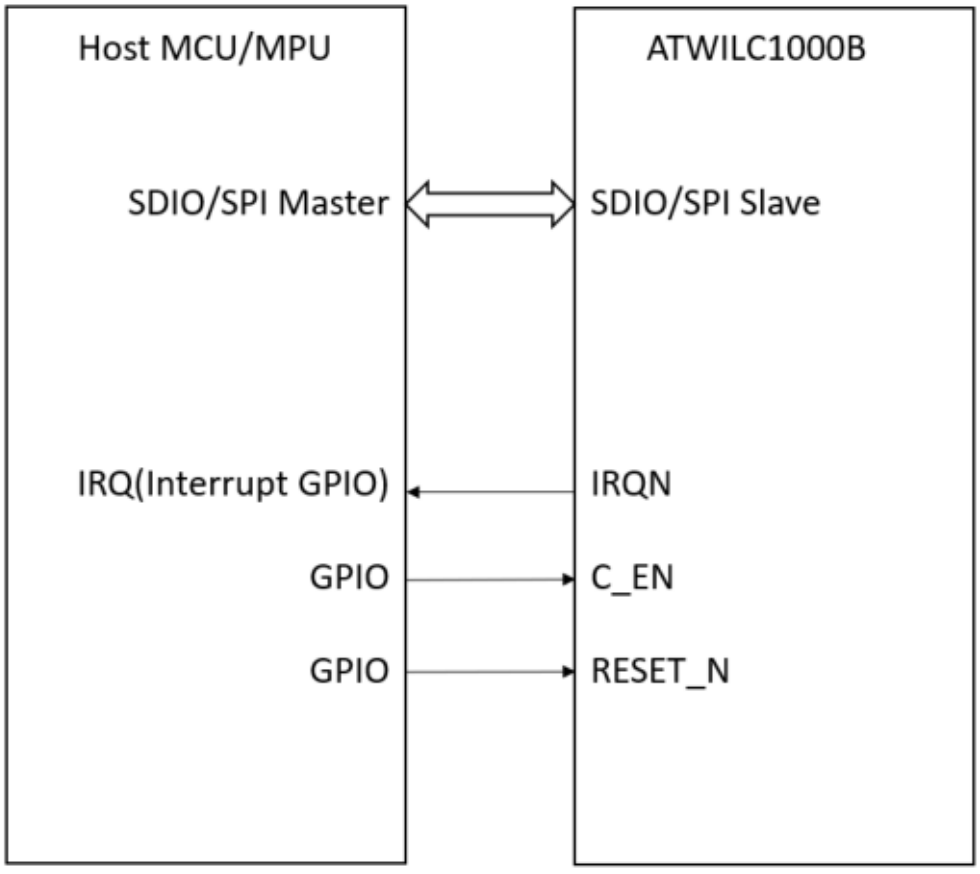


Table 6-1. Host Microcontroller Interface Pins

QFN Pin Number	WLCSP Pin Number	Function
11	F5	IRQN
12	F4	SD_DAT3

.....continued		
QFN Pin Number	**WLCSP Pin Number**	**Function**
13	G5	SD_DAT2/SPI_MOSI
16	G4	SD_DAT1/SPI_SSN
17	G3	SD_DAT0/SPI_MISO
18	H3	SD_CMD/SPI_CLK
19	G2	SD_CLK
23	F2	CHIP_EN
34	A3	RESETN

6.2 SPI Slave Interface

The ATWILC1000B provides a Serial Peripheral Interface (SPI) that operates as an SPI slave. The SPI Slave interface can be used for control and for serial I/O of 802.11 data. The SPI Slave pins are mapped as shown in the the following table. The RXD pin is same as Master Output, Slave Input (MOSI), and the TXD pin is same as Master Input, Slave Output (MISO). The SPI Slave is a full-duplex, slave-synchronous serial interface that is available immediately following reset when pin 9 (SDIO_SPI_CFG) is tied to VDDIO.

Table 6-2. SPI Slave Interface Pin Mapping

Pin Number	SPI Function
9	CFG: Must be tied to VDDIO
16	SSN: Active Low Slave Select
18	SCK: Serial Clock
13	RXD: Serial Data Receive (MOSI)
17	TXD: Serial Data Transmit (MISO)

When the SPI is not selected (i.e., when SSN is high), the SPI interface does not interfere with data transfers between the serial-master and other serial-slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the serial master receive line.

The SPI Slave interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiate DMA transfers.

The SPI Slave interface supports four standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are illustrated in the SPI Slave Modes table and Figure 6-2. The red lines in this figure correspond to Clock Phase = 0 and the blue lines correspond to Clock Phase = 1.

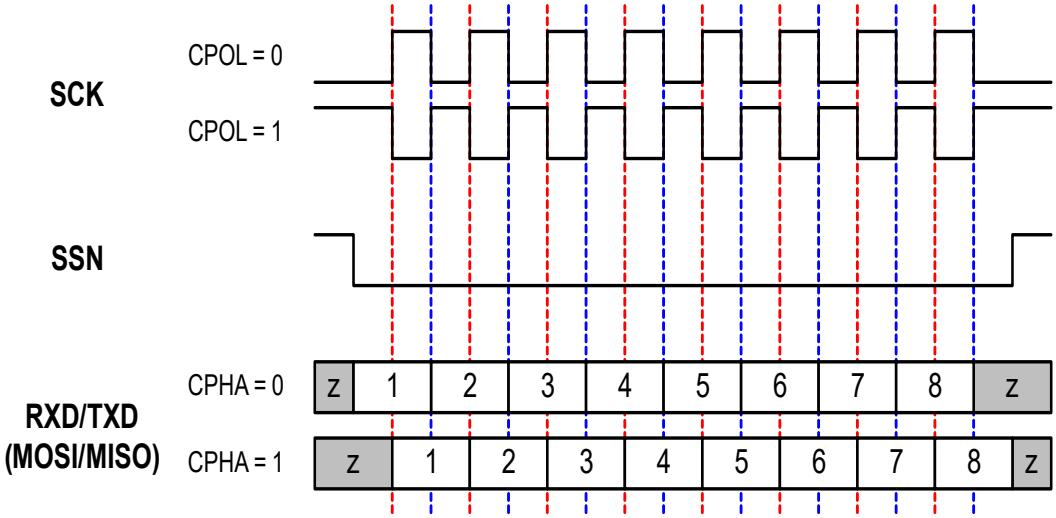
Table 6-3. SPI Slave Modes

Mode	CPOL	CPHA
0(1)	0	0
1	0	1
2	1	0
3	1	1

Note:

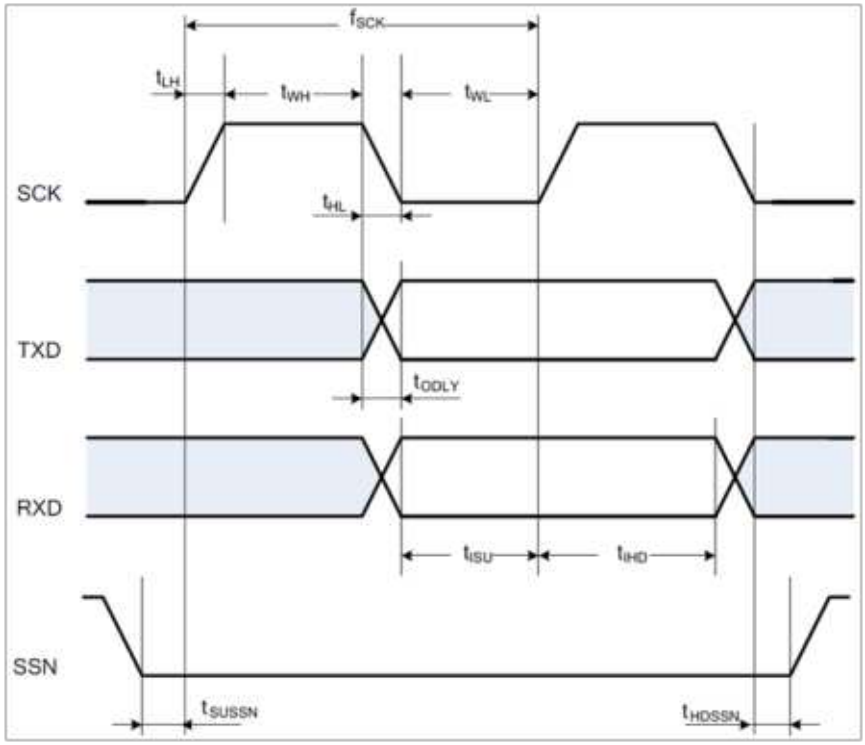
1. The ATWILC1000 firmware uses SPI Mode 0 to communicate with the host.

Figure 6-2. SPI Slave Clock Polarity and Clock Phase Timing



The SPI slave timing is provided in the following figure.

Figure 6-3. SPI Slave Timing Diagram



The SPI slave timing parameters are provided in the following table.

Table 6-4. SPI Slave Timing Parameters(1)

Parameter	Symbol	Min.	Max.	Units
Clock Input Frequency[2]	f_{SCK}	—	48	MHz

.....continued				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**
Clock Low Pulse Width	t_{WL}	4	—	ns
Clock High Pulse Width	t_{WH}	5	—	
Clock Rise Time	t_{LH}	0	7	
Clock Fall Time	t_{HL}	0	7	
TXD Output Delay[3]	t_{ODLY}	4	9 from SCK fall	
RXD Input Setup Time	t_{ISU}	1	—	
RXD Input Hold Time	t_{IHD}	5	—	
SSN Input Setup Time	t_{SUSSN}	3	—	
SSN Input Hold Time	t_{HDSSN}	5.5	—	

Notes:

1. Timing is applicable to all SPI modes.
2. Maximum clock frequency specified is limited by the SPI slave interface internal design; actual maximum clock frequency can be lower and depends on the specific PCB layout.
3. Timing is based on 15 pF output loading. Under all conditions, $t_{LH} + t_{WH} + t_{HL} + t_{WL}$ must be less than or equal to $1/ f_{SCK}$.

6.3 SDIO Slave Interface

The ATWILC1000B SDIO Slave is a full speed interface. The interface supports the 1-bit/4-bit SD Transfer mode at the clock range of 0 to 50 MHz. The host can use this interface to read and write from any register within the chip as well as configure the ATWILC1000B for data DMA. To use this interface, pin 9 (SDIO_SPI_CFG) must be grounded. The SDIO slave pins are mapped as shown in the following table.

Table 6-5. SDIO Interface Pin Mapping

Pin Number	SPI Function
9	CFG: Must be tied to ground
12	DAT3: Data 3
13	DAT2: Data 2
16	DAT1: Data 1
17	DAT0: Data 0
18	CMD: Command
19	CLK: Clock

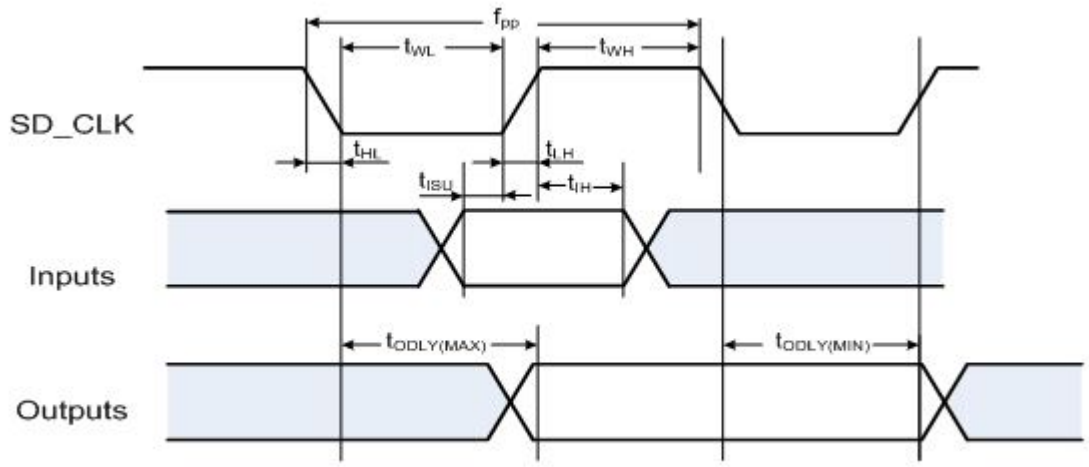
When the SDIO card is inserted into an SDIO aware host, the detection of the card will be via the means described in SDIO specification. During the normal initialization and interrogation of the card by the host, the card identifies itself as an SDIO device. The host software obtains the card information in a tuple (linked list) format and determines if that card's I/O function(s) are acceptable to activate. If the card is acceptable, it is allowed to power-up fully and start the I/O function(s) built into it. The SD memory card communication is based on an advanced 9-pin interface (clock, command, four data and three power lines) designed to operate at a maximum operating frequency of 50 MHz. The SDIO slave interface has the following features:

- Meets SDIO card specification version 2.0
- Host clock rate variable between 0 to 50 MHz
- 1-bit/4-bit SD bus modes supported

- Allows card to interrupt host
- Responds to direct read/write (IO52) and extended read/write (IO53) transactions
- Supports Suspend/Resume operation

The SDIO slave interface timing is provided in the following figure.

Figure 6-4. SDIO Slave Timing Diagram



The SDIO slave timing parameters are provided in the following table.

Table 6-6. SDIO Timing Parameters

Parameter	Symbol	Min.	Max.	Units
Clock Input Frequency(1)	f_{PP}	0	50	MHz
Clock Low Pulse Width	t_{WL}	9	—	ns
Clock High Pulse Width	t_{WH}	4.5	—	
Clock Rise Time	t_{LH}	0	5	
Clock Fall Time	t_{HL}	0	5	
Input Setup Time	t_{ISU}	6	—	
Input Hold Time	t_{IH}	4	—	
Output Delay(2)	t_{ODLY}	3	11	

Notes:

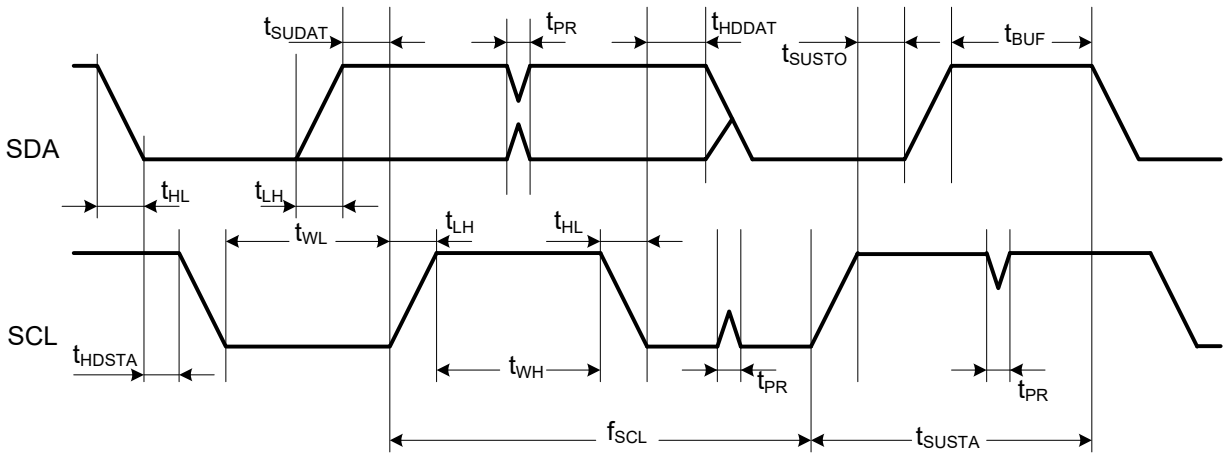
1. Maximum clock frequency specified is limited by the SDIO Slave interface internal design; actual maximum clock frequency can be lower and depends on the specific PCB layout.
2. Timing based on 15 pF output loading.

6.4 I²C Slave Interface

The I²C Slave interface, primarily used for debugging, is a 2-wire serial interface consisting of a serial data line (SDA, Pin 33) and a serial clock (SCL, pin 32). It responds to the seven bit address value 0x60. The ATWILC1000B I²C supports I²C bus Version 2.1 - 2000 and can operate in Standard mode (with data rates up to 100 Kb/s) and Fast mode (with data rates up to 400 Kb/s). The I²C Slave is a synchronous serial interface. The SDA line is a bidirectional signal and changes only while the SCL line is low, except for STOP, START and RESTART conditions. The output drivers are open-drain to perform wire-AND functions on the bus. The maximum number of devices on the bus is limited only by the maximum capacitance specification of 400 pF. Data is transmitted in byte packages. For specific

information, refer to the Philips Specification entitled “The I²C -Bus Specification, Version 2.1”. The I²C Slave timing is provided in the following figure.

Figure 6-5. I²C Slave Timing Diagram



The I²C Slave timing parameters are provided in the following table.

Table 6-7. I²C Slave Timing Parameters

Parameter	Symbol	Min.	Max.	Unit	Remarks
SCL clock frequency	f_{SCL}	0	400	kHz	—
SCL low pulse width	t_{WL}	1.3	—	µs	—
SCL high pulse width	t_{WH}	0.6	—		—
SCL, SDA fall time	t_{HL}	—	300	ns	—
SCL, SDA rise time	t_{LH}	—	300		This is dictated by external components
START setup time	t_{SUSTA}	0.6	—	µs	—
START hold time	t_{HDSTA}	0.6	—		—
SDA setup time	t_{SUDAT}	100	—	ns	—
SDA hold time	t_{HDDAT}	0 40	—		Slave and master default master programming option
STOP setup time	t_{SUSTO}	0.6	—	µs	—
Bus free time between STOP and START	t_{BUF}	1.3	—		—
Glitch pulse reject	t_{PR}	0	50	ns	—

6.5 UART Debug Interface

ATWILC1000B has a Universal Asynchronous Receiver/Transmitter (UART) interface on pin 28 (UART_RxD) and pin 30 (UART_TxD). This interface should be used only for debugging purposes. The UART is compatible with the RS-232 standard, where ATWILC1000B-MUT operates as Data Terminal Equipment (DTE). It has a two-pin RXD/TXD interface.

The default configuration for accessing the UART interface of ATWILC1000B-MUT is as follows:

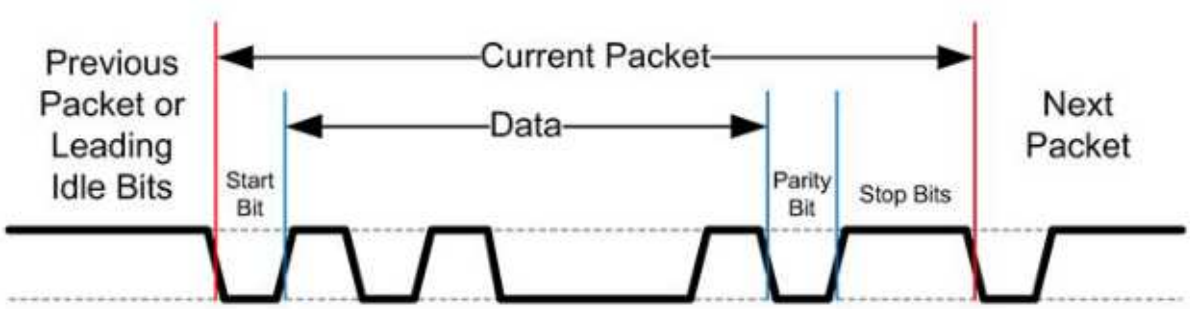
- Baud rate: 115200
- Data: 8 bit
- Parity: None
- Stop bit: 1 bit

- Flow control: None

It also has RX and TX FIFOs, which ensures reliable high speed reception and low software overhead transmission. FIFO size is 4x8 for both RX and TX direction. The UART has status registers that show the number of received characters available in the FIFO and various error conditions; in addition, it has the ability to generate interrupts based on these status bits.

An example of UART receiving or transmitting a single packet is shown in the following figure. This example shows 7-bit data (0x45), odd parity and two stop bits.

Figure 6-6. Example of UART RX or TX Packet



6.6 GPIOs

Nine General Purpose Input/Output (GPIO) pins, labeled GPIO 0-8, are available to allow for application-specific functions. Each GPIO pin can be programmed as an input (the value of the pin can be read by the host or internal processor) or as an output (the output values can be programmed by the host or internal processor), where the default mode after power-up is input. GPIOs 7 and 8 are only available when the host does not use the SDIO interface, which shares two of its pins with these GPIOs. Therefore, for SDIO-based applications, seven GPIOs (0-6) are available.

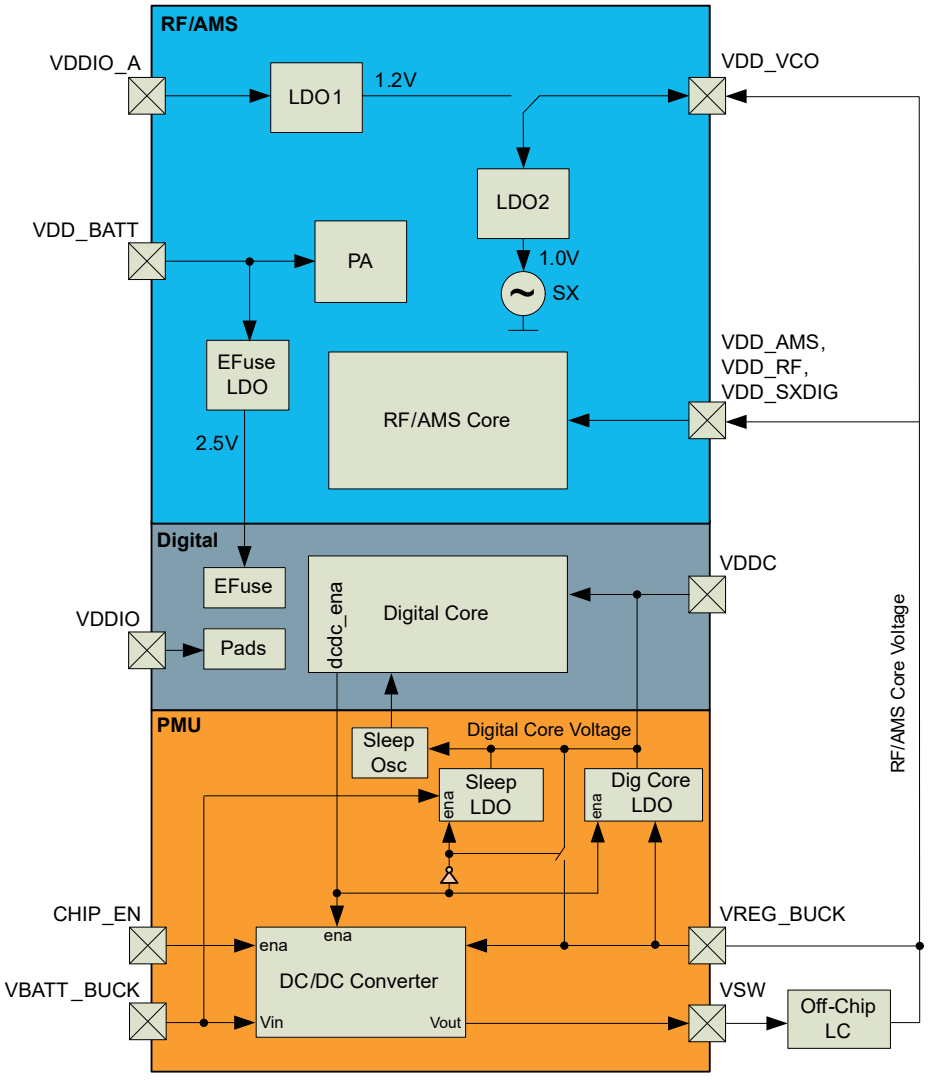
Note: Use of the GPIO functionality is not supported by the ATWILC1000 firmware. The data sheet will be updated once the support for this feature is added.

7. Power Management

7.1 Power Architecture

The ATWILC1000B uses an innovative power architecture to eliminate the need for external regulators and reduce the number of off-chip components. This architecture is shown in the following figure. The Power Management Unit (PMU) has a DC/DC Converter that converts VBATT to the core supply used by the digital and RF/AMS blocks. The PA and eFuse are supplied by dedicated LDOs, and the VCO is supplied by a separate LDO structure. The power connections in the following figure provide a conceptual framework for understanding the ATWILC1000B power architecture.

Figure 7-1. Power Architecture



The following table provides the typical values for the digital and RF/AMS core voltages.

Table 7-1. PMU Output Voltages

Parameter	Typical
RF/AMS core voltage (VREG_BUCK)	1.25V

.....continued	
Parameter	**Typical**
Digital core voltage (VDDC)	1.10V

Refer to the reference design for an example of power supply connections, including proper isolation of the supplies used by the digital and RF/AMS blocks.

7.2 Power Consumption

The ATWILC1000B has several device states:

- ON_Transmit – Device is actively transmitting an 802.11 signal
- ON_Receive – Device is actively receiving an 802.11 signal
- ON_Doze – Device is on but is neither transmitting nor receiving
- Power_Down – Device core supply off (leakage)

The following pins are used to switch between the ON and Power_Down states:

- CHIP_EN – Device pin (pin 23) used to enable DC/DC Converter
- VDDIO – I/O supply voltage from external supply

In the ON states, VDDIO is on and CHIP_EN is high (at VDDIO voltage level). To switch between the ON states and Power_Down state, CHIP_EN has to change between high and low (GND) voltage. When VDDIO is off and CHIP_EN is low, the chip is powered off with no leakage (also see Sections 7.2.1 Restrictions for Power States and 8.4 Current Consumption in Various Device States).

7.2.1 Restrictions for Power States

When no power is supplied to the device, i.e., the DC/DC converter output and VDDIO are both off (at ground potential). In this case, a voltage cannot be applied to the device pins because each pin contains an ESD diode from the pin to supply. This diode turns on when voltage higher than one diode-drop is supplied to the pin.

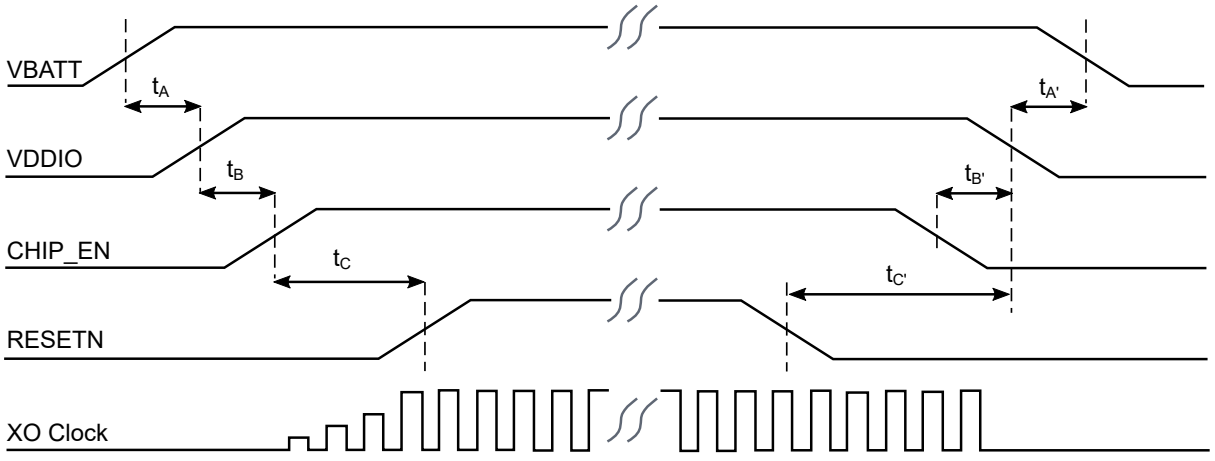
If a voltage must be applied to the signal pads while the chip is in a low power state, the VDDIO supply must be on, so the SLEEP or Power_Down state must be used.

Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode-drop below ground to any pin.

7.3 Power-Up/Down Sequence

The following figure illustrates the power-up/down sequence for the ATWILC1000B.

Figure 7-2. Power-Up/Down Sequence



The following table provides power-up/down sequence timing parameters.

Table 7-2. Power-Up/Down Sequence Timing

Parameter	Min.	Max.	Units	Description	Notes
t_A	0	—	ms	VBAT rise to VDDIO rise	VBAT and VDDIO can rise simultaneously or connected together. VDDIO must not rise before VBAT.
t_B	0	—	ms	VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low and must not be left floating.
t_C	5	—	ms	CHIP_EN rise to RESETN rise	This delay is required to stabilize the XO clock before RESETN removal. RESETN must be driven high or low and must not be left floating.
$t_{A'}$	0	—	ms	VDDIO fall to VBAT fall	VBAT and VDDIO must fall simultaneously or be connected together. VBAT must not fall before VDDIO.
$t_{B'}$	0	—	ms	CHIP_EN fall to VDDIO fall	VDDIO must not fall before CHIP_EN. CHIP_EN and RESETN must fall simultaneously.
$t_{C'}$	0	—	ms	RESETN fall to VDDIO fall	VDDIO must not fall before RESETN. RESETN and CHIP_EN fall simultaneously.

7.4 Digital I/O Pin Behavior During Power-Up Sequences

The following table represents digital I/O pin states corresponding to device power modes.

Table 7-3. Digital I/O Pin Behavior in Different Device States

Device State	VDDIO	CHIP_EN	RESETN	Output Driver	Input Driver	Pull-Up/Down Resistor(1)
Power_Down: core supply off	High	Low	Low	Disabled (Hi-Z)	Disabled	Disabled(2)
Power-On Reset: core supply on, hard reset on	High	High	Low	Disabled (Hi-Z)	Disabled	Enabled
Power-On Default: core supply on, device out of reset but not programmed yet	High	High	High	Disabled (Hi-Z)	Enabled	Enabled
On_Doze/ On_Transmit/ On_Receive: core supply on, device programmed by firmware	High	High	High	Programmed by firmware for each pin: Enabled or Disabled	Opposite of output driver state	Programmed by firmware for each pin: Enabled or Disabled

Notes:

1. Pull-up/down resistor value is 96kΩ ±10%.
2. Exceptions: pull-up resistors are enabled for the GPIO15-18 pins (WLCSP package only) in Power_Down state.

8. Electrical Specifications

8.1 Absolute Ratings

The values listed in this section are the peaked excursions ratings that can be tolerated by the device, and if sustained will cause irreparable damage to the device.

Table 8-1. Absolute Maximum Ratings

Characteristics	Symbol	Min.	Max.	Unit
Core supply voltage	VDDC	-0.3	1.5	V
I/O supply voltage	VDDIO	-0.3	5.0	
Battery supply voltage	VBATT	-0.3	5.0	
Digital input voltage	V_{IN} (1)	-0.3	VDDIO	
Analog input voltage	V_{AIN} (2)	-0.3	1.5	
ESD human body model	V_{ESDHBM} (3)	-1000, -2000 (3)	+1000, +2000 (3)	
Storage temperature	T_A	-65	150	ºC
Junction temperature	–	–	125	
RF input power max.	–	–	23	dBm

Notes:

1. V_{IN} corresponds to all the digital pins.
2. V_{AIN} corresponds to the following analog pins: VDD_RF_RX, VDD_RF_TX, VDD_AMS, RFIOP, RFION, XO_N, XO_P, VDD_SXDIG, and VDD_VCO.
3. For V_{ESDHBM}, each pin is classified as Class 1, or Class 2, or both:
   - The Class 1 pins include all the pins (both analog and digital).
   - The Class 2 pins are all digital pins only.
   - V_{ESDHBM} is ±1 kV for Class 1 pins. V_{ESDHBM} is ±2 kV for Class 2 pins.

8.2 Recommended Operating Conditions

The recommended operating conditions for the ATWILC1000B are listed in the following table.

Table 8-2. Recommended Operating Conditions

Characteristics	Symbol	Min.	Typ.	Max.	Unit
I/O Supply Voltage Low Range	$VDDIO_L$	1.62	1.80	2.00	V
I/O Supply Voltage Mid-Range	$VDDIO_M$	2.00	2.50	3.00	
I/O Supply Voltage High Range	$VDDIO_H$	3.00	3.30	3.60	
Battery Supply Voltage	VBATT	3.00	3.30	4.2	
Operating Temperature	—	-40	—	85	ºC

Notes:

1. The ATWILC1000B is functional across this range of voltages; however, optimal RF performance is assured for VBATT in the range 3.0V < VBATT < 3.6V.
2. I/O supply voltage is applied to the VDDIO_A and VDDIO pins.
3. Battery supply voltage is applied to the VDD_BATT_PPA, VDD_BATT_PA and VBATT_BUCK pins.
4. See Section 7.3 Power-Up/Down Sequence for the details of power-up/down sequence and Section 7.1 Power Architecture for power connections.

8.3 DC Electrical Characteristics

The following table provides the DC characteristics for the ATWILC1000B digital pads.

Table 8-3. DC Electrical Characteristics

VDDIO Condition	Characteristic	Min.	Typ.	Max.	Unit
$VDDIO_L$	Input Low Voltage (V_{IL})	-0.30	—	0.60	V
	Input High Voltage (V_{IH})	VDDIO-0.60	—	VDDIO+0.30	
	Output Low Voltage (V_{OL})	—	—	0.45	
	Output High Voltage (OV_{OH})	VDDIO-0.50	—	—	
$VDDIO_M$	Input Low Voltage (V_{IL})	-0.30	—	0.63	
	Input High Voltage (V_{IH})	VDDIO-0.60	—	VDDIO+0.30	
	Output Low Voltage (V_{OL})	—	—	0.45	
	Output High Voltage (OV_{OH})	VDDIO-0.50	—	—	
$VDDIO_H$	Input Low Voltage (V_{IL})	-0.30	—	0.65	
	Input High Voltage (V_{IH})	VDDIO-0.60	—	VDDIO+0.30 (up to 3.60)	
	Output Low Voltage (V_{OL})	—	—	0.45	
	Output High Voltage (OV_{OH})	VDDIO-0.50	—	—	
All	Output Loading	—	—	20	pF
All	Digital Input Load	—	—	6	

.....continued					
VDDIO Condition	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Unit**
$VDDIO_L$	Pad Drive Strength (regular pads (1))	1.7	2.4	—	mA
$VDDIO_M$	Pad Drive Strength (regular pads (1))	3.4	6.5	—	
$VDDIO_H$	Pad Drive Strength (regular pads (1))	10.6	13.5	—	
$VDDIO_L$	Pad Drive Strength (high-drive pads (1))	3.4	4.8	—	
$VDDIO_M$	Pad Drive Strength (high-drive pads (1))	6.8	13	—	
$VDDIO_H$	Pad Drive Strength (high-drive pads (1))	21.2	27	—	

Note:

1. The following are high-drive pads: I2C_SCL, I2C_SDA; all other pads are regular.

8.4 Current Consumption in Various Device States

The following table provides the ATWILC1000B current consumption in various device states.

Table 8-4. Current Consumption

Device State	Code Rate	Output Power (dBm)	Current Consumption(1, 2)	
			I_{VBATT}	I_{VDDIO}
ON_Transmit	802.11b 1 Mbps	17.6	266 mA	22 mA
	802.11b 11 Mbps	18.5	239 mA	22 mA
	802.11g 6 Mbps	18.6	249 mA	22 mA
	802.11g 54 Mbps	16.9	173 mA	22 mA
	802.11n MCS 0	17.7	253 mA	22 mA
	802.11n MCS 7	14.0	164 mA	22 mA
ON_Receive	802.11b 1 Mbps	N/A	63 mA	22 mA
	802.11b 11 Mbps	N/A	63 mA	22 mA
	802.11g 6 Mbps	N/A	63 mA	22 mA
	802.11g 54 Mbps	N/A	63 mA	22 mA
	802.11n MCS 0	N/A	63 mA	22 mA
	802.11n MCS 7	N/A	63 mA	22 mA

.....continued				
Device State	Code Rate	Output Power (dBm)	Current Consumption(1, 2)	
			I_{VBATT}	I_{VDDIO}
ON_Doze	N/A	N/A	380 µA	<10 µA
Power_Down	N/A	N/A	1.25 µA (3)	

Notes:

1. The power consumption values are measured when VBAT is 3.3V and VDDIO is 3.3V at 25°C.
2. The current consumption in the Active TX state occurs with a Duty cycle configuration - 5.
3. The current consumption mentioned for these states is the sum of the current consumed in the VDDIO and VBAT voltage rails.

8.5 Wi-Fi Performance Characteristics

8.5.1 Receiver Performance

The following are typical conditions for radio receiver performance:

VBATT at 3.3V, VDDIO at 3.3V, temperature at 25°C and WLAN Channel 6 (2437 MHz).

The following table provides the receiver performance characteristics for the ATWILC1000B.

Table 8-5. Receiver Performance

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	—	2,412	—	2,484	MHz
Sensitivity 802.11b	1 Mbps DSSS	—	-94	—	dBm
	2 Mbps DSSS	—	-91	—	
	5.5 Mbps DSSS	—	-89	—	
	11 Mbps DSSS	—	-86	—	
Sensitivity 802.11g	6 Mbps OFDM	—	-88	—	dBm
	9 Mbps OFDM	—	-87	—	
	12 Mbps OFDM	—	-86	—	
	18 Mbps OFDM	—	-84	—	
	24 Mbps OFDM	—	-82	—	
	36 Mbps OFDM	—	-78	—	
	48 Mbps OFDM	—	-74	—	
	54 Mbps OFDM	—	-73	—	

.....continued					
Parameter	**Description**	**Min.**	**Typ.**	**Max.**	**Unit**
Sensitivity 802.11n (BW at 20 MHz)	MCS 0	—	-87	—	dBm
	MCS 1	—	-85	—	
	MCS 2	—	-83	—	
	MCS 3	—	-80	—	
	MCS 4	—	-76	—	
	MCS 5	—	-73	—	
	MCS 6	—	-71	—	
	MCS 7	—	-69	—	
Maximum Receive Signal Level	1-11 Mbps DSSS	—	0	—	dBm
	6-54 Mbps OFDM	—	-5	—	
	MCS 0 – 7	—	-5	—	
Adjacent Channel Rejection	1 Mbps DSSS (30 MHz offset)	—	50	—	dB
	11 Mbps DSSS (25 MHz offset)	—	43	—	
	6 Mbps OFDM (25 MHz offset)	—	40	—	
	54 Mbps OFDM (25 MHz offset)	—	25	—	
	MCS 0 – 20 MHz BW (25 MHz offset)	—	40	—	
	MCS 7 – 20 MHz BW (25 MHz offset)	—	20	—	
Cellular Blocker Immunity	776-794 MHz CDMA	—	-14	—	dBm
	824-849 MHz GSM	—	-10	—	
	880-915 MHz GSM	—	-10	—	
	1710-1785 MHz GSM	—	-15	—	
	1850-1910 MHz GSM	—	-15	—	
	1850-1910 MHz WCDMA	—	-24	—	
	1920-1980 MHz WCDMA	—	-24	—	

8.5.2 Transmitter Performance

The following are typical conditions for radio transmitter performance:

VBAT at 3.3V, VDDIO at 3.3V, temperature at 25°C and WLAN Channel 6 (2437 MHz).

The following table provides the transmitter performance characteristics for the ATWILC1000B.

Table 8-6. Transmitter Performance

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	—	2,412	—	2,484	MHz

.....continued

Parameter	Description	Min.	Typ.	Max.	Unit
Output power[1, 2], ON_Transmit	802.11b 1Mbps	—	13.6	—	dBm
	802.11b 11Mbps	—	15.3	—	
	802.11g 6Mbps	—	18.9	—	
	802.11g 54Mbps	—	14.3	—	
	802.11n MCS 0	—	18.9	—	
	802.11n MCS 7	—	12.2	—	
TX power accuracy	—	—	±1.5 [2]	—	dB
Carrier suppression	802.11b mode	—	-19.4	—	dBc
	802.11g mode	—	-27.5	—	
	802.11n mode	—	-21.1	—	
Out of band Transmit Power	76-108	—	-125	—	dBm/Hz
	776-794	—	-125	—	
	869-960	—	-125	—	
	925-960	—	-125	—	
	1570-1580	—	-125	—	
	1805-1880	—	-125	—	
	1930-1990	—	-125	—	
	2110-2170	—	-125	—	
Harmonic output power[4]	2nd	—	-28	—	dBm/MHz
	3rd	—	-33	—	
	4th	—	-40	—	
	5th	—	-28	—	

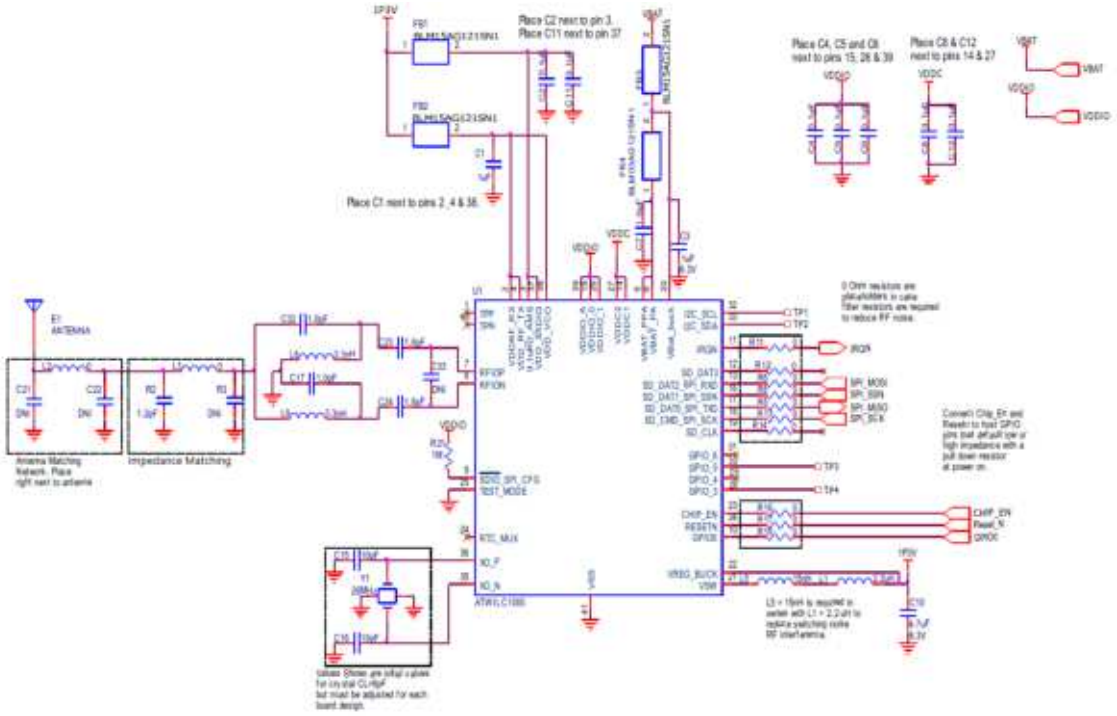
Notes:

1. Measured at 802.11 specification compliant EVM/Spectral mask.
2. Measured after RF matching network.
3. Operating temperature range is -40ºC to +85ºC. RF performance is assured at a room temperature range of 25ºC with 2-3 dB change at boundary conditions.
4. Measured at 11 Mbps, DG (Digital Gain) = -7, WLAN Channel 6 (2437 MHz).
5. With respect to TX power, different (higher/lower) RF output power settings may be used for specific antennas and/or enclosures, in which case re-certification may be required.
6. The availability of some specific channels and/or operational frequency bands are country-dependent and should be programmed at the host product factory to match the intended destination. Regulatory bodies prohibit exposing the settings to the end user. This requirement needs to be taken care of via host implementation.

9. Reference Design

This section provides the reference schematic for ATWILC1000B with SPI and SDIO host interfaces.

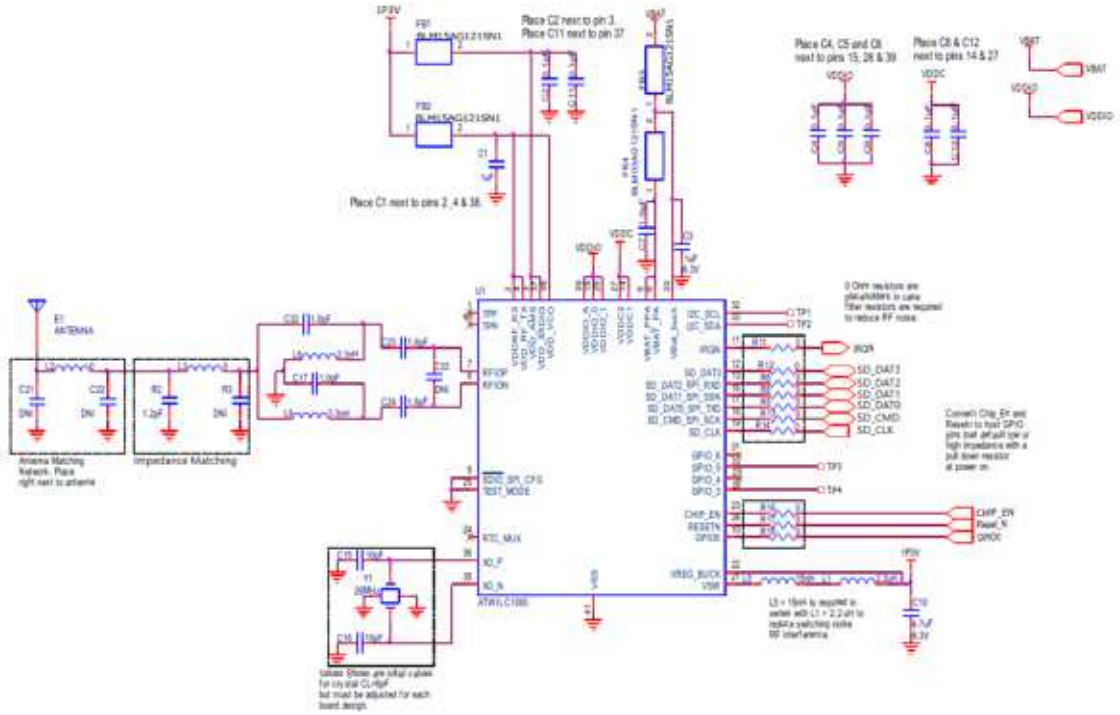
Figure 9-1. Reference Schematic - SPI Host Interface(1, 2)



Notes:

1. Add a 10uF and 0.01uF decoupling capacitor to the 1P3V net. Refer to Section 10.1.3 Power Management Unit for layout guidelines.
2. Add test points for pins 28, 30, 32 and 33.

Figure 9-2. Reference Schematic - SDIO Host Interface(1, 2)



Notes:

1. Add a 10uF and 0.01uF decoupling capacitor to the 1P3V net. Refer to Section 10.1.3 Power Management Unit for layout guidelines.
2. Add test points for pins 28, 30, 32 and 33.

9.1 Bill of Materials

The following table provides the Bill of Materials (BoM) for the reference schematic given in Section 9. Reference Design. The BoM is the same for both of the host interfaces except for pull-up resistor R21.

Table 9-1. Bill of Materials

Item	Quantity	Reference	Value	Description	Manufacturer	Part Number
1	2	C1, C3	1.0 µF	CAP, CER, 1.0 µF, 20%, X5R, 0402, 6.3V	Panasonic	ECJ-0EB0J105M
2	7	C2, C4, C5, C6, C8, C11, C12	0.1 µF	CAP, CER, 0.1 µF, 10%, X5R, 0402, 10V	AVX	0402ZD104KAT2A
3	1	C10	4.7 µF	CAP, CER, 4.7 µF, 4V, 20%, X5R, 0402	Murata	GRM155R60G475 ME47D
4	2	C17, C32	1 pF	CAP, CER, 1 pF, 50V, NP0, 0201	Murata	GRM0335C1H1R0 CA01D

.....continued

Item	Quantity	Reference	Value	Description	Manufacturer	Part Number
5	2	C15, C16	10 pF	CAP, CER, 10PF, 50V, 1%, NP0, 0402	Murata	GRM1555C1H100FA01D
6	2	C23, C24	1.8 pF	CAP, CER, 1.8 pF, 50V, NP0, 0201	Murata	GRM0335C1H1R8CA01D
7	1	R2	1.2 pF	CAP, CER, 1.2PF, 50V, NP0, 0201	Murata	GRM0335C1H1R2CA01D
8	—	C21, C22, C33, R3	DNI	—	—	—
9	1	C7	1.0 µF	CAP, CER, 1 µF, 4V, 20%, X6S, 0201	Murata	GRM033C80G105MEA2D
10	3	FB1, FB2, FB3	BLM15AG121SN1	FERRITE, 120Ω @ 100 MHz, 0402	Murata	BLM15AG121SN1
11	1	FB4	BLM03AG121SN1D	FERRITE BEAD, 120Ω, 200 mA, 0201	Murata	BLM03AG121SN1D
12	1	L1	2.2 µH	POWER INDUCTOR, 2.2 µH, 20%, 750 mA, 0.3 Ωs, 0603	Murata	LQM18PN2R2MFRL
13	1	L5	15 nH	INDUCTOR, 15 nH, 300 mA, 0402	Murata	LQG15HS15NJ02D
15	2	L8, L9	3.3 nH	INDUCTOR, 3.3+/-0.2 nH, 750 mA, 0201	Murata	LQP03TN3N3C02D
16	12	R5, R6, R8, R11, R12, R13, R14, R16, R17, R18, L2, L3	0R	RESISTOR, Thick Film, 0Ω, 0201	Panasonic	ERJ-1GN0R00C
17	1	R21	1 MΩ	RESISTOR, Thick Film, 1 MΩ, 0402	Yageo	RC0100FR-071ML
18	4	TP1, TP2, TP3, TP4	Test point	—	—	—
19	1	U1	ATWILC1000B-MUT	IC, Wi-Fi, 40 QFN	Microchip	ATWILC1000B-MUT
20	1	Y1	26.000 MHz	CRYSTAL, 26 MHz, 10 pF, SMD	Abracon	ABM10-26.000MHZ-D30-T3
21	1	E1	Antenna	2.4 GHz, Antenna	—	—

10. Design Consideration

This chapter provides the guidelines on placement and routing to achieve the best performance.

10.1 Placement and Routing Guidelines

It is critical to follow the recommendations listed below to achieve the best RF performance:

- The board must have a solid ground plane. The center ground pad of the device must be solidly connected to the ground plane by using a 3x3 grid of vias.
- To avoid electromagnetic field blocking, keep any large metal objects as far away from the antenna as possible.
- Do not enclose the antenna within a metal shield.
- Keep noise-radiating components or signals, within the 2.4 GHz to 2.5 GHz frequency band, away from the antenna and shield those components if possible. Any noise radiated from the host board in this frequency band degrades the sensitivity of the chip.

10.1.1 Power and Ground

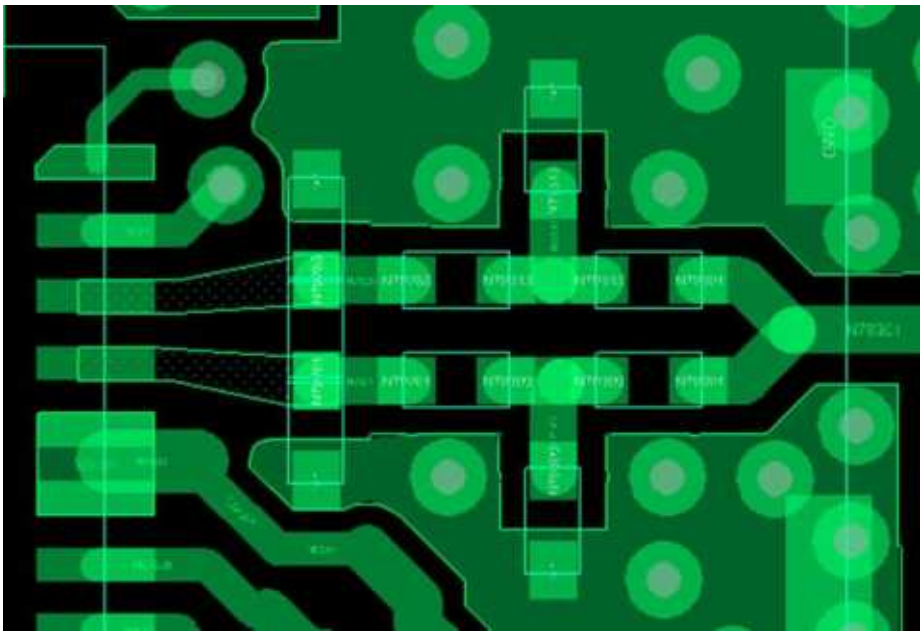
- Dedicate the layer immediately below the layer containing the RF traces from the ATWILC1000B for the ground. Ensure that this ground plane does not get broken up by routes.
- Power traces can be routed on all layers except the ground layer.
- Power supply routes must be heavy copper fill planes to ensure low inductance.
- The power pins of the ATWILC1000B must have a via directly to the power plane, close to the power pin.
- Decoupling capacitors must have a via next to the capacitor pin and this via must be directly connected to the power plane and avoid a long trace for this connection.
- The ground pad of the decoupling capacitor must have a via directly connected to the ground plane.
- Each decoupling capacitor must have its own via directly connected to the ground plane and directly connected to the power plane next to the pad.
- The decoupling capacitors must be placed as close as possible to the pin that it is filtering.

10.1.2 RF Traces and Components

The RF trace from RFIOP (Pin #7) and RFION (Pin #8) of the ATWILC1000B to the balun must be 50Ω differential controlled impedance. The route from the balun to the antenna connector must be a 50Ω controlled impedance trace. This trace must be routed in reference to the ground plane. This ground reference plane must extend entirely under the ATWILC1000B QFN package and to the sides of the these routes.

- Determine the available PCB stack-ups and the trace dimensions to achieve 50Ω single-ended controlled impedance.
- Do not have any signal traces below/adjacent to the RF trace in the PCB.
- Ensure that the RF traces from ATWILC1000B to the antenna is as short as possible to reduce path losses and to mitigate the trace from picking-up noise.
- Place guard ground vias on either side of the RF trace running from device to the antenna feed point in the PCB.
- Do not use thermal relief pads for the ground pads of all components in the RF path. These component pads must be completely filled with GND copper polygon. Place individual vias to the GND pads of these components.
- It is recommended to have a 3x3 grid of ground vias solidly connecting the exposed ground paddle of the ATWILC1000B to the ground plane on the inner/other layers of the PCB. This acts as a good ground and thermal conduction path for the ATWILC1000B.
- Ensure that all digital signals that may be toggling while the ATWILC1000B is active are placed as far away from the antenna as possible.
- Ensure that the matching components and balun are placed as close to the RFIOP and RFION pins as possible (C33, C23, C24, C17, C32, L8 and L9 in the reference schematic). The following figure shows the placement and routing of these components.

Figure 10-1. Placement and Routing of Balun and Matching Components



10.1.3 Power Management Unit

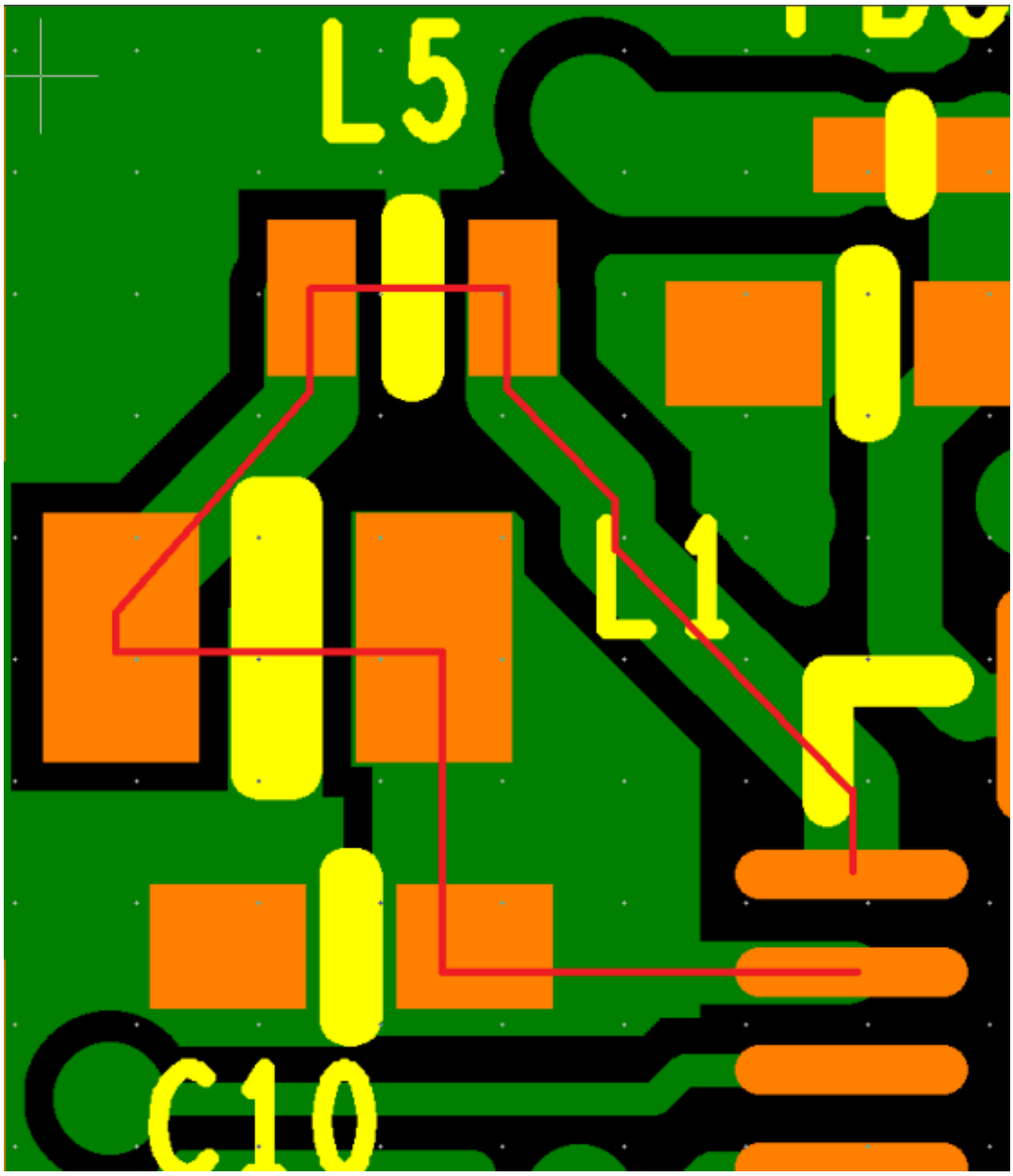
The ATWILC1000B contains an on-chip switching regulator that regulates the V_{BAT} supply for supplying to the rest of the device. It is crucial to place and route the components associated with this circuit correctly to ensure proper operation and especially to reduce any radiated noise that can be picked up by the antenna and can severely reduce the receiver sensitivity. The external components for the PMU consist of two inductors, L5 = 15 nH and L1 = 2.2 µH, and a capacitor, C10 = 4.7 µF. These components must be placed as close as possible to the ATWILC1000B pin #21 (VSW).

The trace loop from the VSW pin to the VREG_BUCK pin through the components, inductors L5 and L1 and then followed by a capacitor, C10, must be as short as possible.

Add a via between C10 and VREG_BUCK to trace out the 1P3V power rail for adding additional capacitors, 10 uF and 0.01 uF, and further route the trace to power the subsystems VDD_VCO, VDD_RF_RX, VDD_RF_TX, VDD_AMS and VDD_SXDIG.

The smaller inductor, L5, must be placed closest to pin #21 (VSW). Current flows from pin #21 (VSW) through L5, then L1, then through C10 to the ground and back to the center ground paddle of the ATWILC1000B package. Place the components so that the current loop is as small as possible. Ensure that there is a ground via to the inner ground plane right next to the ground pin of C10. The ground return path must be extremely low inductance. Failure to provide a short, heavy ground return between the capacitor and the ATWILC1000B ground pad results in incorrect operation of the on-chip switching regulator. The following figure shows an example placement and routing of these components. The trace that creates the loop is highlighted in red.

Figure 10-2. Placement and Routing of PMU Components



10.1.4 Ground

The following are the guidelines for ground vias:

- The center ground pad of the device must be solidly connected to the ground plane by using a 3x3 grid of vias.
- Ground vias must surround the perimeter of the pad.
- One of these ground vias must be placed in the center pad as close as possible to pins #7 (RFIOP) and #8 (RFION).
- The ground via serves as the RF ground return path.
- A ground via must be placed in the center pad and closer to the #21 (VSW) pin.
- This acts as a ground return path for the PMU.

10.2 Sensitive Traces

This section describes the guidelines for sensitive traces and signals.

10.2.1 Signals

The following signals are very sensitive to noise and they must be kept as short as possible and kept isolated from all other signals by routing them far away from other traces or by using a ground to shield them. Also, isolate these signals from the noisy traces on the layers above and below them:

- XO_N
- XO_P
- RFIOP
- RFION

10.2.2 Supplies

The following power supply pins for the ATWILC1000B are sensitive to noise, so the routes to these pins must be isolated from other noisy signals both on the same layer as the route and on the layers above and below. Use a ground between these sensitive signals to isolate them from other signals. It is important that the decoupling capacitors for these supplies are placed as close to the ATWILC1000B pin as possible. This reduces the trace inductance between the capacitor and the ATWILC1000B power pin to an absolute minimum:

- VDDRF_RX (pin #2)
- VDDRF_TX (pin #4)
- VDD_AMS (pin #3)
- VDD_SXDIG (pin #37)
- VDD_VCO (pin #38)

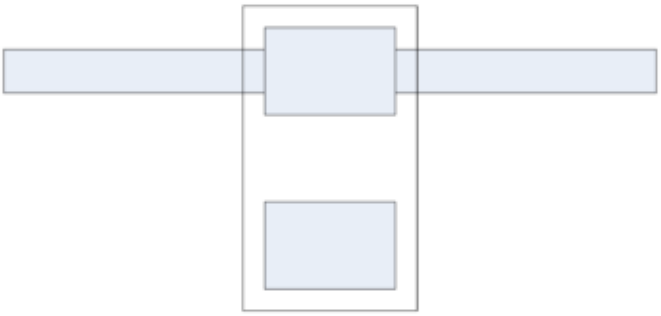
Additionally, while the VDDC (pin #14 and 27) and VBAT_BUCK (pin #20) supplies are not sensitive to picking up noise, they are noise-generating supplies. Therefore, keep the decoupling capacitors for these supply pins as close as possible to the VDDC and VBAT_BUCK pins and make sure that the routes for these supplies stay far away from sensitive pins and supplies.

10.3 Additional Suggestions

Ensure that traces route directly through the pads of all filter capacitors and not by a stub route.

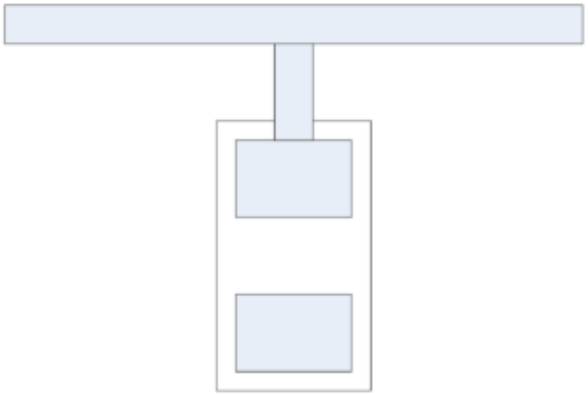
The following figure shows the correct way to route through a capacitor pad.

Figure 10-3. Correct Routing Through Capacitor Pad



The following figure shows a stub route to the capacitor pad. This should be avoided, as it adds additional impedance in series with the capacitor.

Figure 10-4. Incorrect Stub Route To Capacitor Pad



10.4 Interferers

RF receiver performance is impacted due to interferers on the board that radiate noise into the antenna or coupling into the RF traces that go to the LNA input. Follow the guidelines given below to avoid the performance degradation:

- Ensure that there is no noisy circuitry placed anywhere near the antenna or the RF traces.
- All noise-generating circuits must also be shielded so they do not radiate noise that is picked up by the antenna.
- Ensure that there are no traces routed underneath the RF portion of the ATWILC1000B.
- Ensure that there are no traces routed underneath any of the RF traces from the antenna to the ATWILC1000B input. This applies to all layers. Even if there is a ground plane on a layer between the RF route and another signal, the ground return current could flow on the ground plane and couple into the RF traces.

10.5 Antenna

The following guidelines can be used for selecting an antenna:

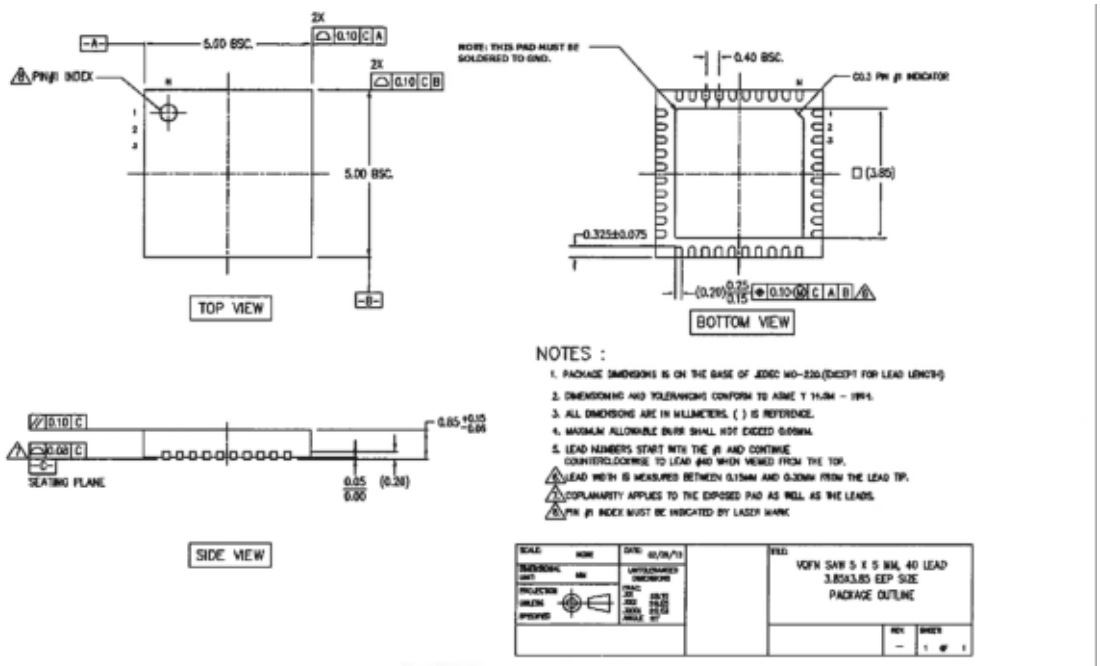
- Choose an antenna that covers the frequency band 2.400 GHz to 2.500 GHz and is designed for a 50Ω feed point.
- Follow the antenna vendor’s recommendations for pad dimensions, the spacing from the pad to the ground reference plane, and the spacing from the edges of the pad to the ground fill on the same layer as the pad.
- Ensure that the antenna matching components are placed as close as to the antenna pad as possible.

10.6 Reflow Profile Information

For information on reflow process guidelines, refer to the Solder Reflow Recommendation Application Note (DS00233).

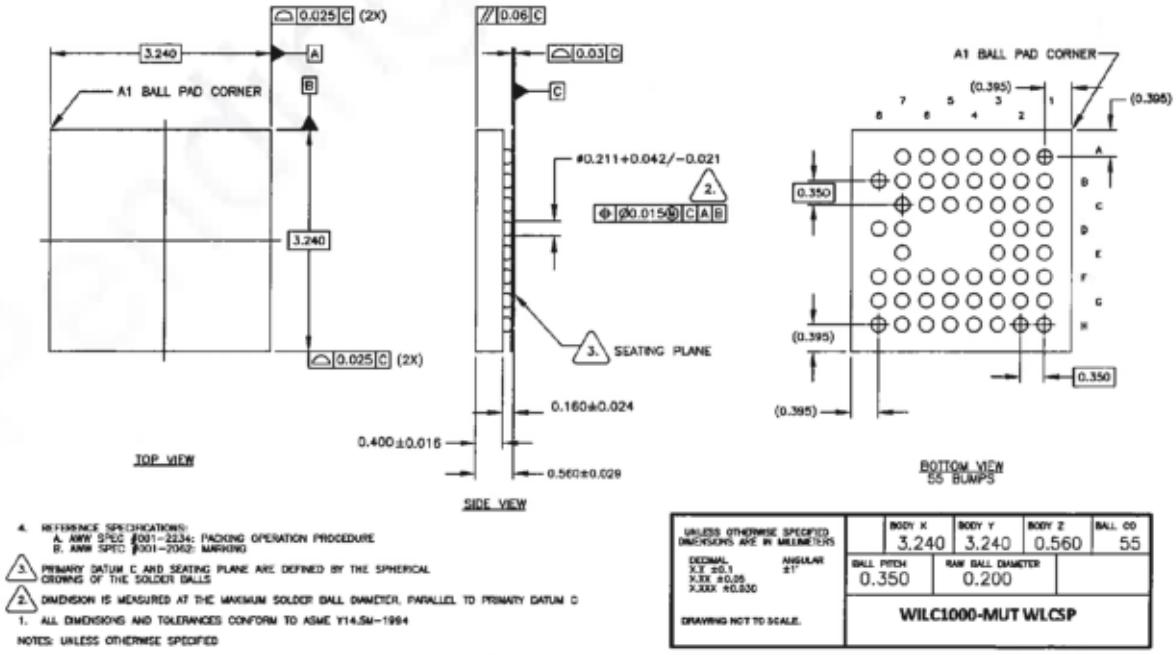
11. Package Drawing Outline

Figure 11-1. QFN Package



The QFN package is a qualified Green Package.

Figure 11-2. WLCSP Package



12. Reference Documentation and Support

The following table provides the set of collateral documents to ease integration and device ramp.

Table 12-1. Reference Documents and Design Package

Title	Content
ATWILC1000/ATWILC3000 Wi-Fi Link Controller Linux® User Guide	This user guide describes how to run Wi-Fi on the ATWILC1000 SD card and how to run Wi-Fi/BLE on the ATWILC3000 Shield board on the SAMA5D4 Xplained Ultra running with the Linux kernel 4.9.
ATWILC1000/ATWILC3000 Devices Linux Porting Guide	This user guide describes how to port the ATWILC1000 and ATWILC3000 Linux drivers to another platform and contains all the required modifications for driver porting.
ATWILC1000/ATWILC3000 Baremetal Wi-Fi®/BLE Link Controller Software Design Guide	This design guide helps the user in integrating ATWILC1000/ATWILC3000 in the application using RTOS from Advanced Software Framework (ASF).
ATWILC1000B/ATWILC1000-MR110xB Errata	This document provides details on the anomalies identified in the ATWILC1000 family of devices.
ATWILC1000B Reference Design Package	The Reference Design Package contains the design collaterals (Schematics, Bill of Materials, PCB design source files, Gerber) of the module, evaluation boards and its associated boards for ATWILC1000B.
ATWILC1000B – Deriving Application Gain Table Application Note	This application note describes the Wi-Fi gain table structure and procedure to derive the application gain table. This document provides further details on the steps to update the device with the gain table.
MCHPRT2 User guide	This document provides detailed information about the MCHPRT2 tool, which allows the user to easily configure, evaluate and test an RF system.

Notes:

- The development support tools and documentation are available in http://www.microchip.com/wwwproducts/en/ATWILC1000.
- For queries or help, visit support.microchip.com or contact your local Microchip sales office.

13. Document Revision History

Revision	Date	Section	Description
C	08/2020	4.3 Nonvolatile Memory (eFuse)	Errors in Bank numbers fixed in 4.3 Nonvolatile Memory (eFuse) description
B	08/2020	Document	Minor edits
		• Introduction • Features	Updated peripheral details and added operating conditions
		2. Functional Overview	• Rearranged sections under this chapter • Updated Figure 2-1 • Updated descriptions of the pins in 2.2 Pin Description • Updated pad width in Table 2-2
		3.2 Low-Power Oscillator	Added software implementation related note
		4.3 Nonvolatile Memory (eFuse)	Updated with new information and Figure 4-1
		5. WLAN Subsystem	• Added a note for FW support of Short GI • Updated Table 5-1
		6. External Interfaces	• Updated lead sentence • Minor edits • Added 6.1 Interfacing with the Host Microcontroller • Updated Table 6-4 • Updated Figure 6-4 and Table 6-6 • Removed I2C Master Interface section and SPI Master Interface section
		7. Power Management	• Updated Figure 7-1 • Updated RF/AMS core voltage (VREG_BUCK)
		8. Electrical Specifications	Modified the following sections and regrouped them under Electrical characteristics from other chapters: • 8.4 Current Consumption in Various Device States • 8.5.1 Receiver Performance • 8.5.2 Transmitter Performance • VDDIO Specification updated • Added Section 8.3 DC Electrical Characteristics
		9. Reference Design	• Updated Figure 9-1 and Figure 9-2 • Added 9.1 Bill of Materials section and updated contents
		10. Design Consideration	Added new chapter
		12. Reference Documentation and Support	Updated Table 12-1 contents

.....continued

Revision	Date	Section	Description
A	12/2018	Document	• Updated from Atmel to Microchip template. • Assigned a new Microchip document number. Previous version is Atmel 42351 revision D. • ISBN number added.

Document Revision History - Atmel

Doc. Rev.	Date	Comments
42351D	05/2015	DS update to Rev. B offering. Changes from ATWILC1000A to ATWILC1000B: 1. Added second UART, increased UART data rates. 2. Increased instruction RAM size from 128KB to 160KB. 3. Updated pin MUX table: added new options for various interfaces. 4. Improved description of Coexistence interface. 5. Added VDD_VCO switch and connection in the power architecture. 6. Updated power consumption numbers. 7. Updated reference schematic. 8. Changed RTC_CLK pad definition from pull-down to pull-up
42351C	02/2015	DS update new Atmel format.
42351B	11/2014	Major document update, new sections added, replaced text in most sections, new and updated drawings.
42351A	07/2014	Initial document release.

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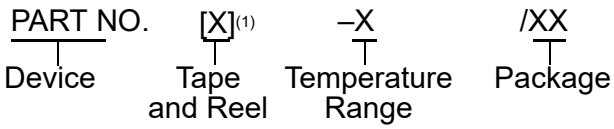

Device:	Device A, Feature A, (Package A) Device B, Feature B, (Package B)	
Tape & Reel Option:	Blank	= Tube
	T	= Tape & Reel
Temperature Range:	I	= -40°C to +85°C (Industrial)
	E	= -40°C to +125°C (Extended)
Package:	AA	= Package AA
	BB	= Package BB

Examples:

- MCPXXXXXAT-E/AA: Tape and Reel, Extended temperature, XAA package
- MCPXXXXXBT-E/BB: Tape and Reel Extended temperature, XBB package

Notes:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
2. Small form-factor packaging options may be available. Please check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

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