


# 74ALVCH16652

## 16-bit transceiver/register with dual enable; 3-state

Rev. 4 — 8 July 2024 Product data sheet

## 1. General description

The 74ALVCH16652 consists of 16 non-inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Data on the ‘A’ or ‘B’, or both buses, will be stored in the internal registers, at the appropriate clock inputs (nCPAB or nCPBA) regardless of the select inputs (nSAB and nSBA) or output enable (nOEAB and $n\overline{OEBA}$) control inputs.

Depending on the select inputs nSAB and nSBA data can directly go from input to output (real-time mode) or data can be controlled by the clock (storage mode), when OE inputs permit this operating mode.

The output enable inputs nOEAB and $n\overline{OEBA}$ determine the operation mode of the transceiver. When nOEAB is LOW, no data transmission from nBn to nAn is possible and when $n\overline{OEBA}$ is HIGH, no data transmission from nBn to nAn is possible.

When nSAB and nSBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling nOEAB and $n\overline{OEBA}$. In this configuration each output reinforces its input.

Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

## 2. Features and benefits

- Wide supply voltage range of 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive ±24 mA at $V_{CC}$ = 3.0 V.
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple $V_{CC}$ and GND pins for minimum noise and ground bounce
- All data inputs have bushold
- Output drive capability 50 Ω transmission lines at 85 °C
- Complies with JEDEC standards:
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74ALVCH16652DGG | −40 °C to +85 °C | TSSOP56 | plastic thin shrink small outline package; 56 leads; body width 6.1 mm | SOT364-1 |

## 4. Functional diagram

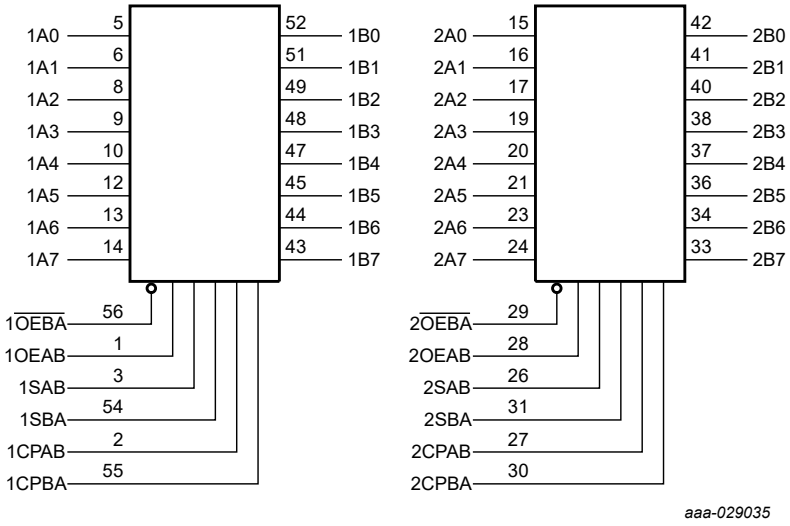



Fig. 1. Logic symbol

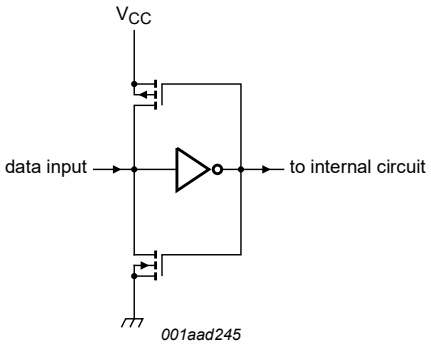



Fig. 2. Bus hold circuit

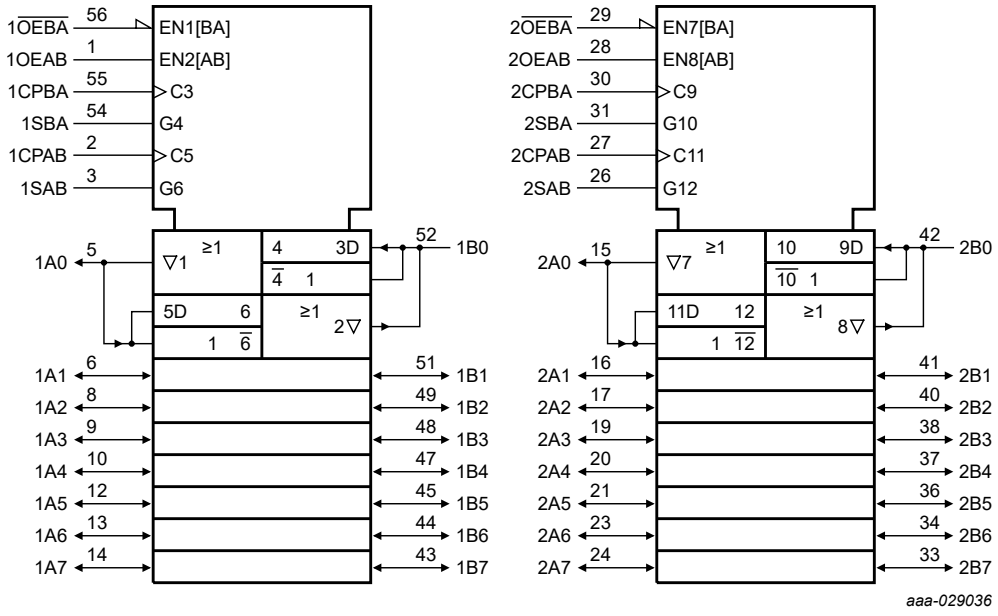



Fig. 3. IEC logic symbol


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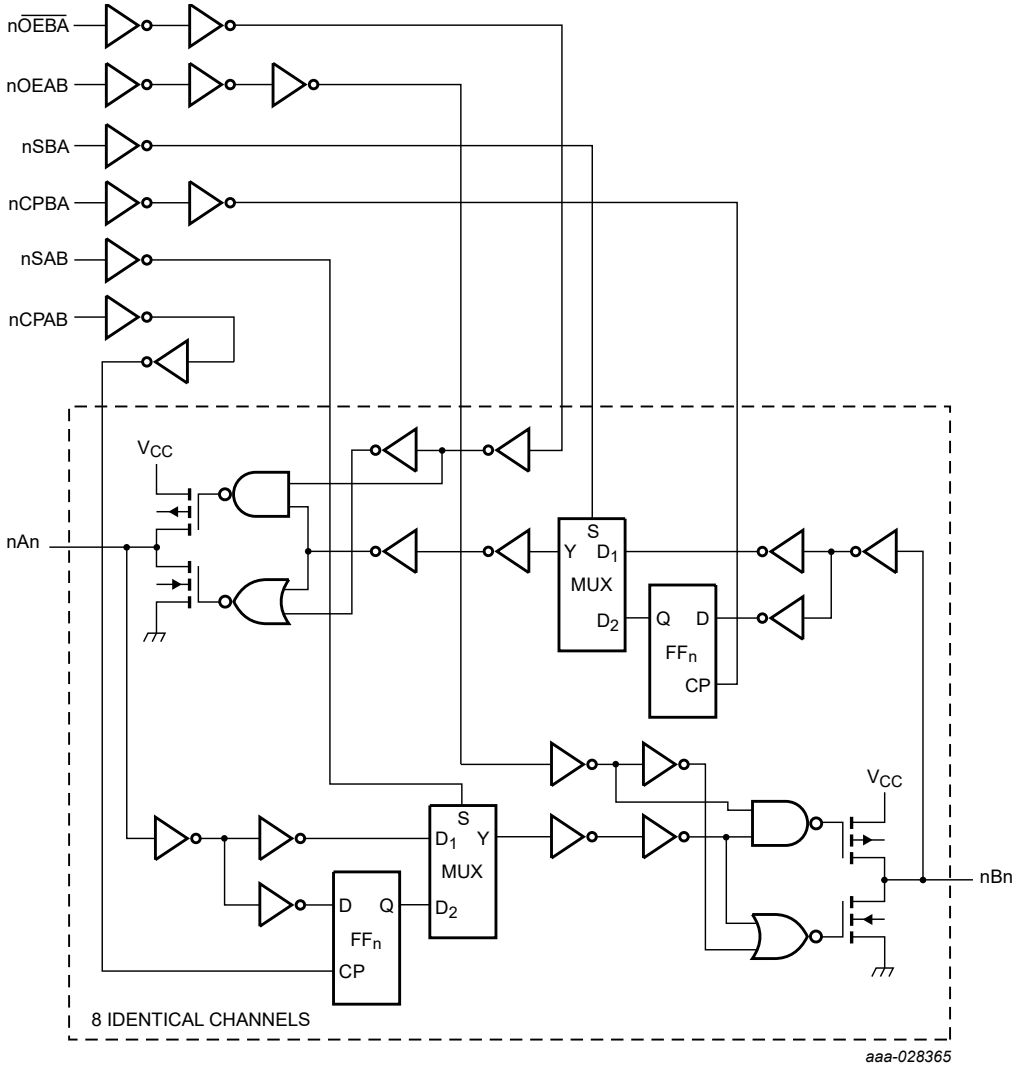


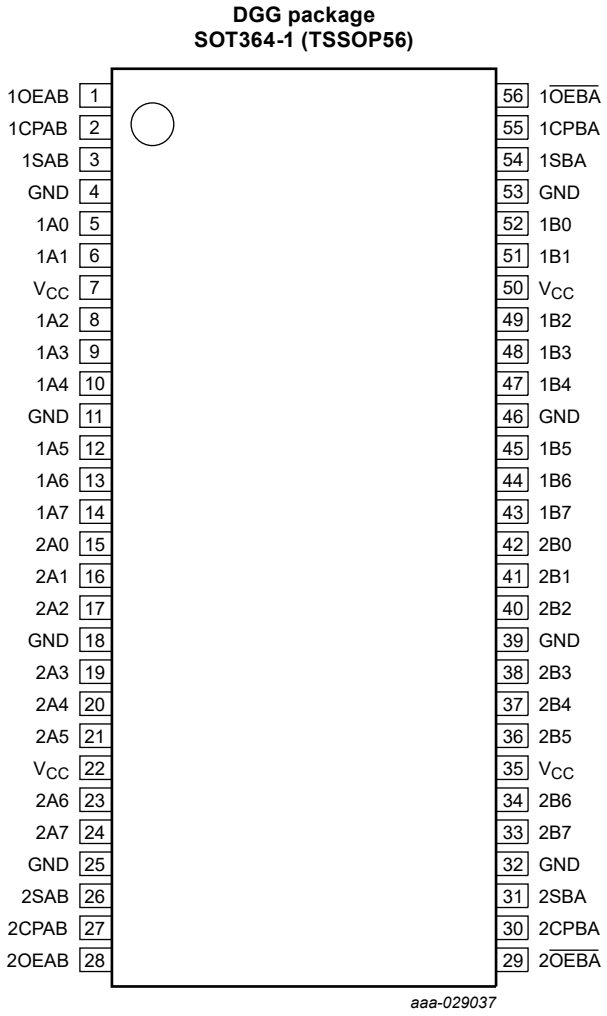

**Fig. 4. Logic diagram (one section)**


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# 5. Pinning information

## 5.1. Pinning





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### 5.2. Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| 1A0, 1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7 | 5, 6, 8, 9, 10, 12, 13, 14 | data input/output |
| 2A0, 2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7 | 15, 16, 17, 19, 20, 21, 23, 24 | data input/output |
| 1B0, 1B1, 1B2, 1B3, 1B4, 1B5, 1B6, 1B7 | 52, 51, 49, 48, 47, 45, 44, 43 | data output/input |
| 2B0, 2B1, 2B2, 2B3, 2B4, 2B5, 2B6, 2B7 | 42, 41, 40, 38, 37, 36, 34, 33 | data output/input |
| 1$\overline{OEBA}$, 2$\overline{OEBA}$ | 56, 29 | output enable inputs (active-LOW) |
| 1OEAB, 2OEAB | 1, 28 | output enable inputs (active-HIGH) |
| 1SAB, 2SAB | 3, 26 | select input A-to-B |
| 1CPAB, 2CPAB | 2, 27 | clock input A-to-B |
| 1SBA, 2SBA | 54, 31 | select input B-to-A |
| 1CPBA, 2CPBA | 55, 30 | clock input B-to-A |
| GND | 4, 11, 18, 25, 32, 39, 46, 53 | ground (0 V) |
| $V_{CC}$ | 7, 22, 35, 50 | supply voltage |

## 6. Functional description

**Table 3. Function selection**

*H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH clock transition.*

| Operating mode | Inputs | | | | | | Data I/O | |
|---|---|---|---|---|---|---|---|---|
| | nOEAB | n$\overline{OEBA}$ | nCPAB | nCPBA | nSAB | nSBA | nAn | nBn |
| isolation, store A and B data | L | H | ↑ | ↑ | X | X | input | input |
| isolation, store A and B data | L | H | H or L | H or L | X | X | input | input |
| store A, hold B[1] | X | H | ↑ | H or L | X | X | input | unspecified[1] |
| store A in both registers | H | H | ↑ | ↑ | L | X | input | output |
| store B, hold A[1] | L | X | H or L | ↑ | X | X | unspecified[1] | input |
| store B in both registers | L | L | ↑ | ↑ | X | L | output | input |
| real-time B data to A bus | L | L | X | X | X | L | output | input |
| stored B data to A bus | L | L | X | H or L | X | H | output | input |
| real-time A data to B bus | H | H | X | X | L | X | input | output |
| stored A data to B bus | H | H | H or L | X | H | X | input | output |
| stored A data to B bus and stored B data to A bus | H | L | H or L | H or L | H | H | output | output |

[1] The data output functions may be enabled or disabled by various signals at the nOEAB and n$\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.


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# 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | -0.5 | +4.6 | V |
| $V_I$ | input voltage | [1] | -0.5 | +4.6 | V |
| $V_O$ | output voltage | [1] | -0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | input clamping current | $V_I$ < 0 V | -50 | - | mA |
| $I_{OK}$ | output clamping current | $V_O$ > $V_{CC}$ or $V_O$ < 0 V | - | ±50 | mA |
| $I_{O\ (sink/source)}$ | output sink or source current | $V_O$ = 0 V to $V_{CC}$ | - | ±50 | mA |
| $I_{CC}$ | supply current | | - | 100 | mA |
| $I_{GND}$ | ground current | | -100 | - | mA |
| $T_{stg}$ | storage temperature | | −65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = −40 °C to +85 °C | - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | for low-voltage applications | 1.2 | 2.4 | 3.6 | V |
| | | for maximum speed performance; 30 pF output load | 2.3 | 2.5 | 2.7 | V |
| | | for maximum speed performance; 50 pF output load | 3.0 | 3.3 | 3.6 | V |
| $V_I$ | input voltage | | 0 | - | $V_{CC}$ | V |
| $V_O$ | output voltage | | 0 | - | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | in free air | -40 | - | +85 | °C |
| Δt/ΔV | input transition rise and fall rate | $V_{CC}$ = 2.3 V to 3.0 V | - | - | 20 | ns/V |
| | | $V_{CC}$ = 3.0 V to 3.6 V | - | - | 10 | ns/V |

# 9. Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | 1.2 | - | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2.0 | 1.5 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 2.3 V to 2.7 V | - | 1.2 | 0.7 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | - | 1.5 | 0.8 | V |


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| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | |
| | | $I_O$ = -100 µA; $V_{CC}$ = 2.3 V to 3.6 V | $V_{CC}$ - 0.2 | $V_{CC}$ | - | V |
| | | $I_O$ = -6 mA; $V_{CC}$ = 2.3 V | $V_{CC}$ - 0.3 | $V_{CC}$ - 0.08 | - | V |
| | | $I_O$ = -12 mA; $V_{CC}$ = 2.3 V | $V_{CC}$ - 0.6 | $V_{CC}$ - 0.26 | - | V |
| | | $I_O$ = -12 mA; $V_{CC}$ = 2.7 V | $V_{CC}$ - 0.5 | $V_{CC}$ - 0.14 | - | V |
| | | $I_O$ = -12 mA; $V_{CC}$ = 3.0 V | $V_{CC}$ - 0.6 | $V_{CC}$ - 0.09 | - | V |
| | | $I_O$ = -24 mA; $V_{CC}$ = 3.0 V | $V_{CC}$ - 1.0 | $V_{CC}$ - 0.28 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | |
| | | $I_O$ = 100 µA; $V_{CC}$ = 2.3 V to 3.6 V | - | GND | 0.20 | V |
| | | $I_O$ = 6 mA; $V_{CC}$ = 2.3 V | - | 0.07 | 0.40 | V |
| | | $I_O$ = 12 mA; $V_{CC}$ = 2.3 V | - | 0.15 | 0.70 | V |
| | | $I_O$ = 12 mA; $V_{CC}$ = 2.7 V | - | 0.14 | 0.40 | V |
| | | $I_O$ = 24 mA; $V_{CC}$ = 3.0 V | - | 0.27 | 0.55 | V |
| $I_I$ | input leakage current | $V_{CC}$ = 2.3 V to 3.6 V; $V_I = V_{CC}$ or GND | - | 0.1 | 5 | µA |
| $I_{OZ}$ | OFF-state output current | $V_{CC}$ = 2.3 V to 3.6 V; $V_I = V_{IH}$ or $V_{IL}$; $V_O = V_{CC}$ or GND | - | 0.1 | 10 | µA |
| $I_{CC}$ | supply current | $V_{CC}$ = 2.3 V to 3.6 V; $V_I = V_{CC}$ or GND; $I_O$ = 0 A | - | 0.2 | 40 | µA |
| $\Delta I_{CC}$ | additional supply current | per data I/O pin; $V_{CC}$ = 2.3 V to 3.6 V; $V_I = V_{CC}$ - 0.6 V; $I_O$ = 0 A | - | 150 | 750 | µA |
| $I_{BHL}$ | bus hold LOW current | $V_{CC}$ = 2.3 V; $V_I$ = 0.7 V | 45 | - | - | µA |
| | | $V_{CC}$ = 3.0 V; $V_I$ = 0.8 V | 75 | 150 | - | µA |
| $I_{BHH}$ | bus hold HIGH current | $V_{CC}$ = 2.3 V; $V_I$ = 1.7 V | -45 | - | - | µA |
| | | $V_{CC}$ = 3.0 V; $V_I$ = 2.0 V | -75 | -175 | - | µA |
| $I_{BHLO}$ | bus hold LOW overdrive current | $V_{CC}$ = 3.6 V | 500 | - | - | µA |
| $I_{BHHO}$ | bus hold HIGH overdrive current | $V_{CC}$ = 3.6 V | -500 | - | - | µA |
| $C_I$ | input capacitance | | - | 4.0 | - | pF |

[1] All typical values are measured at $T_{amb}$ = 25 °C.


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## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*Voltages are referenced to GND (ground = 0 V). For test circuit, see Fig. 10.*

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ [1] | Max | |
| $t_{pd}$ | propagation delay | nAn to nBn; nBn to nAn; see Fig. 5 [2] | | | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.0 | 2.7 | 4.8 | ns |
| | | $V_{CC}$ = 2.7 V | - | 2.8 | 4.5 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 2.6 | 3.9 | ns |
| | | nCPAB to nBn; nCPBA to nAn; see Fig. 6 | | | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.0 | 3.4 | 6.8 | ns |
| | | $V_{CC}$ = 2.7 V | - | 3.1 | 5.2 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.4 | 2.9 | 4.5 | ns |
| | | nSAB to nBn; nSBA to nAn; see Fig. 7 | | | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.0 | 3.4 | 5.6 | ns |
| | | $V_{CC}$ = 2.7 V | - | 3.5 | 6.4 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.3 | 3.1 | 5.3 | ns |
| $t_{en}$ | enable time | nOEAB to nBn; see Fig. 9 [3] | | | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.0 | 2.6 | 4.5 | ns |
| | | $V_{CC}$ = 2.7 V | - | 2.4 | 4.6 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 2.2 | 4.0 | ns |
| | | $n\overline{OEBA}$ to nAn; see Fig. 9 [3] | | | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 3.3 | 2.8 | 4.5 | ns |
| | | $V_{CC}$ = 2.7 V | - | 3.0 | 4.6 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 2.2 | 4.0 | ns |
| $t_{dis}$ | disable time | nOEAB to nBn; see Fig. 9 [4] | | | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.6 | 2.7 | 4.5 | ns |
| | | $V_{CC}$ = 2.7 V | - | 3.4 | 5.1 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.4 | 2.7 | 4.5 | ns |
| | | $n\overline{OEBA}$ to nAn; see Fig. 9 [4] | | | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 3.3 | 2.5 | 4.5 | ns |
| | | $V_{CC}$ = 2.7 V | - | 3.1 | 5.1 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.1 | 2.9 | 4.5 | ns |
| $t_w$ | pulse width | nCPAB HIGH or LOW; nCPBA HIGH or LOW; see Fig. 6 | | | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 2.2 | 1.2 | - | ns |
| | | $V_{CC}$ = 2.7 V | 3.3 | 1.0 | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 3.3 | 0.7 | - | ns |
| $t_{su}$ | set-up time | nAn to nCPAB; nBn to nCPBA; see Fig. 8 | | | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 2.2 | 0.2 | - | ns |
| | | $V_{CC}$ = 2.7 V | 1.7 | 0.2 | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.4 | 0.3 | - | ns |

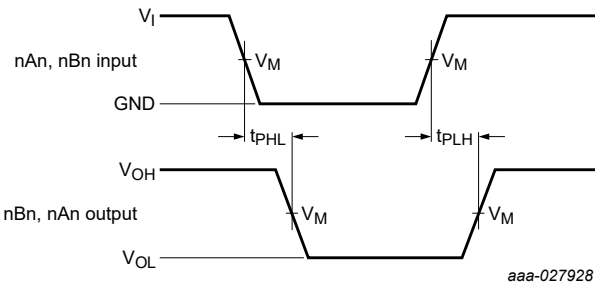

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| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ [1] | Max | |
| $t_h$ | hold time | nAn to nCPAB; nBn to nCPBA; see Fig. 8 | | | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 0.6 | 0.1 | - | ns |
| | | $V_{CC}$ = 2.7 V | 0.4 | 0.1 | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 0.7 | 0.2 | - | ns |
| $f_{max}$ | maximum frequency | nCPAB; nCPBA; see Fig. 6 | | | | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 150 | 300 | - | MHz |
| | | $V_{CC}$ = 2.7 V | 150 | 320 | - | MHz |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 150 | 320 | - | MHz |
| $C_{PD}$ | power dissipation capacitance | per channel; $V_I$ = GND to $V_{CC}$ [5] | | | | |
| | | output enabled | - | 22 | - | pF |
| | | output disabled | - | 4.0 | - | pF |

[1] Typical values are measured at $T_{amb}$ = 25 °C
Typical values for $V_{CC}$ = 2.3 V to 2.7 V are measured at $V_{CC}$ = 2.5 V
Typical values for $V_{CC}$ = 3.0 V to 3.6 V are measured at $V_{CC}$ = 3.3 V
[2] $t_{pd}$ is the same as $t_{PHL}$ and $t_{PLH}$.
[3] $t_{en}$ is the same as $t_{PZH}$ and $t_{PZL}$.
[4] $t_{dis}$ is the same as $t_{PHZ}$ and $t_{PLZ}$.
[5] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz;
$f_o$ = output frequency in MHz;
$C_L$ = output load capacitance in pF;
$V_{CC}$ = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

## 10.1. Waveforms and test circuit

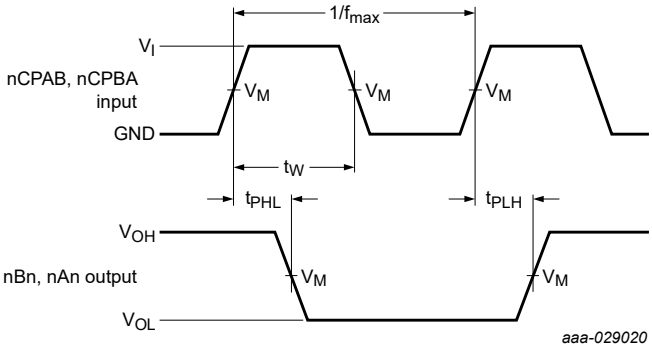



See Table 8 for measurement points.
$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig. 5. Input (nAn, nBn) to output (nBn, nAn) propagation delays**


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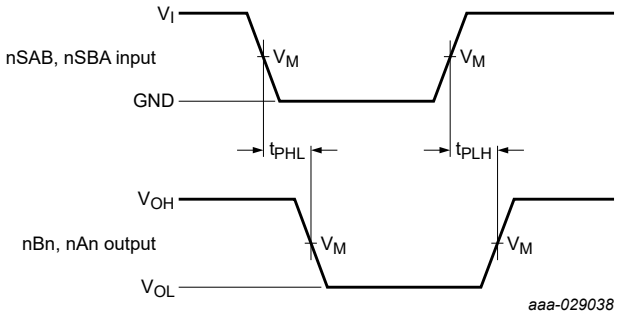
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Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

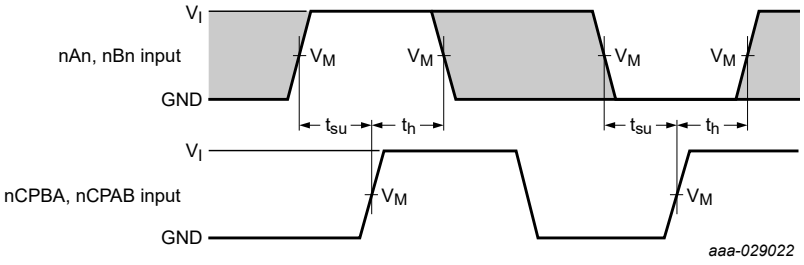
**Fig. 6. Clock input (nCPAB, nCPBA) to data output (nBn, nAn) propagation delays, clock pulse width (nCPAB, nCPBA) and maximum clock frequency (nCPAB, nCPBA)**




Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Fig. 7. Select source inputs (nSAB, nSBA) to data output (nBn, nAn) propagation delays**



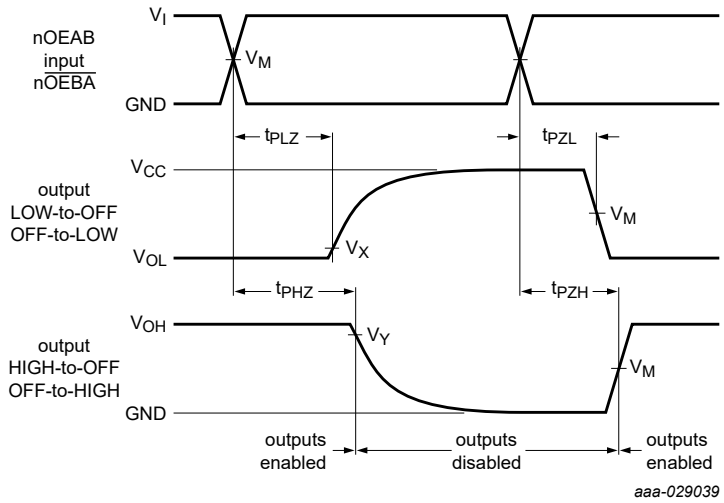

Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig. 8. Data set-up and hold times for nAn, nBn inputs to nCPAB and nCPBA inputs**


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Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

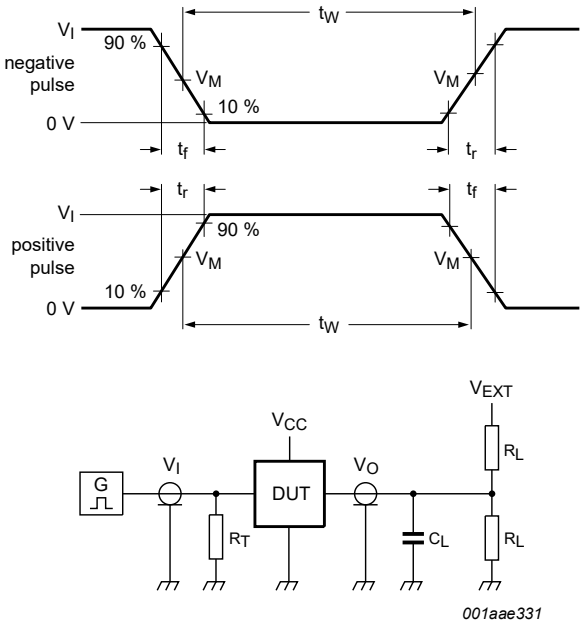
**Fig. 9. 3-state enable and disable times.**

**Table 8. Measurement points**

| Supply voltage | Input | | Output | | |
|---|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 2.3 V to 2.7 V | $V_{CC}$ | 0.5 × $V_{CC}$ | 0.5 × $V_{CC}$ | $V_{OL}$ + 0.15 V | $V_{OH}$ - 0.15 V |
| 2.7 V | 2.7 V | 1.5 V | 1.5 V | $V_{OL}$ + 0.3 V | $V_{OH}$ - 0.3 V |
| 3.0 V to 3.6 V | 2.7 V | 1.5 V | 1.5 V | $V_{OL}$ + 0.3 V | $V_{OH}$ - 0.3 V |


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Test data is given in Table 9.

Definitions for test circuit:

$R_L$ = Load resistance;

$C_L$ = Load capacitance including jig and probe capacitance;

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator;

$V_{EXT}$ = External voltage for measuring switching times.

**Fig. 10. Test circuit for measuring switching times**

**Table 9. Test data**

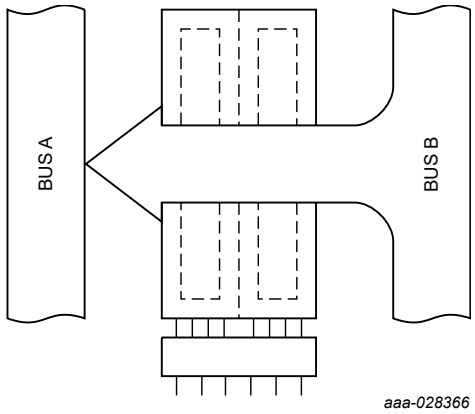
| Supply voltage | Input | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PLH}$, $t_{PHL}$ | $t_{PLZ}$, $t_{PZL}$ | $t_{PHZ}$, $t_{PZH}$ |
| 2.3 V to 2.7 V | $V_{CC}$ | ≤ 2.0 ns | 30 pF | 500 Ω | open | 2 × $V_{CC}$ | GND |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | 2 × $V_{CC}$ | GND |
| 3.0 V to 3.6 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | 2 × $V_{CC}$ | GND |


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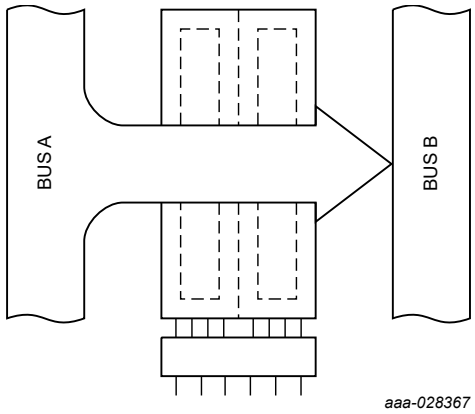
## 11. Application information

*H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH clock transition*



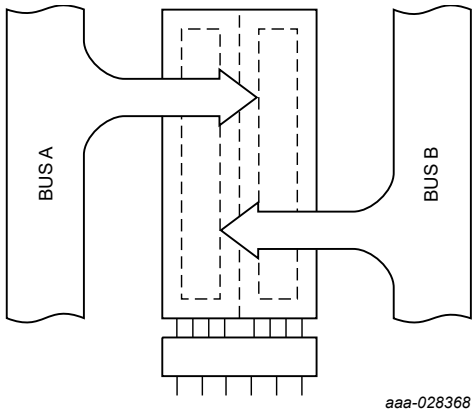

| nOEAB | $\overline{nOEBA}$ | nCPAB | nCPBA | nSAB | nSBA |
|---|---|---|---|---|---|
| L | L | X | X | X | L |

**Fig. 11. Real time transfer bus B to bus A**



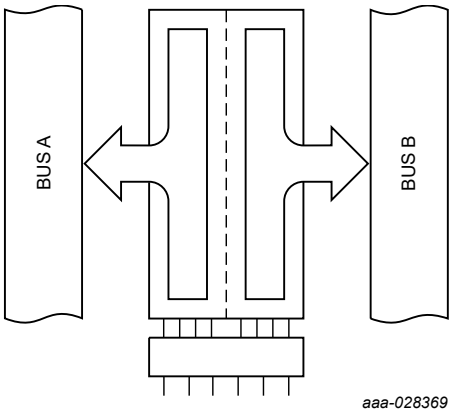

| nOEAB | $\overline{nOEBA}$ | nCPAB | nCPBA | nSAB | nSBA |
|---|---|---|---|---|---|
| H | H | X | X | L | X |

**Fig. 12. Real time transfer bus A to bus B**




| nOEAB | $\overline{nOEBA}$ | nCPAB | nCPBA | nSAB | nSBA |
|---|---|---|---|---|---|
| X | H | ↑ | X | X | X |
| L | X | X | ↑ | X | X |
| L | H | ↑ | ↑ | X | X |

**Fig. 13. Store from bus A, B or A and B in one register**

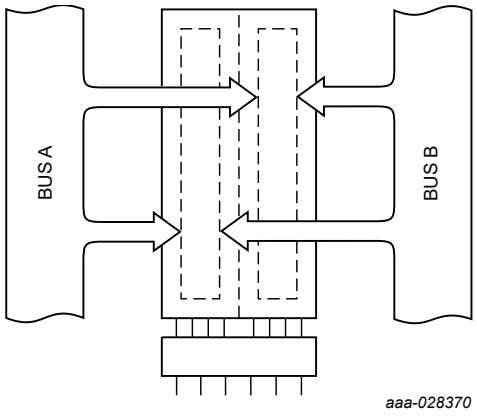



| nOEAB | $\overline{nOEBA}$ | nCPAB | nCPBA | nSAB | nSBA |
|---|---|---|---|---|---|
| H | H | H or L | X | H | X |
| L | L | X | H or L | X | H |
| H | L | H or L | H or L | H | H |

**Fig. 14. Transfer A stored data to B bus or B stored data to A bus or both at the same time**

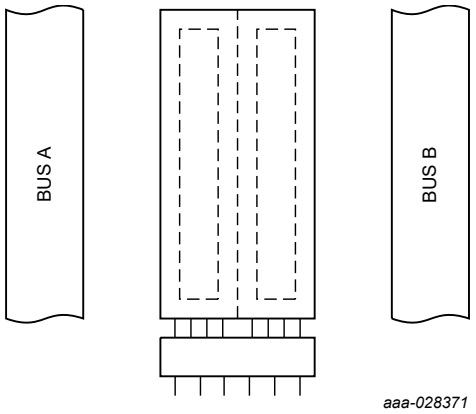

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| nOEAB | $\overline{nOEBA}$ | nCPAB | nCPBA | nSAB | nSBA |
|---|---|---|---|---|---|
| X | H | ↑ | ↑ | X | X |
| L | L | ↑ | ↑ | X | L |

**Fig. 15. Store bus A in both registers or store bus B in both registers**




| nOEAB | $\overline{nOEBA}$ | nCPAB | nCPBA | nSAB | nSBA |
|---|---|---|---|---|---|
| L | H | H or L | H or L | X | X |

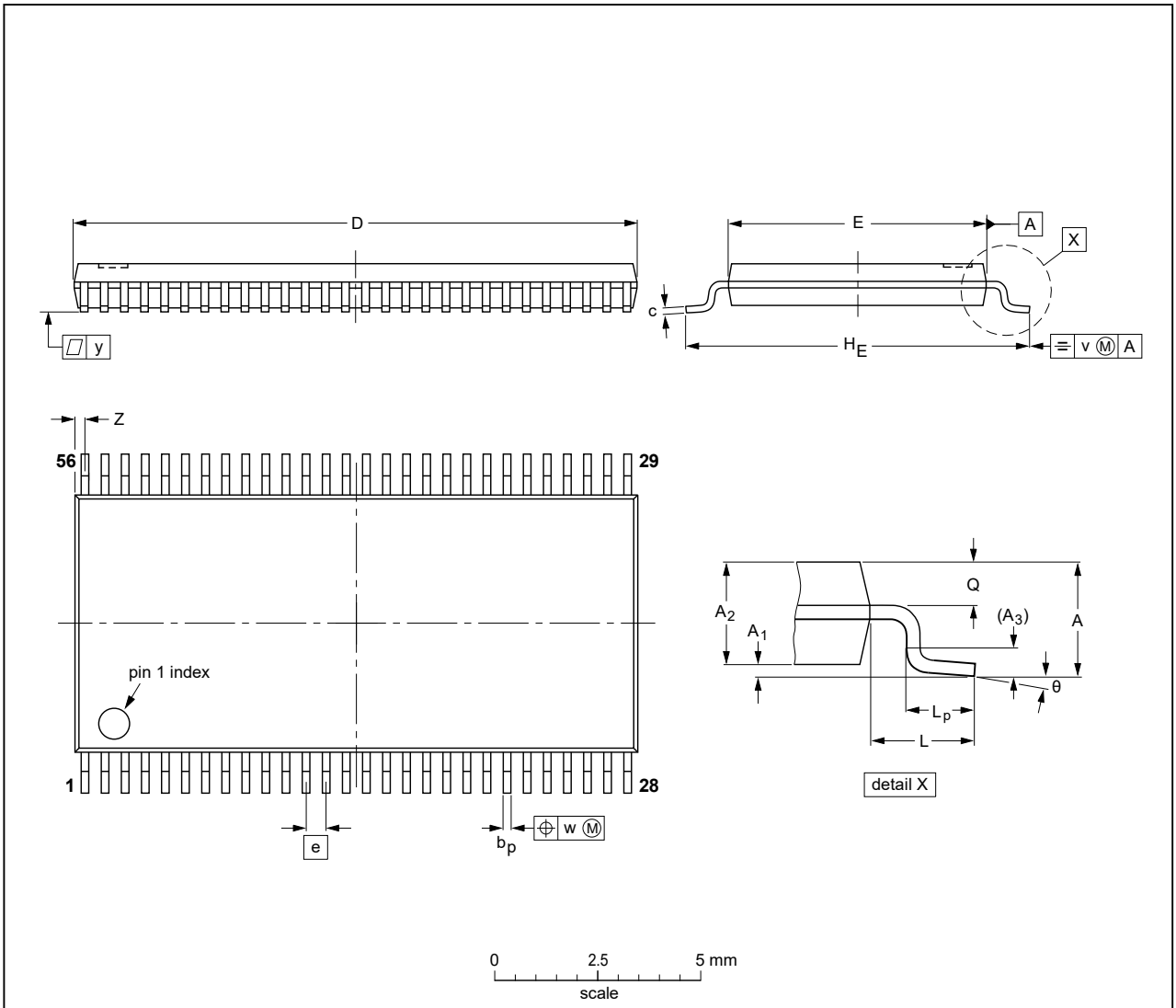
**Fig. 16. Isolation**


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## 12. Package outline

**TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm** **SOT364-1**




**DIMENSIONS (mm are the original dimensions).**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D(1) | E(2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.2 | 0.15<br>0.05 | 1.05<br>0.85 | 0.25 | 0.28<br>0.17 | **0.2**<br>**0.1** | 14.1<br>13.9 | 6.2<br>6.0 | 0.5 | 8.3<br>7.9 | 1 | 0.8<br>0.4 | 0.50<br>0.35 | 0.25 | 0.08 | 0.1 | 0.5<br>0.1 | 8°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT364-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig. 17. Package outline SOT364-1 (TSSOP56)**


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## 13. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| ANSI | American National Standards Institute |
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| ESDA | ElectroStatic Discharge Association |
| HBM | Human Body Model |
| JEDEC | Joint Electron Device Engineering Council |
| TTL | Transistor-Transistor Logic |

## 14. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74ALVCH16652 v.4 | 20240708 | Product data sheet | - | 74ALVCH16652 v.3 |
| Modifications: | • Section 2: ESD specification updated according to the latest JEDEC standard.<br>• Table 4: $P_{tot}$ total power dissipation updated. | | | |
| 74ALVCH16652 v.3 | 20180912 | Product data sheet | - | 74ALVCH16652 v.2 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.<br>• Legal texts have been adapted to the new company name where appropriate. | | | |
| 74ALVCH16652 v.2 | 19991123 | Product specification | - | 74ALVCH16652 v.1 |
| 74ALVCH16652 v.1 | 19980831 | Preliminary specification | - | - |


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# 15. Legal information

## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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