74HC7403; 74HCT7403

4-bit x 64-word FIFO register; 3-state

Rev. 4 — 24 September 2012 Product data sheet

1. General description

The 74HC7403; 74HCT7403 is an expandable, First-In First-Out (FIFO) memory organized as 64 words by 4 bits. A guaranteed 15 MHz data-rate makes it ideal for high-speed applications. A higher data-rate can be obtained in applications where the status flags are not used (burst-mode). With separate controls for shift-in (SI) and shift-out ($\overline{SO}$), reading and writing operations are completely independent, allowing synchronous and asynchronous data transfers. Additional controls include a master-reset input ($\overline{MR}$), an output enable input ($\overline{OE}$) and flags. The data-in-ready (DIR) and data-out-ready (DOR) flags indicate the status of the device. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Synchronous or asynchronous operation
- 30 MHz (typical) shift-in and shift-out rates
- Readily expandable in word and bit dimensions
- Pinning arranged for easy board layout: input pins directly opposite output pins
- Input levels:
  - For 74HC7403: CMOS level
  - For 74HCT7403: TTL level
- 3-state outputs
- Complies with JEDEC standard JESD7A
- ESD protection:
  - HBM JESD22-A114F exceeds 2 000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Applications

- High-speed disc or tape controller
- Communications buffer

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC7403N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HCT7403N				
74HC7403D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT7403D				

5. Functional diagram

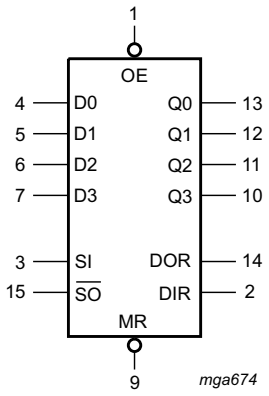


Fig 1. Logic symbol

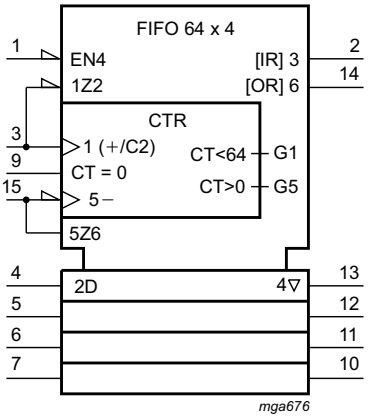


Fig 2. IEC logic symbol

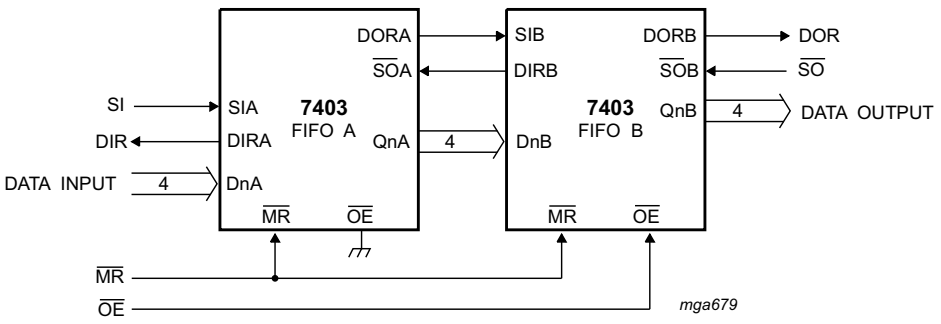
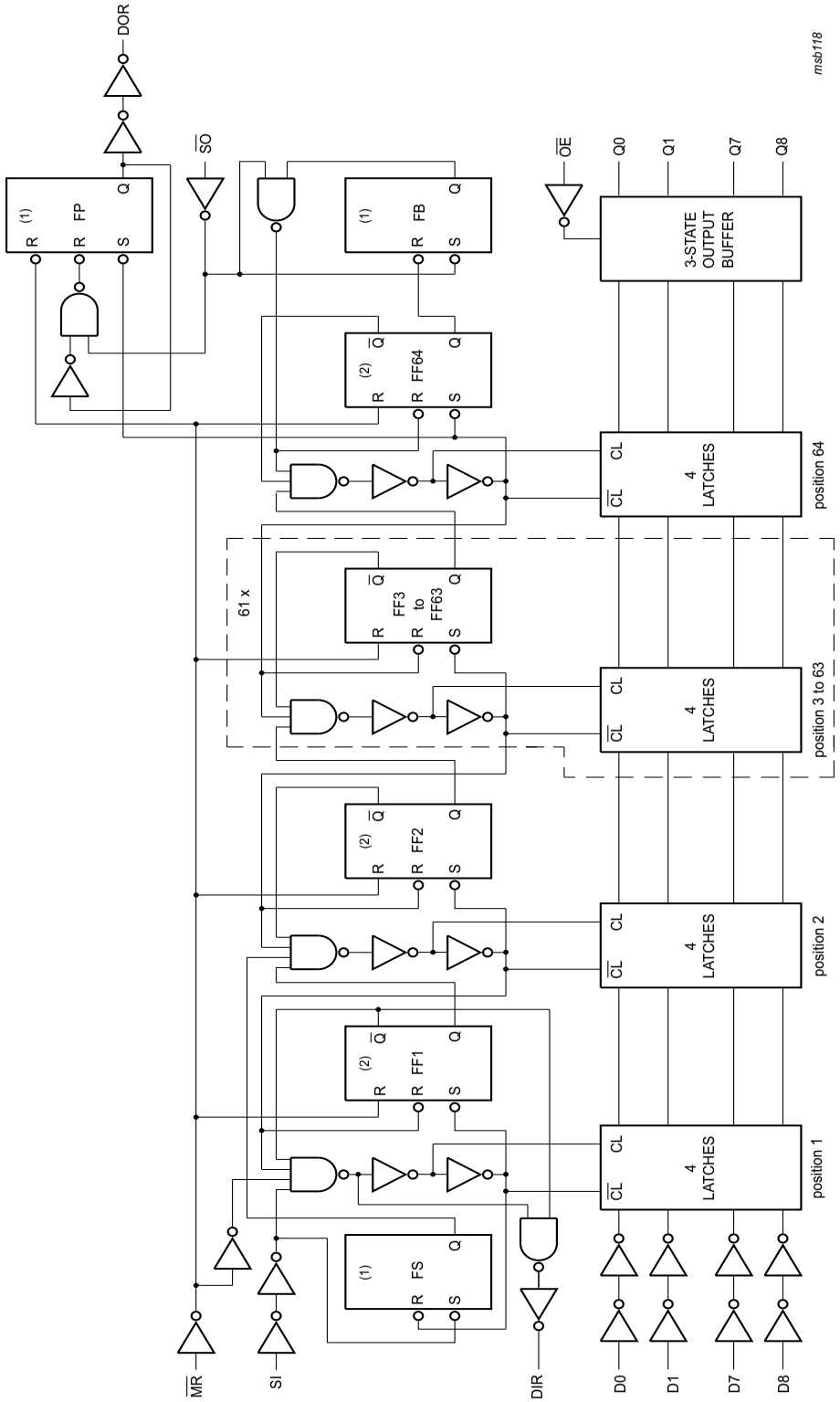


Fig 3. Functional diagram

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.



LOW on $\overline{S}$ input of the flip-flops FS, FB and FP sets Q output to HIGH independent of state on $\overline{R}$ input

LOW on $\overline{R}$ input of FF1 to FF64 sets Q output to LOW independent of state on $\overline{S}$ input

Fig 4. Logic diagram

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

6. Pinning information

6.1 Pinning

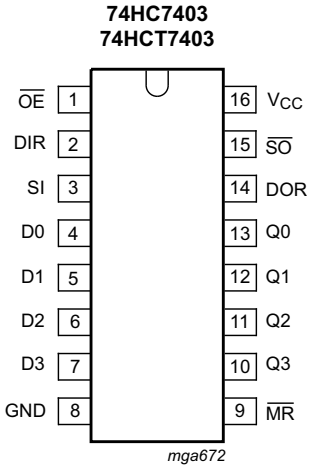


Fig 5. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}$	1	output enable input (active LOW)
DIR	2	data-in-ready output
SI	3	shift-in input (active HIGH)
D0 to D3	4, 5, 6, 7	parallel data input
GND	8	ground (0 V)
$\overline{MR}$	9	asynchronous master-reset input (active LOW)
Q0 to Q3	13, 12, 11, 10	data output
DOR	14	data-out-ready output
$\overline{SO}$	15	shift-out input (active LOW)
V_{CC}	16	supply voltage

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

7. Functional description

A DIR flag indicates the input stage status, either empty and ready to receive data (DIR = HIGH) or full and busy (DIR = LOW). When DIR and SI are HIGH, data present at D0 to D3 is shifted into the input stage; once complete DIR goes LOW. When SI is set LOW, data is automatically shifted to the output stage or to the last empty location. DIR set HIGH indicates a FIFO which can receive data.

A DOR flag indicates the output stage status, either data available (DOR = HIGH) or busy (DOR = LOW). When $\overline{SO}$ and DOR are HIGH, data is available at the outputs (Q0 to Q3). When $\overline{SO}$ is set LOW new data may be shifted into the output stage, once complete DOR is set HIGH.

7.1 Expanded format

The DOR and DIR signals are used to allow the 74HC7403; 74HCT7403 to be cascaded. Both parallel and serial expansion is possible. (see Figure 18).

Serial expansion is only possible with typical devices.

7.1.1 Parallel expension

Parallel expension is accomplished by logically ANDing the DOR and DIR signals to form a composite signal.

7.1.2 Serial expension

Serial expension is accomplished by:

- Tying the data outputs of the first device to the data inputs of the second device.
- Connecting the DOR pin of the first device to the SI pin of the second device.
- Connecting the $\overline{SO}$ pin of the first device to the DIR pin of the second device.

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V		-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V		-	±20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)		-	±35	mA
I_{CC}	supply current			-	+70	mA
I_{GND}	ground current			-	−70	mA
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	total power dissipation	DIP16 package	[1]	-	750	mW
		SO16 package	[2]	-	500	mW

[1] For DIP16 packages: above 70 °C the value of P_{tot} derates linearly with 12 mW/K.

[2] For SO16 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

9. Recommended operating conditions

Table 4. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC7403			74HCT7403			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 5. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC7403										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = –8 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = –10 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 8 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 10 mA; V_{CC} = 6.0 V	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.5	-	±5.0	-	±10.0	μA

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

Table 5. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	50	-	500	-	1000	µA
C_I	input capacitance		-	3.5	-					pF
74HCT7403										
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 4.5$ V								
		$I_O = -20$ µA	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -8$ mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 4.5$ V								
		$I_O = 20$ µA	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 8$ mA	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 5.5$ V; $V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$ A	-	-	±0.5	-	±5.0	-	±10	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	50	-	500	-	1000	µA
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A								
		per input pin; Dn inputs	-	75	270	-	338	-	368	µA
		per input pin; $\overline{OE}$ input	-	100	360	-	450	-	490	µA
		per input pin; SI input	-	150	540	-	675	-	735	µA
		per input pin; $\overline{MR}$ input	-	150	540	-	675	-	735	µA
		per input pin; $\overline{SO}$ input	-	150	540	-	675	-	735	µA
C_I	input capacitance		-	3.5	-					pF

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

11. Dynamic characteristics

Table 6. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 17.

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
74HC7403											
t_{pd}	propagation delay	$\overline{MR}$ to DIR or DOR; see Figure 8	[1]								
		V_{CC} = 2.0 V		-	69	210	-	265	-	315	ns
		V_{CC} = 4.5 V		-	25	42	-	53	-	63	ns
		V_{CC} = 6.0 V		-	20	36	-	45	-	54	ns
		SI to DIR; see Figure 6	[1]								
		V_{CC} = 2.0 V		-	66	205	-	255	-	310	ns
		V_{CC} = 4.5 V		-	24	41	-	51	-	62	ns
		V_{CC} = 5 V; C_L = 15 pF		-	15	-	-	-	-	-	ns
		V_{CC} = 6.0 V		-	19	35	-	43	-	53	ns
		$\overline{SO}$ to DOR; see Figure 9	[1]								
		V_{CC} = 2.0 V		-	94	290	-	365	-	435	ns
		V_{CC} = 4.5 V		-	34	58	-	73	-	87	ns
		V_{CC} = 5 V; C_L = 15 pF		-	15	-	-	-	-	-	ns
		V_{CC} = 6.0 V		-	27	49	-	62	-	74	ns
		DOR to Qn; see Figure 10	[1]								
		V_{CC} = 2.0 V		-	11	35	-	45	-	55	ns
		V_{CC} = 4.5 V		-	4	7	-	9	-	11	ns
		V_{CC} = 6.0 V		-	3	6	-	8	-	9	ns
		$\overline{SO}$ to Qn; see Figure 14	[1]								
		V_{CC} = 2.0 V		-	105	325	-	406	-	488	ns
		V_{CC} = 4.5 V		-	38	65	-	81	-	98	ns
		V_{CC} = 6.0 V		-	30	55	-	69	-	83	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Qn; see Figure 8									
		V_{CC} = 2.0 V		-	52	160	-	200	-	240	ns
		V_{CC} = 4.5 V		-	19	32	-	40	-	48	ns
		V_{CC} = 6.0 V		-	15	27	-	34	-	41	ns
t_{PLH}	LOW to HIGH propagation delay	SI to DOR; see Figure 10	[5]								
		V_{CC} = 2.0 V		-	2.2	7	-	8.8	-	10.5	µs
		V_{CC} = 4.5 V		-	0.8	1.4	-	1.8	-	2.1	µs
		V_{CC} = 6.0 V		-	0.6	1.2	-	1.5	-	1.8	µs
		$\overline{SO}$ to DIR; see Figure 7	[6]								
		V_{CC} = 2.0 V		-	2.8	9	-	11.2	-	13.5	µs
		V_{CC} = 4.5 V		-	1.0	1.8	-	2.2	-	2.7	µs
		V_{CC} = 6.0 V		-	0.8	1.5	-	1.9	-	2.3	µs

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

Table 6. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 17.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{en}	enable time	$\overline{OE}$ to Qn; see Figure 16 [2]								
		V_{CC} = 2.0 V	-	44	150	-	190	-	225	ns
		V_{CC} = 4.5 V	-	16	30	-	38	-	45	ns
		V_{CC} = 6.0 V	-	13	26	-	32	-	38	ns
t_{dis}	disable time	$\overline{OE}$ to Qn; see Figure 16 [3]								
		V_{CC} = 2.0 V	-	50	150	-	190	-	225	ns
		V_{CC} = 4.5 V	-	18	30	-	38	-	45	ns
		V_{CC} = 6.0 V	-	14	26	-	33	-	38	ns
t_t	transition time	Qn; see Figure 14 [4]								
		V_{CC} = 2.0 V	-	14	60	-	75	-	90	ns
		V_{CC} = 4.5 V	-	5	12	-	15	-	18	ns
		V_{CC} = 6.0 V	-	4	10	-	13	-	15	ns
t_W	pulse width	SI HIGH or LOW; see Figure 6								
		V_{CC} = 2.0 V	35	11	-	45	-	55	-	ns
		V_{CC} = 4.5 V	7	4	-	9	-	11	-	ns
		V_{CC} = 6.0 V	6	3	-	8	-	9	-	ns
		$\overline{SO}$ HIGH or LOW; see Figure 9								
		V_{CC} = 2.0 V	70	22	-	90	-	105	-	ns
		V_{CC} = 4.5 V	14	8	-	18	-	21	-	ns
		V_{CC} = 6.0 V	12	6	-	15	-	18	-	ns
		DIR HIGH; see Figure 7								
		V_{CC} = 2.0 V	10	41	130	8	165	8	195	ns
		V_{CC} = 4.5 V	5	15	26	4	33	4	39	ns
		V_{CC} = 6.0 V	4	12	22	3	28	3	23	ns
		DOR HIGH; see Figure 10								
		V_{CC} = 2.0 V	14	52	160	12	200	12	240	ns
		V_{CC} = 4.5 V	7	19	32	6	40	6	48	ns
		V_{CC} = 6.0 V	6	15	27	5	34	5	41	ns
		$\overline{MR}$ LOW; see Figure 8								
		V_{CC} = 2.0 V	120	39	-	150	-	180	-	ns
		V_{CC} = 4.5 V	24	14	-	30	-	36	-	ns
		V_{CC} = 6.0 V	20	11	-	26	-	31	-	ns
t_{rec}	recovery time	$\overline{MR}$ to SI; see Figure 15								
		V_{CC} = 2.0 V	80	24	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	7	-	17	-	20	-	ns

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

Table 6. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 17.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{su}	set-up time	Dn to SI; see Figure 13								
		V_{CC} = 2.0 V	–8	–36	-	–6	-	–6	-	ns
		V_{CC} = 4.5 V	–4	–13	-	–3	-	–3	-	ns
		V_{CC} = 6.0 V	–3	–10	-	–3	-	–3	-	ns
t_h	hold time	Dn to SI; see Figure 13								
		V_{CC} = 2.0 V	135	44	-	170	-	205	-	ns
		V_{CC} = 4.5 V	27	16	-	34	-	41	-	ns
		V_{CC} = 6.0 V	23	13	-	29	-	35	-	ns
f_{max}	maximum frequency	SI, $\overline{SO}$ burst mode; see Figure 11 and Figure 12								
		V_{CC} = 2.0 V	3.6	9.9	-	2.8	-	2.4	-	MHz
		V_{CC} = 4.5 V	18	30	-	14	-	12	-	MHz
		V_{CC} = 5 V; C_L = 15 pF	-	30	-	-	-	-	-	MHz
		V_{CC} = 6.0 V	21	36	-	16	-	14	-	MHz
		SI, $\overline{SO}$ using flags; see Figure 6 and Figure 9								
		V_{CC} = 2.0 V	3.6	9.9	-	2.8	-	2.4	-	MHz
		V_{CC} = 4.5 V	18	30	-	14	-	12	-	MHz
		V_{CC} = 5 V; C_L = 15 pF	-	30	-	-	-	-	-	MHz
		V_{CC} = 6.0 V	21	36	-	16	-	14	-	MHz
		SI, $\overline{SO}$ cascaded; see Figure 6 and Figure 9								
		V_{CC} = 2.0 V	-	7.6	-	-	-	-	-	MHz
		V_{CC} = 4.5 V	-	23	-	-	-	-	-	MHz
		V_{CC} = 6.0 V	-	27	-	-	-	-	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} [7]	-	475	-	-	-	-	-	pF

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

Table 6. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 17.

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
74HCT7403											
t_{pd}	propagation delay	$\overline{MR}$ to DIR or DOR; see Figure 8	[1]								
		V_{CC} = 4.5 V		-	30	51	-	53	-	63	ns
		SI to DIR; see Figure 6	[1]								
		V_{CC} = 4.5 V		-	25	43	-	54	-	65	ns
		V_{CC} = 5 V; C_L = 15 pF		-	17	-	-	-	-	-	ns
		$\overline{SO}$ to DOR; see Figure 9	[1]								
		V_{CC} = 4.5 V		-	36	61	-	76	-	92	ns
		V_{CC} = 5 V; C_L = 15 pF		-	17	-	-	-	-	-	ns
		DOR to Qn; see Figure 10	[1]								
		V_{CC} = 4.5 V		-	7	12	-	15	-	18	ns
		$\overline{SO}$ to Qn; see Figure 14	[1]								
		V_{CC} = 4.5 V		-	42	72	-	90	-	108	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Qn; see Figure 8									
		V_{CC} = 4.5 V		-	22	38	-	48	-	57	ns
t_{PLH}	LOW to HIGH propagation delay	SI to DOR; see Figure 10	[5]								
		V_{CC} = 4.5 V		-	0.8	1.4	-	1.75	-	2.1	µs
		$\overline{SO}$ to DIR; see Figure 7	[6]								
		V_{CC} = 4.5 V		-	1.0	1.8	-	2.25	-	2.7	µs
t_{en}	enable time	$\overline{OE}$ to Qn; see Figure 16	[2]								
		V_{CC} = 4.5 V		-	16	30	-	38	-	45	ns
t_{dis}	disable time	$\overline{OE}$ to Qn; see Figure 16	[3]								
		V_{CC} = 4.5 V		-	19	30	-	38	-	45	ns
t_t	transition time	Qn; see Figure 14	[4]								
		V_{CC} = 4.5 V		-	5	12	-	15	-	18	ns
t_W	pulse width	SI HIGH or LOW; see Figure 6									
		V_{CC} = 4.5 V		9	5	-	6	-	8	-	ns
		$\overline{SO}$ HIGH or LOW; see Figure 9									
		V_{CC} = 4.5 V		14	8	-	18	-	21	-	ns
		DIR HIGH; see Figure 7									
		V_{CC} = 4.5 V		5	17	29	4	36	4	44	ns
		DOR HIGH; see Figure 10									
		V_{CC} = 4.5 V		7	21	36	6	45	6	54	ns
		$\overline{MR}$ LOW; see Figure 8									
		V_{CC} = 4.5 V		26	15	-	33	-	39	-	ns

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

Table 6. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 17.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{rec}	recovery time	$\overline{MR}$ to SI; see Figure 15								
		V_{CC} = 4.5 V	18	10	-	23	-	27	-	ns
t_{su}	set-up time	Dn to SI; see Figure 13								
		V_{CC} = 4.5 V	–5	–16	-	–4	-	–4	-	ns
t_h	hold time	Dn to SI; see Figure 13								
		V_{CC} = 4.5 V	30	18	-	38	-	45	-	ns
f_{max}	maximum frequency	SI, $\overline{SO}$ burst mode; see Figure 11 and Figure 12								
		V_{CC} = 4.5 V	18	30	-	14	-	12	-	MHz
		V_{CC} = 5 V; C_L = 15 pF	-	30	-	-	-	-	-	MHz
		SI, $\overline{SO}$ using flags; see Figure 6 and Figure 9								
		V_{CC} = 4.5 V	18	30	-	14	-	12	-	MHz
		V_{CC} = 5 V; C_L = 15 pF	-	30	-	-	-	-	-	MHz
		SI, $\overline{SO}$ cascaded; see Figure 6 and Figure 9								
		V_{CC} = 4.5 V	-	23	-	-	-	-	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} – 1.5 V [7]	-	490	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_{en} is the same as t_{PZH} and t_{PZL}.

[3] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[4] t_t is the same as t_{THL} and t_{TLH}.

[5] This is the ripple through delay.

[6] This is the bubble-up delay.

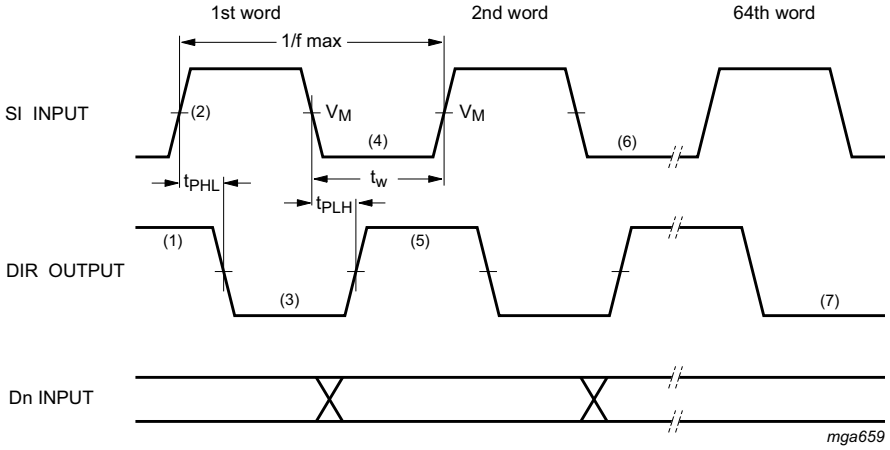
[7] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

12. Waveforms

12.1 Shifting in sequence FIFO empty to FIFO full



Measurement points are given in Table 7.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

(1) DIR initially HIGH; FIFO is prepared for valid data

(2) SI set HIGH; data loaded into input stage

(3) DIR goes LOW; input stage “busy”

(4) SI set LOW; data from first location “ripple through”

(5) DIR goes HIGH; status flag indicates FIFO prepared for additional data

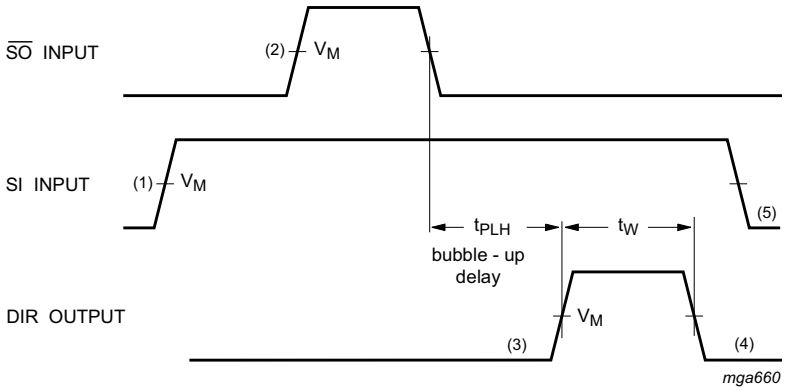
(6) Repeat process to load 2nd word through to 64th word into FIFO; DIR remains LOW; with attempt to shift into full FIFO, no data transfer occurs.

Fig 6. Propagation delay SI input to DIR output, the SI pulse width and the SI maximum frequency

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

12.2 With FIFO full; SI held HIGH in anticipation of empty location



Measurement points are given in Table 7.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

(1) FIFO is initially full, shift-in is held HIGH

(2) $\overline{SO}$ pulse; data in output stage is unloaded, “bubble-up” process of empty location begins

(3) DIR HIGH; when empty location reaches input stage, flag indicates that FIFO is prepared for data input

(4) DIR returns to LOW; data shift-in to empty location is complete, FIFO is full again

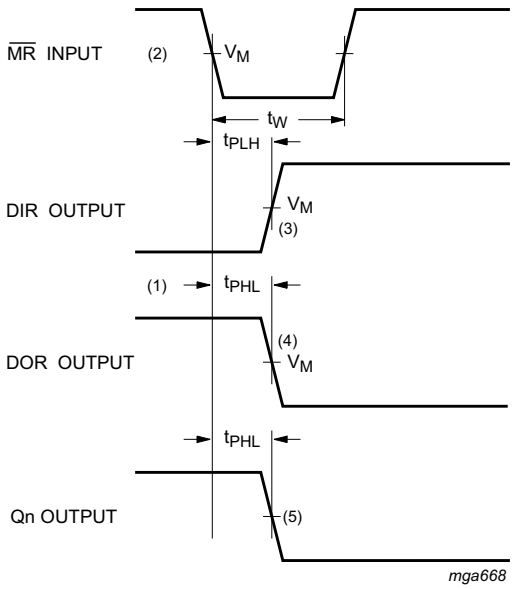
(5) SI set LOW; necessary to complete shift-in process, DIR remains LOW, because FIFO is full

Fig 7. Bubble-up delay $\overline{SO}$ input to DIR output, the DIR pulse width.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

12.3 Master reset applied with FIFO full



Measurement points are given in Table 7.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

(1) DIR LOW; output ready HIGH; assume that FIFO is full

(2) $\overline{MR}$ pulse LOW; clears FIFO

(3) DIR goes HIGH; flag indicates input prepared for valid data

(4) DOR goes LOW; flag indicates FIFO empty

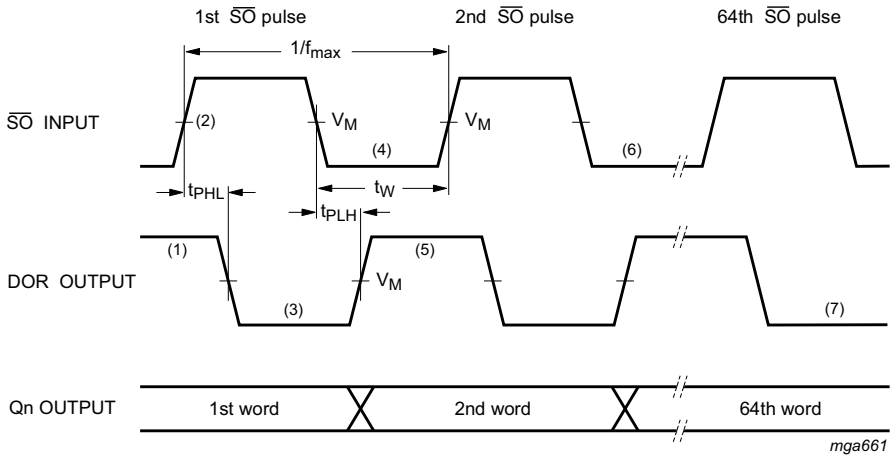
(5) Qn outputs go LOW (only last bit is reset)

Fig 8. Propagation delay $\overline{MR}$ input to DIR output, DOR output and Qn outputs and the $\overline{MR}$ pulse width.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

12.4 $\overline{SO}$ input to DOR output propagation delay



Measurement points are given in Table 7.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

(1) DOR HIGH; no data transfer in progress, valid data is present at the output stage

(2) $\overline{SO}$ set HIGH; result in DOR going LOW

(3) DOR goes LOW; output stage “busy”

(4) $\overline{SO}$ set LOW; data in the input stage is unloaded, and new data replaces it as empty location “bubbles-up” to input stage

(5) DOR goes HIGH; transfer process completed, valid data present at output after the specified propagation delay

(6) Repeat process to unload the 3rd through the 64th word from FIFO

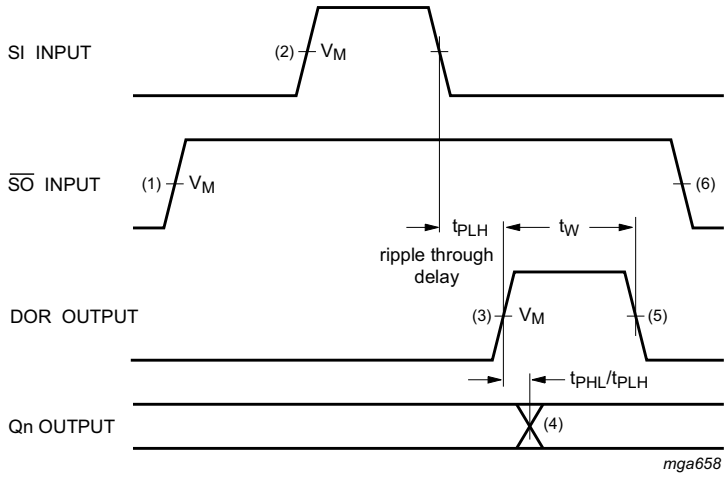
(7) DOR remains LOW; FIFO is empty

Fig 9. Propagation delay $\overline{SO}$ input to DOR output, the $\overline{SO}$ pulse width and the $\overline{SO}$ maximum frequency.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

12.5 With FIFO empty; $\overline{SO}$ is held HIGH in anticipation



Measurement points are given in Table 7.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

(1) FIFO is initially empty. $\overline{SO}$ is held HIGH.

(2) SI pulse; loads data into FIFO and initiates ripple through process

(3) DOR flag signals the arrival of valid data at the output stage

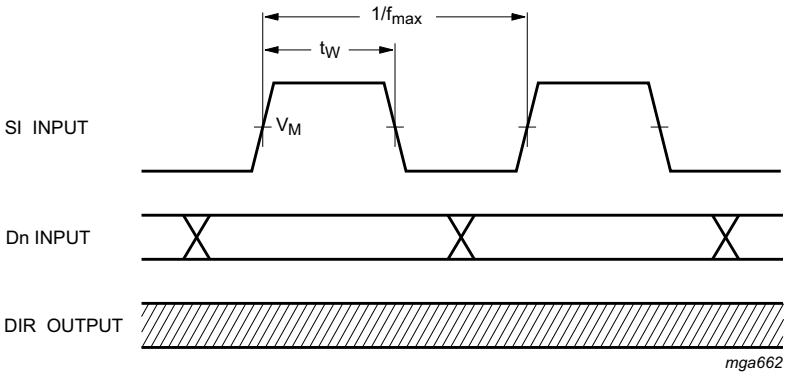
(4) Output transition; data arrives at output stage after the specified propagation delay between the rising and falling edge of the DOR pulse to the Qn output

(5) DOR goes LOW; data shift-out is completed, FIFO is empty again

(6) $\overline{SO}$ set LOW; necessary to complete shift-out process. DOR remains LOW, because FIFO is empty

Fig 10. Ripple through delay SI input to DOR output, propagation delay DOR input to Qn outputs and the DOR pulse width

12.6 Shift-in operation; high speed burst mode



Measurement points are given in Table 7.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

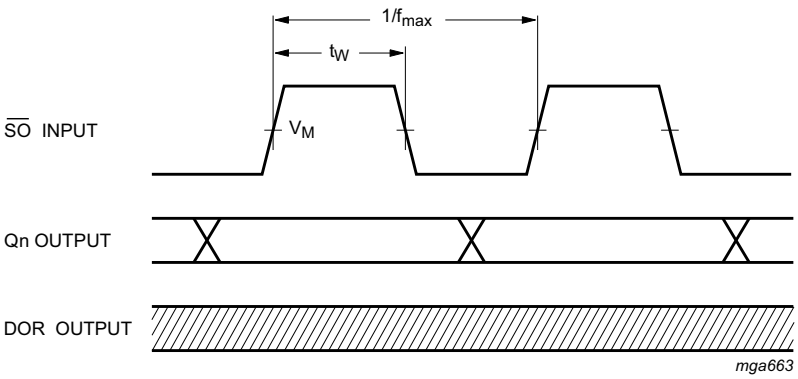
In the high-speed mode, the burst-in rate is determined by the minimum shift-in HIGH and shift-in LOW specifications. The DIR status flag is a “don’t care” condition, and a shift-in pulse can be applied regardless of the flag. An SI pulse which would overflow the storage capacity of the FIFO is ignored.

Fig 11. The SI pulse width and the SI maximum frequency

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

12.7 Shift-out operation; high speed burst mode



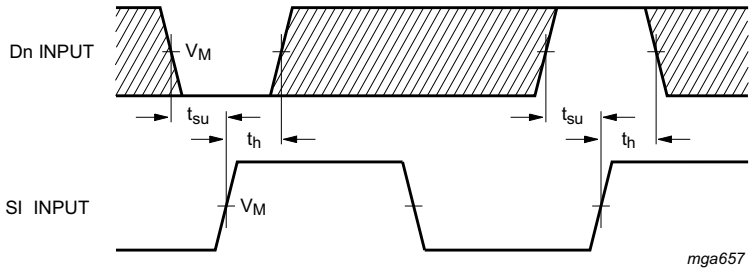
Measurement points are given in Table 7.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

In the high-speed mode, the burst-out rate is determined by the minimum shift-out HIGH and shift-out LOW specifications. The DOR flag is a “don’t care” condition, and an $\overline{SO}$ pulse can be applied without regard to the flag.

Fig 12. The $\overline{SO}$ pulse width and the $\overline{SO}$ maximum frequency

12.8 Set-up and hold times



Measurement points are given in Table 7.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

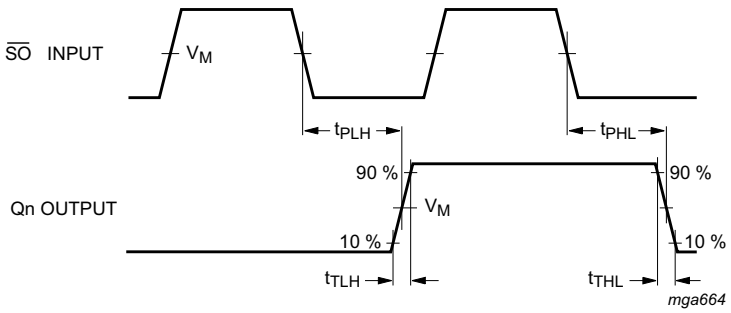
The shaded areas indicate when the output is permitted to change for predictable output performance

Fig 13. Set-up and hold times

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

12.9 $\overline{SO}$ input to Qn outputs propagation delay

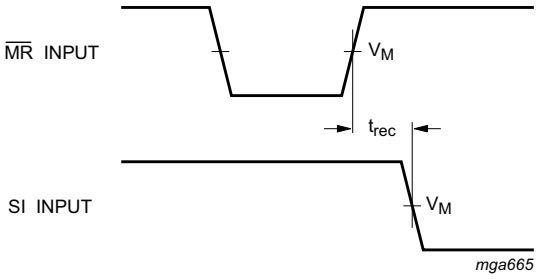


Measurement points are given in Table 7.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 14. Propagation delay $\overline{SO}$ input to Qn outputs and the output transition time

12.10 $\overline{MR}$ to SI recovery time



Measurement points are given in Table 7.

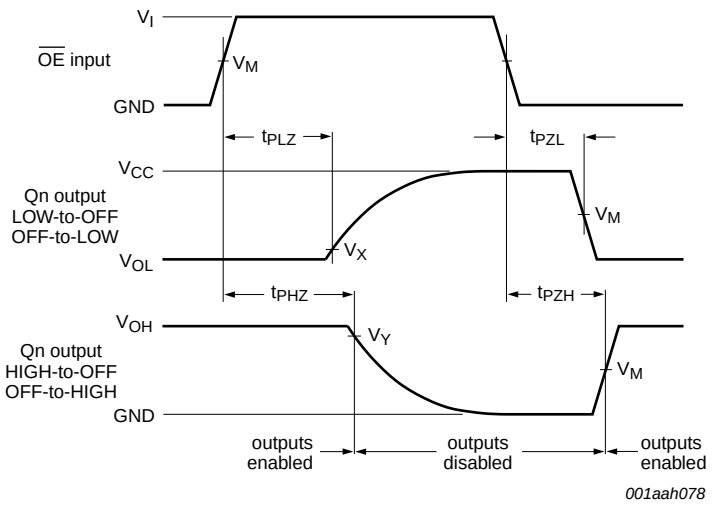
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 15. $\overline{MR}$ to SI recovery time

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

12.11 Enable and disable times



Measurement points are given in Table 7.

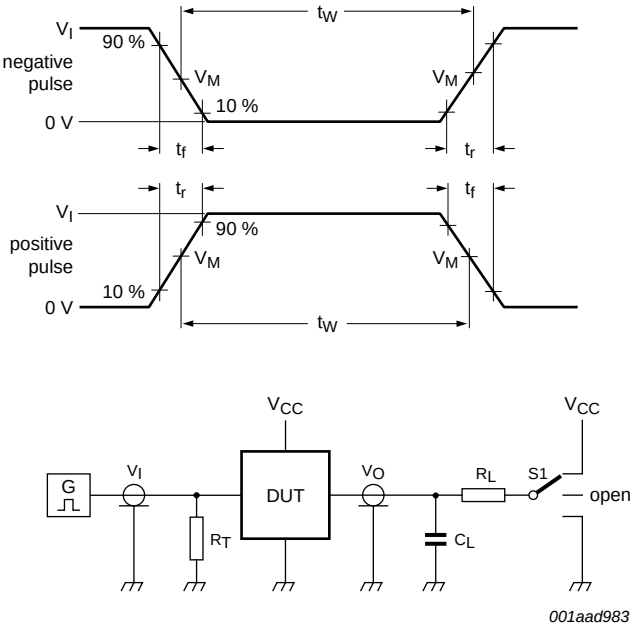
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 16. Enable and disable times

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

12.12 Test circuit for measuring switching times



Test data is given in Table 8.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig 17. Test circuit for measuring switching times

Table 7. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC7403	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
74HCT7403	1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$

Table 8. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC7403	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}
74HCT7403	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

13. Application information

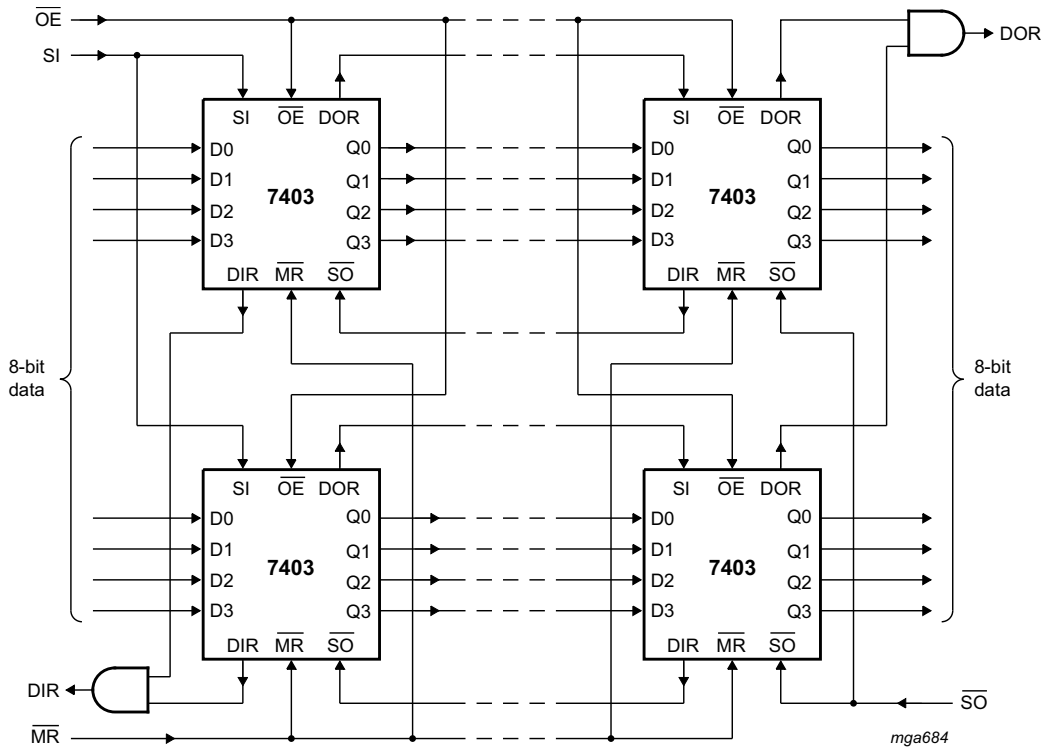
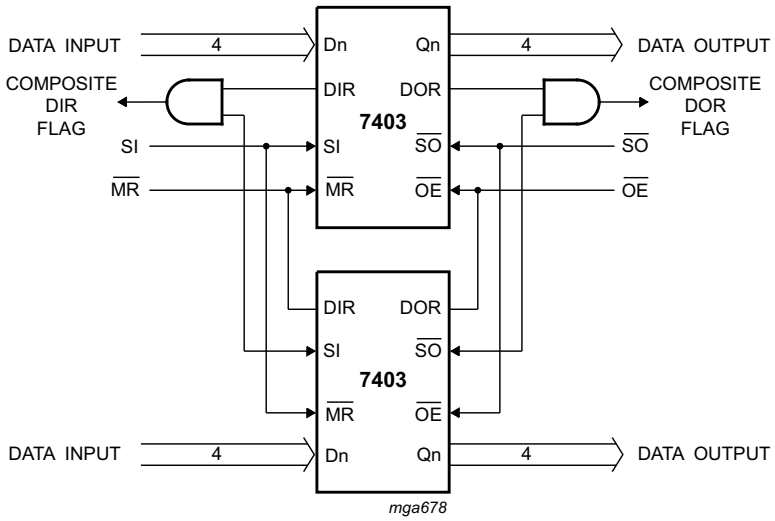


Fig 18. Expanded FIFO (parallel and serial) for increased word length; 8 bits wide x 64 n-bits

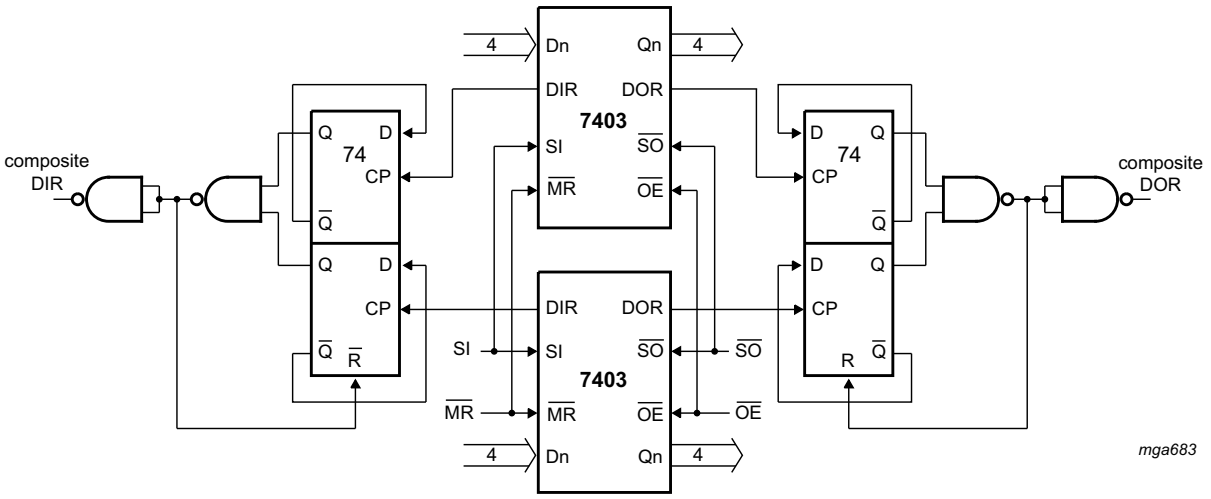


The 74HC7403; 74HCT7403 is easily expanded to increase word length. Composite DIR and DOR flags are formed with the addition of an AND gate. The basic operation and timing are identical to a single FIFO, with the exception of an added gate delay on the flags.

Fig 19. Expanded FIFO for increased word length; 64 words x 10 bits

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.



This circuit is only required if the SI input is constantly held HIGH, when the FIFO is empty and the automatic shift-in cycles are started or if the $\overline{SO}$ output is constantly held HIGH, when the FIFO is full and the automatic shift-out cycles are started (see Figure 7 and Figure 10).

Fig 20. Expanded FIFO for increased word length

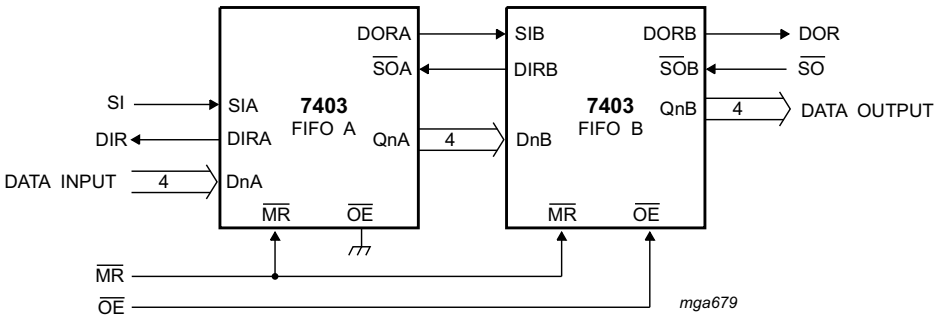
13.1 Expanded format

Figure 21 shows two cascaded FIFOs providing a capacity of 128 words x 4 bits. Figure 22 shows the signals on the nodes of both FIFOs after the application of the SI pulse, when both FIFOs are initially empty. After a ripple through delay, data arrives at the output of FIFOA. Due to $\overline{SO}$A being HIGH, a DORA pulse is generated. The requirements of SIB and DnB are satisfied by the DORA pulse width and the timing between the rising edge of DORA and QnA. After a second ripple through delay data arrives at the output of FIFOB.

Figure 23 shows the signals on the nodes of both FIFOs after the application of the $\overline{SO}$B pulse, when both FIFOs are initially full. After a bubble-up delay, a DIRB pulse is generated, which acts as a $\overline{SO}$A pulse for FIFOA. One word is transferred from the output of FIFOA to the input of FIFOB. The requirements of the $\overline{SO}$A pulse for FIFOA is satisfied by the pulse width of DORB. After a second bubble-up delay, an empty space arrives at DnA, at which time DIRA goes HIGH. Figure 24 shows the waveforms at all external nodes of both FIFOs during a complete shift-in and shift-out sequence.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

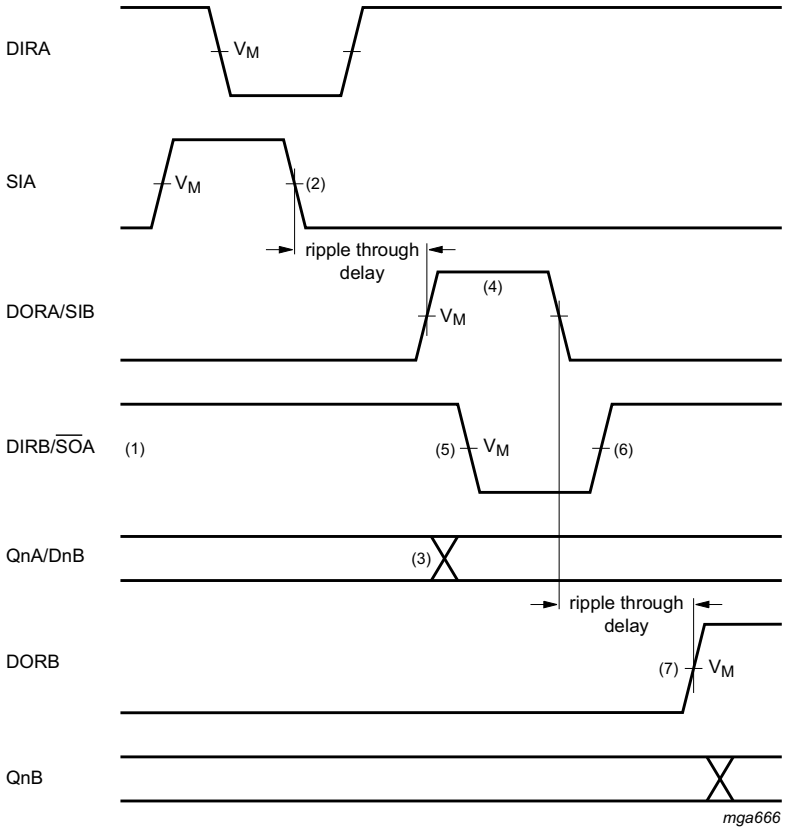


The 74HC7403; 74HCT7403 is easily cascaded to increase word capacity without external circuitry. In cascaded format, all necessary communications are handled by the FIFOs. Figure 22 and Figure 23 demonstrate the communication timing between FIFOA and FIFOB. Figure 24 provides an overview of pulses and timing of two cascaded FIFOs, when shifted full and shifted empty again.

Fig 21. Cascading for increased word capacity; 128 words x 4 bits

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.



(1) FIFOA and FIFOB are initially empty, $\overline{SO}$A held HIGH in anticipation of data

(2) Load one word into FIFOA; SI pulse; applied. results in DIR pulse

(3) Data-out A/ data-in B transition; valid data arrives at FIFOA output stage after a specified delay of the DOR flag, meeting data input set-up requirements of FIFOB.

(4) DORA and SIB pulse HIGH; (ripple through delay after SIA LOW) data is unloaded from FIFOA as a result of the data output ready pulse, data is shifted into FIFOB

(5) DIRB and $\overline{SO}$A go LOW; flag indicates that input stage of FIFOB is busy, shift-out of FIFOA is complete

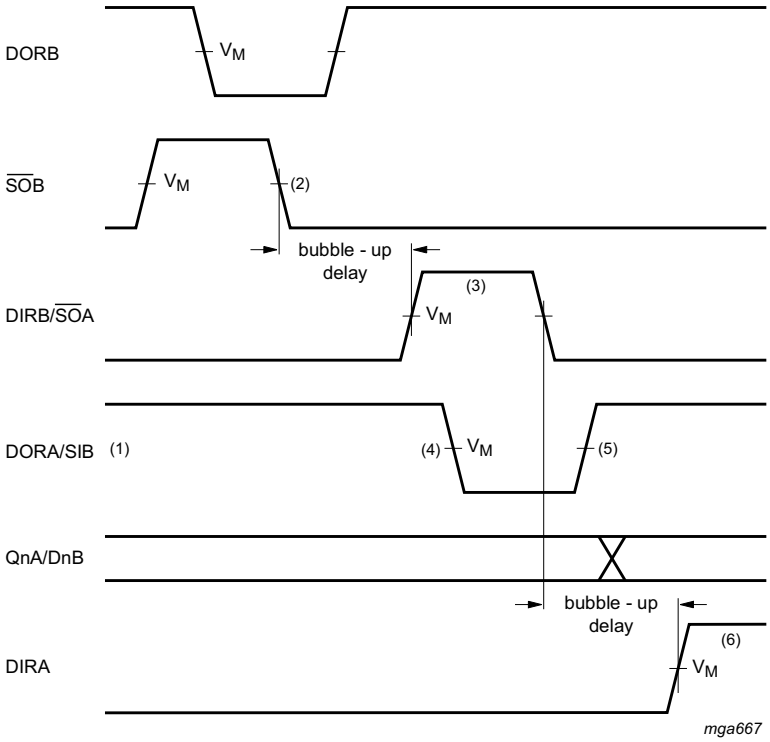
(6) DIRB and $\overline{SO}$A go HIGH automatically; the input stage of FIFOB is again able to receive data, $\overline{SO}$ is held HIGH in anticipation of additional data

(7) DORB goes HIGH; (ripple through delay after SIB LOW) valid data is present one propagation delay later at the FIFOB output stage

Fig 22. FIFO to FIFO communication; input timing under empty condition

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.



(1) FIFOA and FIFOB initially full, SIB held HIGH in anticipation of shifting in new data as an empty location bubbles-up

(2) Unload one word from FIFOB; $\overline{SO}$ pulse applied, results in DOR pulse

(3) DIRB and $\overline{SOA}$ pulse HIGH; (bubble-up delay after $\overline{SOB}$ LOW) data is loaded into FIFOB as a result of the DIR pulse, data is shifted out of FIFOA

(4) DORA and SIB go LOW; flag indicates that the output stage of FIFOA is busy, shift-in of FIFOB is complete

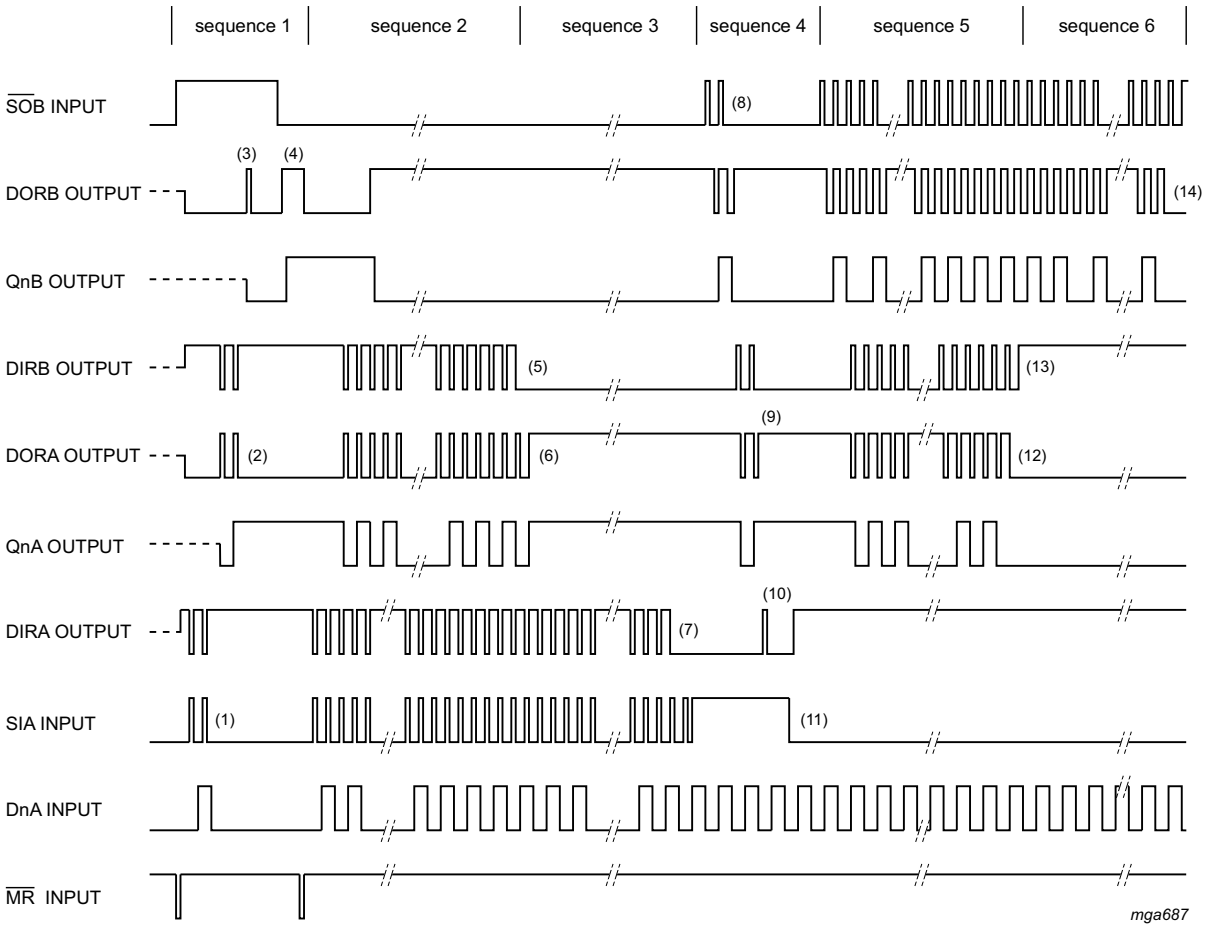
(5) DORA and SIB go HIGH; flag indicates that valid data is again available at FIFOA output stage, SIB is held HIGH, awaiting bubble-up of empty location.

(6) DIRA goes HIGH; (bubble-up delay after $\overline{SOA}$ LOW) an empty location is present at input stage of FIFOA

Fig 23. FIFO to FIFO communication; output timing under full condition

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.



See also Section 13.1.1

Fig 24. Waveforms showing the functionality and intercommunication between to FIFOs (refer to Figure 19)

13.1.1 Sequence 1 (both FIFOs empty, starting SHIFT-IN process)

After an $\overline{MR}$ pulse has been applied, FIFOA and FIFOB are empty. The DOR flags of FIFOA and FIFOB go LOW due to no valid data being present at the outputs. The DIR flags are set HIGH due to the FIFOs being ready to accept data. $\overline{SOB}$ is held HIGH and two SIA pulses are applied (1). These pulses allow two data words to ripple through the output stage of FIFOA and the input stage of FIFOB (2). When data arrives at the output of FIFOB, a DORB pulse is generated (3). When $\overline{SOB}$ goes LOW, the first bit is shifted out and a second bit ripples through to the output after which DORB goes high (4).

13.1.2 Sequence 2 (FIFOB runs full)

After the $\overline{MR}$ pulse, a series of 64 SI pulses are applied. When 64 words are shifted in, DIRB remains LOW due to FIFOB being full (5). DORA goes LOW due to FIFOA being empty.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

13.1.3 Sequence 3 (FIFOA runs full)

When 65 words are shifted in, DORA remains HIGH due to valid data remaining at the output of FIFOA. QnA remains HIGH, being the polarity of the 65th word (6). After the 128th SI pulse, DIR remains LOW and both FIFOs are full (7). Additional pulses have no effect.

13.1.4 Sequence 4 (both FIFOs full, starting SHIFT-OUT)

SIA is held HIGH and two $\overline{SO}$B pulses are applied (8). These pulses shift out two words and thus allow two empty locations to bubble-up to the input stage of FIFOB, and proceed to FIFOA (9). When the first empty location arrives at the input of FIFOA, a DIRA pulse is generated (10) and a new word is shifted into FIFOA. SIA is made LOW and now the second empty location reaches the input stage of FIFOA, after which DIRA remains HIGH (11).

13.1.5 Sequence 5 (FIFOA runs empty)

At the start of sequence 5 FIFOA contains 63 valid words due to two words being shifted out and one word being shifted in, in sequence 4. And additional series of $\overline{SO}$B pulses are applied. After 63 $\overline{SO}$B pulses, all words from FIFOA are shifted in FIFOB. DORA remains LOW (12).

13.1.6 Sequence 6 (FIFOB runs empty)

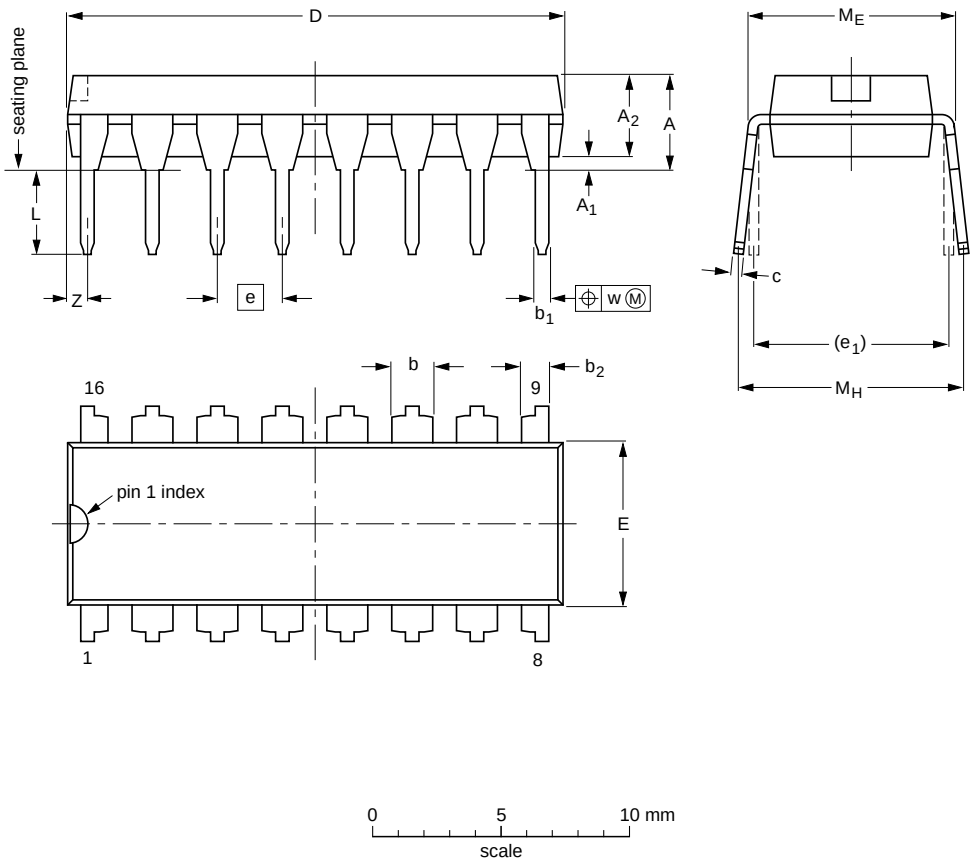
After the next $\overline{SO}$B pulse, DIRB remains HIGH due to the input stage of FIFOB being empty. After another 63 $\overline{SO}$B pulses, DORB remains LOW due to both FIFOS being empty (14). Additional $\overline{SO}$B pulses have no effect. The last word remains available at the output Qn.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

14. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

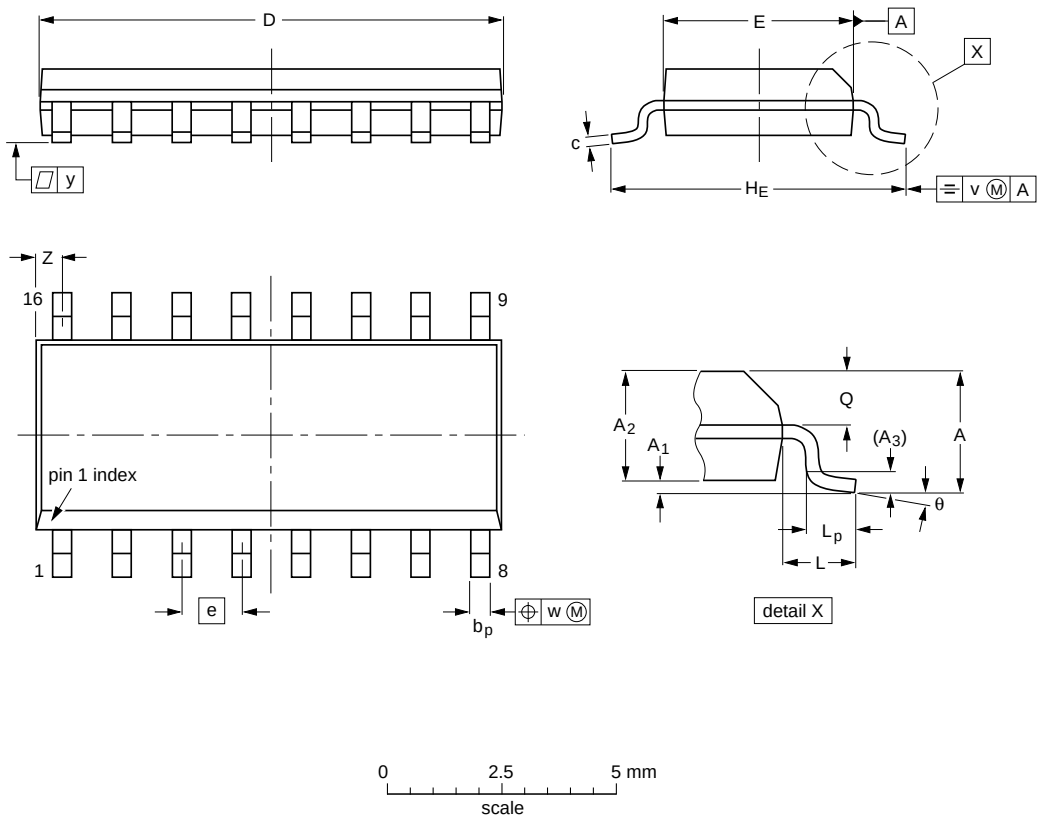
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 25. Package outline SOT38-4 (DIP16)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 26. Package outline SOT109-1 (SO16)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

15. Abbreviations

Table 9. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic
FIFO	First In First Out

16. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT7403 v.4	20120924	Product data sheet	-	74HC_HCT7403_CNV v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT7403_CNV v.3	19970916	Product specification	-	-

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

17.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

18. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2012. All rights reserved.

19. Contents

1 General description 1
2 Features and benefits 1
3 Applications 1
4 Ordering information 2
5 Functional diagram 2
6 Pinning information 4
6.1 Pinning 4
6.2 Pin description 4
7 Functional description 5
7.1 Expanded format 5
7.1.1 Parallel expension 5
7.1.2 Serial expension 5
8 Limiting values 5
9 Recommended operating conditions 6
10 Static characteristics 6
11 Dynamic characteristics 8
12 Waveforms 13
12.1 Shifting in sequence FIFO empty to FIFO full. 13
12.2 With FIFO full; SI held HIGH in anticipation of empty location 14
12.3 Master reset applied with FIFO full 15
12.4 $\overline{SO}$ input to DOR output propagation delay . . 16
12.5 With FIFO empty; $\overline{SO}$ is held HIGH in anticipation 17
12.6 Shift-in operation; high speed burst mode . . . 17
12.7 Shift-out operation; high speed burst mode . . 18
12.8 Set-up and hold times 18
12.9 $\overline{SO}$ input to Qn outputs propagation delay . . . 19
12.10 $\overline{MR}$ to SI recovery time 19
12.11 Enable and disable times 20
12.12 Test circuit for measuring switching times . . . 21
13 Application information 22
13.1 Expanded format 23
13.1.1 Sequence 1 (both FIFOs empty, starting SHIFT-IN process) 27
13.1.2 Sequence 2 (FIFOB runs full) 27
13.1.3 Sequence 3 (FIFOA runs full) 28
13.1.4 Sequence 4 (both FIFOs full, s tarting SHIFT-OUT) 28
13.1.5 Sequence 5 (FIFOA runs empty) 28
13.1.6 Sequence 6 (FIFOB runs empty) 28
14 Package outline 29
15 Abbreviations 31
16 Revision history 31
17 Legal information 32
17.1 Data sheet status 32
17.2 Definitions 32
17.3 Disclaimers 32
17.4 Trademarks 33
18 Contact information 33
19 Contents 34

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2012. All rights reserved.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 24 September 2012
Document identifier: 74HC_HCT7403