74HC86

Quad 2-Input Exclusive OR Gate

High−Performance Silicon−Gate CMOS

The 74HC86 is identical in pinout to the LS86. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

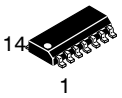
Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with JEDEC Standard No. 7A Requirements
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 56 FETs or 14 Equivalent Gates
- These are Pb−Free Devices

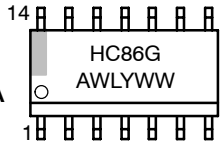
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MARKING DIAGRAMS

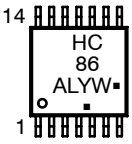


SOIC−14
D SUFFIX
CASE 751A





TSSOP−14
DT SUFFIX
CASE 948G



HC86	= Device Code
A	= Assembly Location
L, WL	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

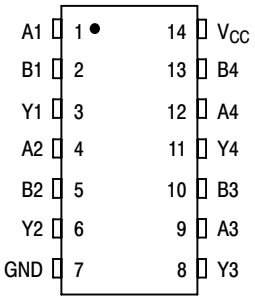
(Note: Microdot may be in either location)

ORDERING INFORMATION

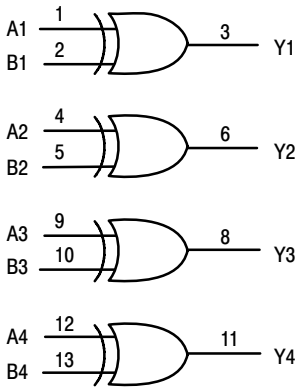
See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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PIN ASSIGNMENT



LOGIC DIAGRAM



$Y = A \oplus B$
$= \overline{A}B + A\overline{B}$

PIN 14 = V_{CC}
PIN 7 = GND

FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	L

ORDERING INFORMATION

Device	Package	Shipping†
74HC86DR2G	SOIC−14 (Pb−Free)	2500 / Tape & Reel
74HC86DTR2G	TSSOP−14*	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	− 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	− 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	− 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	− 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (SOIC or TSSOP Package)	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — SOIC Package: − 7 mW/°C from 65° to 125°C
TSSOP Package: − 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		− 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} (V)	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \leq 20$ μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \leq 20$ μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq 2.4$ mA $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \leq 2.4$ mA $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	6.0	2.0	20	40	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t, = t_f = 6 ns)

Symbol	Parameter	V_{CC} (V)	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 3.0 4.5 6.0	100 80 20 17	125 90 25 21	150 110 31 26	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Gate)*	33	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

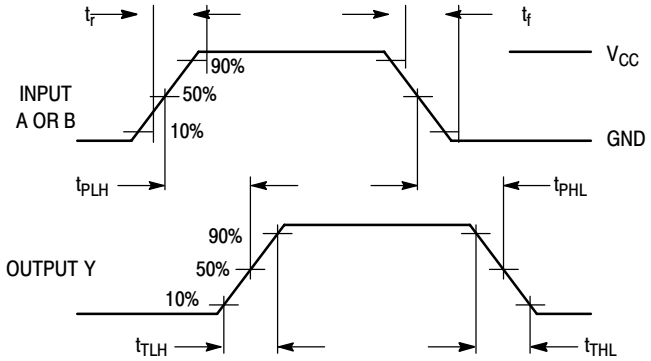
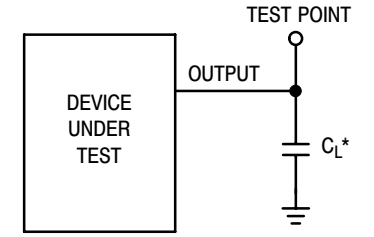


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

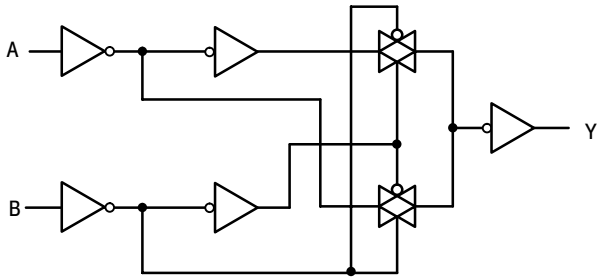
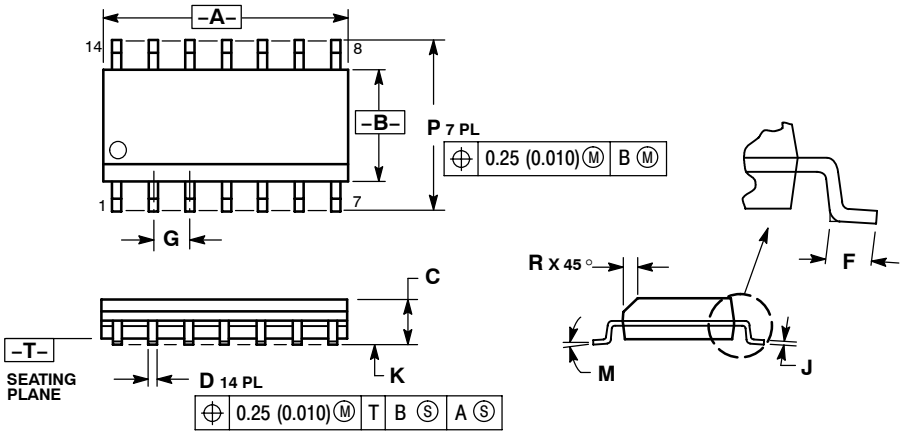


Figure 3. Expanded Logic Diagram
(1/4 of Device)

PACKAGE DIMENSIONS

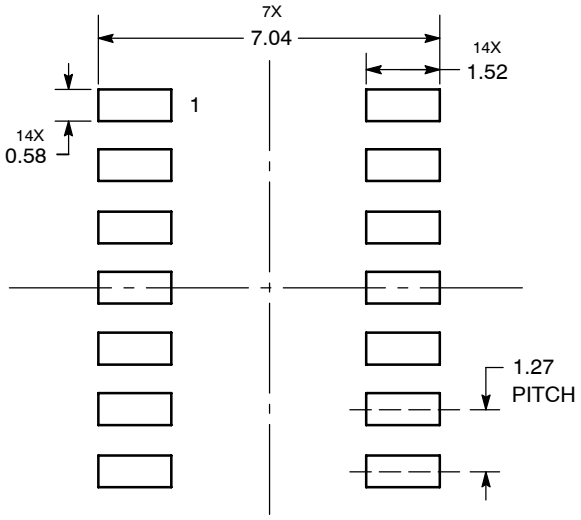
SOIC−14
CASE 751A−03
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*

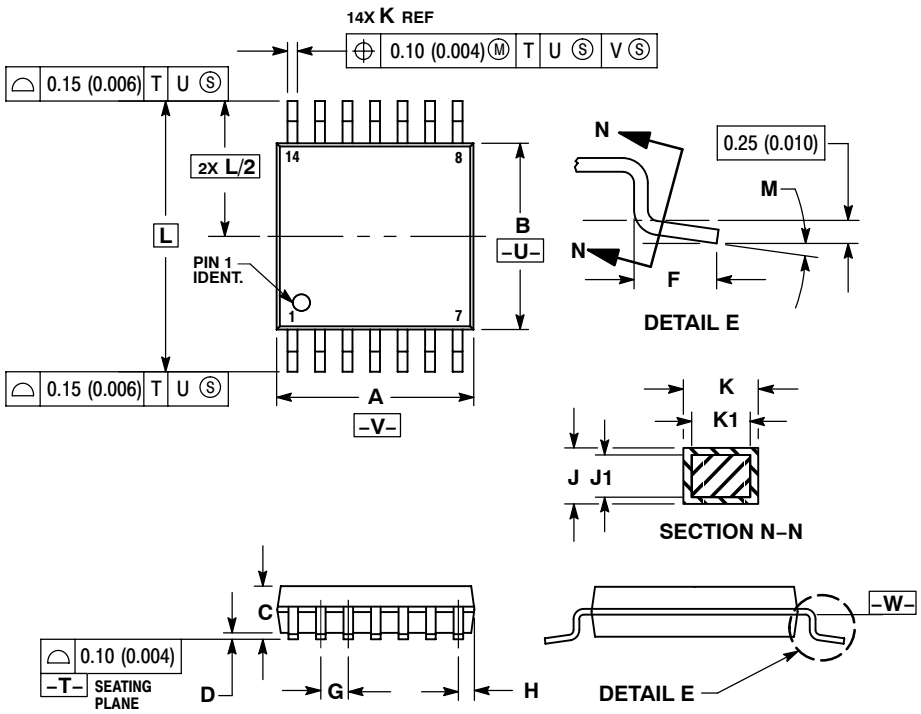


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

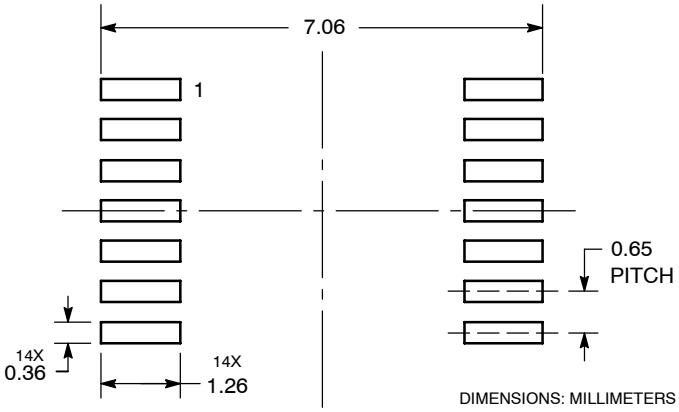
TSSOP−14
CASE 948G−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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