# 74HC03; 74HCT03

## Quad 2-input NAND gate; open-drain output

Rev. 7 — 16 February 2024 Product data sheet

## 1. General description

The 74HC03; 74HCT03 is a quad 2-input NAND gate with open-drain outputs. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of $V_{CC}$.

## 2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Input levels:
  - For 74HC03: CMOS level
  - For 74HCT03: TTL level
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74HC03D<br>74HCT03D | -40 °C to +125 °C | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74HC03PW<br>74HCT03PW | -40 °C to +125 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |

# 4. Functional diagram

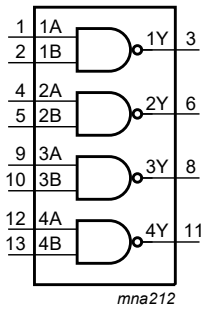



Fig. 1. Logic symbol

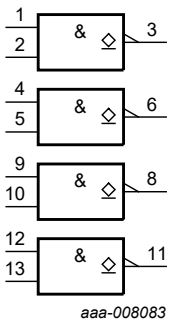



Fig. 2. IEC logic symbol

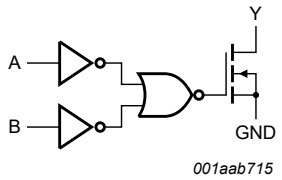
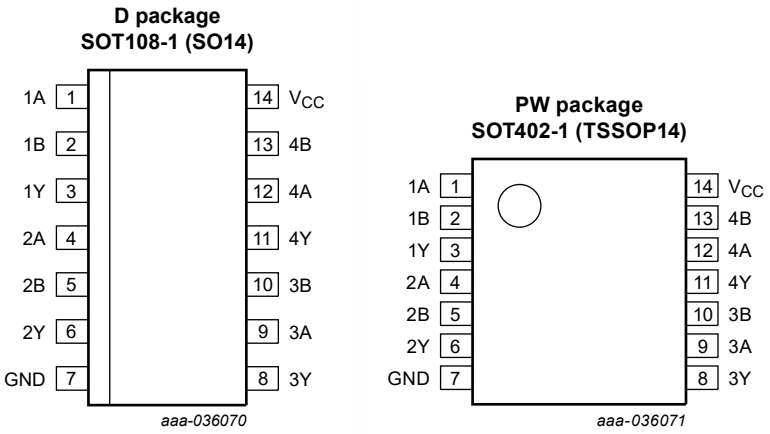



Fig. 3. Logic diagram (one gate)

# 5. Pinning information

## 5.1. Pinning




## 5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|---|---|---|
| 1A, 2A, 3A, 4A | 1, 4, 9, 12 | data input |
| 1B, 2B, 3B, 4B | 2, 5, 10, 13 | data input |
| 1Y, 2Y, 3Y, 4Y | 3, 6, 8, 11 | data output |
| GND | 7 | ground (0 V) |
| $V_{CC}$ | 14 | supply voltage |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# 6. Functional description

**Table 3. Function table**

*H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.*

| Input | | Output |
|---|---|---|
| **nA** | **nB** | **nY** |
| L | L | Z |
| L | H | Z |
| H | L | Z |
| H | H | L |

# 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | -0.5 | +7 | V |
| $V_O$ | output voltage | | [1] | -0.5 | +7 | V |
| $I_{IK}$ | input clamping current | $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V | [1] | - | ±20 | mA |
| $I_{OK}$ | output clamping current | $V_O < -0.5$ V | [1] | - | -20 | mA |
| $I_O$ | output current | $-0.5$ V $< V_O$ | | - | -25 | mA |
| $I_{CC}$ | supply current | | | - | 50 | mA |
| $I_{GND}$ | ground current | | | -50 | - | mA |
| $T_{stg}$ | storage temperature | | | -65 | +150 | °C |
| $P_{tot}$ | total power dissipation | | [2] | - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT108-1 (SO14) package: $P_{tot}$ derates linearly with 10.1 mW/K above 100 °C.
For SOT402-1 (TSSOP14) package: $P_{tot}$ derates linearly with 7.3 mW/K above 81 °C.

# 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

*Voltages are referenced to GND (ground = 0 V)*

| Symbol | Parameter | Conditions | 74HC03 | | | 74HCT03 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{CC}$ | supply voltage | | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V |
| $V_I$ | input voltage | | 0 | - | $V_{CC}$ | 0 | - | $V_{CC}$ | V |
| $V_O$ | output voltage | | 0 | - | $V_{CC}$ | 0 | - | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | | -40 | +25 | +125 | -40 | +25 | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | $V_{CC}$ = 2.0 V | - | - | 625 | - | - | - | ns/V |
| | | $V_{CC}$ = 4.5 V | - | 1.67 | 139 | - | 1.67 | 139 | ns/V |
| | | $V_{CC}$ = 6.0 V | - | - | 83 | - | - | - | ns/V |


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# 9. Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| **74HC03** | | | | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 2.0 V | 1.5 | 1.2 | - | 1.5 | - | 1.5 | - | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | 2.4 | - | 3.15 | - | 3.15 | - | V |
| | | $V_{CC}$ = 6.0 V | 4.2 | 3.2 | - | 4.2 | - | 4.2 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 2.0 V | - | 0.8 | 0.5 | - | 0.5 | - | 0.5 | V |
| | | $V_{CC}$ = 4.5 V | - | 2.1 | 1.35 | - | 1.35 | - | 1.35 | V |
| | | $V_{CC}$ = 6.0 V | - | 2.8 | 1.8 | - | 1.8 | - | 1.8 | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = 20 µA; $V_{CC}$ = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 20 µA; $V_{CC}$ = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 20 µA; $V_{CC}$ = 6.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 4.0 mA; $V_{CC}$ = 4.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| | | $I_O$ = 5.2 mA; $V_{CC}$ = 6.0 V | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V |
| $I_I$ | input leakage current | $V_I$ = $V_{CC}$ or GND; $V_{CC}$ = 6.0 V | - | 0.1 | - | - | ±1 | - | ±1 | µA |
| $I_{OZ}$ | OFF-state output current | $V_I$ = $V_{IL}$; $V_{CC}$ = 6.0 V; $V_O$ = $V_{CC}$ or GND | - | - | ±0.5 | - | ±5.0 | - | ±10 | µA |
| $I_{CC}$ | supply current | $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 6.0 V | - | 2.0 | - | - | 20 | - | 40 | µA |
| $C_I$ | input capacitance | | - | 3.5 | - | - | - | - | - | pF |
| **74HCT03** | | | | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | 2.0 | 1.6 | - | 2.0 | - | 2.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | - | 1.2 | 0.8 | - | 0.8 | - | 0.8 | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$; $V_{CC}$ = 4.5 V | | | | | | | | |
| | | $I_O$ = 20 µA | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 4.0 mA | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| $I_I$ | input leakage current | $V_I$ = $V_{CC}$ or GND; $V_{CC}$ = 5.5 V | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| $I_{OZ}$ | OFF-state output current | $V_I$ = $V_{IL}$; $V_{CC}$ = 5.5 V; $V_O$ = $V_{CC}$ or GND | - | - | ±0.5 | - | ±5.0 | - | ±10 | µA |
| $I_{CC}$ | supply current | $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 5.5 V | - | - | 2.0 | - | 20 | - | 40 | µA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_I$ = $V_{CC}$ - 2.1 V; $I_O$ = 0 A; other inputs at $V_{CC}$ or GND; $V_{CC}$ = 4.5 V to 5.5 V | - | 100 | 360 | - | 450 | - | 490 | µA |
| $C_I$ | input capacitance | | - | 3.5 | - | - | - | - | - | pF |


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# 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*GND = 0 V; $C_L$ = 50 pF; for test circuit, see Fig. 5.*

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | -40 °C to +125 °C | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Max | Max | |
| **74HC03** | | | | | | | | |
| $t_{pd}$ | propagation delay | nA, nB to nY; see Fig. 4 [1] | | | | | | |
| | | $V_{CC}$ = 2.0 V | - | 28 | 95 | 120 | 145 | ns |
| | | $V_{CC}$ = 4.5 V | - | 10 | 19 | 24 | 29 | ns |
| | | $V_{CC}$ = 5.0 V; $C_L$ = 15 pF | - | 8 | - | - | - | ns |
| | | $V_{CC}$ = 6.0 V | - | 8 | 16 | 20 | 25 | ns |
| $t_t$ | transition time | see Fig. 4 [2] | | | | | | |
| | | $V_{CC}$ = 2.0 V | - | 19 | 75 | 95 | 110 | ns |
| | | $V_{CC}$ = 4.5 V | - | 7 | 15 | 19 | 22 | ns |
| | | $V_{CC}$ = 6.0 V | - | 6 | 13 | 16 | 19 | ns |
| $C_{PD}$ | power dissipation capacitance | per package; $V_I$ = GND to $V_{CC}$ [3] | - | 4 | - | - | - | pF |
| **74HCT03** | | | | | | | | |
| $t_{pd}$ | propagation delay | nA, nB to nY; see Fig. 4 [1] | | | | | | |
| | | $V_{CC}$ = 4.5 V | - | 12 | 24 | 30 | 36 | ns |
| | | $V_{CC}$ = 5.0 V; $C_L$ = 15 pF | - | 10 | - | - | - | ns |
| $t_t$ | transition time | $V_{CC}$ = 4.5 V; see Fig. 4 [2] | - | 7 | 15 | 19 | 22 | ns |
| $C_{PD}$ | power dissipation capacitance | per package; $V_I$ = GND to $V_{CC}$ - 1.5 V [3] | - | 4 | - | - | - | pF |

[1] $t_{pd}$ is the same as $t_{PLZ}$ and $t_{PZL}$.

[2] $t_t$ is the same as $t_{THL}$.

[3] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW):

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

$f_i$ = input frequency in MHz;

$f_o$ = output frequency in MHz;

$C_L$ = output load capacitance in pF;

$V_{CC}$ = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.


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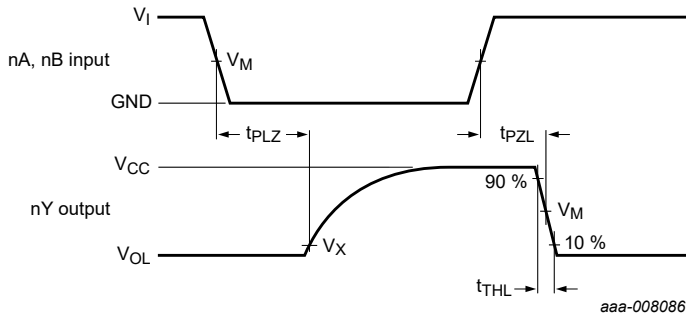
## 10.1. Waveforms and test circuit



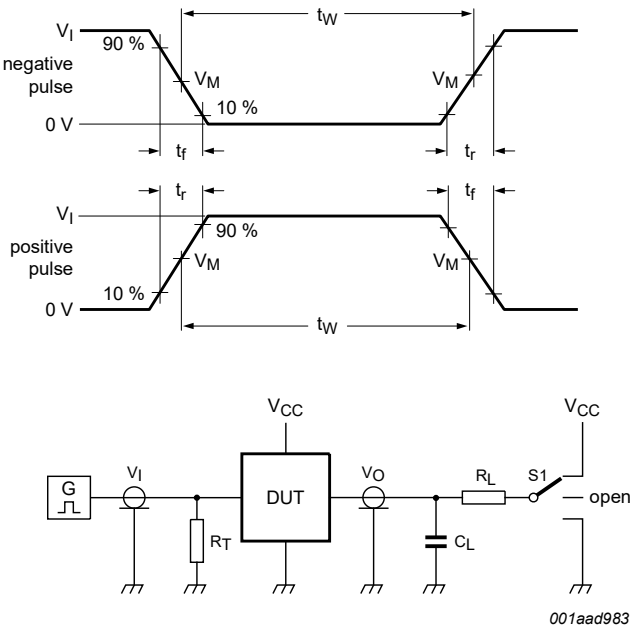

Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Fig. 4. Input to output propagation delays**

**Table 8. Measurement points**

| Type | Input | Output | |
|---|---|---|---|
| | $V_M$ | $V_M$ | $V_X$ |
| 74HC03 | 0.5 × $V_{CC}$ | 0.5 × $V_{CC}$ | 0.1 × $V_{CC}$ |
| 74HCT03 | 1.3 V | 1.3 V | 0.1 × $V_{CC}$ |




Test data is given in Table 9.

Definitions test circuit:

$R_T$ = termination resistance should be equal to output impedance $Z_o$ of the pulse generator;

$C_L$ = load capacitance including jig and probe capacitance.

**Fig. 5. Test circuit for measuring switching times**

**Table 9. Test data**

| Type | Input | | Load | | S1 position |
|---|---|---|---|---|---|
| | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PZL}$, $t_{PLZ}$ |
| 74HC03 | $V_{CC}$ | 6 ns | 15 pF, 50 pF | 1 kΩ | $V_{CC}$ |
| 74HCT03 | 3.0 V | 6 ns | 15 pF, 50 pF | 1 kΩ | $V_{CC}$ |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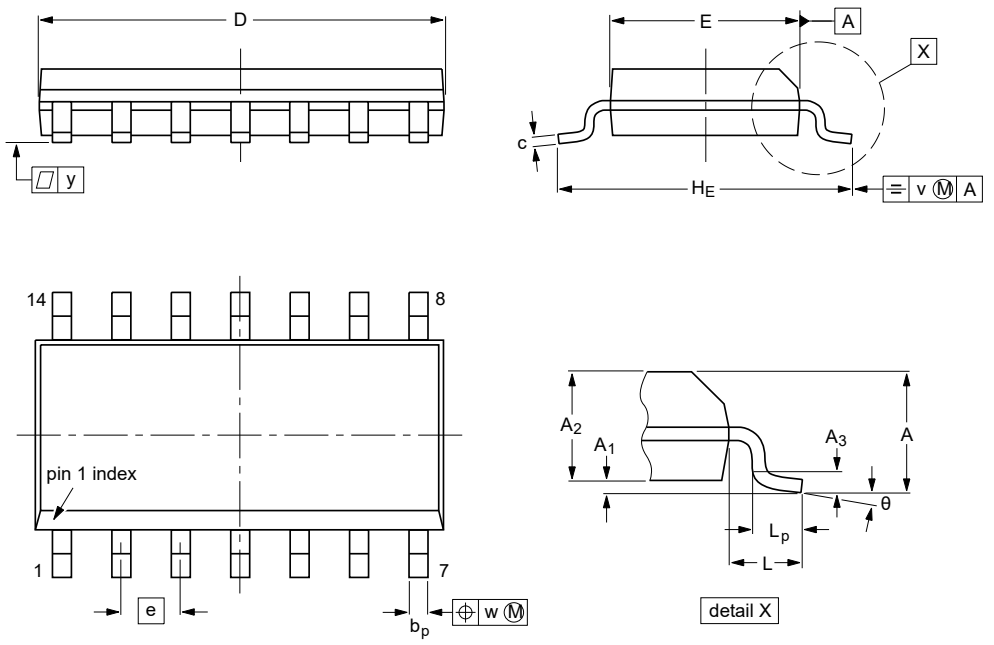
# 11. Package outline

**SO14: plastic small outline package; 14 leads; body width 3.9 mm** **SOT108-1**




Dimensions (inch dimensions are derived from the original mm dimensions)

| Unit | | A | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | v | w | y | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 1.75 | 0.25 | | | 0.51 | 0.25 | 8.75 | 4.0 | | 6.2 | | 1.27 | | | | 8° |
| | nom | | | | 0.25 | | | | | 1.27 | | 1.05 | | 0.2 | 0.25 | 0.1 | |
| | min | | 0.10 | 1.25 | | 0.31 | 0.10 | 8.55 | 3.8 | | 5.8 | | 0.4 | | | | 0° |
| inches | max | 0.069 | 0.010 | | | 0.020 | 0.010 | 0.344 | 0.16 | | 0.244 | | 0.05 | | | | 8° |
| | nom | | | | 0.01 | | | | | 0.05 | | 0.041 | | 0.008 | 0.01 | 0.004 | |
| | min | | 0.004 | 0.049 | | 0.012 | 0.004 | 0.337 | 0.15 | | 0.228 | | 0.016 | | | | 0° |

Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

*sot108-1_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT108-1 | | MS-012 | | | | ~~03-02-19~~ 23-10-27 |

**Fig. 6. Package outline SOT108-1 (SO14)**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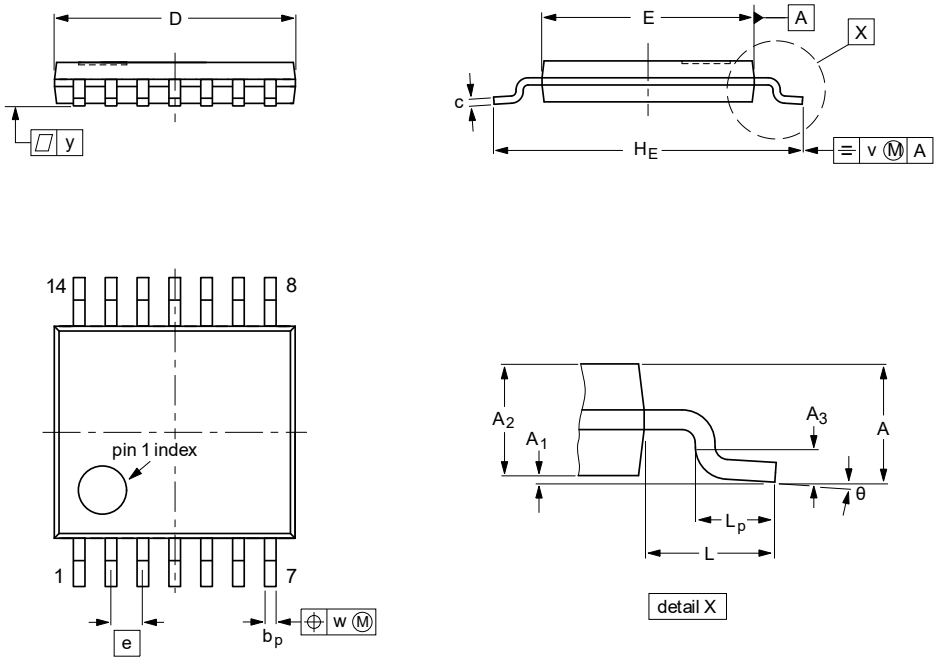
**TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm** **SOT402-1**




Dimensions (mm are the original dimensions)

| Unit | | A | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | v | w | y | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 1.20 | 0.15 | 1.05 | | 0.30 | 0.2 | 5.1 | 4.5 | | 6.6 | | 0.75 | | | | 8° |
| | nom | | | | 0.25 | | | | | 0.65 | | 1 | | 0.2 | 0.1 | 0.1 | |
| | min | | 0.05 | 0.80 | | 0.19 | 0.09 | 4.9 | 4.3 | | 6.2 | | 0.45 | | | | 0° |

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

*sot402-1_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT402-1 | | MO-153 | | | | ~~03-02-18~~ 23-10-27 |

**Fig. 7. Package outline SOT402-1 (TSSOP14)**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## 12. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| TTL | Transistor-Transistor Logic |

## 13. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74HC_HCT03 v.7 | 20240216 | Product data sheet | - | 74HC_HCT03 v.6 |
| Modifications: | • Section 2: ESD specification updated according to the latest JEDEC standard.<br>• Fig. 6, Fig. 7: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153 | | | |
| 74HC_HCT03 v.6 | 20210810 | Product data sheet | - | 74HC_HCT03 v.5 |
| Modifications: | • Section 2 updated.<br>• Type number 74HC03DB (SOT337-1/SSOP14) removed. | | | |
| 74HC_HCT03 v.5 | 20210107 | Product data sheet | - | 74HC_HCT03 v.4 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Type number 74HCT03DB (SOT337-1 / SSOP14) removed.<br>• Section 7: Derating values for $P_{tot}$ total power dissipation have been updated. | | | |
| 74HC_HCT03 v.4 | 20151127 | Product data sheet | - | 74HC_HCT03 v.3 |
| Modifications: | • Type numbers 74HC03N and 74HCT03N (SOT27-1) removed. | | | |
| 74HC_HCT03 v.3 | 20130627 | Product data sheet | - | 74HC_HCT03_CNV v.2 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate. | | | |
| 74HC_HCT03_CNV v.2 | 19970827 | Product specification | - | - |


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## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
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[2] The term 'short data sheet' is explained in section "Definitions".
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For more information, please visit: http://www.nexperia.com
For sales office addresses, please send an email to: salesaddresses@nexperia.com
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