74HC245; 74HCT245

Octal bus transceiver; 3-state

Rev. 9 — 9 May 2025 Product data sheet

1. General description

The 74HC245; 74HCT245 is an 8-bit transceiver with 3-state outputs. The device features an output enable ($\overline{OE}$) and send/receive (DIR) for direction control. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Octal bidirectional bus interface
- Non-inverting 3-state outputs
- Input levels:
  - For 74HC245: CMOS level
  - For 74HCT245: TTL level
- Complies with JEDEC standards
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC245D 74HCT245D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HC245PW 74HCT245PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74HC245BQ 74HCT245BQ	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1
74HC245BZ 74HCT245BZ	-40 °C to +125 °C	DHXQFN20	plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package; no leads; 20 terminals; 0.4 mm pitch; body 2 mm × 3.2 mm × 0.48 mm	SOT8020-1

4. Functional diagram

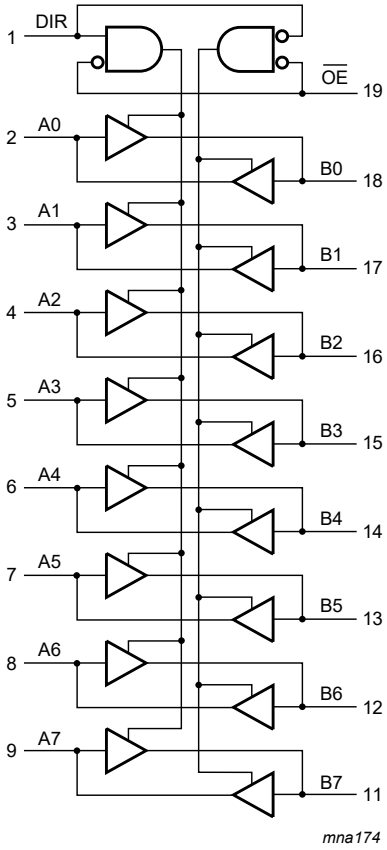


Fig. 1. Logic symbol

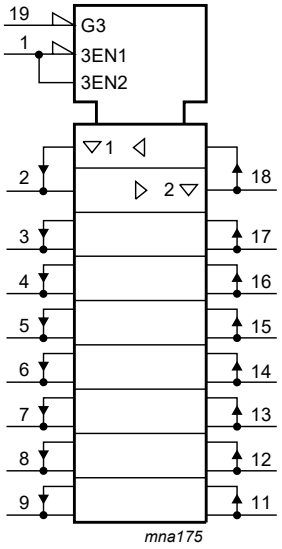


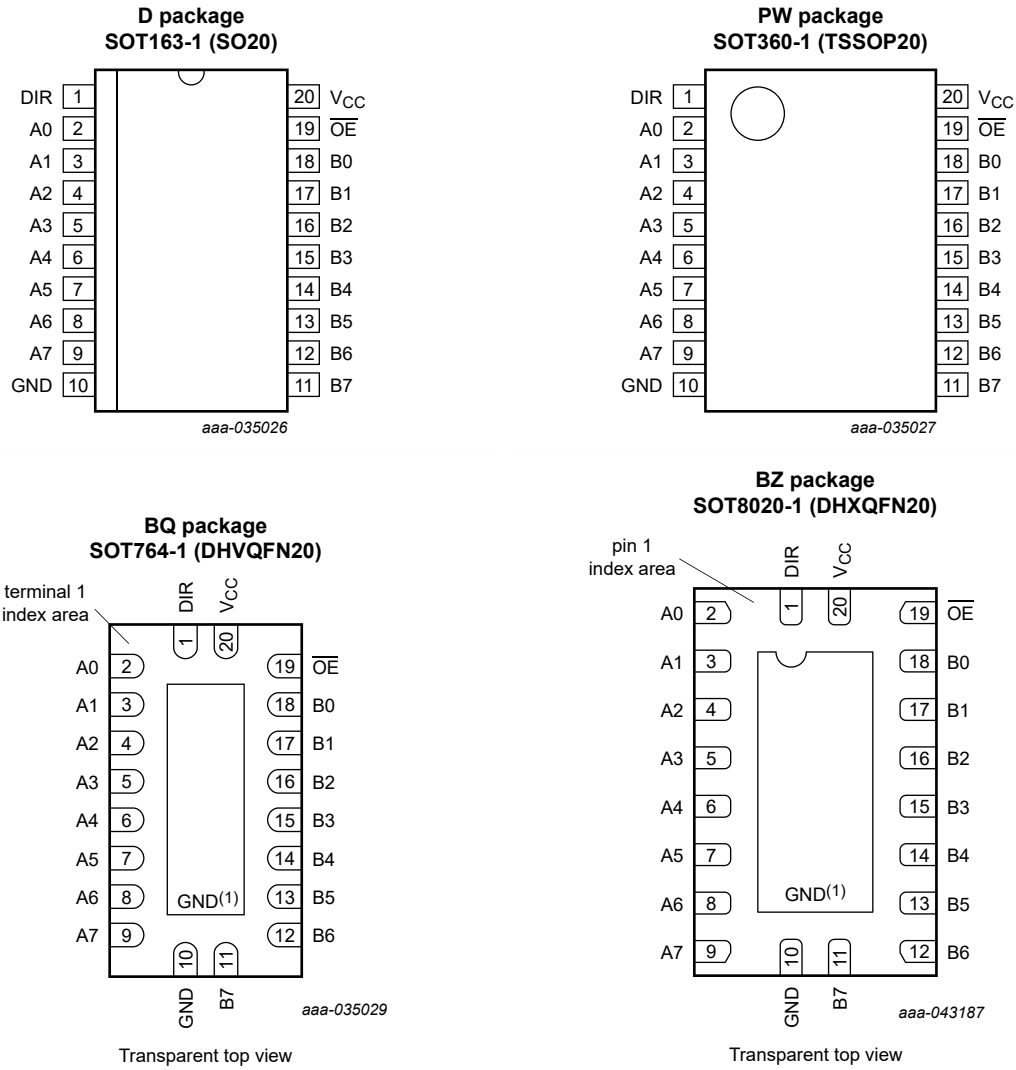
Fig. 2. IEC logic symbol

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5. Pinning information

5.1. Pinning



Transparent top view

Transparent top view

(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
DIR	1	direction control
A0, A1, A2, A3, A4, A5, A6, A7	2, 3, 4, 5, 6, 7, 8, 9	data input/output
GND	10	ground (0 V)
B7, B6, B5, B4, B3, B2, B1, B0	11, 12, 13, 14, 15, 16, 17, 18	data input/output
$\overline{OE}$	19	output enable input (active LOW)
V_{CC}	20	supply voltage

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6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Input/output	
$\overline{OE}$	DIR	An	Bn
L	L	A = B	input
L	H	input	B = A
H	X	Z	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	±35	mA
I_{CC}	supply current		-	70	mA
I_{GND}	ground current		-70	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C			
		SOT163-1 (SO20) [1] SOT360-1 (TSSOP20) [2] SOT764-1 (DHVQFN20) [3]	-	500	mW
		SOT8020-1 (DHXQFN20)	-	250	mW

[1] For SOT163-1 (SO20) package: P_{tot} derates linearly with 12.3 mW/K above 109 °C.
[2] For SOT360-1 (TSSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.
[3] For SOT764-1 (DHVQFN20) package: P_{tot} derates linearly with 12.9 mW/K above 111 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC245			74HCT245			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C

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9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC245										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = -20 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -20 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -20 µA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = -6.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = -7.8 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 µA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 6.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 7.8 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_{CC} = 6.0 V; V_O = V_{CC} or GND	-	-	±0.5	-	±5.0	-	±10	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
$C_{I/O}$	input/output capacitance		-	10	-	-	-	-	-	pF

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Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT245										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -6 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 6.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_{CC} = 5.5 V; V_O = V_{CC} or GND	-	-	±0.5	-	±5.0	-	±10	µA
I_{CC}	supply current	V_I = V_{CC} or GND; V_{CC} = 5.5 V; I_O = 0 A	-	-	8.0	-	80	-	160	µA
ΔI_{CC}	additional supply current	V_I = V_{CC} - 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A								
		An or Bn inputs	-	40	144	-	180	-	196	µA
		$\overline{OE}$ input	-	150	540	-	675	-	735	µA
		DIR input	-	90	324	-	405	-	441	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
$C_{I/O}$	input/output capacitance		-	10	-	-	-	-	-	pF

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10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; for test circuit see Fig. 5.

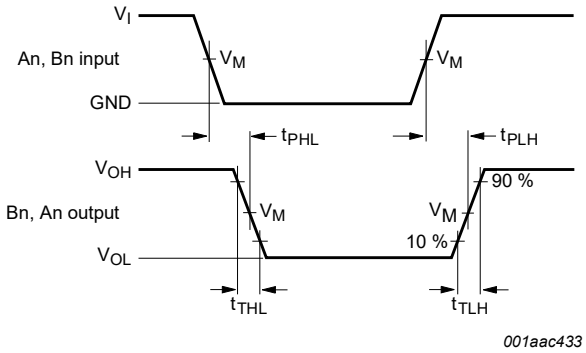
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC245										
t_{pd}	propagation delay	An to Bn or Bn to An; see Fig. 3 [1]								
		V_{CC} = 2.0 V	-	25	90	-	115	-	135	ns
		V_{CC} = 4.5 V	-	9	18	-	23	-	27	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	7	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	7	15	-	20	-	23	ns
t_{en}	enable time	$\overline{OE}$ to An or Bn; see Fig. 4 [2]								
		V_{CC} = 2.0 V	-	30	150	-	190	-	225	ns
		V_{CC} = 4.5 V	-	11	30	-	38	-	45	ns
		V_{CC} = 6.0 V	-	9	26	-	33	-	38	ns
t_{dis}	disable time	$\overline{OE}$ to An or Bn; see Fig. 4 [3]								
		V_{CC} = 2.0 V	-	41	150	-	190	-	225	ns
		V_{CC} = 4.5 V	-	15	30	-	38	-	45	ns
		V_{CC} = 6.0 V	-	12	26	-	33	-	38	ns
t_t	transition time	see Fig. 3 [4]								
		V_{CC} = 2.0 V	-	14	60	-	75	-	90	ns
		V_{CC} = 4.5 V	-	5	12	-	15	-	18	ns
		V_{CC} = 6.0 V	-	4	10	-	13	-	15	ns
C_{PD}	power dissipation capacitance	per transceiver; V_I = GND to V_{CC} [5]	-	30	-	-	-	-	-	pF
74HCT245										
t_{pd}	propagation delay	An to Bn or Bn to An; see Fig. 3 [1]								
		V_{CC} = 4.5 V	-	12	22	-	28	-	33	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	10	-	-	-	-	-	ns
t_{en}	enable time	$\overline{OE}$ to An or Bn; see Fig. 4 [2]	-	16	30	-	38	-	45	ns
t_{dis}	disable time	$\overline{OE}$ to An or Bn; see Fig. 4 [3]	-	16	30	-	38	-	45	ns
t_t	transition time	V_{CC} = 4.5 V; see Fig. 3 [4]	-	5	12	-	15	-	18	ns
C_{PD}	power dissipation capacitance	per transceiver; V_I = GND to V_{CC} - 1.5 V [5]	-	30	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.
[2] t_{en} is the same as t_{PZH} and t_{PZL}.
[3] t_{dis} is the same as t_{PHZ} and t_{PLZ}.
[4] t_t is the same as t_{THL} and t_{TLH}.
[5] C_{PD} is used to determine the dynamic power dissipation (P_D in µW): $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

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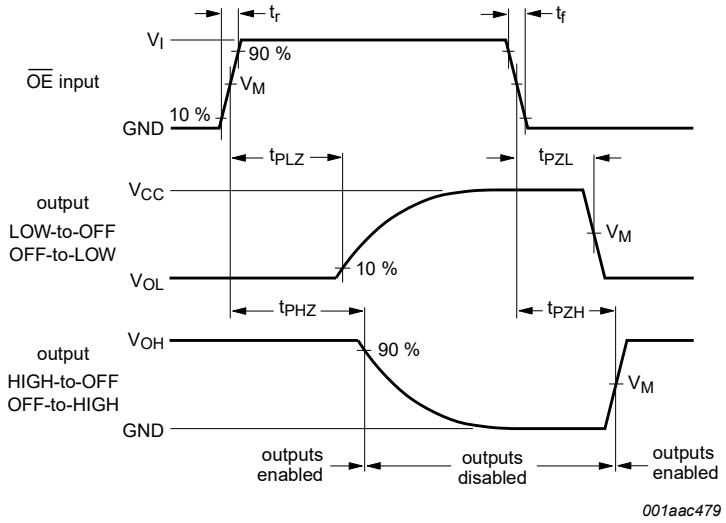
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 3. Input (An, Bn) to output (Bn, An) propagation delays and output transition times



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

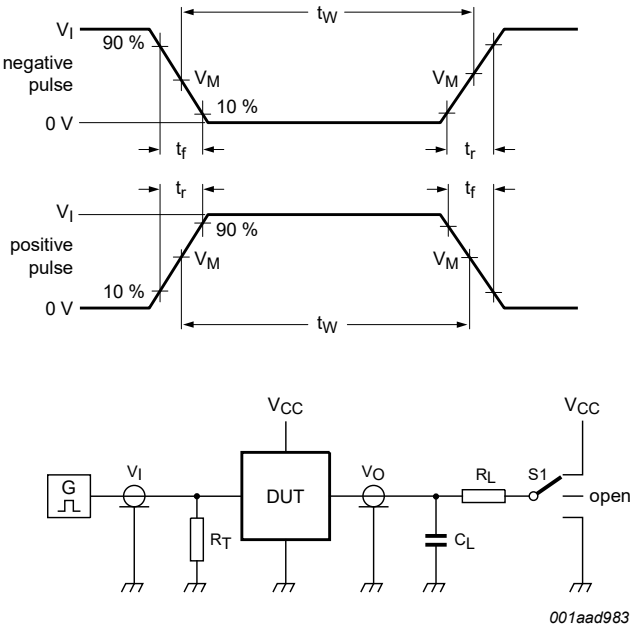
Fig. 4. 3-state output enable and disable times

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC245	0.5 × V_{CC}	0.5 × V_{CC}
74HCT245	1.3 V	1.3 V

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Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistance;

S1 = Test selection switch.

Fig. 5. Test circuit for measuring switching times

Table 9. Test data

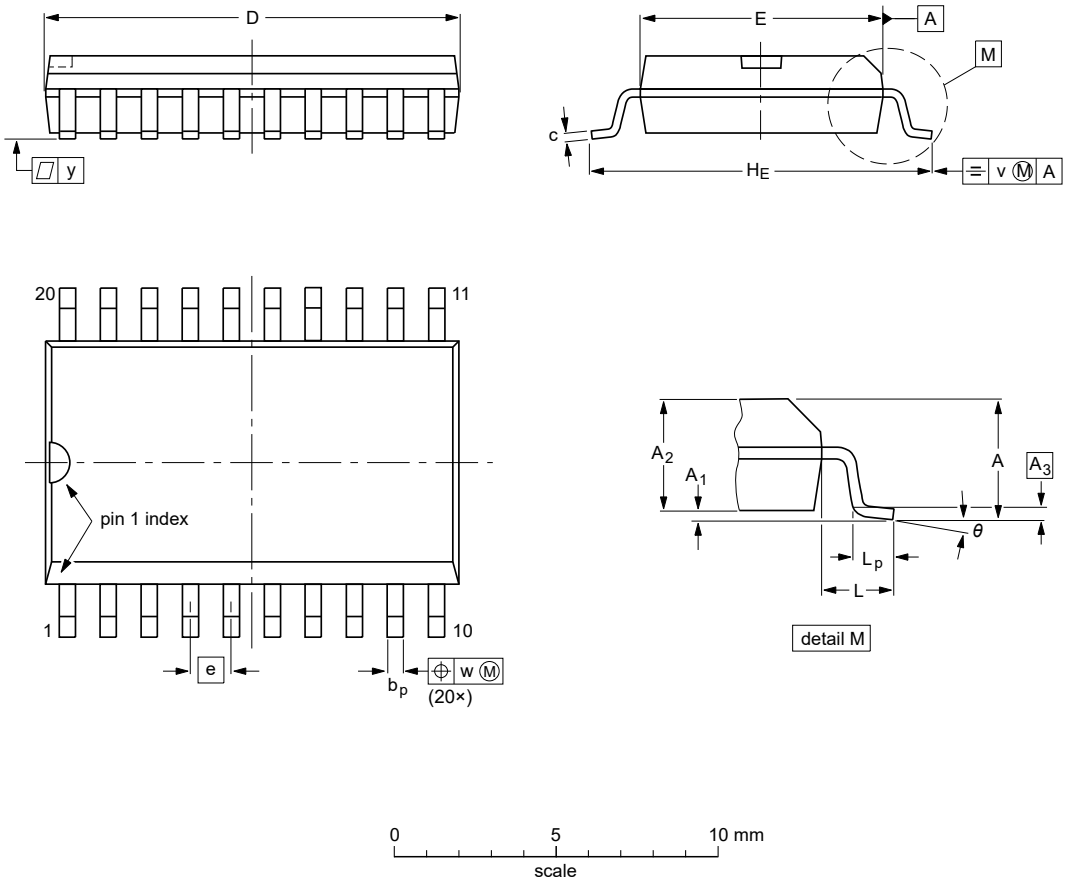
Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC245	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}
74HCT245	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

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11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	2.65	0.3		0.25	0.51	0.33	13.0	7.6	1.27	10.63	1.4	1.27	0.25	0.25	0.1	8°
	nom				BSC					BSC		REF					0°
	min		0.1	2.05		0.31	0.10	12.6	7.4		9.97		0.4				
inches	max	0.1	0.012		0.01	0.020	0.013	0.512	0.30	0.05	0.419	0.055	0.050	0.01	0.01	0.004	
	nom				BSC					BSC		REF					
	min		0.004	0.081		0.012	0.004	0.496	0.29		0.393		0.016				

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot163-1_po

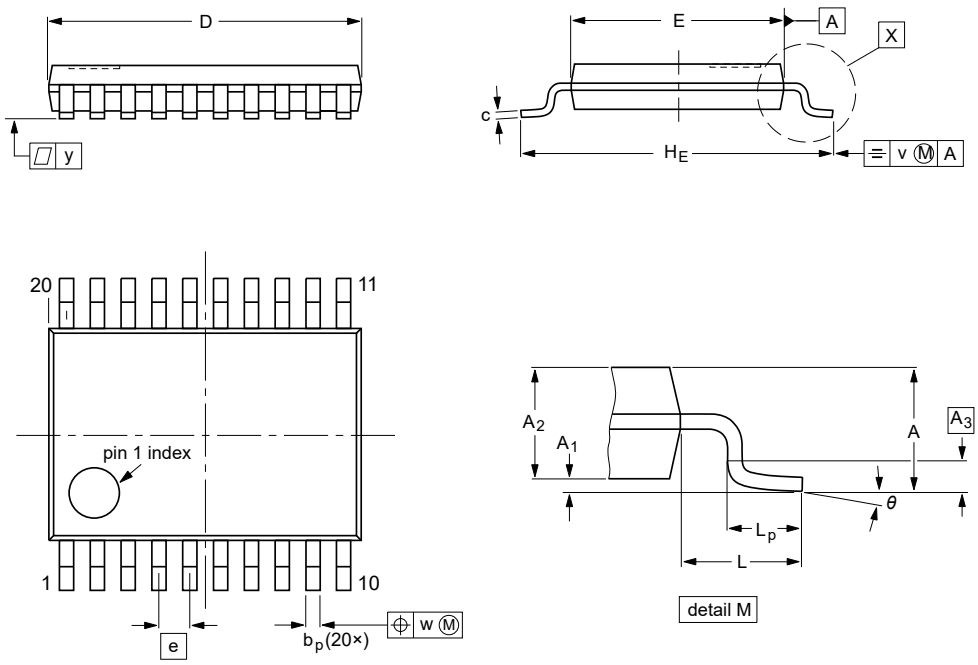
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1		MS-013				~~03-02-19~~ 24-11-07

Fig. 6. Package outline SOT163-1 (SO20)

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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05	0.25	0.30	0.20	6.60	4.50	0.65	6.60	1.00	0.75	0.2	0.1	0.1	8°
	nom				BSC					BSC		REF					
	min		0.05	0.80		0.19	0.09	6.40	4.30		6.20		0.45				0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot360-1_po

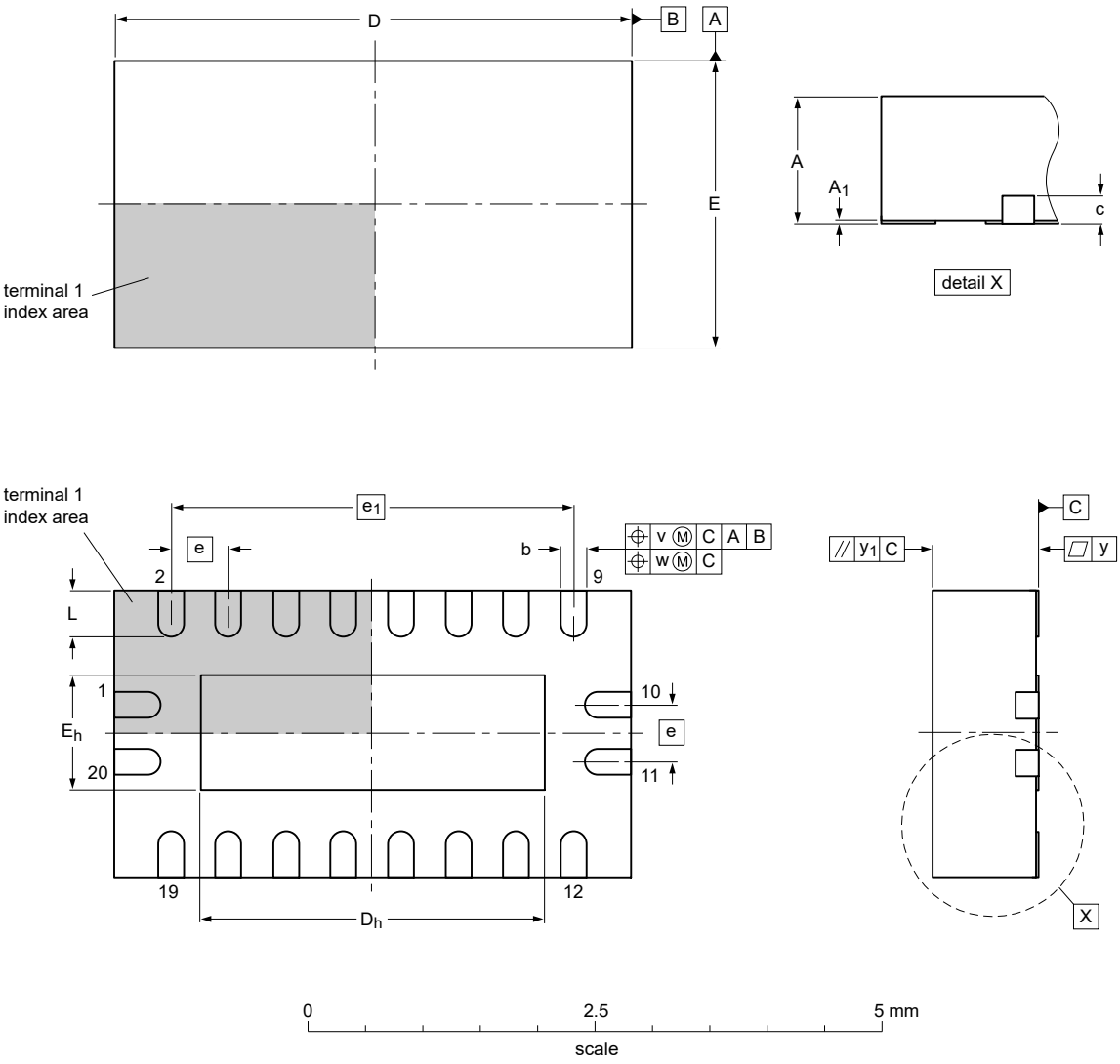
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153				~~03-02-19~~ 24-11-07

Fig. 7. Package outline SOT360-1 (TSSOP20)

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DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm **SOT764-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
	max	1.00	0.05	0.30		4.6	3.15	2.6	1.15			0.5				
mm	nom	0.90	0.02	0.25	0.2	4.5	3.00	2.5	1.00	0.5	3.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		4.4	2.85	2.4	0.85			0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot764-1_po

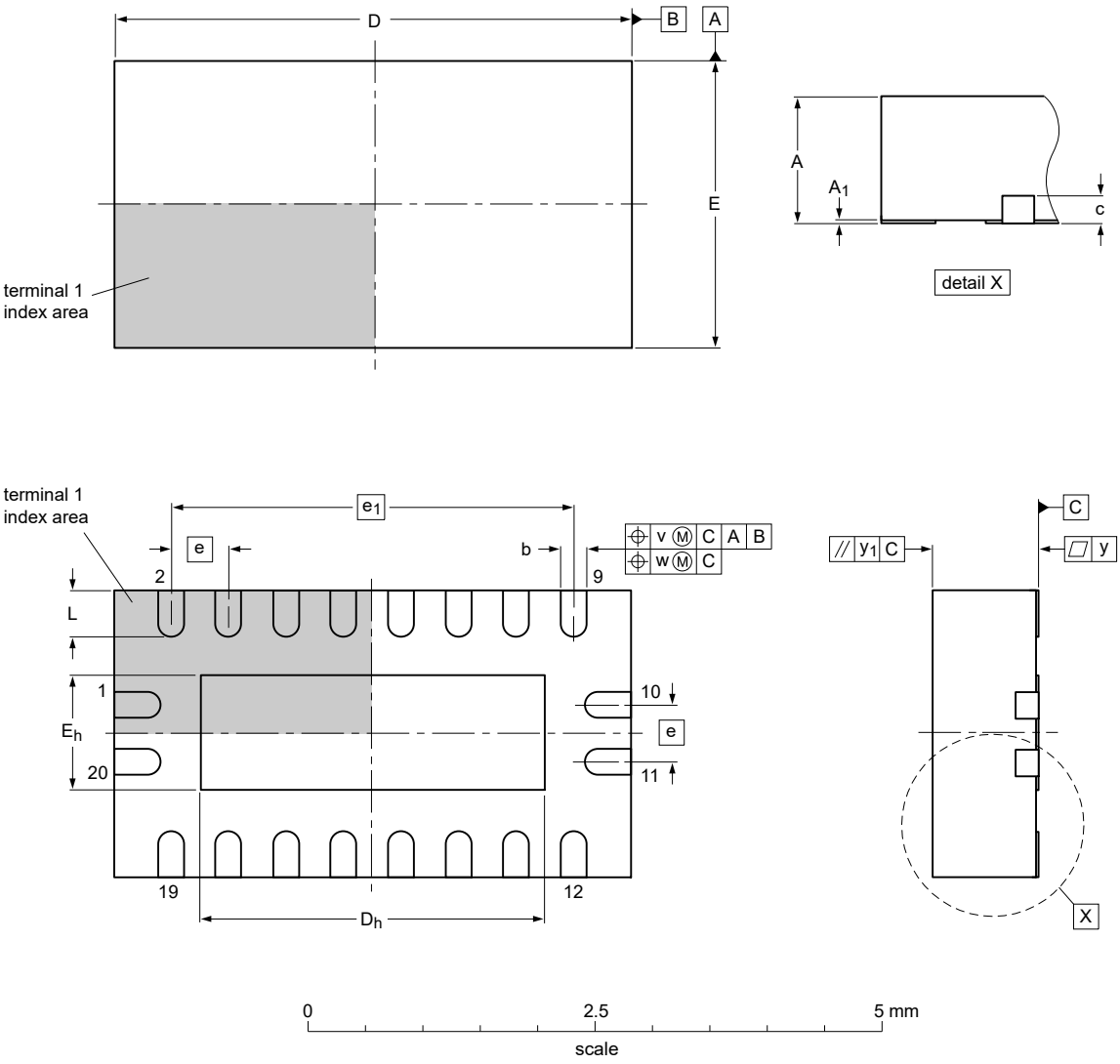
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT764-1	- - -	MO-241	- - -			~~03-01-27~~ 14-12-12

Fig. 8. Package outline SOT764-1 (DHVQFN20)

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DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm **SOT764-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
	max	1.00	0.05	0.30		4.6	3.15	2.6	1.15			0.5				
mm	nom	0.90	0.02	0.25	0.2	4.5	3.00	2.5	1.00	0.5	3.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		4.4	2.85	2.4	0.85			0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot764-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT764-1	- - -	MO-241	- - -			~~03-01-27~~ 14-12-12

Fig. 9. Package outline SOT764-1 (DHVQFN20)

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12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT245 v.9	20250509	Product data sheet	-	74HC_HCT245 v.8
Modifications:	• Type numbers 74HC245BZ and 74HCT245BZ (SOT8020-1/DHXQFN20) added.			
74HC_HCT245 v.8	20241129	Product data sheet	-	74HC_HCT245 v.7
Modifications:	• Fig. 6 and Fig. 7: Aligned SO and TSSOP package outline drawings to JEDEC MS-013 and MO-153.			
74HC_HCT245 v.7	20240805	Product data sheet	-	74HC_HCT245 v.6
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74HC_HCT245 v.6	20210906	Product data sheet	-	74HC_HCT245 v.5
Modifications:	• Types 74HC245DB and 74HCT245DB (SOT339-1) were removed. • Section 2 updated.			
74HC_HCT245 v.5	20200714	Product data sheet	-	74HC_HCT245 v.4
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Table 4: Derating values for P_{tot} total power dissipation have been updated.			
74HC_HCT245 v.4	20160226	Product data sheet	-	74HC_HCT245 v.3
Modifications:	• Type numbers 74HC245N and 74HCT245N (SOT146-1) removed.			
74HC_HCT245 v.3	20050131	Product data sheet	-	74HC_HCT245_CNV v.2
Modifications:	• The format of this data sheet is redesigned to comply with the new presentation and information standard of Philips Semiconductors • Section 3 "Ordering information", Section 5 "Pinning information" and Section 11 "Package outline" are modified to include the DHVQFN20 package.			
74HC_HCT245_CNV v.2	19930930	Product specification	-	-

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14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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