74LCX00

Low-voltage CMOS quad dual input NAND gate with 5 V tolerant inputs

Datasheet – production data

Features

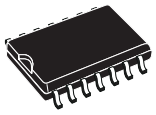
- 5 V tolerant inputs
- High speed
  - t_{PD} = 4.3 ns (max.) at V_{CC} = 3 V
- Power-down protection on inputs and outputs
- Symmetrical output impedance
  - $|I_{OH}| = I_{OL}$ = 24 mA (min.) at V_{CC} = 3 V
- PCI bus levels guaranteed at 24 mA
- Balanced propagation delay
  - $t_{PLH} \cong t_{PHL}$
- Operating voltage range
  - V_{CC} (opr.) = 2.0 V to 3.6 V
- Pin and function compatible with 74 series 00
- Latch-up performance exceeds 500 mA (JESD 17)
- ESD performance
  - HBM: 2000 V (MIL STD 883 method 3015)
  - MM: 200 V
  - CDM: 1000 V

Applications

- Automotive
- Industrial
- Computer
- Consumer



TSSOP14



SO-14

Description

The 74LCX00 device is a low-voltage CMOS quad dual input NAND gate manufactured with sub-micron silicon gate and double layer metal wiring C^2MOS technology. It is ideal for low-power and high-speed 3.3 V applications and can be interfaced to a 5 V signal environment for inputs.

It has the same speed performance at 3.3 V as the 5 V AC/ACT family, combined with lower power consumption.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2 kV ESD immunity and transient excess voltage.

Table 1. Device summary

Order code	Temperature range	Package	Packaging	Marking
74LCX00TTR	-40/+85 °C	TSSOP14	Tape and reel	LCX00
74LCX00YTTR(1)	-40/+85 °C	TSSOP14 (automotive grade)	Tape and reel	LCX00Y
74LCX00MTR	-40/+85 °C	SO-14	Tape and reel	74LCX00
74LCX00YMTR(1)	-40/+85 °C	SO-14 (automotive grade)	Tape and reel	74LCX00Y

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.

This is information on a product in full production. www.st.com

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1 Logic symbols and I/O equivalent circuit

Figure 1. IEC logic symbols

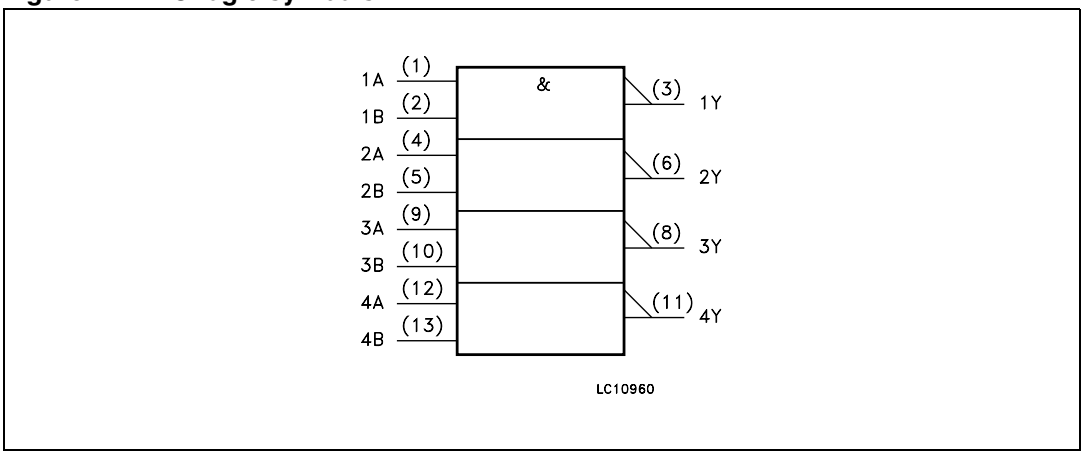
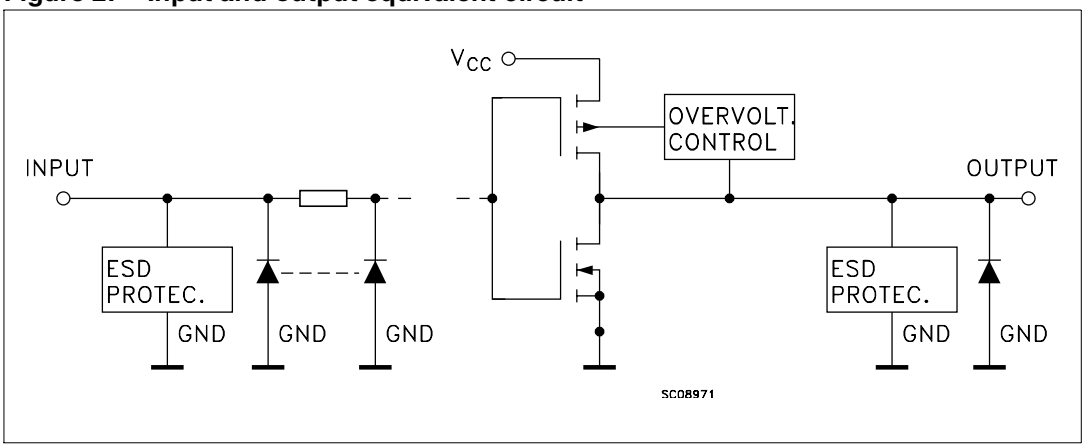


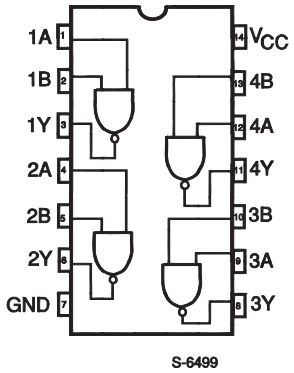
Figure 2. Input and output equivalent circuit



2 Pin settings

2.1 Pin connections

Figure 3. Pin connections (top through view)



2.2 Pin description

Table 2. Pin description

Pin number	Symbol	Name and function
1, 4, 9, 12	1A to 4A	Data inputs
2, 5, 10, 13	1B to 4B	Data inputs
3, 6, 8, 11	1Y to 4Y	Data outputs
7	GND	Ground (0 V)
14	V_{CC}	Positive supply voltage

2.3 Truth table

Table 3. Truth table

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

3 Maximum ratings

Stressing the device above the rating listed in *Table 4: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in *Table 5: Recommended operating conditions* of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_I	DC input voltage	-0.5 to +7.0	V
V_O	DC output voltage (V_{CC} = 0 V)	-0.5 to +7.0	V
V_O	DC output voltage (high or low state)(1)	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC input diode current	-50	mA
I_{OK}	DC output diode current(2)	-50	mA
I_O	DC output current	±50	mA
I_{CC}	DC supply current per supply pin	±100	mA
I_{GND}	DC ground current per supply pin	±100	mA
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec.)	300	°C

1. I_O absolute maximum rating must be observed.
2. V_O < GND.

Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	2.0 to 3.6	V
V_I	Input voltage	0 to 5.5	V
V_O	Output voltage (V_{CC} = 0 V)	0 to 5.5	V
V_O	Output voltage (high or low state)	0 to V_{CC}	V
I_{OH}, I_{OL}	High or low level output current (V_{CC} = 3.0 to 3.6 V)	±24	mA
I_{OH}, I_{OL}	High or low level output current (V_{CC} = 2.7 V)	±12	mA
dt/dv	Input rise and fall time(2)	0 to 10	ns/V

1. Truth table guaranteed: 1.5 V to 3.6 V.
2. V_{IN} from 0.8 V to 2 V at V_{CC} = 3.0 V.

4 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	Test condition		Value		Unit
		V_{CC} (V)		-40 to 85 °C		
				Min.	Max.	
V_{IH}	High level input voltage	2.7 to 3.6		2.0		V
V_{IL}	Low level input voltage				0.8	V
V_{OH}	High level output voltage	2.7 to 3.6	I_O = -100 µA	V_{CC} - 0.2		V
		2.7	I_O = -12 mA	2.2		
		3.0	I_O = -18 mA	2.4		
			I_O = -24 mA	2.2		
V_{OL}	Low level output voltage	2.7 to 3.6	I_O = 100 µA		0.2	V
		2.7	I_O = 12 mA		0.4	
		3.0	I_O = 16 mA		0.4	
			I_O = 24 mA		0.55	
I_I	Input leakage current	2.7 to 3.6	V_I = 0 to 5.5 V		±5	µA
I_{off}	Power OFF leakage current	0	V_I or V_O = 5.5 V		10	µA
I_{CC}	Quiescent supply current	2.7 to 3.6	V_I = V_{CC} or GND		10	µA
			V_I or V_O = 3.6 to 5.5 V		±10	
ΔI_{CC}	I_{CC} incr. per input	2.7 to 3.6	V_{IH} = V_{CC} - 0.6 V		500	µA

Table 7. Dynamic switching characteristics

Symbol	Parameter	Test condition		Value			Unit
		V_{CC} (V)		T_A = 25 °C			
				Min.	Typ.	Max.	
V_{OLP}	Dynamic low level quiet output (1)	3.3	C_L = 50 pF V_{IL} = 0 V, V_{IH} = 3.3 V		0.8		V
V_{OLV}					-0.8		

1. Number of outputs defined as “n”. Measured with “n-1” outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.

Table 8. AC electrical characteristics

Symbol	Parameter	Test condition				Value		Unit
		V_{CC} (V)	C_L (pF)	R_L (Ω)	$t_s = t_r$ (ns)	-40 to 85 °C		
						Min.	Max.	
t_{PLH} t_{PHL}	Propagation delay time	2.7	50	500	2.5		5.1	ns
		3.0 to 3.6				1.0	4.3	
t_{OSLH} t_{OSHL}	Output-to-output skew time(1), (2)	3.0 to 3.6	50	500	2.5		1.0	ns

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$).
2. Parameter guaranteed by design.

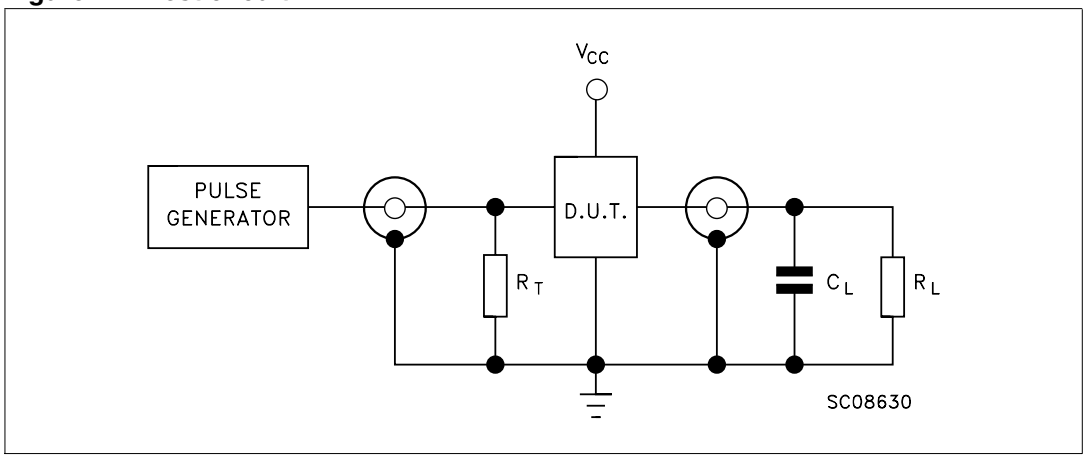
Table 9. Capacitive characteristics

Symbol	Parameter	Test condition		Value			Unit
		V_{CC} (V)		T_A = 25 °C			
				Min.	Typ.	Max.	
C_{IN}	Input capacitance	3.3	V_{IN} = 0 to V_{CC}		6		pF
C_{PD}	Power dissipation capacitance(1)	3.3	f_{IN} = 10 MHz V_{IN} = 0 or V_{CC}		35		pF

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to *Section 5: Test circuit*). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/4$ (per gate).

5 Test circuit

Figure 4. Test circuit



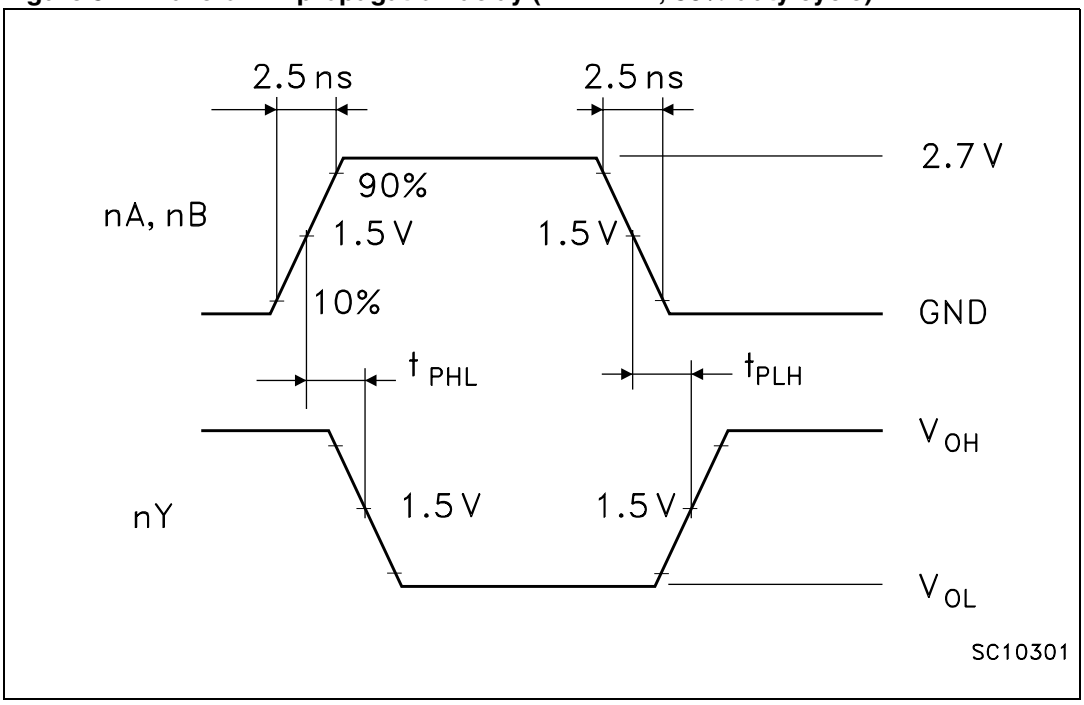
Note: C_L = 50 pF or equivalent (includes jig and probe capacitance)

R_L = 500 Ω or equivalent

$R_T = Z_{OUT}$ of pulse generator (typically 50 Ω).

6 Waveforms

Figure 5. Waveform - propagation delay (f = 1 MHz; 50% duty cycle)



7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 6. SO-14 package outline

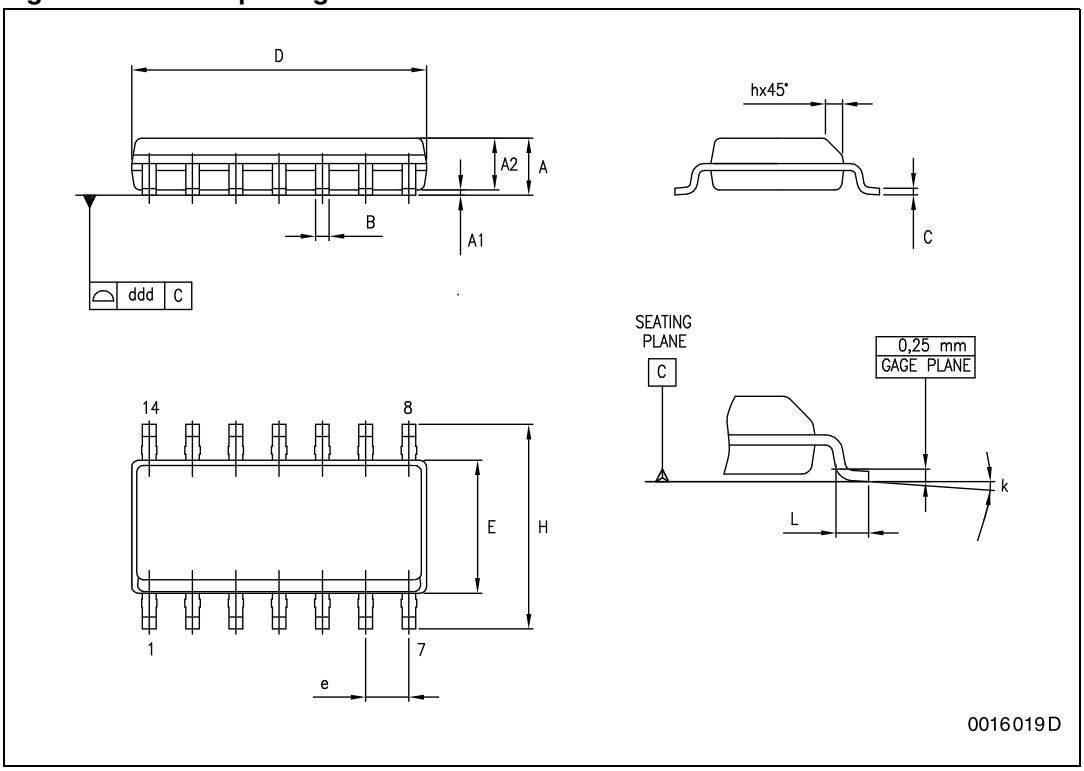


Table 10. SO-14 package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.053		0.069
A1	0.1		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	8.55		8.75	0.337		0.344
E	3.8		4.0	0.150		0.157
e		1.27			0.050	
H	5.8		6.2	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.4		1.27	0.016		0.050
k	0°		8°	0°		8°
ddd			0.100			0.004

Figure 7. TSSOP14 package outline

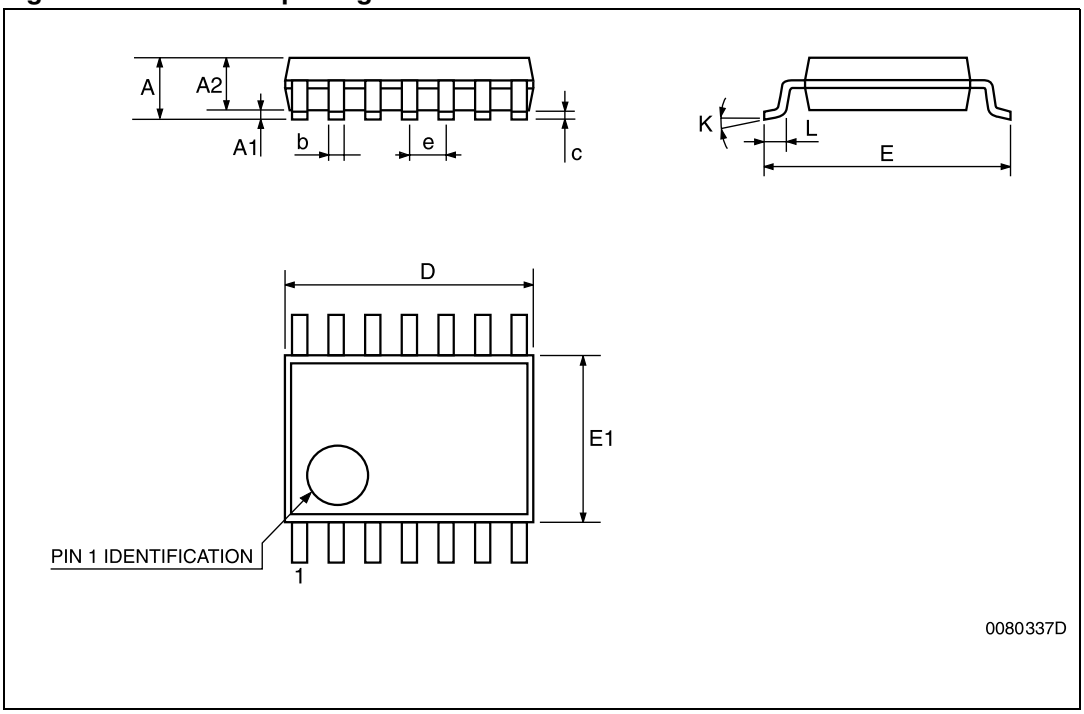
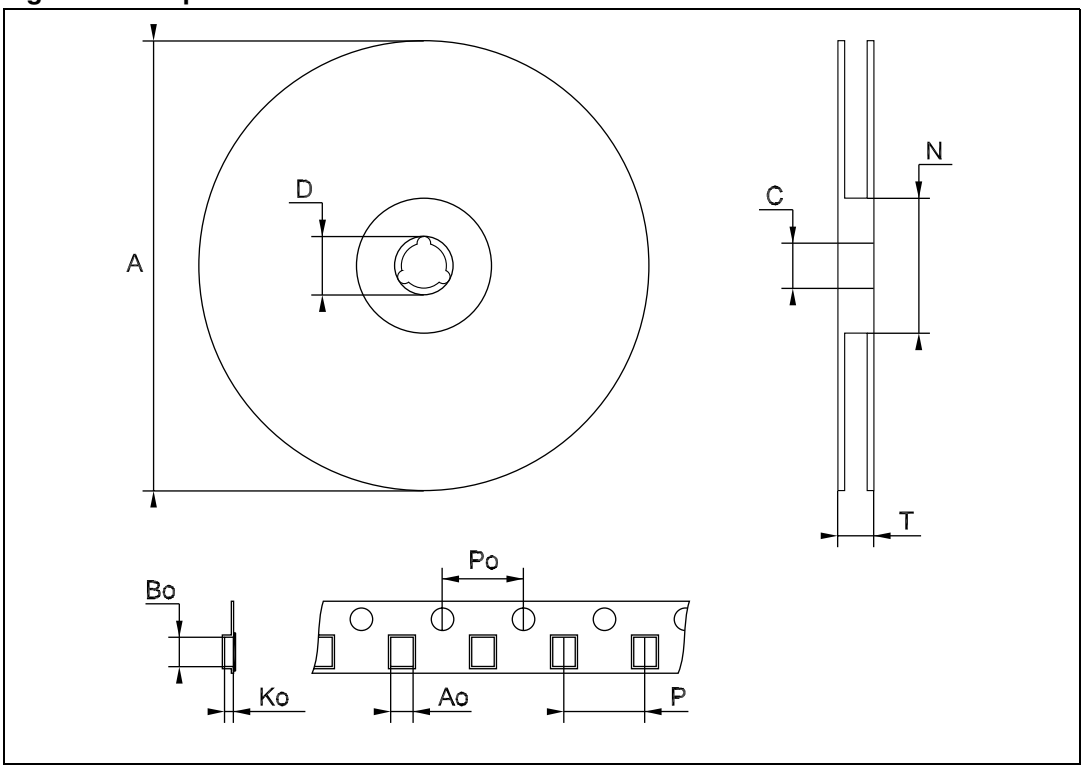


Table 11. TSSOP14 package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

Figure 8. Tape and reel SO-14 outline

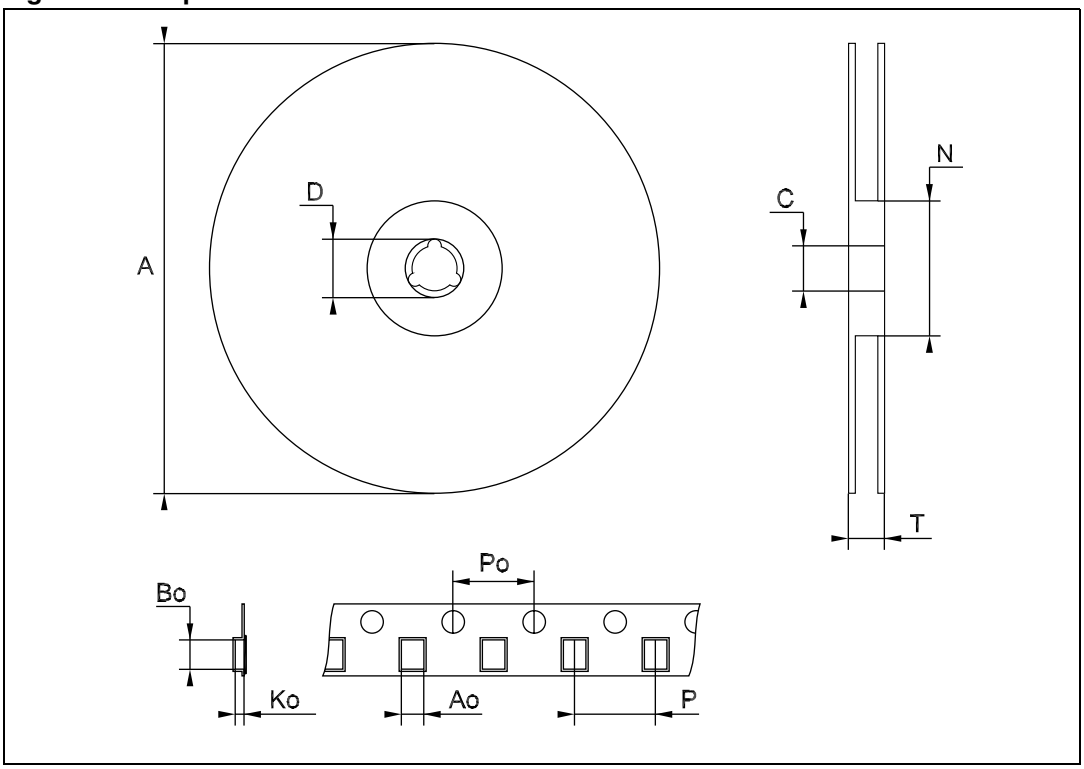


1. Drawing is not in scale.

Table 12. Tape and reel SO-14 mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.4		6.6	0.252		0.260
Bo	9		9.2	0.354		0.362
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319

Figure 9. Tape and reel TSSOP14 outline



Drawing is not in scale.

Table 13. Tape and reel TSSOP14 mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.7		6.9	0.264		0.272
Bo	5.3		5.5	0.209		0.217
Ko	1.6		1.8	0.063		0.071
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319

8 Revision history

Table 14. Document revision history

Date	Revision	Changes
15-Sep-2004	4	Ordering code revision - pag 1
07-Jul-2006	5	New template, temperature ranges updated
20-Jun-2012	6	Added *Applications on page 1* Updated *Table 1: Device summary on page 1* Updated T_{op} in *Table 5: Recommended operating conditions* Updated ECOPACK® text in *Section 7: Package mechanical data* Minor textual updates
02-Oct-2012	7	Updated ESD performance in *Features* (updated HBM and MM, added CDM). Added 74LCX00YMTR device and “Marking” to *Table 1*, updated temperature range, note *1*. Updated *Section 3: Maximum ratings* (added cross-references). Removed “Operating temperature” from *Table 5*. Reformatted *Section 7: Package mechanical data*. Minor corrections throughout document.

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