# 74LVC2G53

## 2-channel analog multiplexer/demultiplexer

Rev. 15 — 28 August 2023 Product data sheet

## 1. General description

The 74LVC2G53 is a single-pole double-throw analog switch with a digital select input (S), two independent inputs/outputs (Y0 and Y1), a common input/output (Z) and a digital enable input ($\overline{E}$). When $\overline{E}$ is HIGH, the switch is turned off. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt trigger action at the select and enable inputs makes the circuit tolerant of slower input rise and fall times across the entire $V_{CC}$ range from 1.65 V to 5.5 V.

## 2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- Very low ON resistance:
  - 7.5 Ω (typical) at $V_{CC}$ = 2.7 V
  - 6.5 Ω (typical) at $V_{CC}$ = 3.3 V
  - 6 Ω (typical) at $V_{CC}$ = 5 V
- Switch current capability of 32 mA
- High noise immunity
- CMOS low-power consumption
- Overvoltage tolerant inputs to 5.5 V
- TTL interface compatibility at 3.3 V
- Latch-up performance meets requirements of JESD 78 Class I
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74LVC2G53DP | -40 °C to +125 °C | TSSOP8 | plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm | SOT505-2 |
| 74LVC2G53DC | -40 °C to +125 °C | VSSOP8 | plastic very thin shrink small outline package; 8 leads; body width 2.3 mm | SOT765-1 |
| 74LVC2G53GT | -40 °C to +125 °C | XSON8 | plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm | SOT833-1 |
| 74LVC2G53GN | -40 °C to +125 °C | XSON8 | extremely thin small outline package; no leads; 8 terminals; body 1.2 × 1.0 × 0.35 mm | SOT1116 |
| 74LVC2G53GS | -40 °C to +125 °C | XSON8 | extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1.0 × 0.35 mm | SOT1203 |

## 4. Marking

**Table 2. Marking codes**

| Type number | Marking code[1] |
|---|---|
| 74LVC2G53DP | V53 |
| 74LVC2G53DC | V53 |
| 74LVC2G53GT | V53 |
| 74LVC2G53GN | V3 |
| 74LVC2G53GS | V3 |

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

## 5. Functional diagram

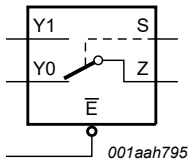



**Fig. 1. Logic symbol**

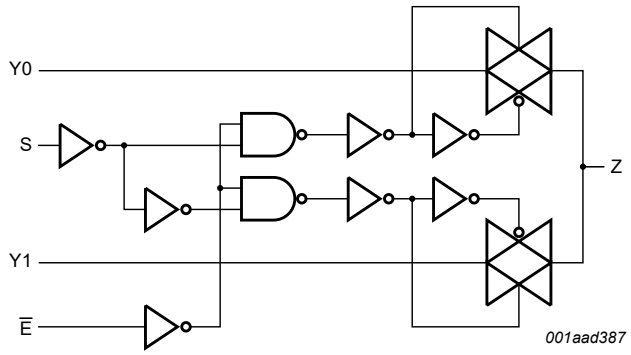


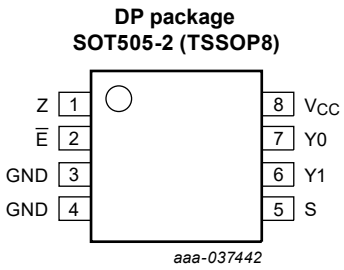

**Fig. 2. Logic diagram**

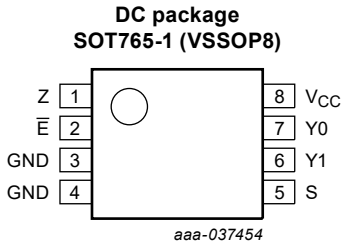

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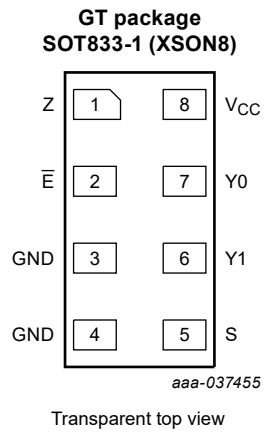
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# 6. Pinning information

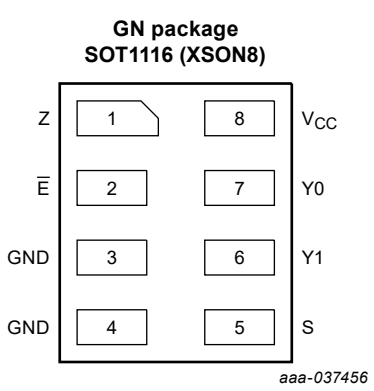
## 6.1. Pinning



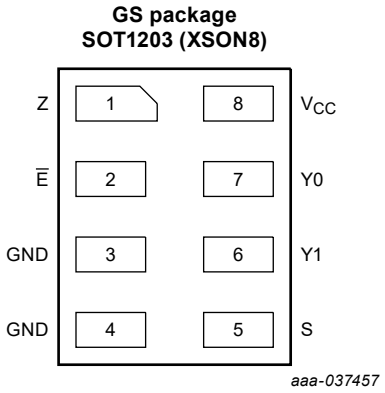




Transparent top view




Transparent top view




Transparent top view

## 6.2. Pin description

**Table 3. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| Z | 1 | common output or input |
| $\overline{E}$ | 2 | enable input (active LOW) |
| GND | 3 | ground (0 V) |
| GND | 4 | ground (0 V) |
| S | 5 | select input |
| Y1 | 6 | independent input or output |
| Y0 | 7 | independent input or output |
| $V_{CC}$ | 8 | supply voltage |


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# 7. Functional description

**Table 4. Function table**

*H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.*

| Input | | Channel on |
|---|---|---|
| **S** | $\overline{\mathbf{E}}$ | |
| L | L | Y0 to Z or Z to Y0 |
| H | L | Y1 to Z or Z to Y1 |
| X | H | Z |

# 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | -0.5 | +6.5 | V |
| $V_I$ | input voltage | | [1] | -0.5 | +6.5 | V |
| $I_{IK}$ | input clamping current | $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V | | -50 | - | mA |
| $I_{SK}$ | switch clamping current | $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V | | - | ±50 | mA |
| $V_{SW}$ | switch voltage | enable and disable mode | [2] | -0.5 | $V_{CC} + 0.5$ | V |
| $I_{SW}$ | switch current | $V_{SW} > -0.5$ V or $V_{SW} < V_{CC} + 0.5$ V | | - | ±50 | mA |
| $I_{CC}$ | supply current | | | - | 100 | mA |
| $I_{GND}$ | ground current | | | -100 | - | mA |
| $T_{stg}$ | storage temperature | | | -65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = -40 °C to +125 °C | [3] | - | 250 | mW |

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.
[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.
[3] For SOT505-2 (TSSOP8) package: $P_{tot}$ derates linearly with 4.6 mW/K above 96 °C.
For SOT765-1 (VSSOP8) package: $P_{tot}$ derates linearly with 4.9 mW/K above 99 °C.
For SOT833-1 (XSON8) package: $P_{tot}$ derates linearly with 3.1 mW/K above 68 °C.
For SOT1116 (XSON8) package: $P_{tot}$ derates linearly with 4.2 mW/K above 90 °C.
For SOT1203 (XSON8) package: $P_{tot}$ derates linearly with 3.6 mW/K above 81 °C.

# 9. Recommended operating conditions

**Table 6. Operating conditions**

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | 1.65 | 5.5 | V |
| $V_I$ | input voltage | | | 0 | 5.5 | V |
| $V_{SW}$ | switch voltage | enable and disable mode | [1] | 0 | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | | | -40 | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | $V_{CC}$ = 1.65 V to 2.7 V | [2] | - | 20 | ns/V |
| | | $V_{CC}$ = 2.7 V to 5.5 V | [2] | - | 10 | ns/V |

[1] To avoid sinking GND current from terminal Z when switch current flows in terminal Yn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no GND current will flow from terminal Yn. In this case, there is no limit for the voltage drop across the switch.
[2] Applies to control signal levels.


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# 10. Static characteristics

**Table 7. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground 0 V).*

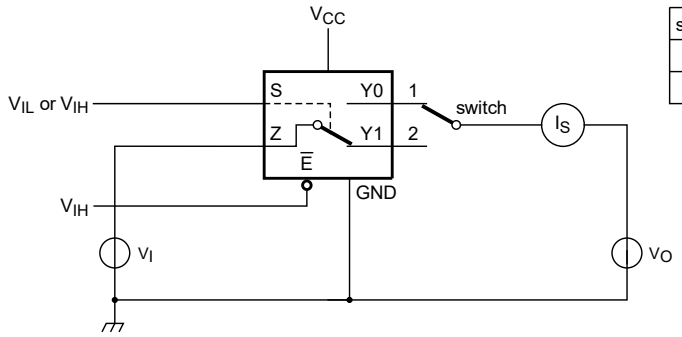
| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ [1] | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | $0.65V_{CC}$ | - | - | $0.65V_{CC}$ | - | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | - | - | 1.7 | - | V |
| | | $V_{CC}$ = 3 V to 3.6 V | 2.0 | - | - | 2.0 | - | V |
| | | $V_{CC}$ = 4.5 V to 5.5 V | $0.7V_{CC}$ | - | - | $0.7V_{CC}$ | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | - | - | $0.35V_{CC}$ | - | $0.35V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | - | - | 0.7 | - | 0.7 | V |
| | | $V_{CC}$ = 3 V to 3.6 V | - | - | 0.8 | - | 0.8 | V |
| | | $V_{CC}$ = 4.5 V to 5.5 V | - | - | $0.3V_{CC}$ | | $0.3V_{CC}$ | V |
| $I_I$ | input leakage current | pin S and pin $\overline{E}$; $V_I$ = 5.5 V or GND; $V_{CC}$ = 0 V to 5.5 V [2] | - | ±0.1 | ±1 | - | ±1 | µA |
| $I_{S(OFF)}$ | OFF-state leakage current | $V_{CC}$ = 5.5 V; see Fig. 3 [2] | - | ±0.1 | ±0.2 | - | ±0.5 | µA |
| $I_{S(ON)}$ | ON-state leakage current | $V_{CC}$ = 5.5 V; see Fig. 4 [2] | - | ±0.1 | ±1 | - | ±2 | µA |
| $I_{CC}$ | supply current | $V_I$ = 5.5 V or GND; $V_{SW}$ = GND or $V_{CC}$; $V_{CC}$ = 1.65 V to 5.5 V [2] | - | 0.1 | 4 | - | 4 | µA |
| $\Delta I_{CC}$ | additional supply current | pin S and pin $\overline{E}$; $V_I$ = $V_{CC}$ - 0.6 V; $V_{SW}$ = GND or $V_{CC}$; $V_{CC}$ = 5.5 V [2] | - | 5 | 500 | - | 500 | µA |
| $C_I$ | input capacitance | | - | 2.5 | - | - | - | pF |
| $C_{S(OFF)}$ | OFF-state capacitance | | - | 6.0 | - | - | - | pF |
| $C_{S(ON)}$ | ON-state capacitance | | - | 18 | - | - | - | pF |

[1] Typical values are measured at $T_{amb}$ = 25 °C.
[2] These typical values are measured at $V_{CC}$ = 3.3 V.


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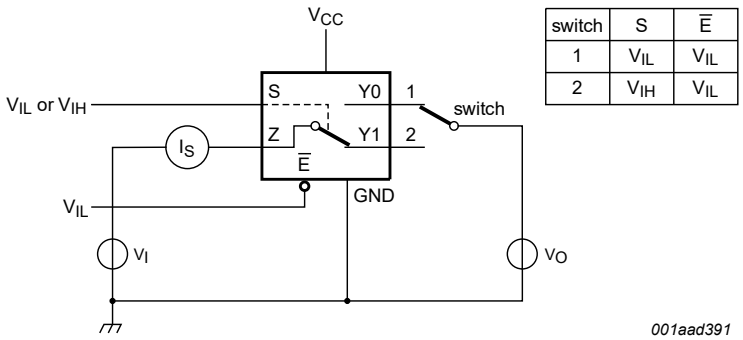
## 10.1. Test circuits




| switch | S | $\overline{E}$ |
|---|---|---|
| 1 | $V_{IL}$ | $V_{IH}$ |
| 2 | $V_{IH}$ | $V_{IH}$ |

$V_I = V_{CC}$ or GND; $V_O$ = GND or $V_{CC}$.

**Fig. 3. Test circuit for measuring OFF-state leakage current**




| switch | S | $\overline{E}$ |
|---|---|---|
| 1 | $V_{IL}$ | $V_{IL}$ |
| 2 | $V_{IH}$ | $V_{IL}$ |

$V_I = V_{CC}$ or GND and $V_O$ = open circuit.

**Fig. 4. Test circuit for measuring ON-state leakage current**

## 10.2. ON resistance

**Table 8. ON resistance**

*At recommended operating conditions; voltages are referenced to GND (ground 0 V); for graphs see Fig. 6 to Fig. 11.*

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $R_{ON(peak)}$ | ON resistance (peak) | $V_I$ = GND to $V_{CC}$; see Fig. 5 | | | | | | |
| | | $I_{SW}$ = 4 mA; $V_{CC}$ = 1.65 V to 1.95 V | - | 34.0 | 130 | - | 195 | Ω |
| | | $I_{SW}$ = 8 mA; $V_{CC}$ = 2.3 V to 2.7 V | - | 12.0 | 30 | - | 45 | Ω |
| | | $I_{SW}$ = 12 mA; $V_{CC}$ = 2.7 V | - | 10.4 | 25 | - | 38 | Ω |
| | | $I_{SW}$ = 24 mA; $V_{CC}$ = 3 V to 3.6 V | - | 7.8 | 20 | - | 30 | Ω |
| | | $I_{SW}$ = 32 mA; $V_{CC}$ = 4.5 V to 5.5 V | - | 6.2 | 15 | - | 23 | Ω |


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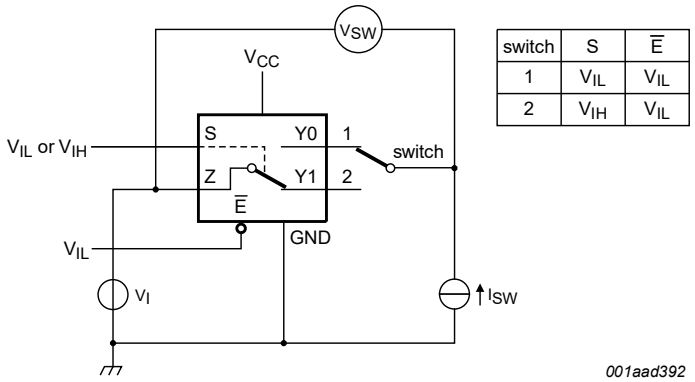
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| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $R_{ON(rail)}$ | ON resistance (rail) | $V_I$ = GND; see Fig. 5 | | | | | | |
| | | $I_{SW}$ = 4 mA; $V_{CC}$ = 1.65 V to 1.95 V | - | 8.2 | 18 | - | 27 | Ω |
| | | $I_{SW}$ = 8 mA; $V_{CC}$ = 2.3 V to 2.7 V | - | 7.1 | 16 | - | 24 | Ω |
| | | $I_{SW}$ = 12 mA; $V_{CC}$ = 2.7 V | - | 6.9 | 14 | - | 21 | Ω |
| | | $I_{SW}$ = 24 mA; $V_{CC}$ = 3 V to 3.6 V | - | 6.5 | 12 | - | 18 | Ω |
| | | $I_{SW}$ = 32 mA; $V_{CC}$ = 4.5 V to 5.5 V | - | 5.8 | 10 | - | 15 | Ω |
| | | $V_I$ = $V_{CC}$; see Fig. 5 | | | | | | |
| | | $I_{SW}$ = 4 mA; $V_{CC}$ = 1.65 V to 1.95 V | - | 10.4 | 30 | - | 45 | Ω |
| | | $I_{SW}$ = 8 mA; $V_{CC}$ = 2.3 V to 2.7 V | - | 7.6 | 20 | - | 30 | Ω |
| | | $I_{SW}$ = 12 mA; $V_{CC}$ = 2.7 V | - | 7.0 | 18 | - | 27 | Ω |
| | | $I_{SW}$ = 24 mA; $V_{CC}$ = 3 V to 3.6 V | - | 6.1 | 15 | - | 23 | Ω |
| | | $I_{SW}$ = 32 mA; $V_{CC}$ = 4.5 V to 5.5 V | - | 4.9 | 10 | - | 15 | Ω |
| $R_{ON(flat)}$ | ON resistance (flatness) | $V_I$ = GND to $V_{CC}$ [2] | | | | | | |
| | | $I_{SW}$ = 4 mA;$V_{CC}$ = 1.65 V to 1.95 V | - | 26.0 | - | - | - | Ω |
| | | $I_{SW}$ = 8 mA; $V_{CC}$ = 2.3 V to 2.7 V | - | 5.0 | - | - | - | Ω |
| | | $I_{SW}$ = 12 mA; $V_{CC}$ = 2.7 V | - | 3.5 | - | - | - | Ω |
| | | $I_{SW}$ = 24 mA; $V_{CC}$ = 3 V to 3.6 V | - | 2.0 | - | - | - | Ω |
| | | $I_{SW}$ = 32 mA; $V_{CC}$ = 4.5 V to 5.5 V | - | 1.5 | - | - | - | Ω |

[1] Typical values are measured at $T_{amb}$ = 25 °C and nominal $V_{CC}$.

[2] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical $V_{CC}$ and temperature.

## 10.3. ON resistance test circuit and graphs



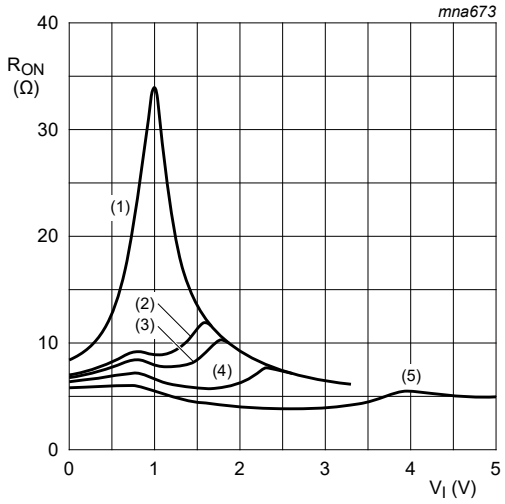

| switch | S | $\overline{E}$ |
|---|---|---|
| 1 | $V_{IL}$ | $V_{IL}$ |
| 2 | $V_{IH}$ | $V_{IL}$ |

$R_{ON} = V_{SW} / I_{SW}$.

**Fig. 5. Test circuit for measuring ON resistance**


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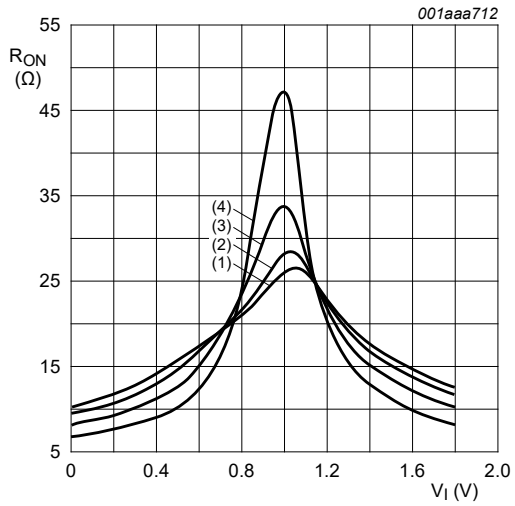
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$T_{amb}$ = 25 °C

1. $V_{CC}$ = 1.8 V
2. $V_{CC}$ = 2.5 V
3. $V_{CC}$ = 2.7 V
4. $V_{CC}$ = 3.3 V
5. $V_{CC}$ = 5.0 V

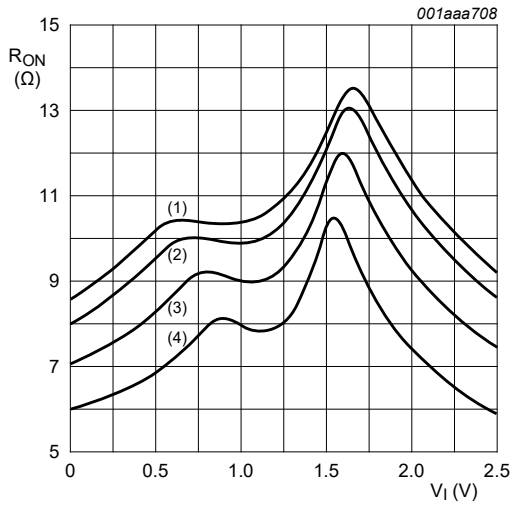
**Fig. 6. Typical ON resistance as a function of input voltage**




$V_{CC}$ = 1.8 V

1. $T_{amb}$ = 125 °C
2. $T_{amb}$ = 85 °C
3. $T_{amb}$ = 25 °C
4. $T_{amb}$ = -40 °C

**Fig. 7. ON resistance as a function of input voltage**



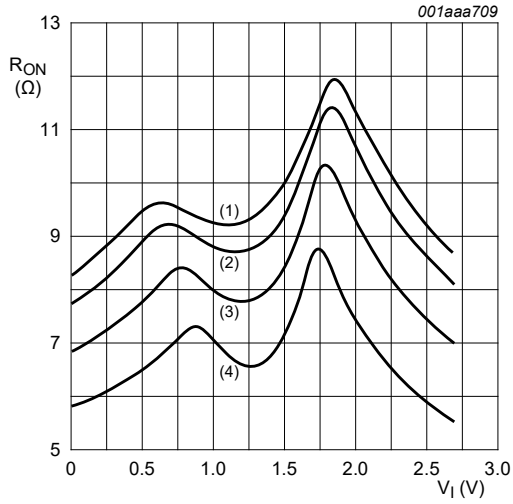

$V_{CC}$ = 2.5 V

1. $T_{amb}$ = 125 °C
2. $T_{amb}$ = 85 °C
3. $T_{amb}$ = 25 °C
4. $T_{amb}$ = -40 °C

**Fig. 8. ON resistance as a function of input voltage**


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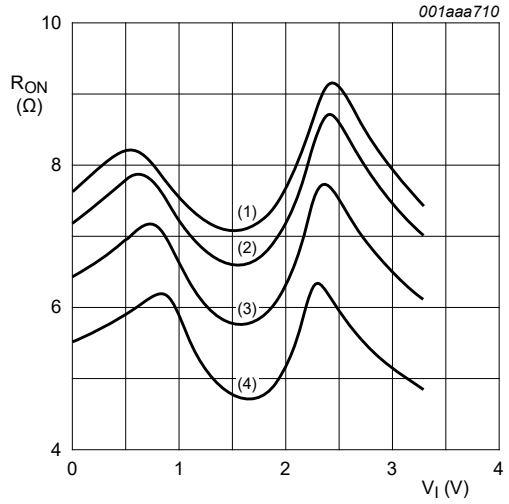
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$V_{CC}$ = 2.7 V

1. $T_{amb}$ = 125 °C
2. $T_{amb}$ = 85 °C
3. $T_{amb}$ = 25 °C
4. $T_{amb}$ = -40 °C

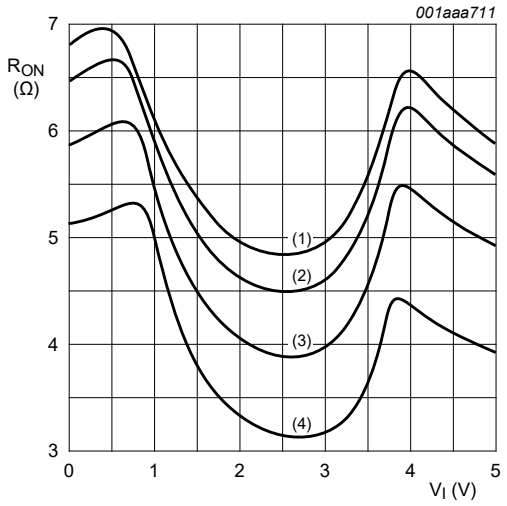
**Fig. 9. ON resistance as a function of input voltage**




$V_{CC}$ = 3.3 V

1. $T_{amb}$ = 125 °C
2. $T_{amb}$ = 85 °C
3. $T_{amb}$ = 25 °C
4. $T_{amb}$ = -40 °C

**Fig. 10. ON resistance as a function of input voltage**




$V_{CC}$ = 5.0 V

1. $T_{amb}$ = 125 °C
2. $T_{amb}$ = 85 °C
3. $T_{amb}$ = 25 °C
4. $T_{amb}$ = -40 °C

**Fig. 11. ON resistance as a function of input voltage**


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# 11. Dynamic characteristics

**Table 9. Dynamic characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 14.*

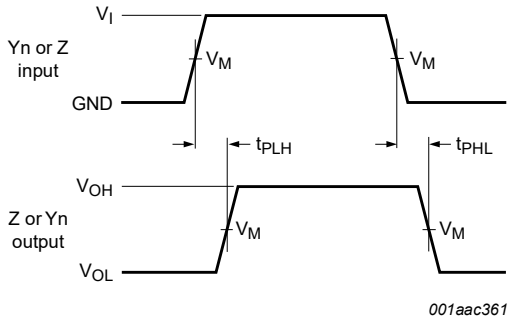
| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $t_{pd}$ | propagation delay | Z to Yn or Yn to Z; see Fig. 12 [2] [3] | | | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | - | - | 2 | - | 2.5 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | - | - | 1.2 | - | 1.5 | ns |
| | | $V_{CC}$ = 2.7 V | - | - | 1.0 | - | 1.25 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | - | - | 0.8 | - | 1.0 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | - | - | 0.6 | - | 0.8 | ns |
| $t_{en}$ | enable time | S to Z or Yn; see Fig. 13 [2] | | | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 2.6 | 6.7 | 10.3 | 2.6 | 12.9 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.9 | 4.1 | 6.4 | 1.9 | 8.0 | ns |
| | | $V_{CC}$ = 2.7 V | 1.9 | 4.0 | 5.5 | 1.8 | 7.0 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.8 | 3.4 | 5.0 | 1.8 | 6.3 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 1.3 | 2.6 | 3.8 | 1.3 | 4.8 | ns |
| | | $\overline{E}$ to Z or Yn; see Fig. 13 [2] | | | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 1.9 | 4.0 | 7.3 | 1.9 | 9.2 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.4 | 2.5 | 4.4 | 1.4 | 5.5 | ns |
| | | $V_{CC}$ = 2.7 V | 1.1 | 2.6 | 3.9 | 1.1 | 4.9 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.2 | 2.2 | 3.8 | 1.2 | 4.8 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 1.0 | 1.7 | 2.6 | 1.0 | 3.3 | ns |
| $t_{dis}$ | disable time | S to Z or Yn; see Fig. 13 [2] | | | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 2.1 | 6.8 | 10.0 | 2.1 | 12.5 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.4 | 3.7 | 6.1 | 1.4 | 7.7 | ns |
| | | $V_{CC}$ = 2.7 V | 1.4 | 4.9 | 6.2 | 1.4 | 7.8 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.1 | 4.0 | 5.4 | 1.1 | 6.8 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 1.0 | 2.9 | 3.8 | 1.0 | 4.8 | ns |
| | | $\overline{E}$ to Z or Yn; see Fig. 13 [2] | | | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 2.3 | 5.6 | 8.6 | 2.3 | 11.0 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.2 | 3.2 | 4.8 | 1.2 | 6.0 | ns |
| | | $V_{CC}$ = 2.7 V | 1.4 | 4.0 | 5.2 | 1.4 | 6.5 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 2.0 | 3.7 | 5.0 | 2.0 | 6.3 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 1.3 | 2.9 | 3.8 | 1.3 | 4.8 | ns |

[1] Typical values are measured at $T_{amb}$ = 25 °C and nominal $V_{CC}$.
[2] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$; $t_{en}$ is the same as $t_{PZH}$ and $t_{PZL}$; $t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$
[3] Propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified capacitance when driven by an ideal voltage source (zero output impedance).


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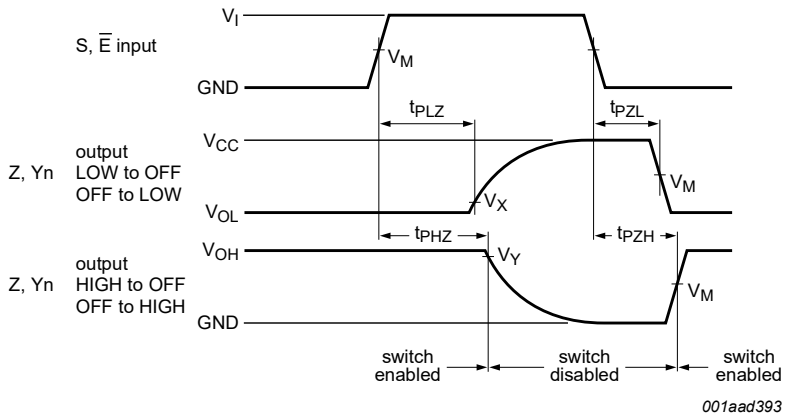
## 11.1. Waveforms and test circuits




Measurement points are given in Table 10.

Logic levels: $V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig. 12. Input (Yn or Z) to output (Z or Yn) propagation delays**




Measurement points are given in Table 10.

Logic levels: $V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

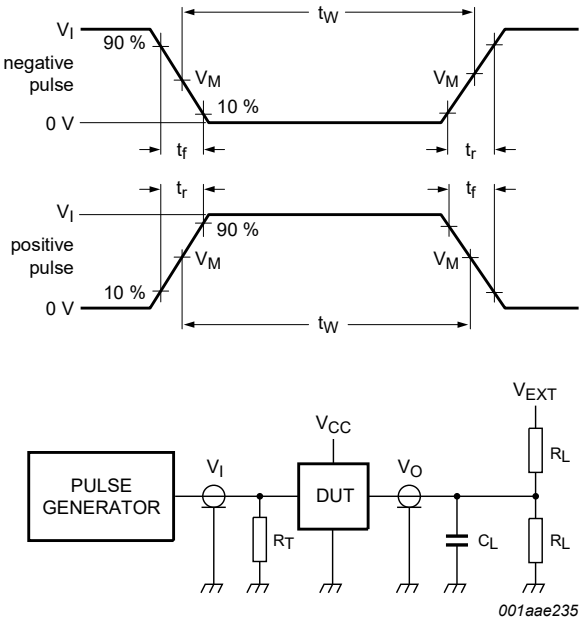
**Fig. 13. Enable and disable times**

**Table 10. Measurement points**

| Supply voltage | Input | Output | | |
|---|---|---|---|---|
| $V_{CC}$ | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 1.65 V to 2.7 V | $0.5V_{CC}$ | $0.5V_{CC}$ | $V_{OL}$ + 0.15 V | $V_{OH}$ - 0.15 V |
| 2.7 V to 5.5 V | $0.5V_{CC}$ | $0.5V_{CC}$ | $V_{OL}$ + 0.3 V | $V_{OH}$ - 0.3 V |


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Test data is given in Table 11.

Definitions for test circuit:

$R_L$ = Load resistance;

$C_L$ = Load capacitance including jig and probe capacitance;

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator;

$V_{EXT}$ = Test voltage for switching times.

**Fig. 14. Test circuit for measuring switching times**

**Table 11. Test data**

| Supply voltage | Input | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PLH}$, $t_{PHL}$ | $t_{PZH}$, $t_{PHZ}$ | $t_{PZL}$, $t_{PLZ}$ |
| 1.65 V to 1.95 V | $V_{CC}$ | ≤ 2.0 ns | 30 pF | 1 kΩ | open | GND | $2V_{CC}$ |
| 2.3 V to 2.7 V | $V_{CC}$ | ≤ 2.0 ns | 30 pF | 500 Ω | open | GND | $2V_{CC}$ |
| 2.7 V | $V_{CC}$ | ≤ 2.5 ns | 50 pF | 500 Ω | open | GND | $2V_{CC}$ |
| 3 V to 3.6 V | $V_{CC}$ | ≤ 2.5 ns | 50 pF | 500 Ω | open | GND | $2V_{CC}$ |
| 4.5 V to 5.5 V | $V_{CC}$ | ≤ 2.5 ns | 50 pF | 500 Ω | open | GND | $2V_{CC}$ |


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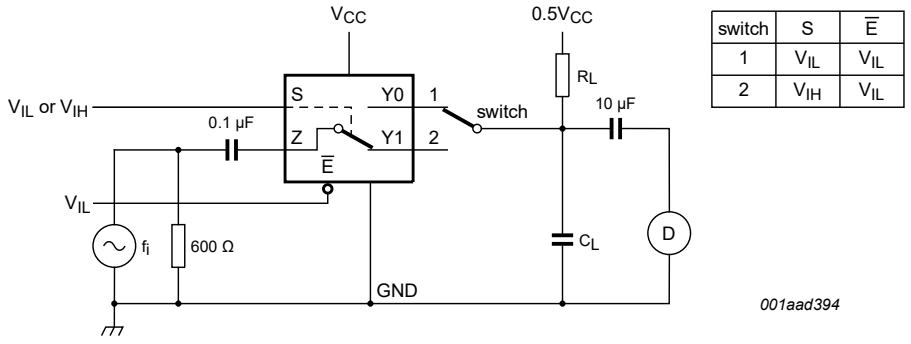
## 11.2. Additional dynamic characteristics

**Table 12. Additional dynamic characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $T_{amb}$ = 25 °C.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| THD | total harmonic distortion | $f_i$ = 600 Hz to 20 kHz; $R_L$ = 600 Ω; $C_L$ = 50 pF; $V_I$ = 0.5 V (p-p); see Fig. 15 | | | | |
| | | $V_{CC}$ = 1.65 V | - | 0.260 | - | % |
| | | $V_{CC}$ = 2.3 V | - | 0.078 | - | % |
| | | $V_{CC}$ = 3.0 V | - | 0.078 | - | % |
| | | $V_{CC}$ = 4.5 V | - | 0.078 | - | % |
| $f_{(-3dB)}$ | -3 dB frequency response | $R_L$ = 50 Ω; $C_L$ = 5 pF; see Fig. 16 | | | | |
| | | $V_{CC}$ = 1.65 V | - | 200 | - | MHz |
| | | $V_{CC}$ = 2.3 V | - | 300 | - | MHz |
| | | $V_{CC}$ = 3.0 V | - | 300 | - | MHz |
| | | $V_{CC}$ = 4.5 V | - | 300 | - | MHz |
| $\alpha_{iso}$ | isolation (OFF-state) | $R_L$ = 50 Ω; $C_L$ = 5 pF; $f_i$ = 10 MHz; see Fig. 17 | | | | |
| | | $V_{CC}$ = 1.65 V | - | -42 | - | dB |
| | | $V_{CC}$ = 2.3 V | - | -42 | - | dB |
| | | $V_{CC}$ = 3.0 V | - | -40 | - | dB |
| | | $V_{CC}$ = 4.5 V | - | -40 | - | dB |
| $Q_{inj}$ | charge injection | $C_L$ = 0.1 nF; $V_{gen}$ = 0 V; $R_{gen}$ = 0 Ω; $f_i$ = 1 MHz; $R_L$ = 1 MΩ; see Fig. 18 | | | | |
| | | $V_{CC}$ = 1.8 V | - | 3.3 | - | pC |
| | | $V_{CC}$ = 2.5 V | - | 4.1 | - | pC |
| | | $V_{CC}$ = 3.3 V | - | 5.0 | - | pC |
| | | $V_{CC}$ = 4.5 V | - | 6.4 | - | pC |
| | | $V_{CC}$ = 5.5 V | - | 7.5 | - | pC |

## 11.3. Test circuits

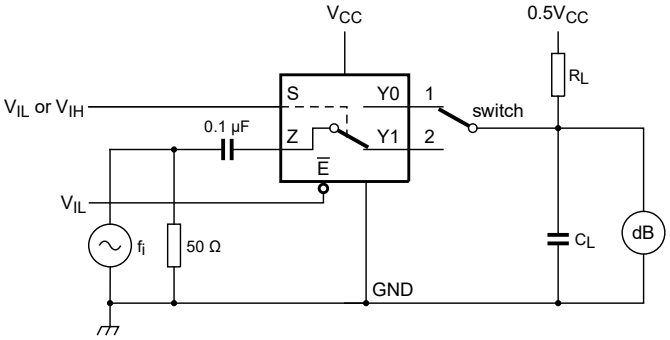



| switch | S | $\overline{E}$ |
|---|---|---|
| 1 | $V_{IL}$ | $V_{IL}$ |
| 2 | $V_{IH}$ | $V_{IL}$ |

**Fig. 15. Test circuit for measuring total harmonic distortion**


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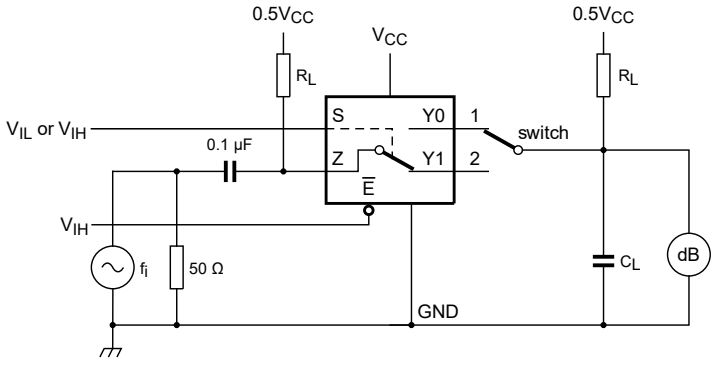
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| switch | S | $\overline{E}$ |
|---|---|---|
| 1 | $V_{IL}$ | $V_{IL}$ |
| 2 | $V_{IH}$ | $V_{IL}$ |

Adjust $f_i$ voltage to obtain 0 dBm level at output. Increase $f_i$ frequency until dB meter reads -3 dB.

**Fig. 16. Test circuit for measuring the frequency response when switch is in ON-state**



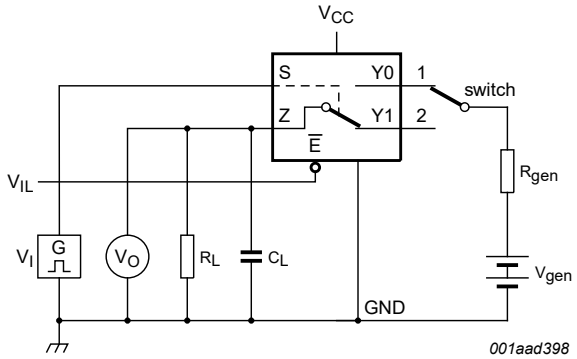

| switch | S | $\overline{E}$ |
|---|---|---|
| 1 | $V_{IH}$ | $V_{IH}$ |
| 2 | $V_{IL}$ | $V_{IH}$ |

Adjust $f_i$ voltage to obtain 0 dBm level at input.

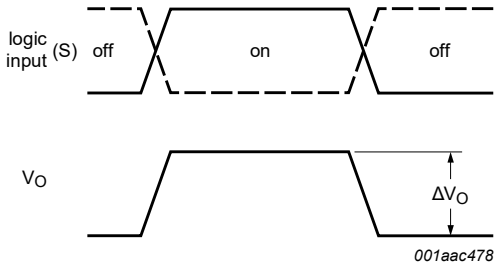
**Fig. 17. Test circuit for measuring isolation (OFF-state)**


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a. Test circuit




b. Input and output pulse definitions

$Q_{inj} = \Delta V_O \times C_L$.

$\Delta V_O$ = output voltage variation.

$R_{gen}$ = generator resistance.

$V_{gen}$ = generator voltage.

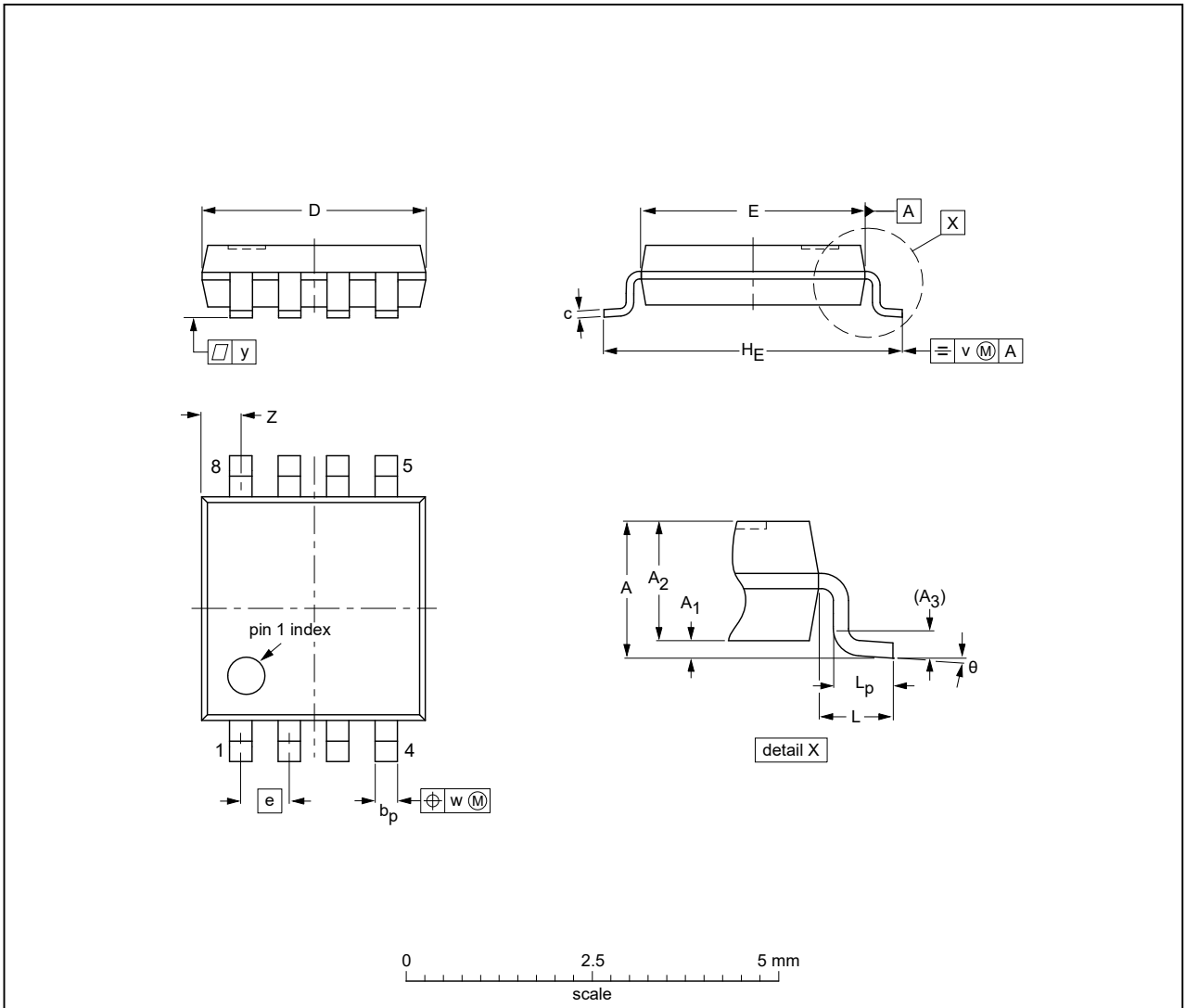
**Fig. 18. Test circuit for measuring charge injection**


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## 12. Package outline

**TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.00 | 0.95<br>0.75 | 0.25 | 0.38<br>0.22 | 0.18<br>0.08 | 3.1<br>2.9 | 3.1<br>2.9 | 0.65 | 4.1<br>3.9 | 0.5 | 0.47<br>0.33 | 0.2 | 0.13 | 0.1 | 0.70<br>0.35 | 8°<br>0° |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

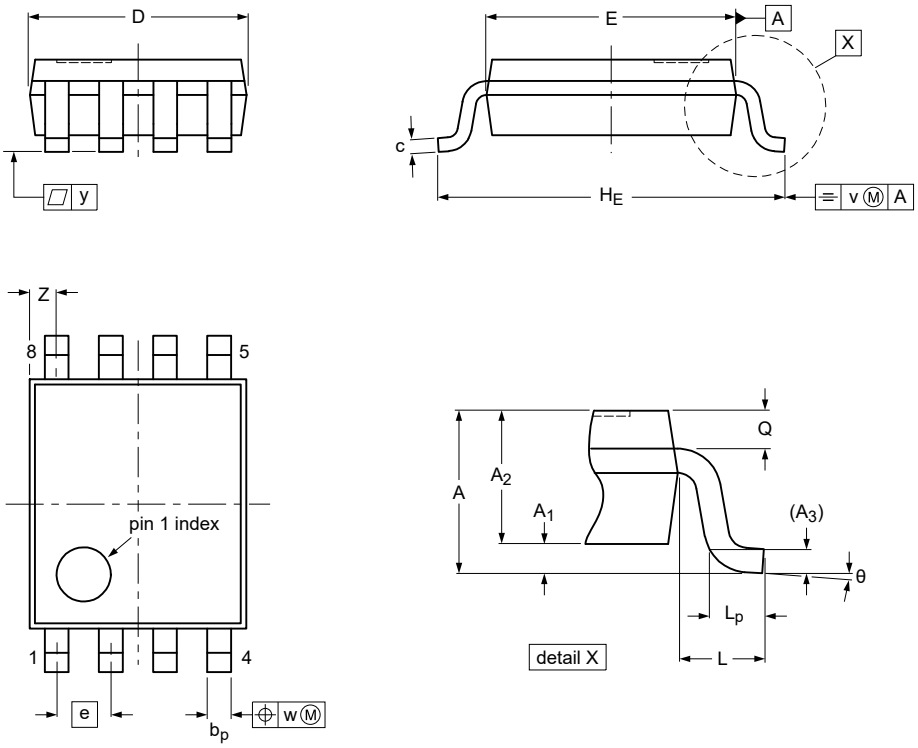
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT505-2 | | - - - | | | | 02-01-16 |

**Fig. 19. Package outline SOT505-2 (TSSOP8)**


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**VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm** **SOT765-1**




Dimensions (mm are the original dimensions)

| Unit | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| max | | 0.15 | 0.85 | | 0.27 | 0.23 | 2.1 | 2.4 | | 3.2 | | 0.40 | 0.21 | | | | 0.4 | 8° |
| mm nom | 1 | | | 0.12 | | | | | 0.5 | | 0.4 | | | 0.2 | 0.08 | 0.1 | | |
| min | | 0.00 | 0.60 | | 0.17 | 0.08 | 1.9 | 2.2 | | 3.0 | | 0.15 | 0.19 | | | | 0.1 | 0° |

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

*sot765-1_po*

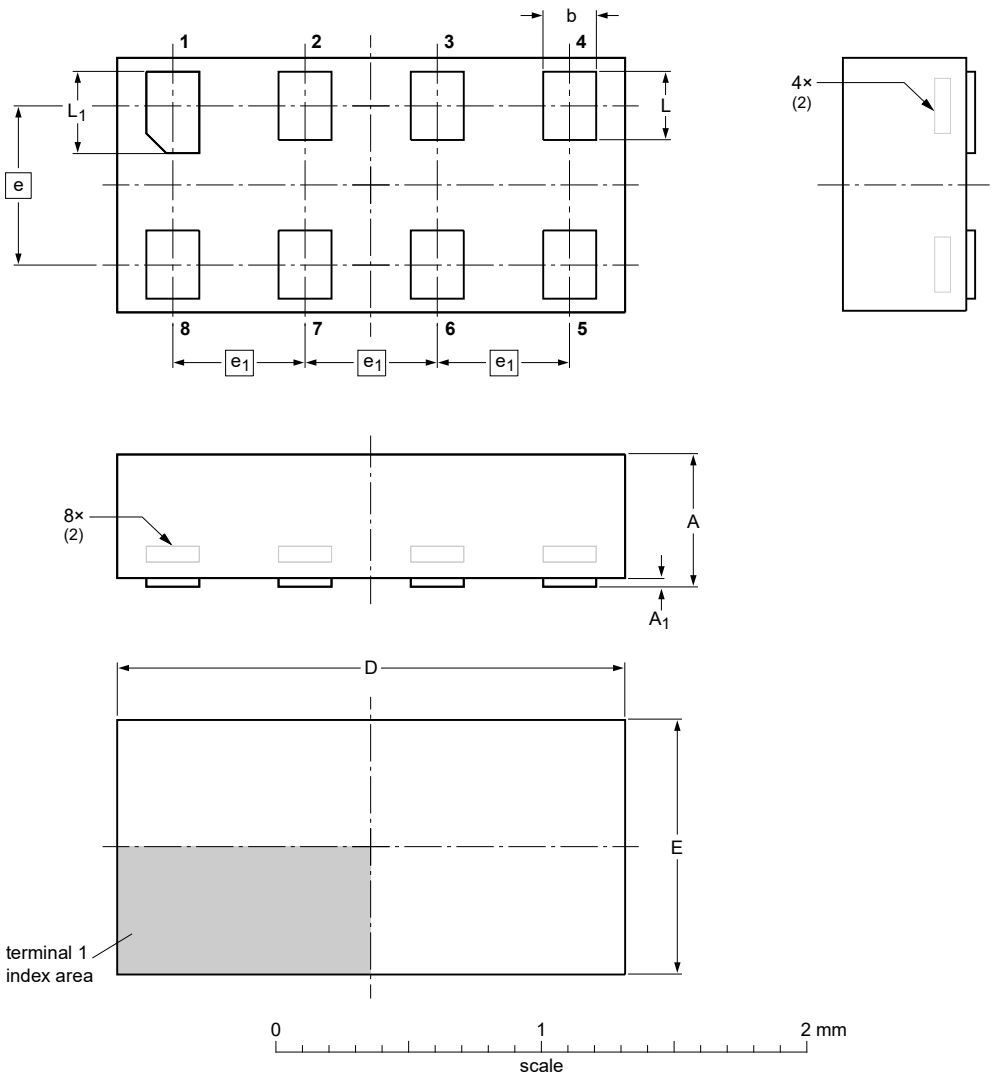
| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT765-1 | | MO-187 | | | | ~~07-06-02~~ 16-05-31 |

**Fig. 20. Package outline SOT765-1 (VSSOP8)**


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**XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm** **SOT833-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A(1) max | $A_1$ max | b | D | E | e | $e_1$ | L | $L_1$ |
|---|---|---|---|---|---|---|---|---|---|
| mm | 0.5 | 0.04 | 0.25<br>0.17 | 2.0<br>1.9 | 1.05<br>0.95 | 0.6 | 0.5 | 0.35<br>0.27 | 0.40<br>0.32 |

**Notes**

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

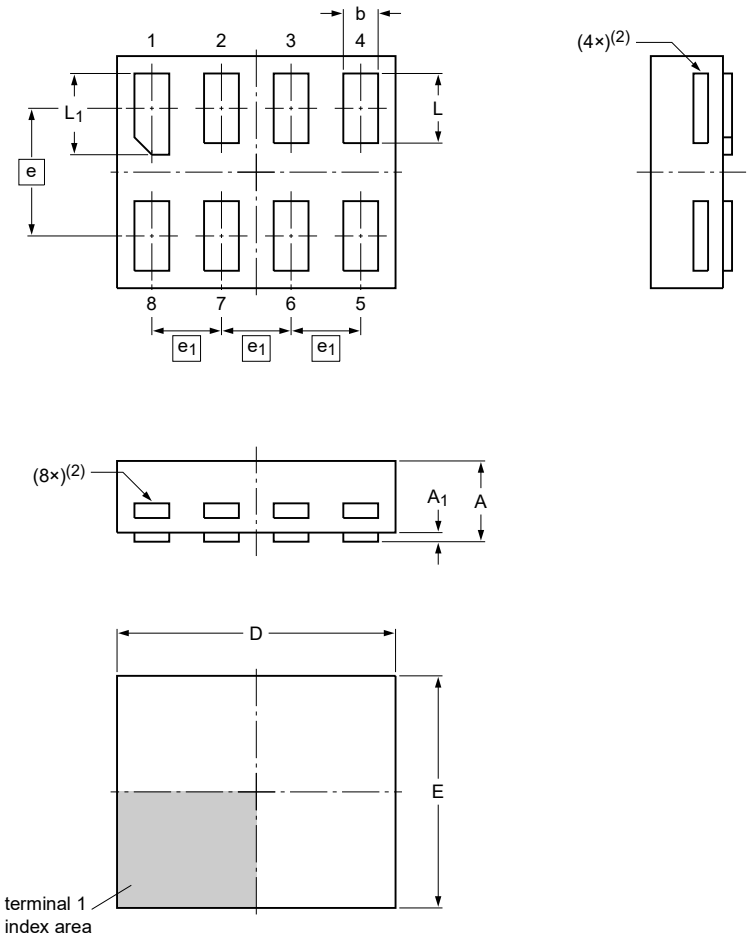
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT833-1 | - - - | MO-252 | - - - | | | ~~07-11-14~~<br>07-12-07 |

**Fig. 21. Package outline SOT833-1 (XSON8)**


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**XSON8: extremely thin small outline package; no leads;**
**8 terminals; body 1.2 x 1.0 x 0.35 mm** **SOT1116**




Dimensions

| Unit | | A(1) | $A_1$ | b | D | E | e | $e_1$ | L | $L_1$ |
|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.35 | 0.04 | 0.20 | 1.25 | 1.05 | | | 0.35 | 0.40 |
| | nom | | | 0.15 | 1.20 | 1.00 | 0.55 | 0.3 | 0.30 | 0.35 |
| | min | | | 0.12 | 1.15 | 0.95 | | | 0.27 | 0.32 |

Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

*sot1116_po*

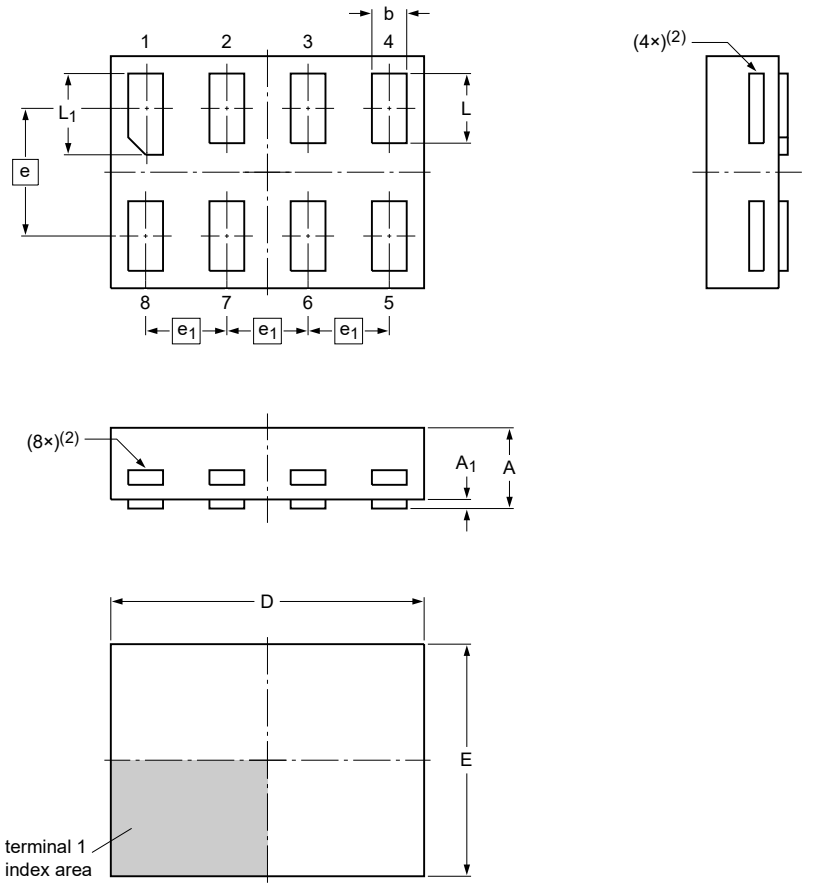
| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1116 | | | | | | ~~10-04-02~~ 10-04-07 |

**Fig. 22. Package outline SOT1116 (XSON8)**


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**XSON8: extremely thin small outline package; no leads;**
**8 terminals; body 1.35 x 1.0 x 0.35 mm** **SOT1203**




Dimensions

| Unit | | A(1) | $A_1$ | b | D | E | e | $e_1$ | L | $L_1$ |
|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.35 | 0.04 | 0.20 | 1.40 | 1.05 | | | 0.35 | 0.40 |
| | nom | | | 0.15 | 1.35 | 1.00 | 0.55 | 0.35 | 0.30 | 0.35 |
| | min | | | 0.12 | 1.30 | 0.95 | | | 0.27 | 0.32 |

Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

*sot1203_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1203 | | | | | | ~~10-04-02~~ 10-04-06 |

**Fig. 23. Package outline SOT1203 (XSON8)**


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# 13. Abbreviations

**Table 13. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| TTL | Transistor-Transistor Logic |

# 14. Revision history

**Table 14. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74LVC2G53 v.15 | 20230828 | Product data sheet | - | 74LVC2G53 v.14 |
| Modifications: | • Section 2: ESD specification updated according to the latest JEDEC standard. | | | |
| 74LVC2G53 v.14 | 20210422 | Product data sheet | - | 74LVC2G53 v.13 |
| Modifications: | • Section 1 and Section 2 updated.<br>• Type number 74LVC2G53GF (SOT1089 / XSON8) removed. | | | |
| 74LVC2G53 v.13 | 20190731 | Product data sheet | - | 74LVC2G53 v.12 |
| Modifications: | • Type number 74LVC2G53GM (SOT902-2/XQFN8) removed.<br>• Table 5: Derating values for $P_{tot}$ total power dissipation updated. | | | |
| 74LVC2G53 v.12 | 20181116 | Product data sheet | - | 74LVC2G53 v.11 |
| Modifications: | • Type number 74LVC2G53GD (SOT996-2/XSON8) removed. | | | |
| 74LVC2G53 v.11 | 20170821 | Product data sheet | - | 74LVC2G53 v.10 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.<br>• Legal texts have been adapted to the new company name where appropriate. | | | |
| 74LVC2G53 v.10 | 20161215 | Product data sheet | - | 74LVC2G53 v.9 |
| Modifications: | • Table 7: The maximum limits for leakage current and supply current have changed. | | | |
| 74LVC2G53 v.9 | 20130405 | Product data sheet | - | 74LVC2G53 v.8 |
| Modifications: | • For type number 74LVC2G53GD XSON8U has changed to XSON8. | | | |
| 74LVC2G53 v.8 | 20120622 | Product data sheet | - | 74LVC2G53 v.7 |
| Modifications: | • For type number 74LVC2G53GM the SOT code has changed to SOT902-2. | | | |
| 74LVC2G53 v.7 | 20111125 | Product data sheet | - | 74LVC2G53 v.6 |
| Modifications: | • Legal pages updated. | | | |
| 74LVC2G53 v.6 | 20100927 | Product data sheet | - | 74LVC2G53 v.5 |
| 74LVC2G53 v.5 | 20080618 | Product data sheet | - | 74LVC2G53 v.4 |
| 74LVC2G53 v.4 | 20080228 | Product data sheet | - | 74LVC2G53 v.3 |
| 74LVC2G53 v.3 | 20070828 | Product data sheet | - | 74LVC2G53 v.2 |
| 74LVC2G53 v.2 | 20060331 | Product data sheet | - | 74LVC2G53 v.1 |
| 74LVC2G53 v.1 | 20060110 | Product data sheet | - | - |


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# 15. Legal information

## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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**Date of release: 28 August 2023**