DATA SHEET

74LVC543A
Octal D-type registered transceiver; 3-state

Product specification
Supersedes data of 2004 Feb 05

2004 Apr 07

Philips
Semiconductors

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Octal D-type registered transceiver; 3-state 74LVC543A

FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Supply voltage range from 1.2 V to 3.6 V
- Complies with JEDEC standard JESD8-B/JESD36
- CMOS low-power consumption
- Direct interface with TTL levels
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- 3-state non-inverting outputs for bus oriented applications
- High-impedance when V_{CC} = 0 V
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

DESCRIPTION

The 74LVC543A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC543A is an octal registered transceiver containing two sets of D-type latches for temporary storage of the data flow in either direction. Separate latch enable inputs (pins $\overline{LE}_{AB}$ and $\overline{LE}_{BA}$) and output enable inputs (pins $\overline{OE}_{AB}$ and $\overline{OE}_{BA}$) are provided for each register to permit independent control of inputting and outputting in either direction of the data flow.

The 74LVC543A contains eight D-type latches, with separate inputs and controls for each set. For data flow from pins A to B, for example, the A to B enable input (pin $\overline{E}_{AB}$) must be LOW in order to enter data from pins A0 to A7 or take data from pins B0 to B7, as indicated in the “Function table”. With pin $\overline{E}_{AB}$ LOW, a LOW signal on the A to B latch enable input (pin $\overline{LE}_{AB}$) makes the A to B latches transparent; a subsequent LOW-to-HIGH transition on pin $\overline{LE}_{AB}$ puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With pins $\overline{E}_{AB}$ and $\overline{OE}_{AB}$ both LOW, the 3-state B output buffers are active and display the data present at the outputs of the A latches.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay An to Bn; Bn to An	C_L = 50 pF; V_{CC} = 3.3 V	3.0	ns
C_I	input capacitance		4.0	pF
$C_{I/O}$	input/output capacitance		5.0	pF
C_{PD}	power dissipation capacitance per latch	V_{CC} = 3.3 V; notes 1 and 2		
		outputs enabled	15.0	pF
		outputs disabled	3.0	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

OPERATING MODES	INPUT				OUTPUT
	$\overline{OE}_{XX}$	$\overline{E}_{XX}$	$\overline{LE}_{XX}$	DATA	
Disabled	H	X	X	X	Z
	X	H	X	X	Z
Disabled plus latch	L	↑	L	h	Z
	L	↑	L	l	Z
Latch plus display	L	L	↑	h	H
	L	L	↑	l	L
Transparent	L	L	L	H	H
	L	L	L	L	L
Hold (do nothing)	L	L	H	X	NC

Note

1. XX = AB for A to B direction; BA for B to A direction;
   H = HIGH voltage level;
   L = LOW voltage level;
   h = HIGH state must be present one set-up time before the LOW-to-HIGH transition of $\overline{LE}_{AB}$, $\overline{LE}_{BA}$, $\overline{E}_{AB}$ and $\overline{E}_{BA}$;
   l = LOW state must be present one set-up time before the LOW-to-HIGH transition of $\overline{LE}_{AB}$, $\overline{LE}_{BA}$, $\overline{E}_{AB}$ and $\overline{E}_{BA}$;
   X = don't care;
   ↑ = LOW-to-HIGH level transition;
   NC = no change;
   Z = high-impedance OFF-state.

ORDERING INFORMATION

TYPE NUMBER	TEMPERATURE RANGE	PACKAGE			
		PINS	PACKAGE	MATERIAL	CODE
74LVC543AD	–40 °C to +125 °C	24	SO24	plastic	SOT137-1
74LVC543ADB	–40 °C to +125 °C	24	SSOP24	plastic	SOT340-1
74LVC543APW	–40 °C to +125 °C	24	TSSOP24	plastic	SOT355-1
74LVC543ABQ	–40 °C to +125 °C	24	DHVQFN24	plastic	SOT815-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	$\overline{LE}_{BA}$	B to A latch enable input (active LOW)
2	$\overline{OE}_{BA}$	B to A output enable input (active LOW)
3	A0	A data input or output
4	A1	A data input or output
5	A2	A data input or output
6	A3	A data input or output
7	A4	A data input or output
8	A5	A data input or output
9	A6	A data input or output
10	A7	A data input or output
11	$\overline{E}_{AB}$	A to B enable input (active LOW)
12	GND	ground (0 V)
13	$\overline{OE}_{AB}$	A to B output enable input (active LOW)
14	$\overline{LE}_{AB}$	A to B latch enable input (active LOW)
15	B7	B data output or input
16	B6	B data output or input
17	B5	B data output or input
18	B4	B data output or input
19	B3	B data output or input
20	B2	B data output or input
21	B1	B data output or input
22	B0	B data output or input
23	$\overline{E}_{BA}$	B to A enable input (active LOW)
24	V_{CC}	positive supply voltage

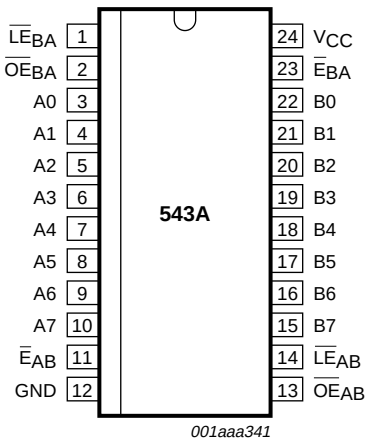
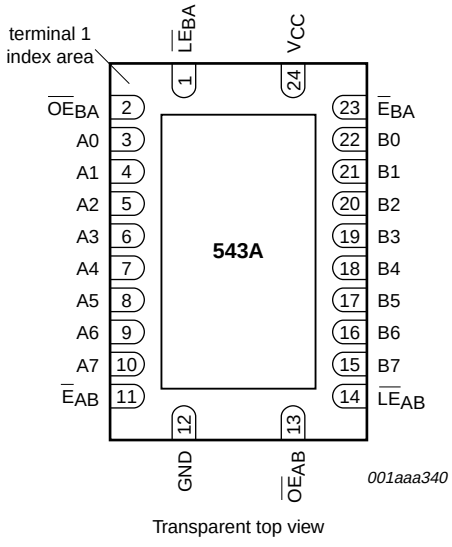


Fig.1 Pin configuration SO24 and (T)SSOP24.



Transparent top view

The die substrate is attached to the exposed die pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN24.

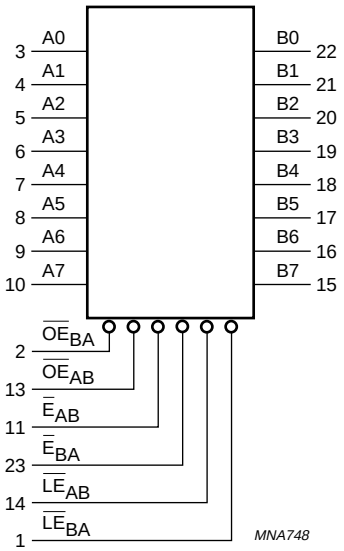


Fig.3 Logic symbol.

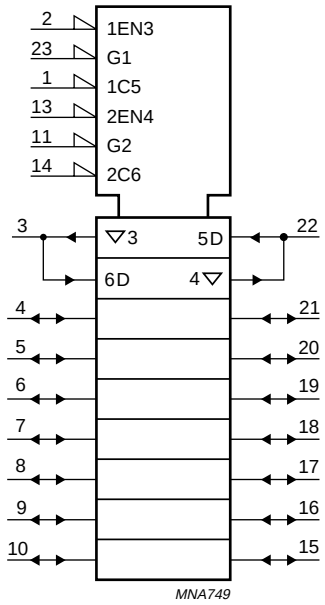


Fig.4 Logic symbol (IEEE/IEC).

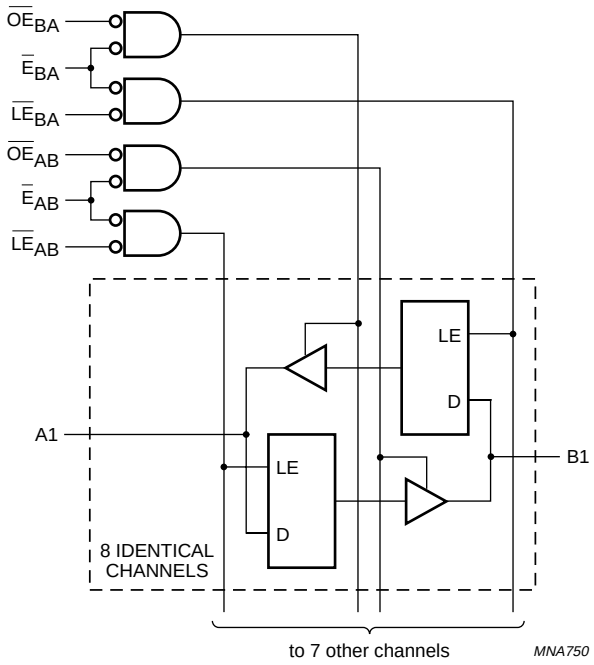


Fig.5 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
V_I	input voltage		0	5.5	V
V_O	output voltage	output HIGH or LOW state	0	V_{CC}	V
		output 3-state	0	5.5	V
T_{amb}	operating ambient temperature	in free air	–40	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.2 V to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V); note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+6.5	V
I_{IK}	input diode current	V_I < 0 V	–	–50	mA
V_I	input voltage	note 2	–0.5	+6.5	V
I_{OK}	output diode current	V_O > V_{CC} or V_O < 0 V	–	±50	mA
V_O	output voltage	output HIGH or LOW state; note 2	–0.5	V_{CC} + 0.5	V
		output 3-state; note 2	–0.5	+6.5	V
I_O	output source or sink current	V_O = 0 V to V_{CC}	–	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +125 °C; note 3	–	500	mW

Notes

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
3. For SO24 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.

   For (T)SSOP24 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

   For DHVQFN24 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 °C to +85 °C; note 1							
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V_{IL}	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = −100 μA	2.7 to 3.6	V_{CC} − 0.2	V_{CC}[2]	–	V
		I_O = −12 mA	2.7	V_{CC} − 0.5	–	–	V
		I_O = −18 mA	3.0	V_{CC} − 0.6	–	–	V
		I_O = −24 mA	3.0	V_{CC} − 0.8	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 μA	2.7 to 3.6	–	GND[2]	0.2	V
		I_O = 12 mA	2.7	–	–	0.4	V
		I_O = 24 mA	3.0	–	–	0.55	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	3.6	–	±0.1	±5	μA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND; note 3	3.6	–	0.1	±10	μA
I_{off}	power-off leakage supply	V_I or V_O = 5.5 V	0.0	–	0.1	±10	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A	3.6	–	0.1	10	μA
ΔI_{CC}	additional quiescent supply current per pin	V_I = V_{CC} − 0.6 V; I_O = 0 A	2.7 to 3.6	–	5[2]	500	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 °C to +125 °C							
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V_{IL}	LOW-level input voltage		1.2	–	–	0	V
			2.7 to 3.6	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = −100 μA	2.7 to 3.6	V_{CC} − 0.3	–	–	V
		I_O = −12 mA	2.7	V_{CC} − 0.65	–	–	V
		I_O = −18 mA	3.0	V_{CC} − 0.75	–	–	V
		I_O = −24 mA	3.0	V_{CC} − 1	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 μA	2.7 to 3.6	–	–	0.3	V
		I_O = 12 mA	2.7	–	–	0.6	V
		I_O = 24 mA	3.0	–	–	0.8	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	3.6	–	–	±20	μA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND; note 3	3.6	–	–	±20	μA
I_{off}	power-off leakage supply	V_I or V_O = 5.5 V	0.0	–	–	±20	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A	3.6	–	–	40	μA
ΔI_{CC}	additional quiescent supply current per pin	V_I = V_{CC} − 0.6 V; I_O = 0 A	2.7 to 3.6	–	–	5000	μA

Notes

1. All typical values are measured T_{amb} = 25 °C.
2. These typical values are measured at V_{CC} = 3.3 V.
3. For transceivers, the parameter I_{OZ} includes the input leakage current.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF.

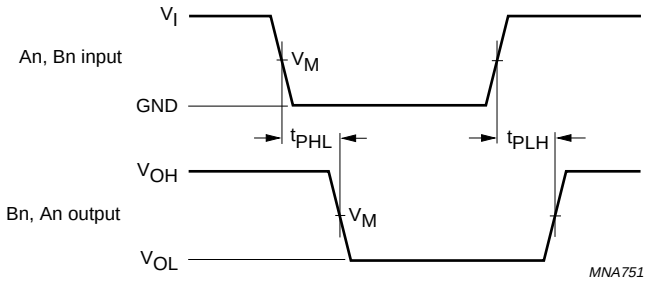
SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 °C to +85 °C; note 1							
t_{PHL}/t_{PLH}	propagation delay An to Bn; Bn to An	see Figs 6 and 10	1.2	–	15	–	ns
			2.7	1.5	–	8.0	ns
			3.0 to 3.6	1.0	3.0(2)	7.0	ns
	propagation delay $\overline{LE}_{BA}$ to An; LE_{AB} to Bn	see Figs 7 and 10	1.2	–	16	–	ns
			2.7	1.5	–	9.5	ns
			3.0 to 3.6	1.2	4.2(2)	8.5	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$ to An; $\overline{OE}_{AB}$ to Bn	see Figs 8 and 10	1.2	–	17	–	ns
			2.7	1.5	–	9.2	ns
			3.0 to 3.6	1.3	3.4(2)	7.7	ns
	3-state output enable time $\overline{E}_{BA}$ to An; $\overline{E}_{AB}$ to Bn	see Figs 8 and 10	1.2	–	18	–	ns
			2.7	1.5	–	9.3	ns
			3.0 to 3.6	1.3	3.6(2)	8.0	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$ to An; $\overline{OE}_{AB}$ to Bn	see Figs 8 and 10	1.2	–	8.0	–	ns
			2.7	1.5	–	7.5	ns
			3.0 to 3.6	1.5	3.2(2)	7.0	ns
	3-state output disable time $\overline{E}_{BA}$ to An; $\overline{E}_{AB}$ to Bn	see Figs 8 and 10	1.2	–	8.5	–	ns
			2.7	1.5	–	7.5	ns
			3.0 to 3.6	1.5	3.3(2)	7.0	ns
t_W	$\overline{LE}_{XX}$ pulse with LOW	see Fig.7	1.2	–	4.0	–	ns
			2.7	3.0	–	–	ns
			3.0 to 3.6	3.0	0.9(2)	–	ns
t_{su}	set-up time An, Bn to $\overline{LE}_{XX}$; An, Bn to $\overline{E}_{XX}$	see Fig.9	1.2	–	–1.5	–	ns
			2.7	1.5	–	–	ns
			3.0 to 3.6	+1.5	–0.5(2)	–	ns
t_h	hold time An, Bn to $\overline{LE}_{XX}$; An, Bn to $\overline{E}_{XX}$	see Fig.9	1.2	–	2.0	–	ns
			2.7	1.5	–	–	ns
			3.0 to 3.6	1.5	0.6(2)	–	ns
$t_{sk(0)}$	skew	note 3		–	–	1.0	ns

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 °C to +125 °C							
t_{PHL}/t_{PLH}	propagation delay An to Bn; Bn to An	see Figs 6 and 10	1.2	–	–	–	ns
			2.7	1.5	–	10.0	ns
			3.0 to 3.6	1.0	–	9.0	ns
	propagation delay $\overline{LE}_{BA}$ to An; LE_{AB} to Bn	see Figs 7 and 10	1.2	–	–	–	ns
			2.7	1.5	–	12.0	ns
			3.0 to 3.6	1.2	–	11.0	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$ to An; $\overline{OE}_{AB}$ to Bn	see Figs 8 and 10	1.2	–	–	–	ns
			2.7	1.5	–	11.5	ns
			3.0 to 3.6	1.3	–	10.0	ns
	3-state output enable time $\overline{E}_{BA}$ to An; $\overline{E}_{AB}$ to Bn	see Figs 8 and 10	1.2	–	–	–	ns
			2.7	1.5	–	12.0	ns
			3.0 to 3.6	1.3	–	10.0	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$ to An; $\overline{OE}_{AB}$ to Bn	see Figs 8 and 10	1.2	–	–	–	ns
			2.7	1.5	–	9.5	ns
			3.0 to 3.6	1.5	–	9.0	ns
	3-state output disable time $\overline{E}_{BA}$ to An; $\overline{E}_{AB}$ to Bn	see Figs 8 and 10	1.2	–	–	–	ns
			2.7	1.5	–	11.5	ns
			3.0 to 3.6	1.5	–	9.0	ns
t_W	$\overline{LE}_{XX}$ pulse with LOW	see Fig.7	1.2	–	–	–	ns
			2.7	3.0	–	–	ns
			3.0 to 3.6	3.0	–	–	ns
t_{su}	set-up time An, Bn to $\overline{LE}_{XX}$; An, Bn to $\overline{E}_{XX}$	see Fig.9	1.2	–	–	–	ns
			2.7	1.5	–	–	ns
			3.0 to 3.6	1.5	–	–	ns
t_h	hold time An, Bn to $\overline{LE}_{XX}$; An, Bn to $\overline{E}_{XX}$	see Fig.9	1.2	–	–	–	ns
			2.7	1.5	–	–	ns
			3.0 to 3.6	1.5	–	–	ns
$t_{sk(0)}$	skew	note 3		–	–	1.5	ns

Notes

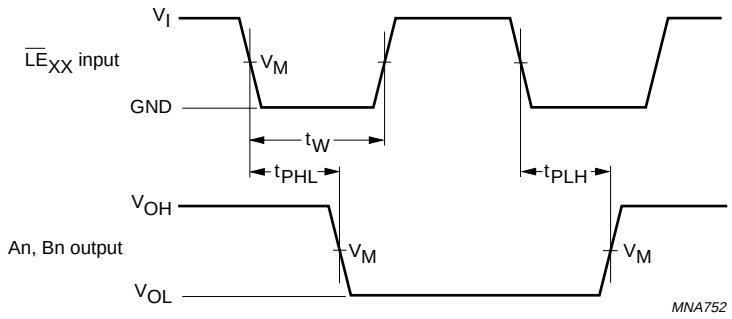
1. All typical values are measured at T_{amb} = 25 °C.
2. These typical values are measured at V_{CC} = 3.3 V.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

AC WAVEFORMS



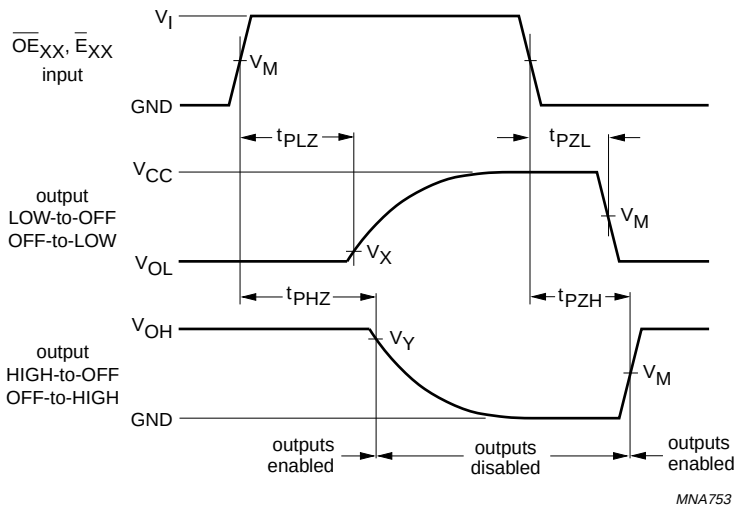
V_M = 1.5 V at $V_{CC} \geq$ 2.7 V.
$V_M = 0.5 \times V_{CC}$ at V_{CC} < 2.7 V.
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.6 Input (An and Bn) to output (Bn and An) propagation delays.



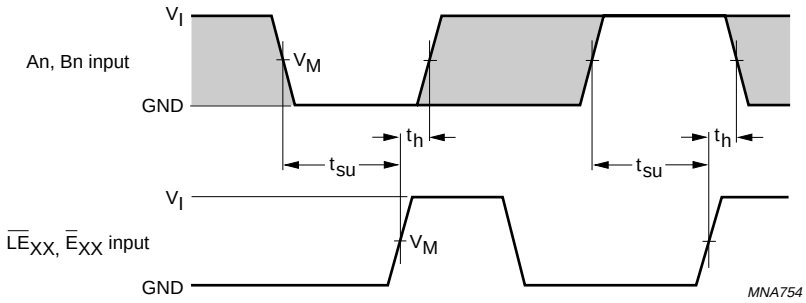
V_M = 1.5 V at $V_{CC} \geq$ 2.7 V.
$V_M = 0.5 \times V_{CC}$ at V_{CC} < 2.7 V.
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.7 Latch enable input ($\overline{LE}_{XX}$) pulse width and latch enable input to output An and Bn propagation delays.



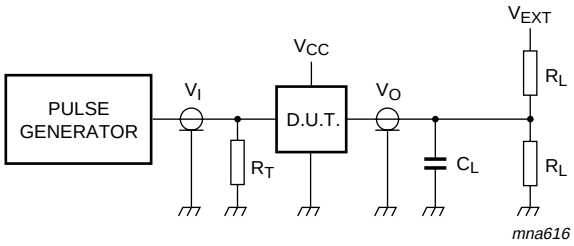
V_M = 1.5 V at $V_{CC} \geq$ 2.7 V.
$V_M = 0.5 \times V_{CC}$ at V_{CC} < 2.7 V.
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.
$V_X = V_{OL} + 0.3$ V at $V_{CC} \geq$ 2.7 V; $V_X = V_{OL} + 0.1 \times V_{CC}$ at V_{CC} < 2.7 V.
$V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq$ 2.7 V; $V_Y = V_{OH} - 0.1 \times V_{CC}$ at V_{CC} < 2.7 V.

Fig.8 3-state enable and disable times.



V_M = 1.5 V at $V_{CC} \geq$ 2.7 V.
$V_M = 0.5 \times V_{CC}$ at V_{CC} < 2.7 V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.9 Data set-up and hold times for the inputs An and Bn to $\overline{LE}_{XX}$ and $\overline{E}_{XX}$ inputs.



V_{CC}	V_I	C_L	R_L	V_{EXT}		
				t_{PLH}/t_{PHL}	t_{PZH}/t_{PHZ}	t_{PZL}/t_{PLZ}
1.2 V	V_{CC}	50 pF	500 Ω[1]	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

Note

1. The circuit performs better when R_L = 1000 Ω.

Definitions for test circuits:

R_L = Load resistor.

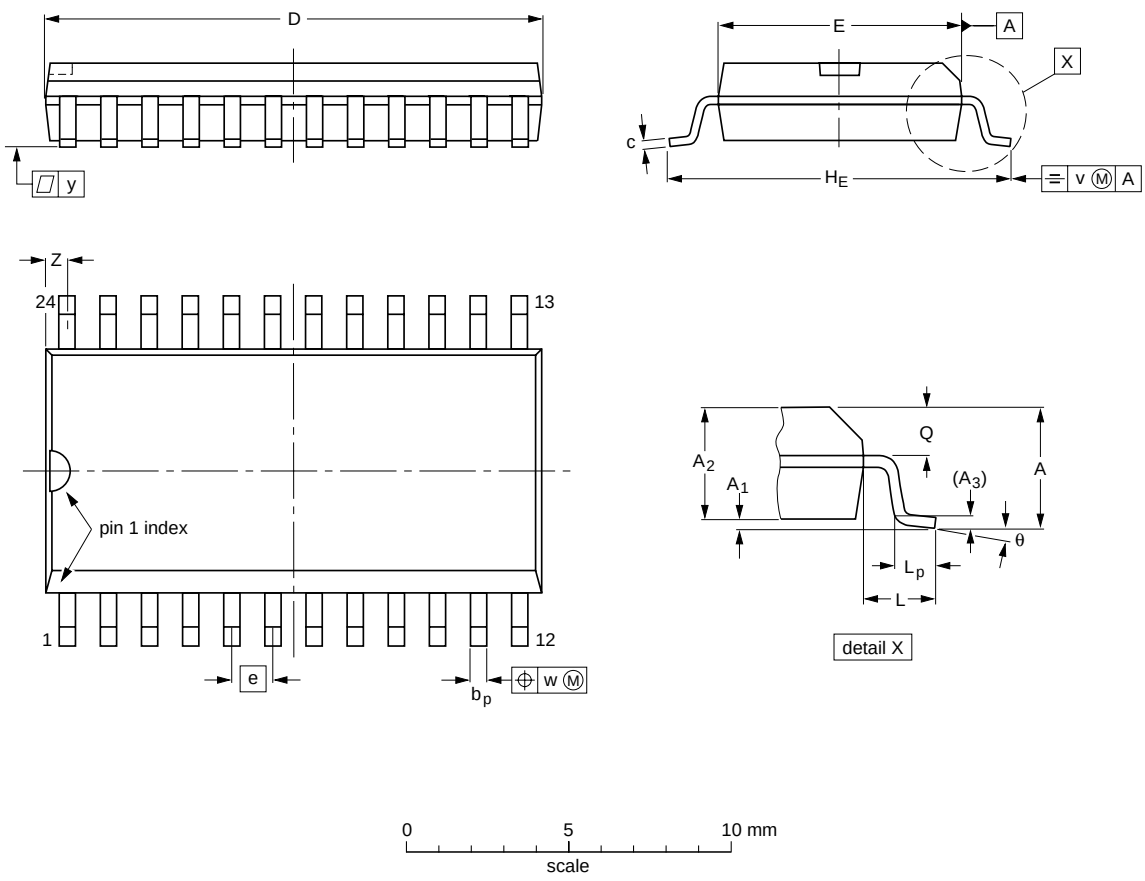
C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.10 Load circuitry for switching times.

PACKAGE OUTLINES

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

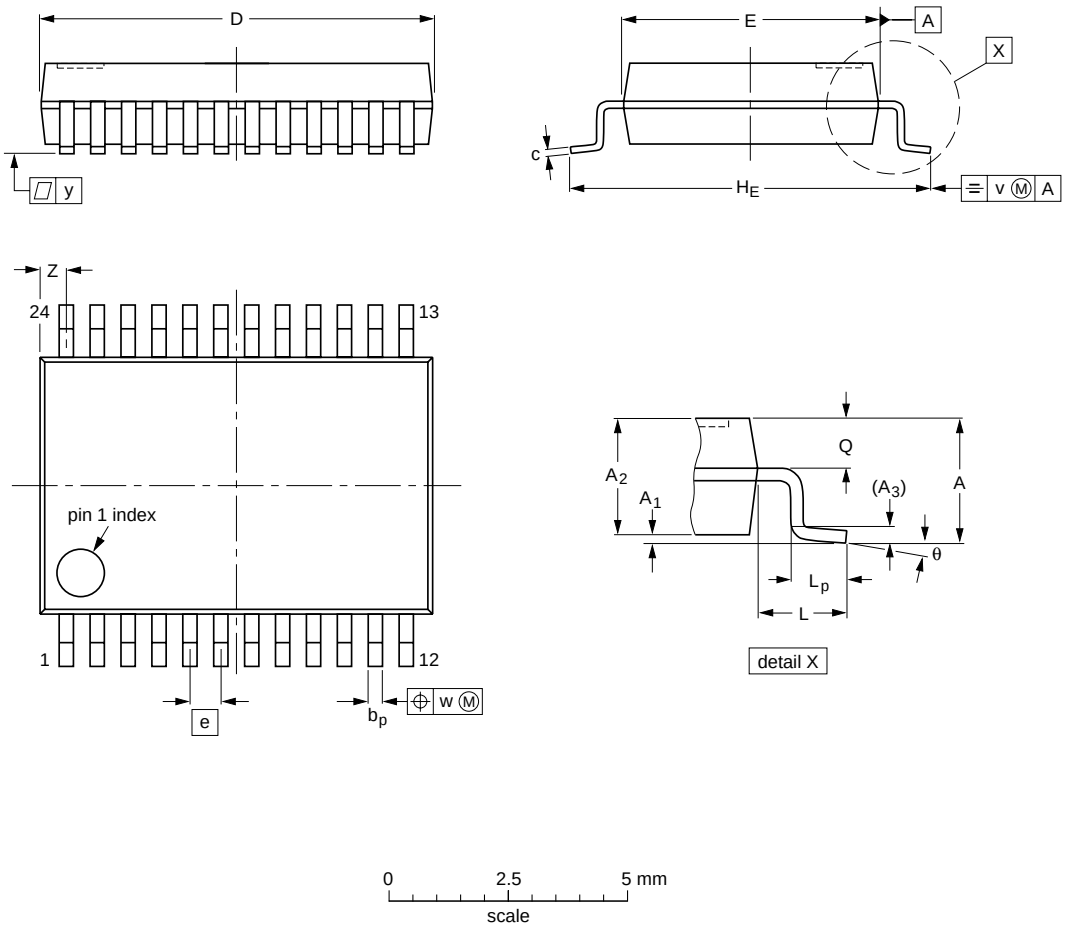
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

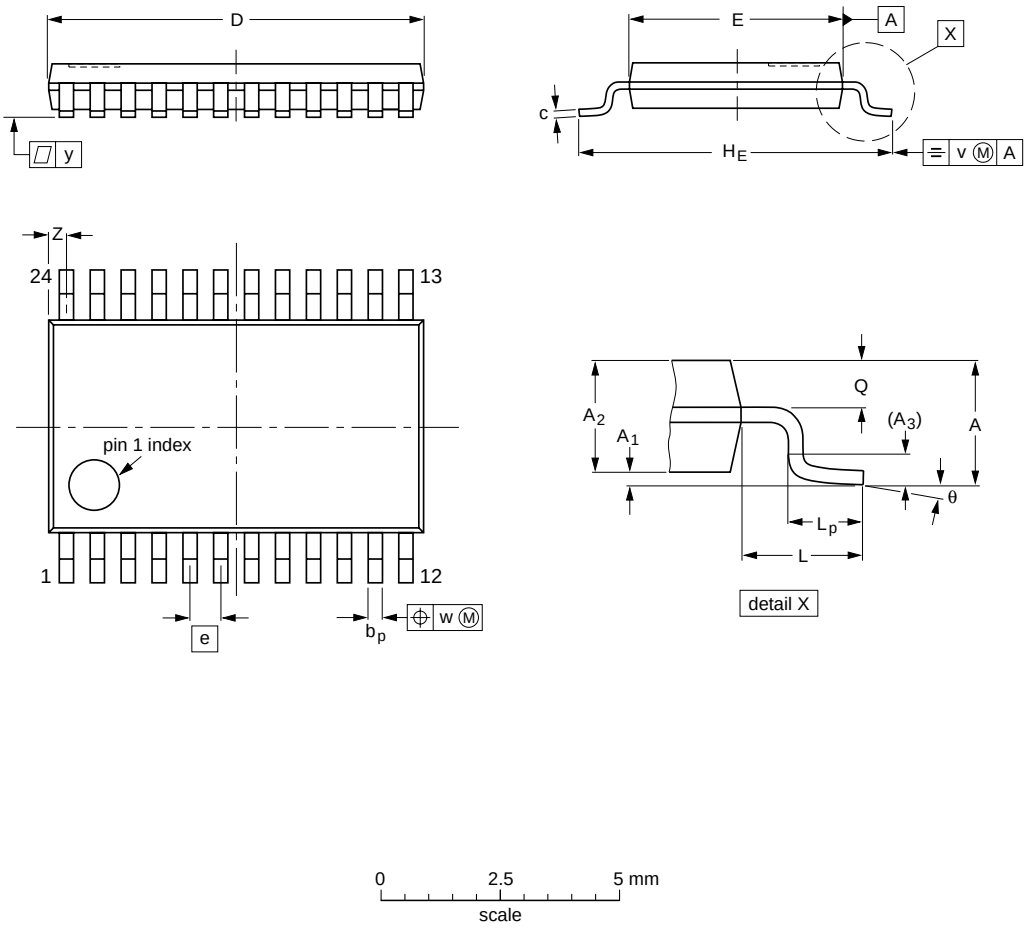
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

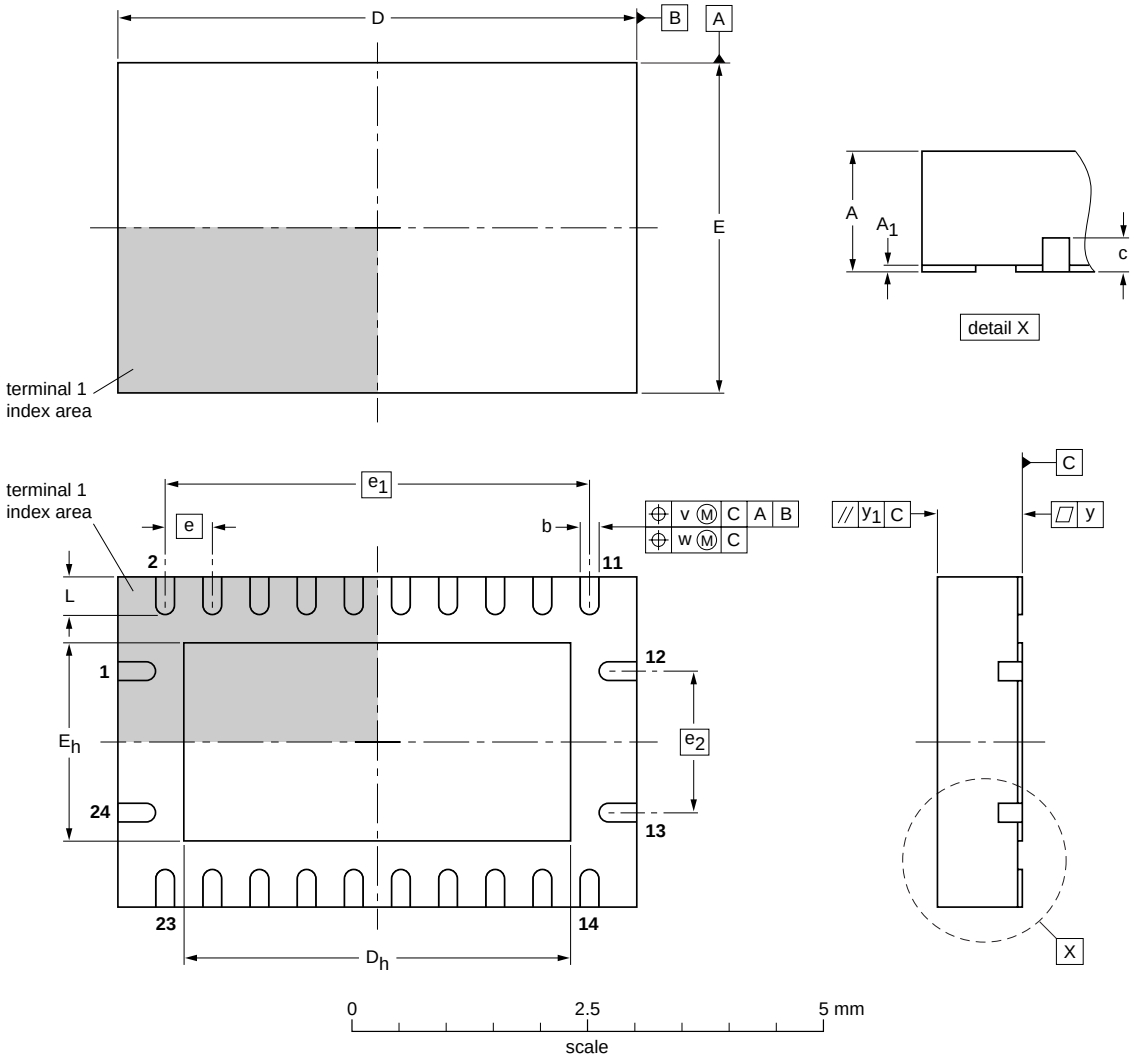
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm **SOT815-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.6 5.4	4.25 3.95	3.6 3.4	2.25 1.95	0.5	4.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT815-1	- - -	- - -	- - -			03-04-29

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
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Printed in The Netherlands R20/06/pp19 Date of release: 2004 Apr 07 Document order number: 9397 750 13074

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