DATA SHEET

74LVT534

3.3 V Octal D-type flip-flop; inverting (3-State)

Product data
Supersedes data of 1998 Feb 19

2004 Aug 25

Philips
Semiconductors

PHILIPS

3.3 V Octal D-type flip-flop, inverting (3-State) 74LVT534

FEATURES

- 3-State outputs for bus interfacing
- Common output enable
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5 V bus
- Power-up 3-State
- Power-up reset
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The LVT534 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

This device is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates. The state of each D input (one set-up time before the LOW-to-HIGH clock transition) is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the clock operation.

When $\overline{OE}$ is LOW, the stored data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance "off" state, which means they will neither drive nor load the bus.

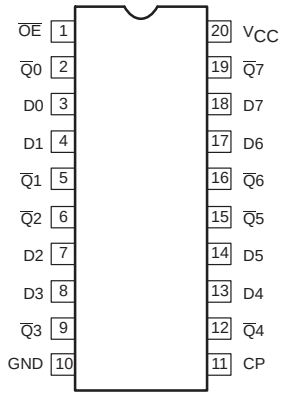
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25 °C; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50 pF; V_{CC} = 3.3 V	3.0 3.5	ns
C_{IN}	Input capacitance	V_I = 0 V or 3.0 V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; $V_{I/O}$ = 0 V or 3.0 V	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6 V	0.13	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	TYPE NUMBER	DWG NUMBER
20-Pin Plastic SOL	–40 °C to +85 °C	74LVT534D	SOT163-1
20-Pin Plastic SSOP Type II	–40 °C to +85 °C	74LVT534DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40 °C to +85 °C	74LVT534PW	SOT360-1

PIN CONFIGURATION



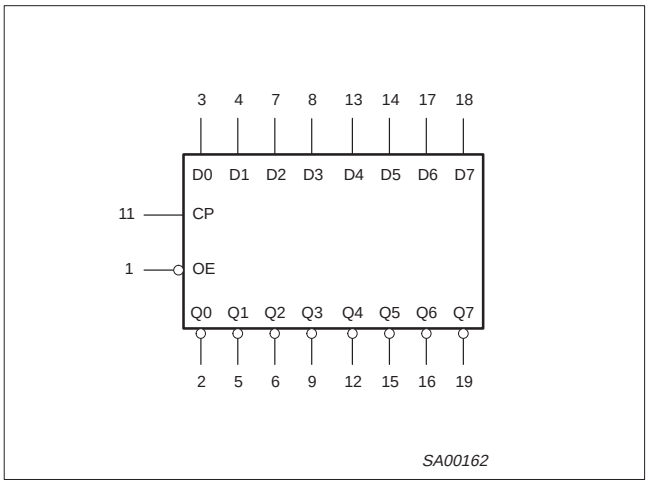
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PIN DESCRIPTION

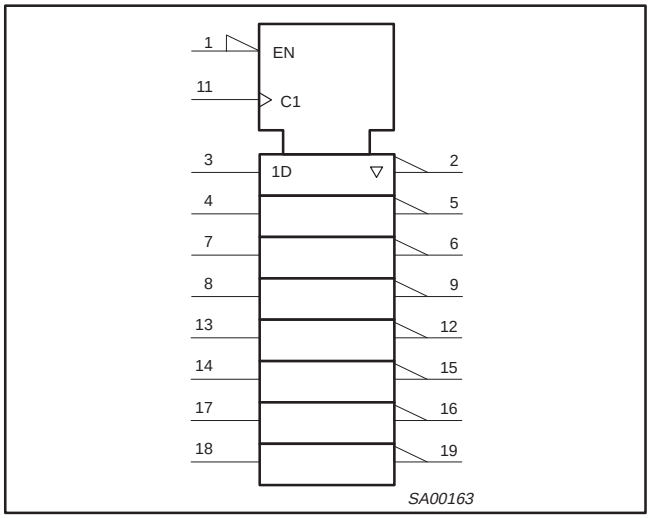
PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-LOW)
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	$\overline{Q}$0 to $\overline{Q}$7	Inverting 3-State outputs
11	CP	Clock pulse input (active rising edge)
10	GND	Ground (0 V)
20	V_{CC}	Positive supply voltage

3.3 V Octal D-type flip-flop, inverting (3-State) 74LVT534

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

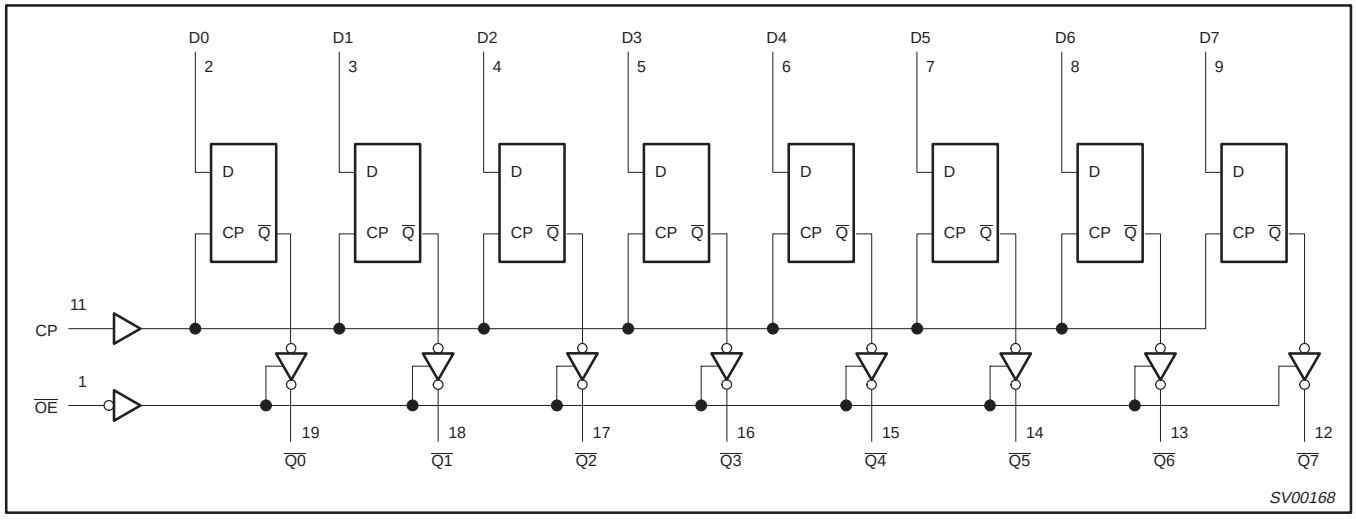


FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn		$\overline{Q0}$ to $\overline{Q7}$	
L L	↑ ↑	l h	L H	H L	Latch and read register
L	↥	X	NC	NC	Hold
H H	↥ ↑	X Dn	NC Dn	Z Z	Disable outputs

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
NC = No change
X = Don't care
Z = high-impedance "off" state
↑ = LOW-to-HIGH clock transition
↥ = not a LOW-to-HIGH clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$ V	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$ V	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or HIGH state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in LOW state	128	mA
		Output in HIGH state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	HIGH-level input voltage	2.0	–	V
V_{IL}	Input voltage	–	0.8	V
I_{OH}	HIGH-level output current	–	–32	mA
I_{OL}	LOW-level output current	–	32	mA
	LOW-level output current; current duty cycle ≤ 50 %, f ≥ 1 kHz	–	64	
$\Delta t/\Delta v$	Input transition rise or fall rate; outputs enabled	–	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				T_{amb} = –40° C to +85 °C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7 V; I_{IK} = –18 mA		–	–0.9	–1.2	V
V_{OH}	HIGH-level output voltage	V_{CC} = 2.7 V to 3.6 V; I_{OH} = –100 µA		V_{CC} – 0.2	V_{CC} – 0.1	–	V
		V_{CC} = 2.7 V; I_{OH} = –8 mA		2.4	2.5	–	V
		V_{CC} = 3.0 V; I_{OH} = –32 mA		2.0	2.2	–	V
V_{OL}	LOW-level output voltage	V_{CC} = 2.7 V; I_{OL} = 100 µA		–	0.1	0.2	V
		V_{CC} = 2.7 V; I_{OL} = 24 mA		–	0.3	0.5	V
		V_{CC} = 3.0 V; I_{OL} = 16 mA		–	0.25	0.4	V
		V_{CC} = 3.0 V; I_{OL} = 32 mA		–	0.3	0.5	V
		V_{CC} = 3.0 V; I_{OL} = 64 mA		–	0.4	0.55	V
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6 V; I_O = 1 mA; V_I = GND or V_{CC}		–	0.13	0.55	V
I_I	Input leakage current	V_{CC} = 0 V or 3.6 V; V_I = 5.5 V		–	1	10	µA
		V_{CC} = 3.6 V; V_I = V_{CC} or GND	Control pins	–	± 0.1	± 1	µA
		V_{CC} = 3.6 V; V_I = V_{CC}	Data pins[4]	–	0.1	1	µA
		V_{CC} = 3.6 V; V_I = 0 V		–	–1	–5	µA
I_{OFF}	Output off current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V		–	1	± 100	µA
I_{HOLD}	Bus Hold current A inputs[7]	V_{CC} = 3 V; V_I = 0.8 V		75	150	–	µA
		V_{CC} = 3 V; V_I = 2.0 V		–75	–150	–	µA
		V_{CC} = 0 V to 3.6 V; V_{CC} = 3.6 V		± 500	–	–	µA
I_{EX}	Current into an output in the HIGH state when $V_O > V_{CC}$	V_O = 5.5 V; V_{CC} = 3.0 V		–	60	125	µA
$I_{PU/PD}$	Power-up/down 3-State output current[3]	$V_{CC} \leq$ 1.2 V; V_O = 0.5 V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care		–	1	± 100	µA
I_{OZH}	3-State output HIGH current	V_{CC}= 3.6 V; V_O = 3 V; V_I = V_{IL} or V_{IH}		–	1	5	µA
I_{OZL}	3-State output LOW current	V_{CC}= 3.6 V; V_O = 0.5 V; V_I = V_{IL} or V_{IH}		–	1	–5	µA
I_{CCH}	Quiescent supply current[3]	V_{CC} = 3.6 V; Outputs HIGH; V_I = GND or V_{CC}; I_O = 0 mA		–	0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6 V; Outputs LOW, V_I = GND or V_{CC}; I_O = 0 mA		–	3	12	mA
I_{CCZ}		V_{CC} = 3.6 V; Outputs Disabled; V_I = GND or V_{CC}; I_O = 0 mA[6]		–	0.13	0.19	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3 V to 3.6 V; One input at V_{CC} – 0.6 V; Other inputs at V_{CC} or GND		–	0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
3. This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 msec. From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 µsec is permitted. This parameter is valid for T_{amb} = 25 °C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
6. I_{CCZ} is measured with outputs pulled to V_{CC} or down to GND.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0 V; $t_R = t_F$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω; T_{amb} = –40 °C to +85 °C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	TYP[1]	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	100	150	–	100	–	ns
t_{PLH} t_{PHL}	Propagation delay CP to Qn	1	1.7 2.2	3.0 3.5	4.6 4.9	– –	5.4 5.2	ns
t_{PZH} t_{PZL}	Output enable time to HIGH and LOW level	3 4	1.7 1.7	3.2 3.3	5.4 5.5	– –	7.0 5.6	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH and LOW level	3 4	2.1 2.1	3.5 3.4	4.8 4.8	– –	5.3 4.6	ns

NOTE:

1. All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

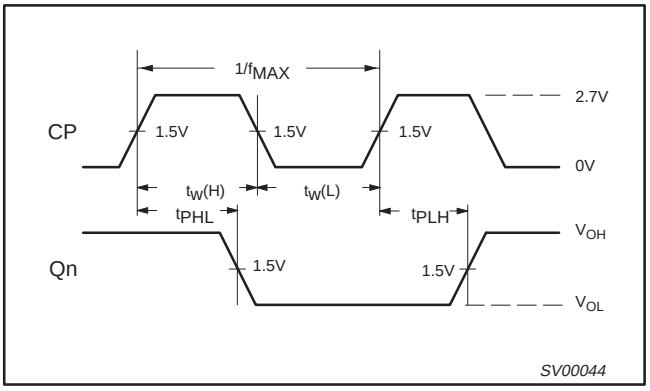
AC SETUP REQUIREMENTS

GND = 0 V; $t_R = t_F$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω; T_{amb} = –40 °C to +85 °C.

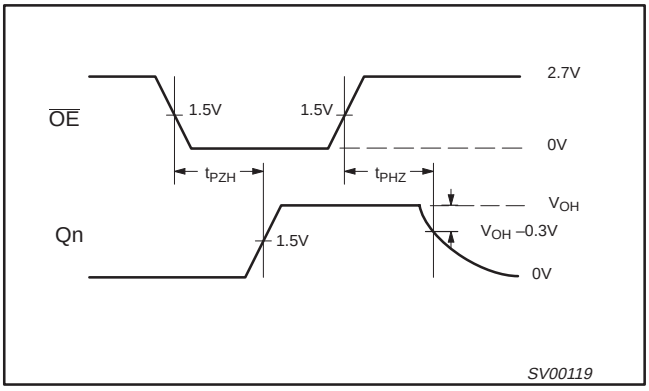
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V	
			MIN	TYP	MIN	
$t_S(H)$ $t_S(L)$	Setup time, HIGH or LOW, Dn to CP	2	2.0 2.6	1.0 1.3	2.0 3.2	ns
$t_H(H)$ $t_H(L)$	Hold time, HIGH or LOW, Dn to CP	2	0 0	–1.3 –0.9	0 0	ns
$t_W(H)$ $t_W(L)$	CP pulse width HIGH or LOW	1	1.5 4.2	0.8 3.0	1.5 5.0	ns

AC WAVEFORMS

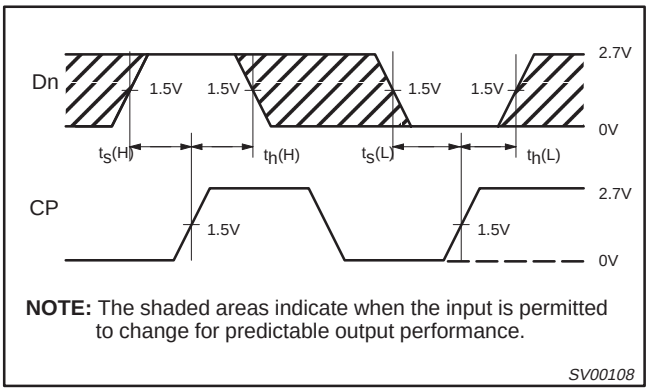
V_M = 1.5 V, V_{IN} = GND to 2.7 V



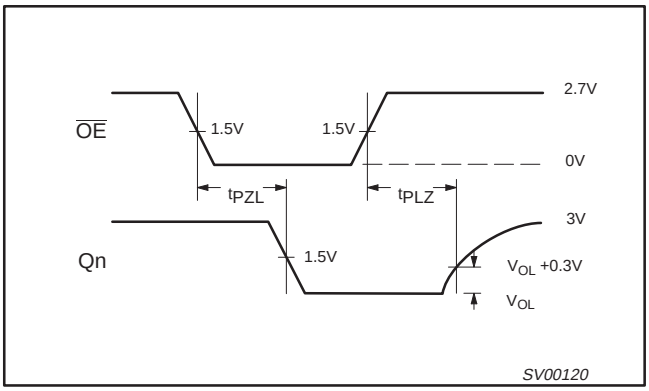
Waveform 1. Propagation delay, clock input to output, clock pulse width, and maximum clock frequency



Waveform 3. 3-State Output Enable time to HIGH level and Output Disable time from HIGH level

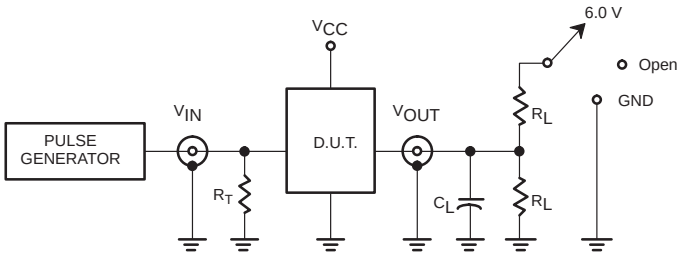


Waveform 2. Data setup and hold times

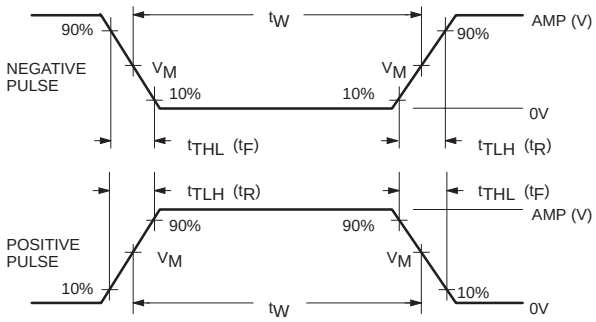


Waveform 4. 3-State Output Enable time to LOW level and Output Disable time from LOW level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5 V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

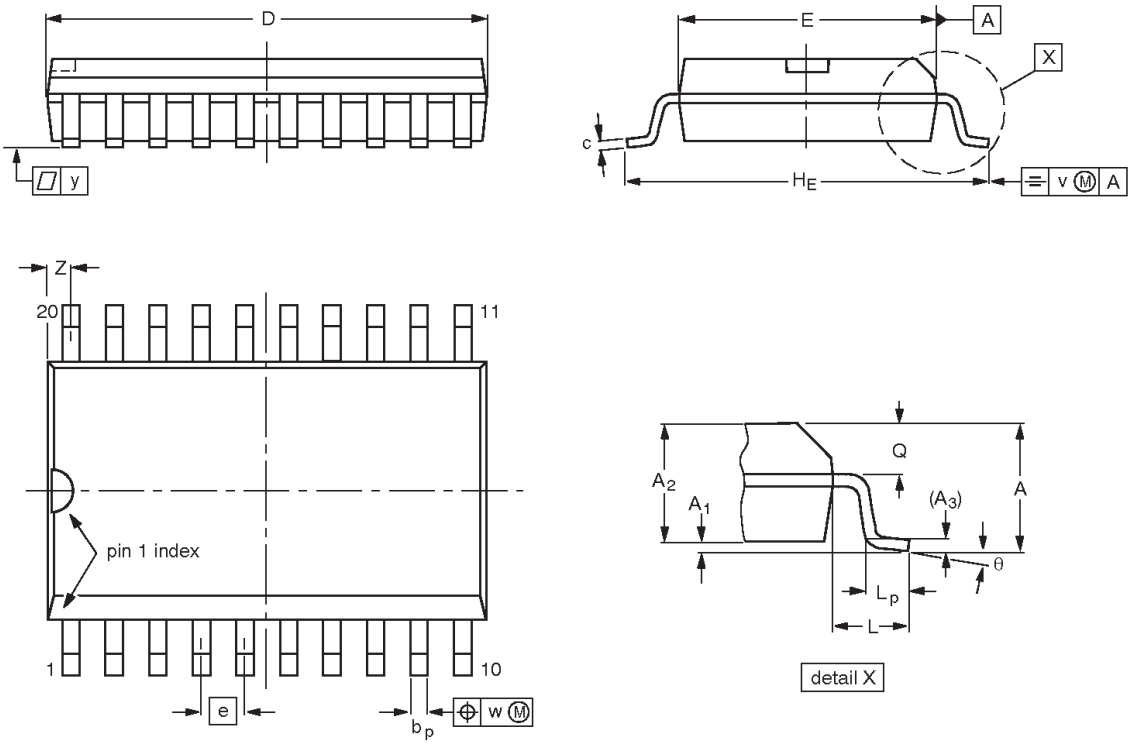
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	≤ 2.5 ns

SV00092

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

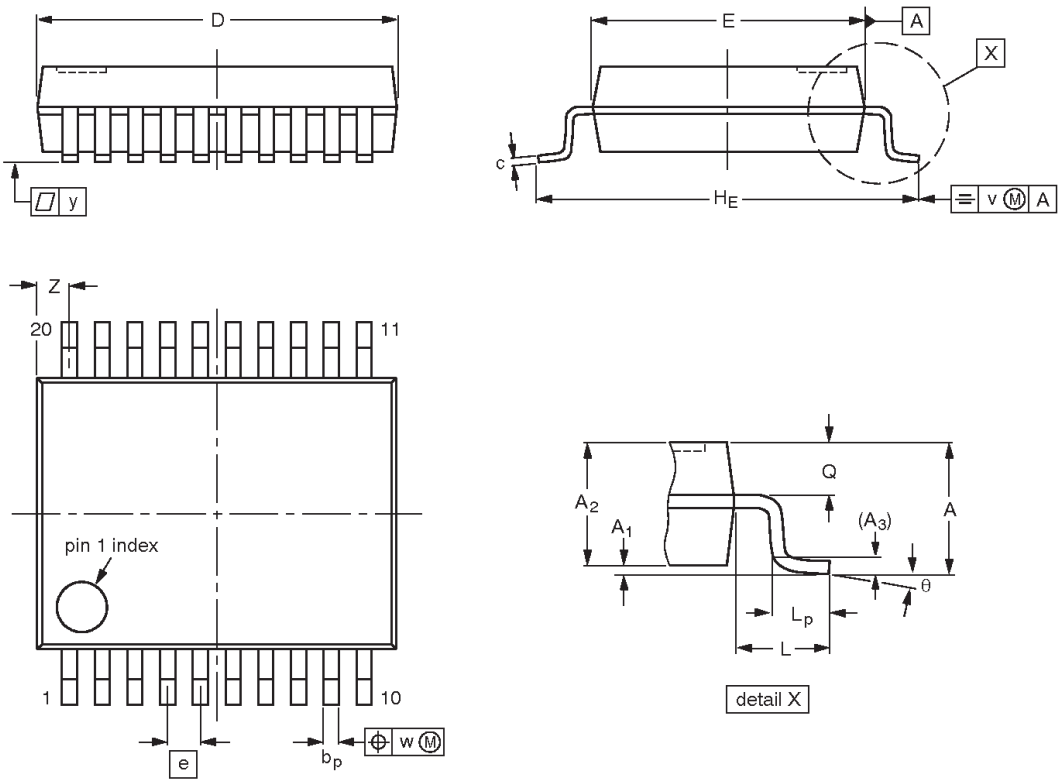
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

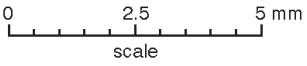
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**





DIMENSIONS (mm are the original dimensions)

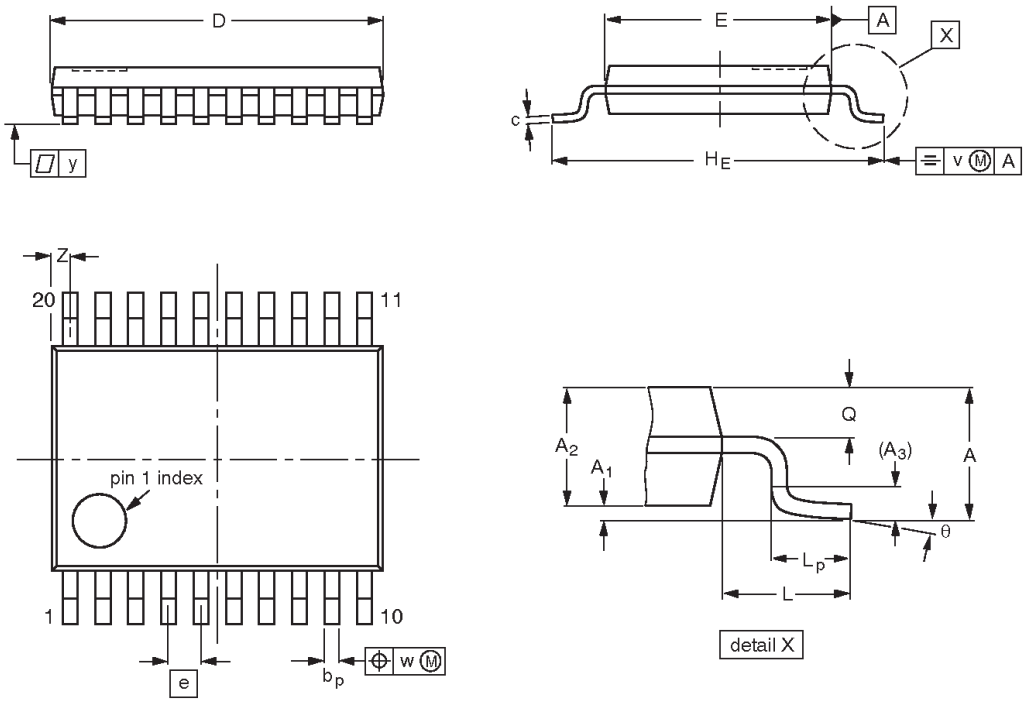
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8^o 0^o

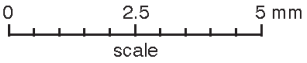
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				~~99-12-27~~ 03-02-19

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

REVISION HISTORY

Rev	Date	Description
_3	20040825	**Product data sheet (9397 750 14004). Supersedes Product specification of 1998 Feb 19 (9397 750 03536).** Modifications: ● Ordering information table on page 2: – remove ‘North America’ column – change column heading ‘Outside North America’ to ‘Type Number’ ● AC characteristics table on page 6: change Max. value of t_{PHZ} from ‘3.0 ns’ to ‘4.8 ns’
_2	19980219	**Product specification (9397 750 03536). ECN 853-1855 18988 of 19 February 1998. Supersedes data of 1996 Aug 13.**
_1	19960813	

3.3 V Octal D-type flip-flop, inverting (3-State) 74LVT534

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data sheet	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data sheet	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data sheet	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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