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September 2000
Revised May 2005

74LCXH162244
Low Voltage 16-Bit Buffer/Line Driver with Bushold and 26Ω Series Resistors in Outputs

General Description

The LCXH162244 contains sixteen non-inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

The LCXH162244 data inputs include active bushold circuitry, eliminating the need for external pull-up resistors to hold unused or floating data inputs at a valid logic level.

In addition, the outputs include equivalent 26Ω (nominal) series resistors to reduce overshoot and undershoot and are designed to sink/source up to 12 mA at V_{CC} = 3.0V.

The LCXH162244 is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCXH162244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

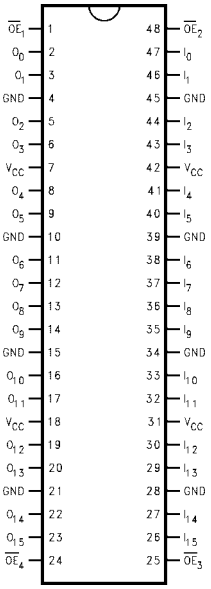
- 5V tolerant control inputs and outputs
- 2.3V–3.6V V_{CC} specifications provided
- Outputs include equivalent series resistance of 26Ω to make external termination resistors unnecessary and reduce overshoot and undershoot
- Bushold on data inputs eliminates the need for external pull-up/pull-down resistors
- 5.3 ns t_{PD} max (V_{CC} = 3.0V), 20 μA I_{CC} max
- Power down high impedance inputs and outputs
- ±12 mA output drive (V_{CC} = 3.0V)
- Implements proprietary noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V

Ordering Code:

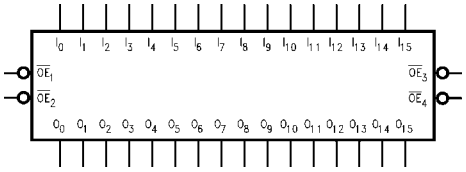
Order Number	Package Number	Package Description
74LCXH162244MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [RAIL]
74LCXH162244MEX	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [TAPE and REEL]
74LCXH162244MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [RAIL]
74LCXH162244MTX	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TAPE and REEL]

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Connection Diagram



Logic Symbol



Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
I_0–I_{15}	Bushold Inputs
O_0–O_{15}	Outputs

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_0–I_3	O_0–O_3
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I_8–I_{11}	O_8–O_{11}
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_4–I_7	O_4–O_7
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	I_{12}–I_{15}	O_{12}–O_{15}
L	L	L
L	H	H
H	X	Z

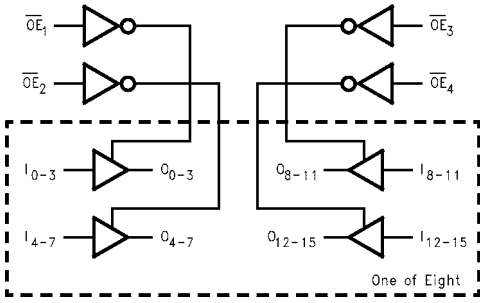
H = HIGH Voltage Level
L = LOW Voltage Level

X = Immaterial
Z = High Impedance

Functional Description

The LCXH162244 contains sixteen non-inverting buffers with 3-STATE standard outputs. The LCXH162244 data inputs include active bushold circuitry eliminating the need for pull-up resistors to hold unused or floating data inputs at a valid logic level. The devise is also designed with 26Ω series resistors in the outputs. This design reduces line noise in applications such as memory address drivers, clock drivers and bus transceiver/transmitters. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. The 3-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input for each nibble. When $\overline{OE}_n$ is LOW, the outputs are in 2-state mode. When $\overline{OE}_n$ is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Logic Diagram



Absolute Maximum Ratings(Note 1)

Symbol	Parameter		Value	Conditions	Units
V_{CC}	Supply Voltage		−0.5 to +7.0		V
V_I	DC Input Voltage	$\overline{OE}$	−0.5 to +7.0		V
		I_0 - I_{15}	−0.5 to V_{CC} + 0.5		
V_O	DC Output Voltage		−0.5 to +7.0	Output in 3-STATE	V
			−0.5 to V_{CC} + 0.5	Output in HIGH or LOW State (Note 2)	
I_{IK}	DC Input Diode Current		−50	V_I < GND	mA
I_{OK}	DC Output Diode Current		−50	V_O < GND	mA
			+50	V_O > V_{CC}	
I_O	DC Output Source/Sink Current		±50		mA
I_{CC}	DC Supply Current per Supply Pin		±100		mA
I_{GND}	DC Ground Current per Ground Pin		±100		mA
T_{STG}	Storage Temperature		−65 to +150		°C

Recommended Operating Conditions (Note 3)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	V_{CC}	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		3-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V – 3.6V		±12	mA
		V_{CC} = 2.7V – 3.0V		±8	
		V_{CC} = 2.3V – 2.7V		±4	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC}	T_A = −40°C to +85°C		Units
			(V)	Min	Max	
V_{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		
V_{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.3 – 3.6	V_{CC} – 0.2		V
		I_{OH} = −4 mA	2.3	1.8		
		I_{OH} = −4 mA	2.7	2.2		
		I_{OH} = −6 mA	3.0	2.4		
		I_{OH} = −8 mA	2.7	2.0		
		I_{OH} = −12 mA	3.0	2.0		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.3 – 3.6		0.2	V
		I_{OL} = 4 mA	2.3		0.6	
		I_{OL} = 4 mA	2.7		0.4	
		I_{OL} = 6 mA	3.0		0.55	
		I_{OL} = 8 mA	2.7		0.6	
		I_{OL} = 12 mA	3.0		0.8	

DC Electrical Characteristics (Continued)

Symbol	Parameter		Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units
					Min	Max	
I_I	Input Leakage Current	Data	$V_I = V_{CC}$ or GND	2.3 – 3.6		±5.0	μA
		Control	$0 \le V_I \le 5.5$	2.3 – 3.6		±5.0	
$I_{I(HOLD)}$	Bushold Input Minimum Drive Hold Current		$V_{IN} = 0.7V$	2.3	45		μA
			$V_{IN} = 1.7V$		−45		
			$V_{IN} = 0.8V$	3.0	75		
			$V_{IN} = 2.0V$		−75		
$I_{I(OD)}$	Bushold Input Over-Drive Current to Change State		(Note 4)	2.7	300		μA
			(Note 5)		−300		
			(Note 4)	3.6	450		
			(Note 5)		−450		
I_{OZ}	3-STATE Output Leakage		$0 \le V_O \le 5.5V$ $V_I = V_{IH}$ or V_{IL}	2.3 – 3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current		$V_O = 5.5V$	0		10	μA
I_{CC}	Quiescent Supply Current		$V_I = V_{CC}$ or GND	2.3 – 3.6		20	μA
ΔI_{CC}	Increase in I_{CC} per Input		$V_{IH} = V_{CC} - 0.6V$	2.3 – 3.6		500	μA

Note 4: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 5: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $R_L = 500\ \Omega$						Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5V \pm 0.2V$		
		$C_L = 50$ pF		$C_L = 50$ pF		$C_L = 30$ pF		
		Min	Max	Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.0	5.3	1.0	6.0	1.0	6.4	ns
t_{PLH}	Data to Output	1.0	5.3	1.0	6.0	1.0	6.4	
t_{PZL}	Output Enable Time	1.0	6.3	1.0	7.1	1.0	8.2	ns
t_{PZH}		1.0	6.3	1.0	7.1	1.0	8.2	
t_{PLZ}	Output Disable Time	1.0	5.4	1.0	5.7	1.0	6.5	ns
t_{PHZ}		1.0	5.4	1.0	5.7	1.0	6.5	
t_{OSHL}	Output to Output Skew (Note 6)		1.0					ns
t_{OSLH}			1.0					

Note 6: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.35	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	0.25	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	−0.35	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	−0.25	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, f = 10 MHz	20	pF

AC LOADING and WAVEFORMS Generic for LCX Family

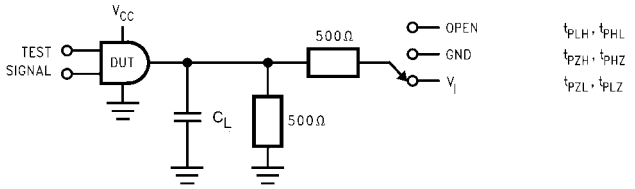
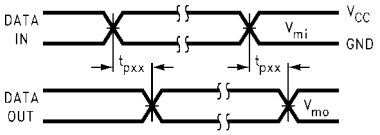
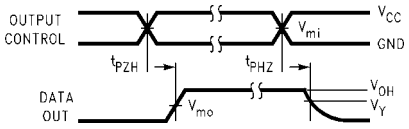


FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

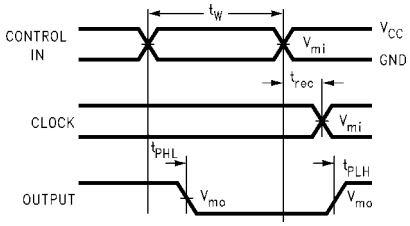
V_I	C_L
6V for V_{CC} = 3.3V, 2.7V	50 pF
V_{CC} * 2 for V_{CC} = 2.5V	30 pF



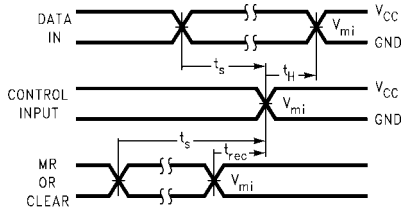
Waveform for Inverting and Non-Inverting Functions



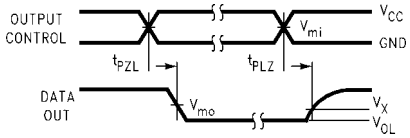
3-STATE Output High Enable and Disable Times for Logic



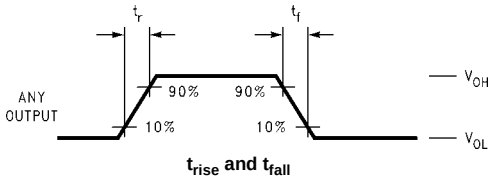
Propagation Delay. Pulse Width and t_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

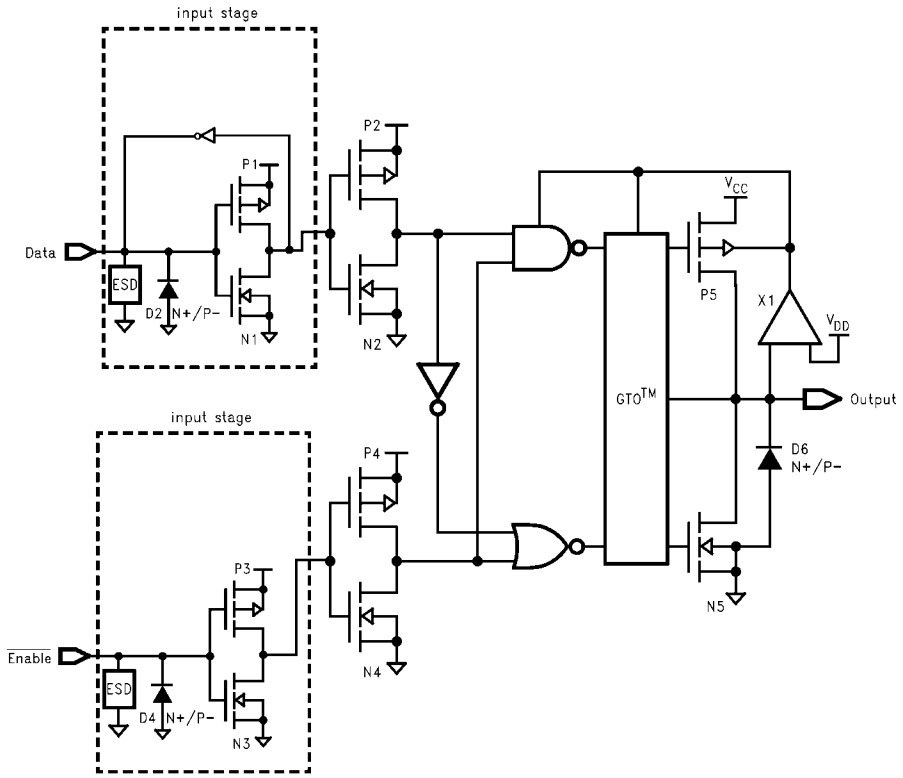


t_{rise} and t_{fall}

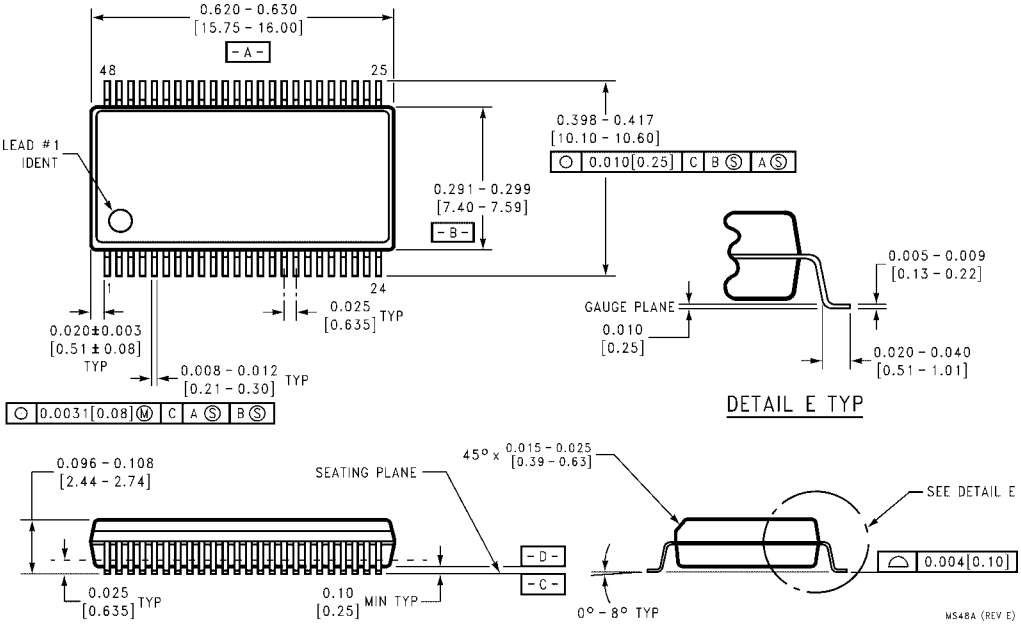
FIGURE 2. Waveforms
(Input Characteristics; f =1MHz, t_R = t_F = 3ns)

Symbol	V_{CC}		
	3.3V ± 0.3V	2.7V	2.5V ± 0.2V
V_{mi}	1.5V	1.5V	V_{CC}/2
V_{mo}	1.5V	1.5V	V_{CC}/2
V_x	V_{OL} + 0.3V	V_{OL} + 0.3V	V_{OL} + 0.15V
V_y	V_{OH} − 0.3V	V_{OH} − 0.3V	V_{OH} − 0.15V

Schematic Diagram Generic for LCXH Family

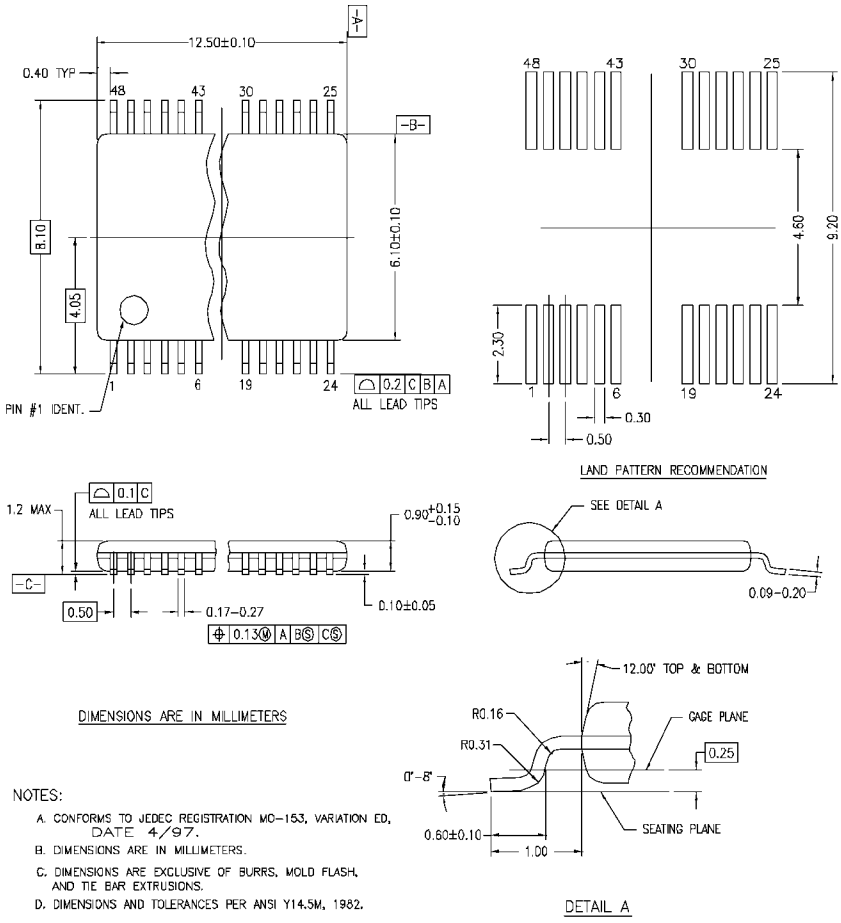


Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

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