RoHS Compliant

2GB ECC DDR3 1.35V SO-DIMM

Product Specifications

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Version 1.1

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General Description

Apacer **78.A2GD2.4010C** is a 256M x 72 DDR3 SDRAM (Synchronous DRAM) ECC SO-DIMM. This high-density memory module consists of 9 pieces 256M x 8 bits with 8 banks DDR3 synchronous DRAMs in BGA packages and a 2K EEPROM. The module is a 204-pins small-outlined, dual in-line memory module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR3 SDRAM. The following provides general specifications of this module.

Ordering Information

Part Number	Bandwidth	Speed Grade	Max Frequency	CAS Latency
78.A2GD2.4010C	10.6 GB/sec	1333 Mbps	666 MHz	CL9

Density	Organization	Component	Rank
2GB	256M x 72	256M x8*9	1

Key Parameters

MT/s	DDR3-1066	DDR3-1333	DDR3-1600	Unit
Grade	-CL7	-CL9	-CL11	
tCK (min)	1.875	1.5	1.25	ns
CAS latency	7	9	11	tCK
tRCD (min)	13.125	13.5	13.75	ns
tRP (min)	13.125	13.5	13.75	ns
tRAS (min)	37.5	36	35	ns
tRC (min)	50.625	49.5	48.75	ns
CL-tRCD-tRP	7-7-7	9-9-9	11-11-11	tCK

Specifications:

- Support ECC error detection and correction
- On-DIMM thermal sensor : Yes
- Organization: 256 words x 72 bits, 1 rank
- Integrating 9 pieces of 2G bits DDR3 SDRAM sealed FBGA
- Package: 204-pin socket type small outline dual in-line memory module (ECC SO-DIMM)
- PCB: height 30.0 mm, lead pitch 0.6 mm (pin), lead-free (RoHS compliant)
- Power supply VDD: 1.35V (+0.1V ~ -0.067V)
- Serial Presence Detect (SPD)
- Eight Internal banks for concurrent operation (Components)
- Interface: SSTL_13
- Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- /CAS Latency (CL): 6, 7, 8, 9
- /CAS Write Latency (CWL): 5, 6, 7
- Supports auto pre-charge option for each burst access
- Supports auto-refresh/self-refresh
- Refresh cycles: 7.8 μs at 0℃ ≦ TC ≦ +85℃
- PCB: 30µ gold finger

Features:

- Double-date-rate architecture: 2 data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted / received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Data mask (DM) for writing data
- Posted /CAS by programmable additive latency for enhanced command and data bus efficiency
- On-Die-Termination (ODT) for improved signal quality: Synchronous ODT/Dynamic ODT/Asynchronous ODT
- Multi-Purpose Register (MPR) for temperature read out
- ZQ calibration for DQ drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- /Reset pin for power-up sequence and reset function
- SRT range: normal/extended, auto/manual self-refresh
- Programmable output driver impedance control
- Commands entered at each positive clock input, while data and data mask are referenced to both edges of DQS

Pin Assignments

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VREFDQ	53	VSS	105	A1	157	DM5
3	VSS	55	DQ24	107	A0	159	DQ42
5	DQ0	57	DQ25	109	VDD	161	DQ43
7	DQ1	59	DM3	111	CK0	163	VSS
9	VSS	61	VSS	113	/CK0	165	DQ48
11	DM0	63	DQ26	115	VDD	167	DQ49
13	DQ2	65	DQ27	117	A10(/AP)	169	VSS
15	DQ3	67	VSS	119	BA0	171	/DQS6
17	VSS	69	CB0	121	/WE	173	DQS6
19	DQ8	71	CB1	123	VDD	175	VSS
21	DQ9	73	VSS	125	/CAS	177	DQ50
23	VSS	75	/DQS8	127	/CS0	179	DQ51
25	/DQS1	77	DQS8	129	/CS1	181	VSS
27	DQS1	79	VSS	131	VDD	183	DQ56
29	VSS	81	CB2	133	DQ32	185	DQ57
31	DQ10	83	CB3	135	DQ33	187	VSS
33	DQ11	85	VDD	137	VSS	189	DM7
35	VSS	87	CKE0	139	/DQS4	191	DQ58
37	DQ16	89	CKE1	141	DQS4	193	DQ59
39	DQ17	91	BA2	143	VSS	195	VSS
41	VSS	93	VDD	145	DQ34	197	SA0
43	/DQS2	95	A12(/BC)	147	DQ35	199	VDDSPD
45	DQS2	97	A8	149	VSS	201	SA1
47	VSS	99	A5	151	DQ40	203	VTT
49	DQ18	101	VDD	153	DQ41		
51	DQ19	103	A3	155	VSS		

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
2	VSS	54	DQ28	106	A2	158	VSS
4	DQ4	56	DQ29	108	BA1	160	DQ46
6	DQ5	58	VSS	110	VDD	162	DQ47
8	VSS	60	/DQS3	112	CK1	164	VSS
10	/DQS0	62	DQS3	114	/CK1	166	DQ52
12	DQS0	64	VSS	116	VDD	168	DQ53
14	VSS	66	DQ30	118	NC(/CS3)	170	VSS
16	DQ6	68	DQ31	120	NC(/CS2)	172	DM6
18	DQ7	70	VSS	122	/RAS	174	DQ54
20	VSS	72	CB4	124	VDD	176	DQ55
22	DQ12	74	CB5	126	ODT0	178	VSS
24	DQ13	76	DM8	128	ODT1	180	DQ60
26	VSS	78	VSS	130	A13	182	DQ61
28	DM1	80	CB6	132	VDD	184	VSS
30	/RESET	82	CB7	134	DQ36	186	/DQS7
32	VSS	84	VREFCA	136	DQ37	188	DQS7
34	DQ14	86	VDD	138	VSS	190	VSS
36	DQ15	88	A15(NC)	140	DM4	192	DQ62
38	VSS	90	A14(NC)	142	DQ38	194	DQ63
40	DQ20	92	A9	144	DQ39	196	VSS
42	DQ21	94	VDD	146	VSS	198	/EVENT*
44	DM2	96	A11	148	DQ44	200	SDA
46	VSS	98	A7	150	DQ45	202	SCL
48	DQ22	100	A6	152	VSS	204	VTT
50	DQ23	102	VDD	154	/DQS5		
52	VSS	104	A4	156	DQS5		

Notes:

1. /CS1, ODT1, CKE1: Used for dual-rank UDIMMs; NC on single-rank UDIMMs.
2. CK1, NC and /CK1, NC : Used for dual-rank UDIMMs; not used on single-rank UDIMMs, but terminated.

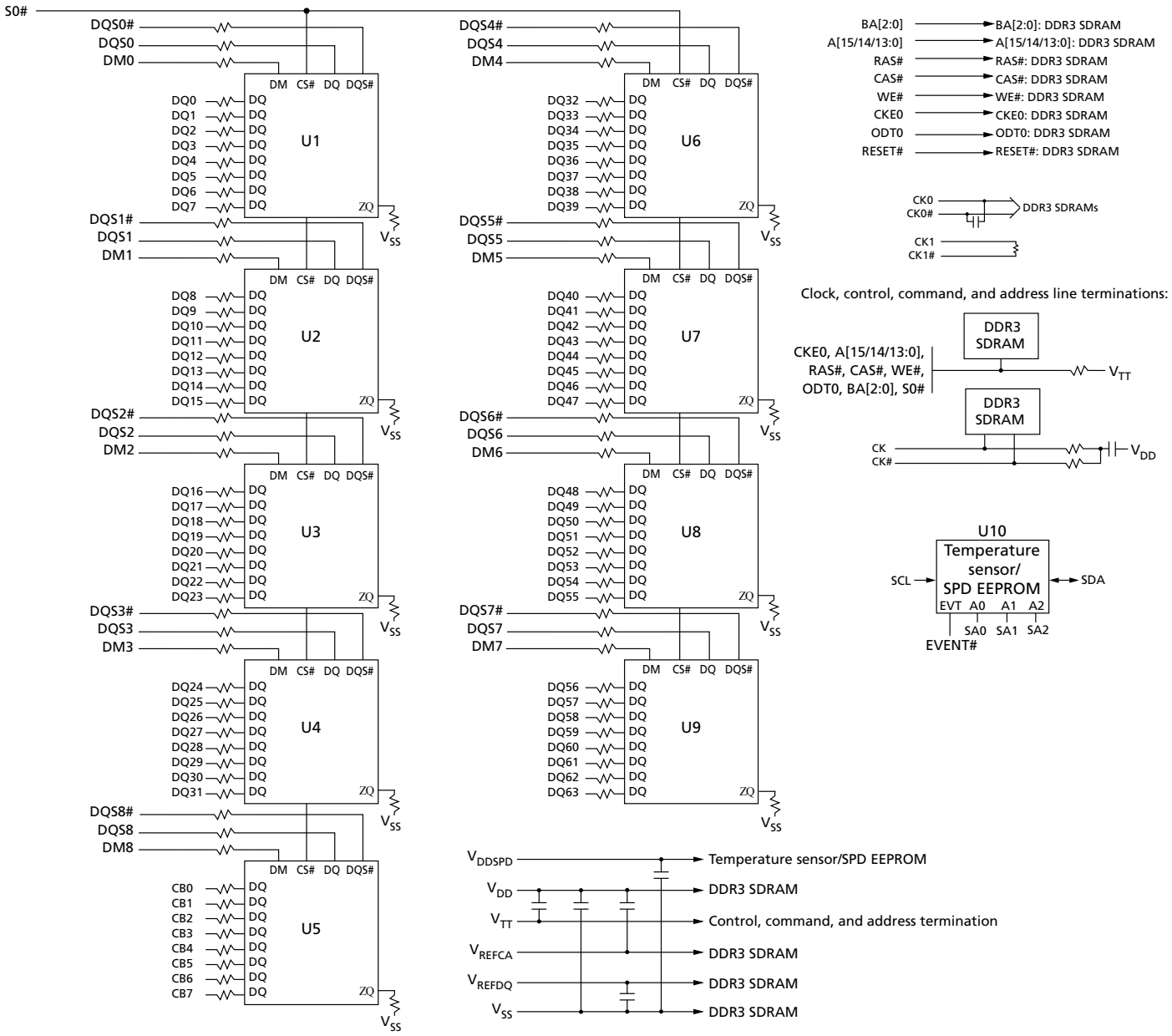
Pin Descriptions

Pin Name	Description
Ax*	SDRAM address bus
BAx	SDRAM bank select
DQx	DIMM memory data bus
CBx	DIMM ECC check bits
/RAS	SDRAM row address strobe
/CAS	SDRAM column address strobe
/WE	SDRAM write enable
/CSx	SDRAM Chip select lines
CKEx	SDRAM clock enable lines
CKx	SDRAM clock input
/CKx	SDRAM Differential clock input
DQSx	SDRAM data strobes(positive line of differential pair)
/DQSx	SDRAM data strobes(negative line of differential pair)
DMx	SDRAM input mask
SCL	Clock input for serial PD
SDA	Data input/output for serial PD
SAx	Serial address input
VDD	Power for internal circuit
VDDSPD	Serial EEPROM positive power supply
VREFDQ	SDRAM I/O reference supply
VREFCA	SDRAM command/address reference supply
VSS	Power supply return(ground)
VTT	SDRAM I/O termination supply
/RESET	Set DRAM to known state
ODTx	On-die termination control lines
/EVENT	An output of the thermal sensor to indicate critical module temperature
NC	Spare pins(no connect)

*IC Component Composition:

128Mx8	A0~A13
256Mx8	A0~A14
512Mx8	A0~A15
1024Mx8	A0~A15

Functional Block Diagram



Note: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

Absolute Maximum Ratings

Parameter	Symbol	Description	Units
Voltage on VDD pin relative to Vss	V_{DD}	- 0.4 V ~ 1.975 V	V
Voltage on VDDQ pin relative to Vss	V_{DDQ}	- 0.4 V ~ 1.975 V	V
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	- 0.4 V ~ 1.975 V	V
Storage Temperature	TSTG	-55 to +100	℃

Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6 x VDDQ, when VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

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DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
TOPER	Normal Operating Temperature Range	0 to 85	℃	1,2
	Extended Temperature Range	85 to 95	℃	1,3

Notes:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported during operation, the DRAM case temperature must be maintained between 0℃ - 85℃ under all operating Conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85℃ and 95℃ case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs.
   b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b), in this case IDD6 current can be increased around 10~20% than normal Temperature range.

Operating Conditions

Recommended DC Operating Conditions - DDR3L (1.35V) operation

Symbol	Parameter	Rating			Units
		Min.	Typ.	Max.	
VDD	Supply Voltage	1.283	1.35	1.45	V
VDDQ	Supply Voltage for Output	1.283	1.35	1.45	V

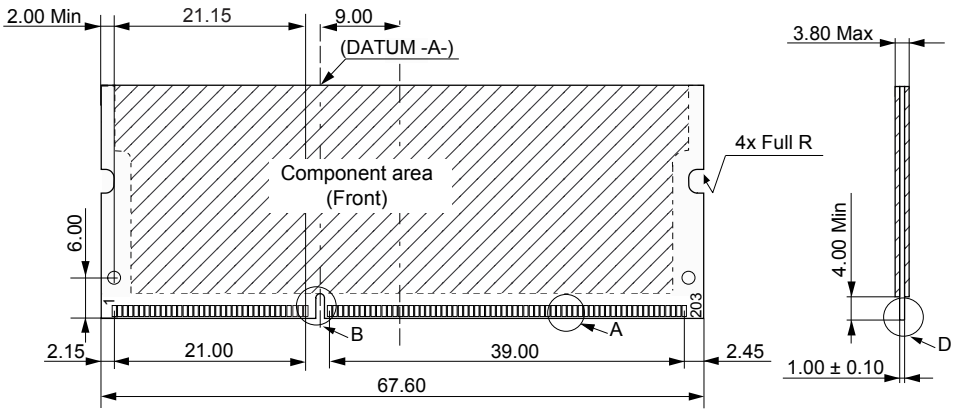
Notes:

1. If minimum limit is exceeded, input levels shall be governed by DDR3L specifications.
2. Under 1.5V operation, this DDR3L device operates to the DDR3 specifications under the same speed timings as defined for this device.
3. Once initialized for DDR3 operation, DDR3L operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3L operation.

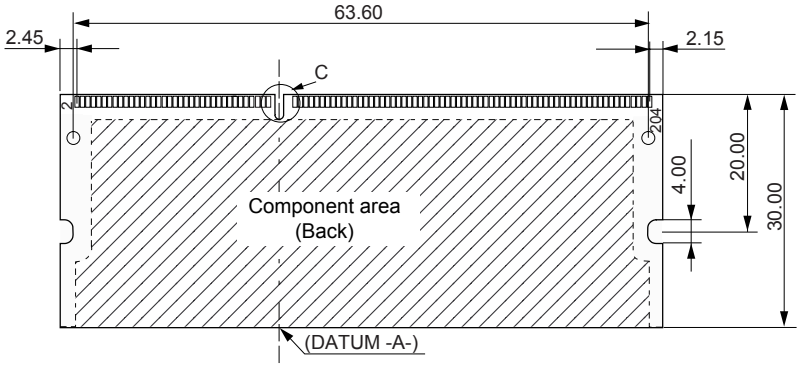
Mechanical Drawing

Unit: mm

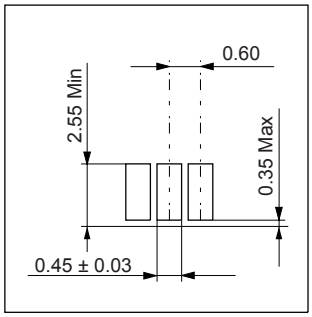
Front side



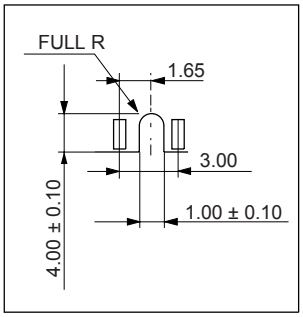
Back side



Detail A

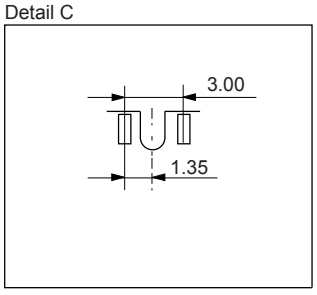


Detail B

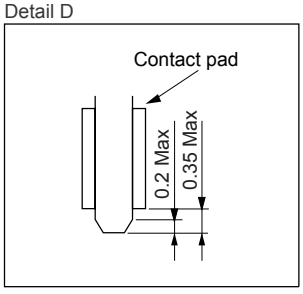


30µ gold finger

Detail C



Detail D



(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)

Revision History

Revision	Date	Description	Remark
0.9	08/28/2012	Official release	
1.0	08/29/2012	release	
1.1	07/23/2013	1. Changed headquarters address 2. Added 30µ gold finger	

Global Presence

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