Ultralow Noise EMC 36V_{IN}, 3A DC/DC µModule Regulator

FEATURES

- **Complete Step-Down Switch Mode Power Supply**
- **Wide Input Voltage Range: 3.6V to 36V**
- **3A Output Current**
- **0.8V to 24V Output Voltage**
- **EN55022 Class B Compliant**
- Current Share Multiple LTM8033 Regulators for More Than 3A Output
- Selectable Switching Frequency: 200kHz to 2.4MHz
- Current Mode Control
- SnPb or RoHS Compliant Finish
- Programmable Soft-Start
- Compact Package (11.25mm × 15mm × 4.32mm) Surface Mount LGA and (11.25mm × 15mm × 4.92mm) BGA Packages

APPLICATIONS

- Automotive Battery Regulation
- Power for Portable Products
- Distributed Supply Regulation
- Industrial Supplies
- Wall Transformer Regulation

DESCRIPTION

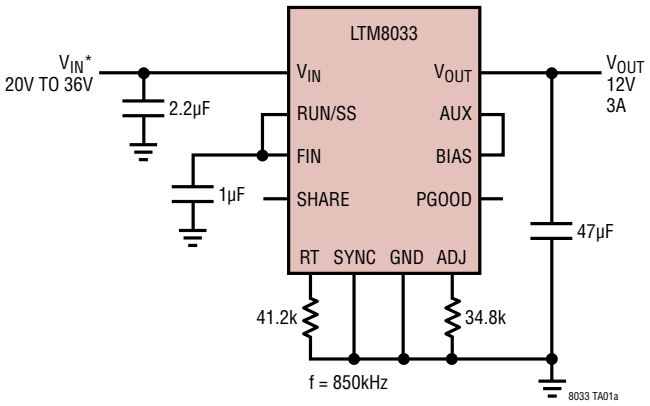
The LTM®8033 is an electromagnetic compatible (EMC) 36V, 3A DC/DC µModule® buck converter designed to meet the radiated emissions requirements of EN55022. Conducted emission requirements can be met by adding standard filter components. Included in the package are the switching controller, power switches, inductor, filters and all support components. Operating over an input voltage range of 3.6V to 36V, the LTM8033 supports an output voltage range of 0.8V to 24V, and a switching frequency range of 200kHz to 2.4MHz, each set by a single resistor. Only the bulk input and output filter capacitors are needed to finish the design.

The LTM8033 is packaged in a compact (11.25mm × 15mm × 4.32mm) overmolded land grid array (LGA) and ball grid array (BGA) package suitable for automated assembly by standard surface mount equipment. The LTM8033 is available with SnPb (BGA) or RoHS compliant terminal finish.

LT, LTC, LTM, Linear Technology, the Linear logo, µModule and Burst Mode are registered trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners.

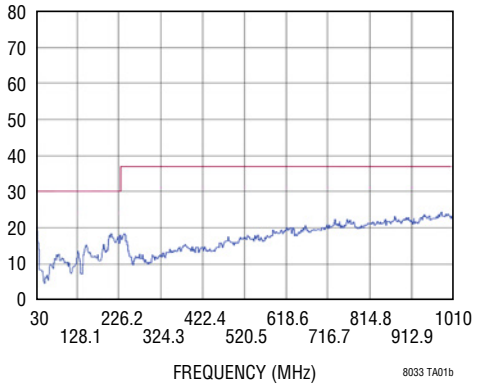
TYPICAL APPLICATION

Ultralow Noise 12V/3A DC/DC µModule Regulator



* RUNNING VOLTAGE RANGE. PLEASE REFER TO THE APPLICATIONS INFORMATION SECTION FOR START-UP DETAILS.

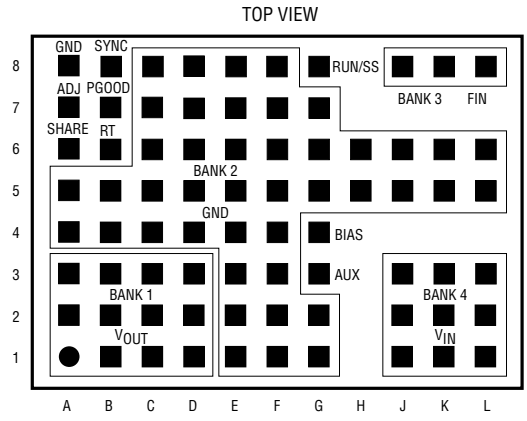
EMI Performance



ABSOLUTE MAXIMUM RATINGS (Note 1)

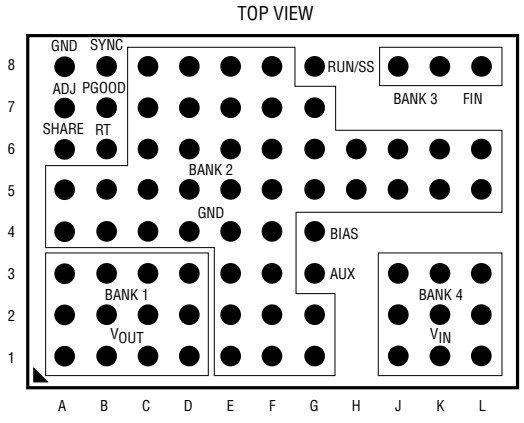
V_{IN}, FIN, RUN/SS Voltage 36V
ADJ, RT, SHARE Voltage 6V
V_{OUT}, AUX 25V
PGOOD, SYNC 30V
BIAS 25V
Maximum Junction Temperature (Note 2) ..... 125°C
Solder Temperature ..... 245°C

PIN CONFIGURATION



LGA PACKAGE
76-LEAD (15mm × 11.25mm × 4.32mm)

T_{JMAX} = 125°C, θ_{JA} = 15.4°C/W, $\theta_{JCbottom}$ = 5.2°C/W, θ_{JB} = 9.8°C/W, θ_{JCtop} = 16.7°C/W
θ VALUES DERIVED FROM A 4 LAYER 6.35cm × 6.35cm PCB
WEIGHT = 2.2g



BGA PACKAGE
76-LEAD (15mm × 11.25mm × 4.92mm)

T_{JMAX} = 125°C, θ_{JA} = 15.4°C/W, $\theta_{JCbottom}$ = 5.2°C/W, θ_{JB} = 9.8°C/W, θ_{JCtop} = 16.7°C/W
θ VALUES DERIVED FROM A 4 LAYER 6.35cm × 6.35cm PCB
WEIGHT = 2.2g

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (Note 2)
		DEVICE	FINISH CODE			
LTM8033EV#PBF	Au (RoHS)	LTM8033V	e4	LGA	3	–40°C to 125°C
LTM8033IV#PBF	Au (RoHS)	LTM8033V	e4	LGA	3	–40°C to 125°C
LTM8033MPV#PBF	Au (RoHS)	LTM8033V	e4	LGA	3	–55°C to 125°C
LTM8033EY#PBF	SAC305 (RoHS)	LTM8033Y	e1	BGA	3	–40°C to 125°C
LTM8033IY#PBF	SAC305 (RoHS)	LTM8033Y	e1	BGA	3	–40°C to 125°C
LTM8033IY	SnPb (63/67)	LTM8033Y	e0	BGA	3	–40°C to 125°C
LTM8033MPY#PBF	SAC305 (RoHS)	LTM8033Y	e1	BGA	3	–55°C to 125°C
LTM8033MPY	SnPb (63/67)	LTM8033Y	e0	BGA	3	–55°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Terminal Finish Part Marking:
  www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures:
  www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings:
  www.linear.com/packaging

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, RUN/SS = 12V unless otherwise noted (Note 2).

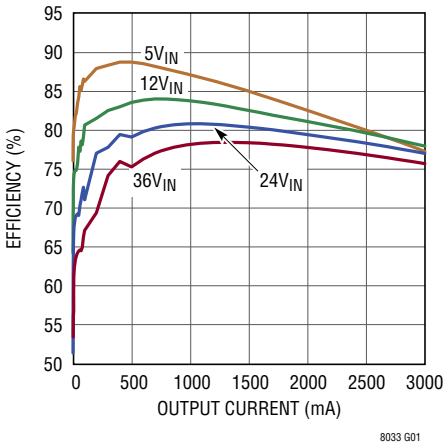
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage		●			3.6	V
Output DC Voltage	0A < I_{OUT} < 3A, R_{ADJ} Open, V_{IN} = 24V 0A < I_{OUT} < 3A, R_{ADJ} = 16.5k, V_{IN} = 32V			0.8 24		V V
Output DC Current	V_{IN} = 24V		0		3	A
Quiescent Current into V_{IN}	RUN/SS = 0.2V Not Switching BIAS = 0V, Not Switching			0.01 30 100	1 60 150	µA µA µA
Quiescent Current into BIAS	RUN/SS = 0.2V Not Switching BIAS = 0V, Not Switching			0.01 75 0	0.5 120 5	µA µA µA
Line Regulation	5.5V < V_{IN} < 36V			0.3		%
Load Regulation	0A < I_{OUT} < 3A, V_{IN} = 24V			0.4		%
Output RMS Voltage Ripple	V_{IN} = 24V, 0A < I_{OUT} < 3A			5		mV
Switching Frequency	R_T = 45.3k			780		kHz
Voltage at ADJ Pin		●	775	790	805	mV
Current Out of ADJ Pin	ADJ = 1V, V_{OUT} = 0V			2		µA
Minimum BIAS Voltage for Proper Operation				2	2.8	V
RUN/SS Pin Current	RUN/SS = 2.5V			5	10	µA
RUN/SS Input High Voltage			2.5			V
RUN/SS Input Low Voltage					0.2	V
PGOOD Threshold (at ADJ)	V_{OUT} Rising			730		mV
PGOOD Leakage Current	PGOOD = 30V, RUN/SS = 0V			0.1	1	µA
PGOOD Sink Current	PGOOD = 0.4V		200	735		µA
SYNC Input Low Threshold	f_{SYNC} = 550kHz		0.5			V
SYNC Input High Threshold	f_{SYNC} = 550kHz				0.7	V
SYNC Bias Current	SYNC = 0V			0.1		µA
500kHz Narrowband Conducted Emissions	24V_{IN}, 3.3V_{OUT}, I_{OUT} = 3A, 5µH LISN			89		dBµV
1MHz Narrowband Conducted Emissions				69		dBµV
3MHz Narrowband Conducted Emissions				51		dBµV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

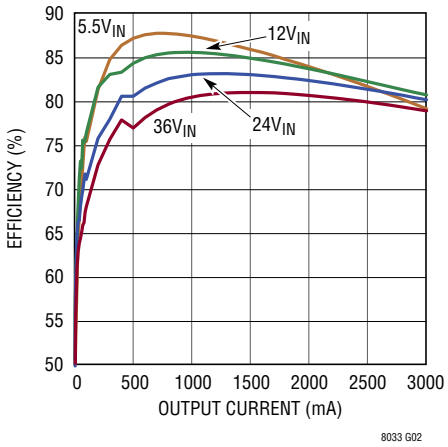
Note 2: The LTM8033E is guaranteed to meet performance specifications from 0°C to 125°C internal. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM8033I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. The LTM8033MP is guaranteed to meet specifications over the full –55°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

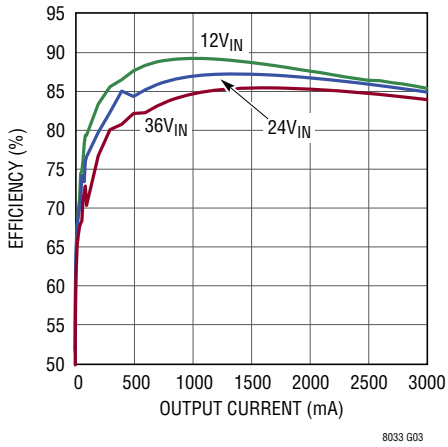
2.5V_{OUT} Efficiency



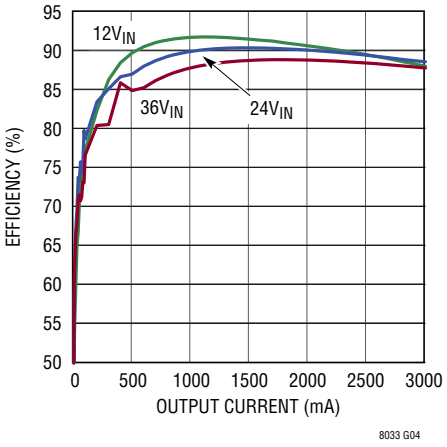
3.3V_{OUT} Efficiency



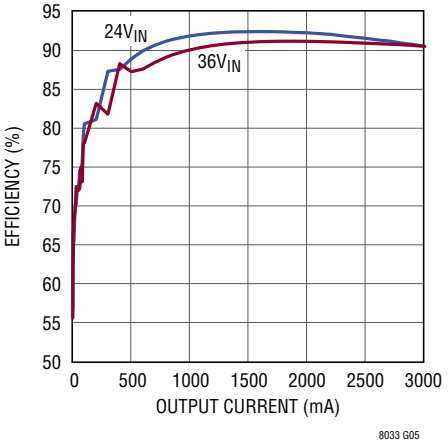
5V_{OUT} Efficiency



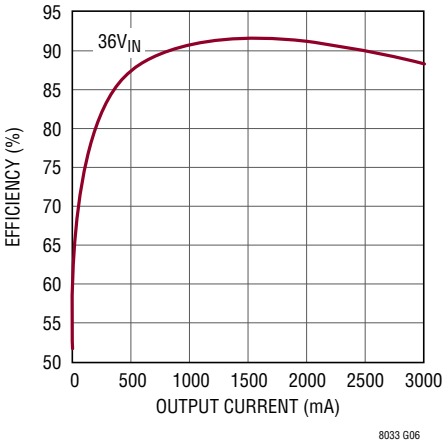
8V_{OUT} Efficiency



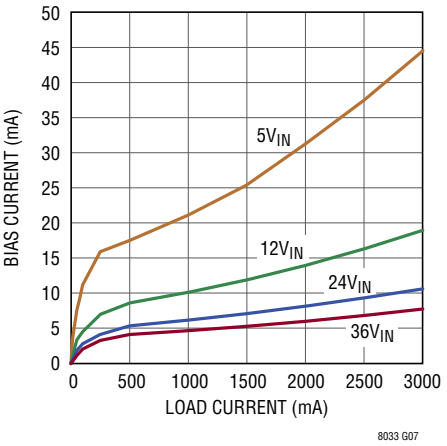
12V_{OUT} Efficiency



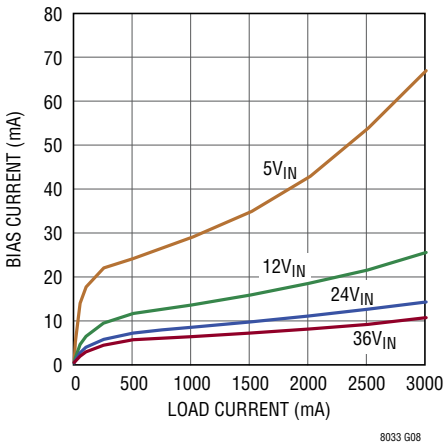
18V_{OUT} Efficiency



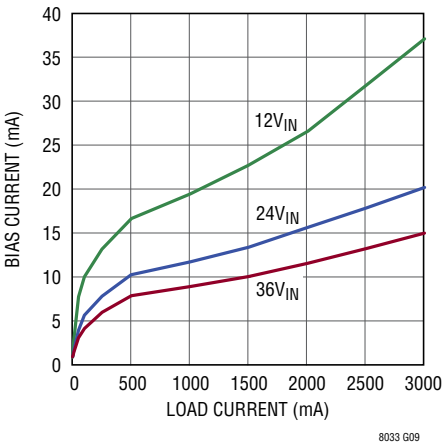
Bias Current vs Load Current, 2.5V_{OUT}



Bias Current vs Load Current, 3.3V_{OUT}

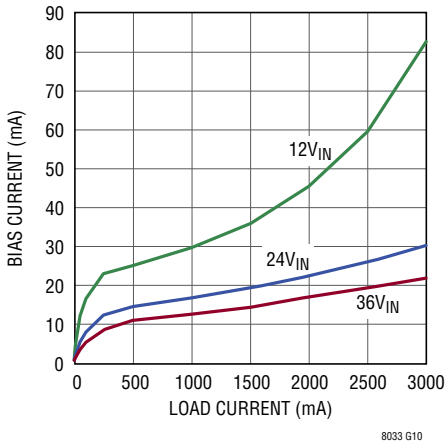


Bias Current vs Load Current, 5V_{OUT}

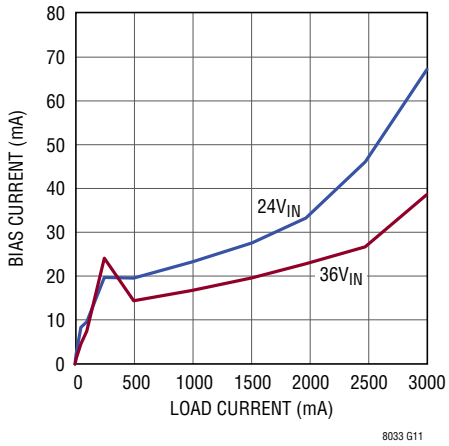


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

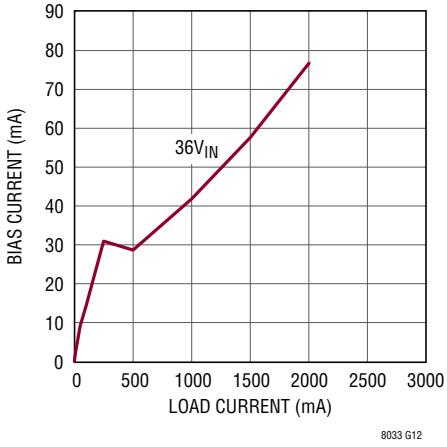
Bias Current vs Load Current, $8V_{OUT}$



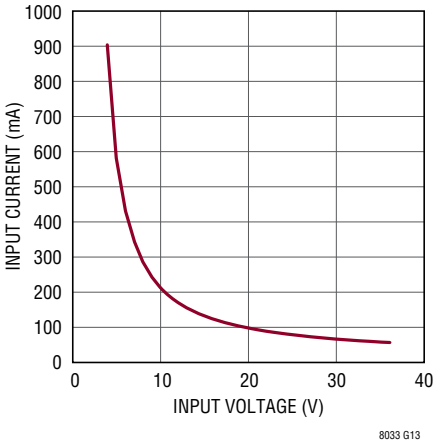
Bias Current vs Load Current, $12V_{OUT}$



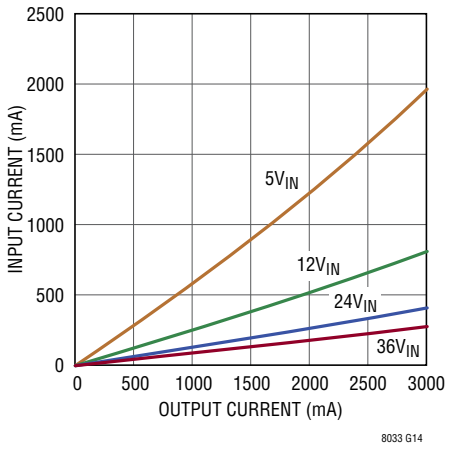
Bias Current vs Load Current, $18V_{OUT}$



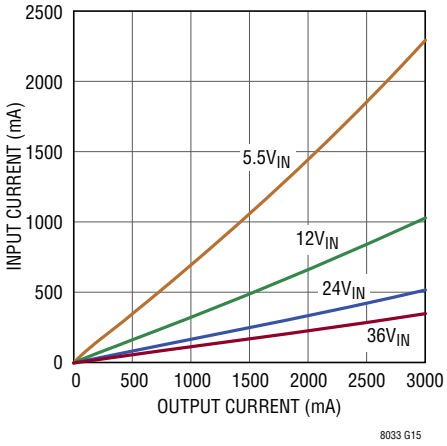
Input Current vs Input Voltage Output Shorted



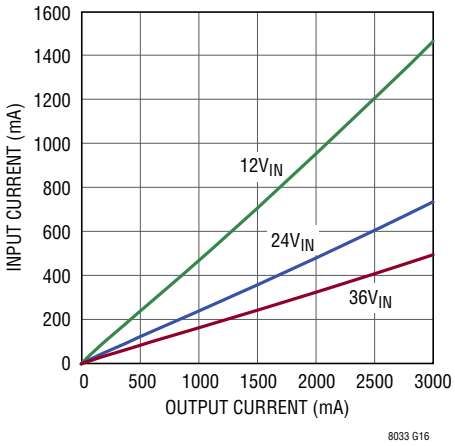
Input Current vs Output Current $2.5V_{OUT}$



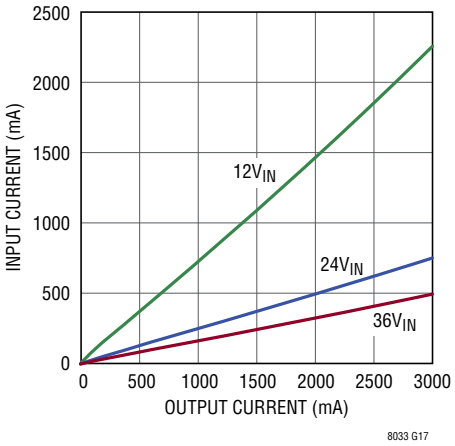
Input Current vs Output Current $3.3V_{OUT}$



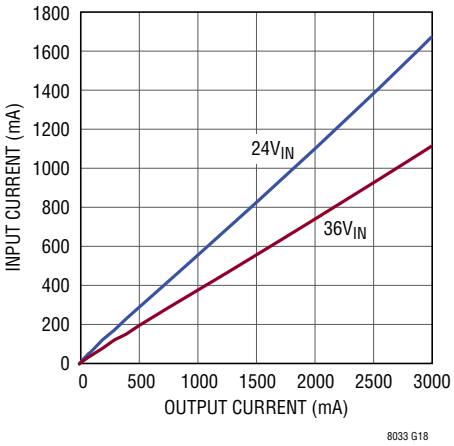
Input Current vs Output Current $5V_{OUT}$



Input Current vs Output Current $8V_{OUT}$

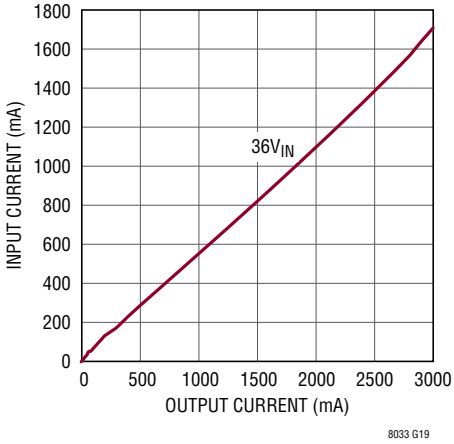


Input Current vs Output Current $12V_{OUT}$

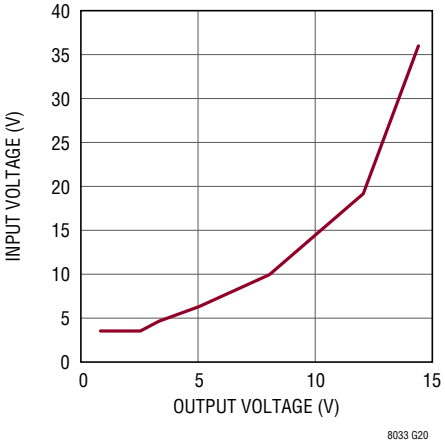


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

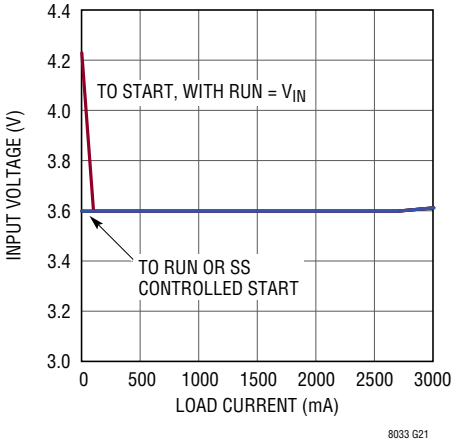
Input Current vs Output Current 18V_{OUT}



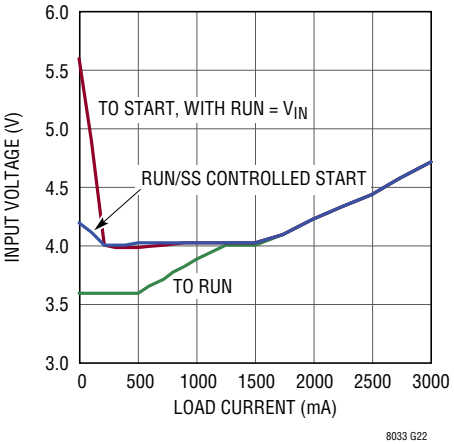
Minimum Required Input Voltage vs Output Voltage, I_{OUT} = 3A



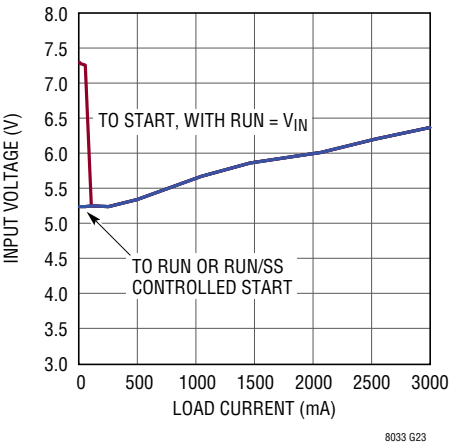
Minimum Required Input Voltage vs Load Current, 2.5V_{OUT}



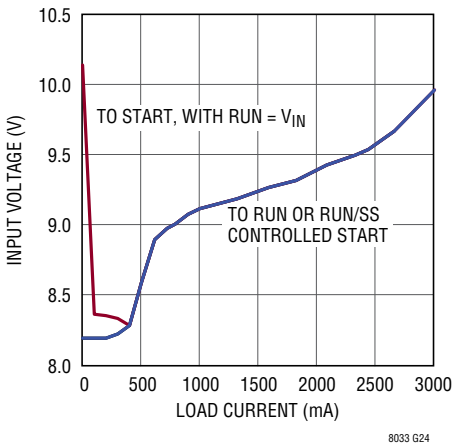
Minimum Required Input Voltage vs Load Current, 3.3V_{OUT}



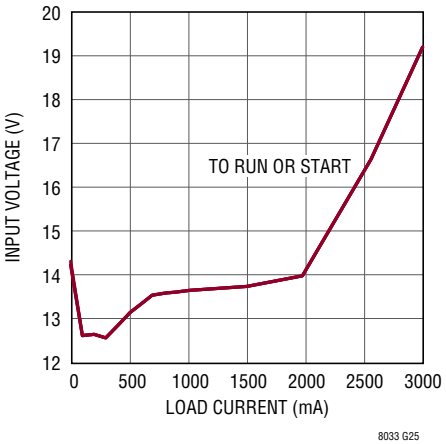
Minimum Required Input Voltage vs Load Current, 5V_{OUT}



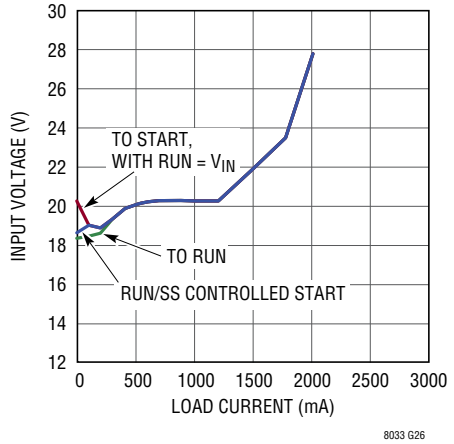
Minimum Required Input Voltage vs Load Current, 8V_{OUT}



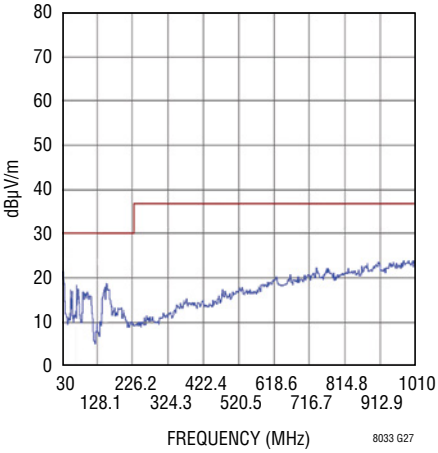
Minimum Required Input Voltage vs Load Current, 12V_{OUT}



Minimum Required Input Voltage vs Load Current, 18V_{OUT}

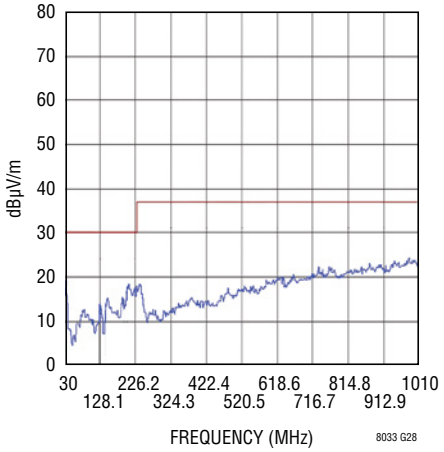


Radiated Emissions, 36V_{IN}, 24V_{OUT} at 1.5A Load

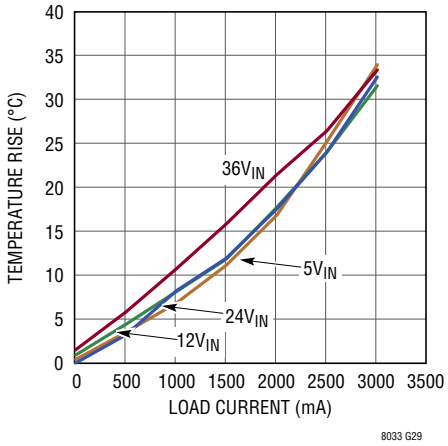


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

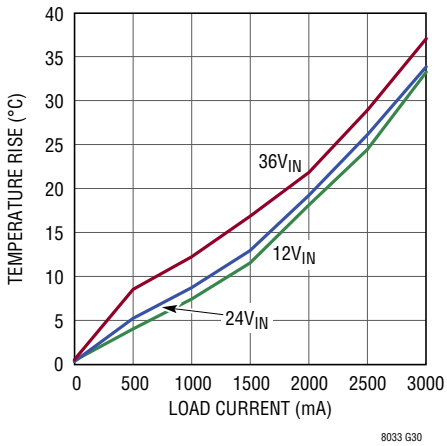
Radiated Emissions, 36V_{IN}, 1.2V_{OUT} at 3A Load



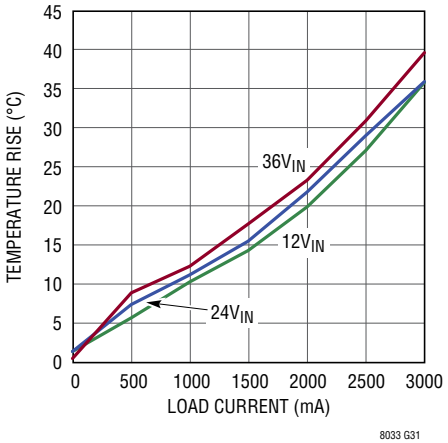
Temperature Rise vs Load Current, 2.5V_{OUT}



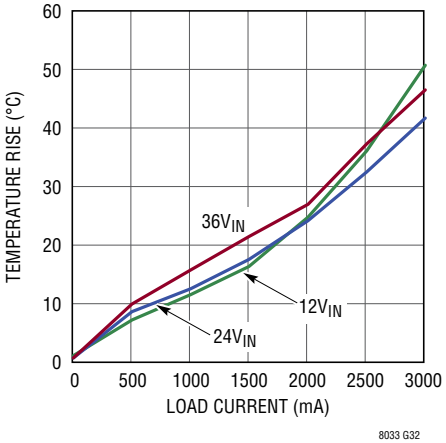
Temperature Rise vs Load Current, 3.3V_{OUT}



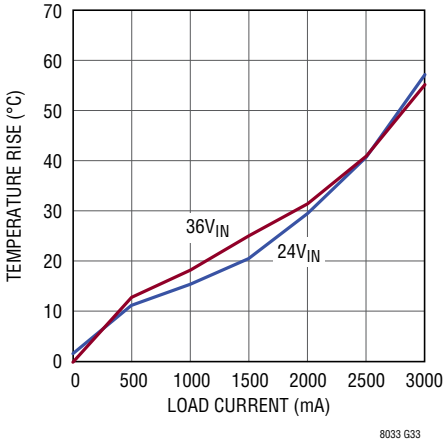
Temperature Rise vs Load Current, 5V_{OUT}



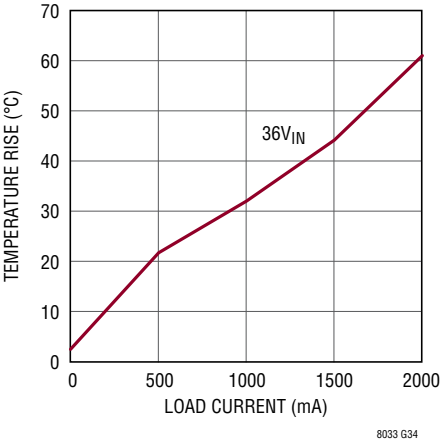
Temperature Rise vs Load Current, 8V_{OUT}



Temperature Rise vs Load Current, 12V_{OUT}



Temperature Rise vs Load Current, 18V_{OUT}



PIN FUNCTIONS

V_{OUT} (Bank 1): Power Output Pins. Apply the output filter capacitor and the output load between these pins and GND pins.

GND (A8, Bank 2): Tie these GND pins to a local ground plane below the LTM8033 and the circuit components. Return the feedback divider (R_{ADJ}) to this net.

FIN (Bank 3): Filtered Input. This is the node after the input EMI filter. Apply the capacitor recommended by Table 1. Additional capacitance may be applied if there is a need to modify the behavior of the integrated EMI filter; otherwise, leave these pins unconnected. See the Applications Information section for more details.

V_{IN} (Bank 4): The V_{IN} pin supplies current to the LTM8033's internal regulator and to the internal power switch. This pin must be locally bypassed with an external, low ESR capacitor; see Table 1 for recommended values. Ensure that V_{IN} + BIAS is less than 56V.

SHARE (Pin A6): Tie this to the SHARE pin of another LTM8033 when paralleling the outputs. Otherwise, do not connect.

ADJ (Pin A7): The LTM8033 regulates its ADJ pin to 0.79V. Connect the adjust resistor from this pin to ground. The value of R_{ADJ} is given by the equation $R_{ADJ} = 394.21/(V_{OUT} – 0.79)$, where R_{ADJ} is in kΩ.

RT (Pin B6): The RT pin is used to program the switching frequency of the LTM8033 by connecting a resistor from this pin to ground. The Applications Information section of the data sheet includes a table to determine the resistance value based on the desired switching frequency. Minimize capacitance at this pin.

SYNC (Pin B8): This is the external clock synchronization input. Ground this pin for low ripple Burst Mode® operation at low output loads. Tie to a stable voltage source greater than 0.7V to disable Burst Mode operation. Do not leave this pin floating. Tie to a clock source for synchronization. Clock edges should have rise and fall times faster than 1µs. See the Synchronization section in the Applications Information section.

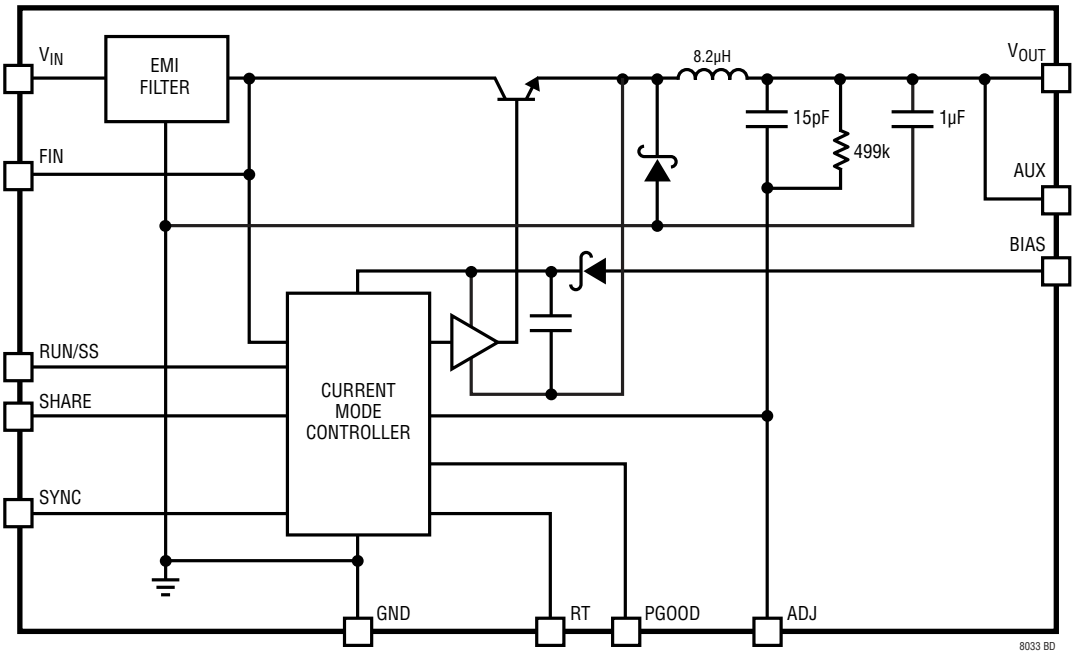
PGOOD (Pin B7): The PGOOD pin is the open-collector output of an internal comparator. PGOOD remains low until the ADJ pin is greater than 90% of the final regulation voltage. PGOOD output is valid when V_{IN} is above 3.6V and RUN/SS is high. If this function is not used, leave this pin floating.

AUX (Pin G3): Low Current Voltage Source for BIAS. In many designs, the BIAS pin is simply connected to V_{OUT}. The AUX pin is internally connected to V_{OUT} and is placed adjacent to the BIAS pin to ease printed circuit board routing. Although this pin is internally connected to V_{OUT}, it is not intended to deliver a high current, so do **not** connect this pin to the load. If this pin is not tied to BIAS, leave it floating.

BIAS (Pin G4): The BIAS pin connects to the internal power bus. Connect to a power source greater than 2.8V and less than 25V. If the output is greater than 2.8V, connect this pin there. If the output voltage is less, connect this to a voltage source between 2.8V and 25V but ensure that V_{IN} + BIAS is less than 56V.

RUN/SS (Pin G8): Pull the RUN/SS pin below 0.2V to shut down the LTM8033. Tie to 2.5V or more for normal operation. If the shutdown feature is not used, tie this pin to the V_{IN} pin. RUN/SS also provides a soft-start function; see the Applications Information section.

BLOCK DIAGRAM



OPERATION

The LTM8033 is a standalone nonisolated step-down switching DC/DC power supply that can deliver up to 3A of output current. It is an EMC product; its radiated emissions are so quiet that it can pass the stringent requirements of EN55022 class B as a stand alone product. This µModule provides a precisely regulated output voltage programmable via one external resistor from 0.8V to 24V. The input voltage range is 3.6V to 36V. Given that the LTM8033 is a step-down converter, make sure that the input voltage is high enough to support the desired output voltage and load current.

As shown in the Block Diagram, the LTM8033 contains an EMI filter, current mode controller, power switching element, power inductor, power Schottky diode and a modest amount of input and output capacitance. The LTM8033 is a fixed frequency PWM regulator. The switching frequency is set by simply connecting the appropriate resistor value from the RT pin to GND.

An internal regulator provides power to the control circuitry. The bias regulator normally draws power from the V_{IN} pin, but if the BIAS pin is connected to an external voltage higher than 2.8V, bias power will be drawn from the external source (typically the regulated output voltage). This improves efficiency. The RUN/SS pin is used to place the LTM8033 in shutdown, disconnecting the output and reducing the input current to less than 1µA.

To further optimize efficiency, the LTM8033 automatically switches to Burst Mode operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down reducing the input supply current to 50µA in a typical application.

The oscillator reduces the LTM8033's operating frequency when the voltage at the ADJ pin is low. This frequency foldback helps to control the output current during start-up and overload.

The LTM8033 contains a power good comparator which trips when the ADJ pin is at roughly 90% of its regulated value. The PGOOD output is an open-collector transistor that is off when the output is in regulation, allowing an external resistor to pull the PGOOD pin high. Power good is valid when the LTM8033 is enabled and V_{IN} is above 3.6V.

The LTM8033 is equipped with a thermal shutdown that will inhibit power switching at high junction temperatures. The activation threshold of this function, however, is above 125°C to avoid interfering with normal operation. Thus, prolonged or repetitive operation under a condition in which the thermal shutdown activates may damage or impair the reliability of the device.

APPLICATIONS INFORMATION

For most applications, the design process is straight forward, summarized as follows:

- Look at Table 1 and find the row that has the desired input range and output voltage.
- Apply the recommended C_{IN}, C_{FIN}, C_{OUT}, R_{ADJ} and R_T values.
- Connect BIAS as indicated.

As the integrated input EMI filter may ring in response to an application of a step input voltage, a bulk capacitance may be applied between FIN and GND. See the Hot-Plugging Safely section for details.

While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions. Bear in mind that the maximum output current is limited by junction temperature, the relationship between the input and output voltage magnitude and polarity and other factors. Please refer to the graphs in the Typical Performance Characteristics section for guidance.

The maximum frequency (and attendant R_T value) at which the LTM8033 should be allowed to switch is given in Table 1 in the f_{MAX} column, while the recommended frequency (and R_T value) for optimal efficiency over the given input condition is given in the $f_{OPTIMAL}$ column. There are additional conditions that must be satisfied if the synchronization function is used. Please refer to the Synchronization section for details.

Note: An input bulk capacitance is required at either V_{IN} or FIN. Refer to the Typical Performance Characteristics section for load conditions.

Capacitor Selection Considerations

The C_{IN}, C_{FIN} and C_{OUT} capacitor values in Table 1 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in Table 1 is not recommended, and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if it is necessary. Again, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

Ceramic capacitors are small, robust and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U have very large temperature and voltage coefficients of capacitance. In an application circuit they may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected.

Ceramic capacitors are also piezoelectric. In Burst Mode operation, the LTM8033's switching frequency depends on the load current, and can excite a ceramic capacitor at audio frequencies, generating audible noise. Since the LTM8033 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear.

If this audible noise is unacceptable, use a high performance electrolytic capacitor at the output. It may also be a parallel combination of a ceramic capacitor and a low cost electrolytic capacitor.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8033. A ceramic input capacitor combined with trace or cable inductance forms a high Q (under damped) tank circuit. If the LTM8033 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation can be easily avoided; see the Hot-Plugging Safely section.

APPLICATIONS INFORMATION

Table 1. Recommended Component Values and Configuration (T_A = 25°C)

V_{IN}	V_{OUT}	C_{IN}	C_{FIN}	C_{OUT}	BIAS	R_{ADJ}	$f_{OPTIMAL}$	$R_{T(OPTIMAL)}$	f_{MAX}	$R_{T(MIN)}$
3.6V to 36V	0.8V	4.7µF, 50V, 1206	10µF, 50V, 1210	4 × 100µF, 6.3V, 1210	2.8V to 25V	30M	230kHz	182k	250kHz	169k
3.6V to 36V	1V	4.7µF, 50V, 1206	10µF, 50V, 1210	4 × 100µF, 6.3V, 1210	2.8V to 25V	1.87M	240kHz	174k	285kHz	147k
3.6V to 36V	1.2V	4.7µF, 50V, 1206	10µF, 50V, 1210	4 × 100µF, 6.3V, 1210	2.8V to 25V	953k	255kHz	162k	315kHz	130k
3.6V to 36V	1.5V	4.7µF, 50V, 1206	10µF, 50V, 1210	4 × 100µF, 6.3V, 1210	2.8V to 25V	549k	270kHz	154k	360kHz	113k
3.6V to 36V	1.8V	4.7µF, 50V, 1206	10µF, 50V, 1210	4 × 100µF, 6.3V, 1210	2.8V to 25V	383k	285kHz	147k	420kHz	95.3k
4.1V to 36V	2.5V	4.7µF, 50V, 1206	10µF, 50V, 1210	3 × 100µF, 6.3V, 1210	2.8V to 25V	226k	345kHz	118k	540kHz	71.5k
5.3V to 36V	3.3V	4.7µF, 50V, 1206	10µF, 50V, 1210	100µF, 6.3V, 1210	AUX	154k	425kHz	93.1k	675kHz	54.9k
7.5V to 36V	5V	4.7µF, 50V, 1206	4.7µF, 50V, 1206	100µF, 6.3V, 1210	AUX	93.1k	500kHz	76.8k	950kHz	36.5k
10.5V to 36V	8V	4.7µF, 50V, 1206	1µF, 50V, 1206	47µF, 16V, 1210	AUX	54.9k	700kHz	52.3k	1.45MHz	20.5k
20V to 36V	12V	2.2µF, 50V, 1206	1µF, 50V, 1206	47µF, 16V, 1210	AUX	34.8k	850kHz	41.2k	2.3MHz	9.09k
25.5V to 36V	18V	2.2µF, 50V, 1206	Open	22µF, 25V, 1812	AUX	22.6k	1.1MHz	29.4k	2.4MHz	8.25k
32.5V to 36V	24V	1µF, 50V, 1206	Open	22µF, 25V, 1812	2.8V to 20V	16.5k	1.2MHz	25.5k	2.4MHz	8.25k
3.6V to 15V	0.8V	4.7µF, 25V, 1206	10µF, 16V, 1210	4 × 100µF, 6.3V, 1210	V_{IN}	30M	230kHz	182k	575kHz	66.5k
3.6V to 15V	1V	4.7µF, 25V, 1206	10µF, 16V, 1210	4 × 100µF, 6.3V, 1210	V_{IN}	1.87M	240kHz	174k	660kHz	56.2k
3.6V to 15V	1.2V	4.7µF, 25V, 1206	10µF, 16V, 1210	4 × 100µF, 6.3V, 1210	V_{IN}	953k	255kHz	162k	760kHz	47.5k
3.6V to 15V	1.5V	4.7µF, 25V, 1206	10µF, 16V, 1210	4 × 100µF, 6.3V, 1210	V_{IN}	549k	270kHz	154k	840kHz	42.2k
3.6V to 15V	1.8V	4.7µF, 25V, 1206	10µF, 16V, 1210	4 × 100µF, 6.3V, 1210	V_{IN}	383k	285kHz	147k	1.0MHz	34.0k
4.1V to 15V	2.5V	4.7µF, 16V, 1206	10µF, 16V, 1210	3 x 100µF, 6.3V, 1210	V_{IN}	226k	345kHz	118k	1.3MHz	23.7k
5.3V to 15V	3.3V	4.7µF, 16V, 1206	10µF, 16V, 1210	100µF, 6.3V, 1210	AUX	154k	425kHz	93.1k	1.6MHz	17.8k
7.5V to 15V	5V	4.7µF, 16V, 1206	4.7µF, 50V, 1206	100µF, 6.3V, 1210	AUX	93.1k	500kHz	76.8k	2.4MHz	8.25k
10.5V to 15V	8V	2.2µF, 25V, 1206	Open	47µF, 16V, 1210	AUX	54.9k	700kHz	52.3k	2.4MHz	8.25k
9V to 24V	0.8V	4.7µF, 25V, 1206	4.7µF, 25V, 1206	4 × 100µF, 6.3V, 1210	V_{IN}	30M	270kHz	154k	360kHz	113k
9V to 24V	1V	4.7µF, 25V, 1206	4.7µF, 25V, 1206	4 × 100µF, 6.3V, 1210	V_{IN}	1.87M	285kHz	147k	410kHz	97.6k
9V to 24V	1.2V	4.7µF, 25V, 1206	4.7µF, 25V, 1206	4 × 100µF, 6.3V, 1210	V_{IN}	953k	295kHz	140k	475kHz	82.5k
9V to 24V	1.5V	4.7µF, 25V, 1206	4.7µF, 25V, 1206	4 × 100µF, 6.3V, 1210	V_{IN}	549k	310kHz	133k	550kHz	69.8k
9V to 24V	1.8V	4.7µF, 25V, 1206	4.7µF, 25V, 1206	3 × 100µF, 6.3V, 1210	V_{IN}	383k	330kHz	124k	620kHz	60.4k
9V to 24V	2.5V	4.7µF, 25V, 1206	4.7µF, 25V, 1206	2 × 100µF, 6.3V, 1210	V_{IN}	226k	345kHz	118k	800kHz	44.2k
9V to 24V	3.3V	4.7µF, 25V, 1206	4.7µF, 25V, 1206	100µF, 6.3V, 1210	AUX	154k	425kHz	93.1k	1.0MHz	34.0k
9V to 24V	5V	4.7µF, 25V, 1206	4.7µF, 25V, 1206	100µF, 6.3V, 1210	AUX	93.1k	500kHz	76.8k	1.4MHz	21.5k
10.5V to 24V	8V	2.2µF, 25V, 1206	1µF, 25V, 1206	47µF, 16V, 1210	AUX	54.9k	700kHz	52.3k	2.2MHz	9.76k
20V to 24V	12V	2.2µF, 25V, 1206	1µF, 25V, 1206	47µF, 16V, 1210	AUX	34.8k	850kHz	41.2k	2.3MHz	9.09k
18V to 36V	0.8V	1µF, 50V, 1206	2.2µF, 50V, 1206	4 × 100µF, 6.3V, 1210	2.8V to 25V	30M	230kHz	182k	250kHz	169k
18V to 36V	1V	1µF, 50V, 1206	2.2µF, 50V, 1206	4 × 100µF, 6.3V, 1210	2.8V to 25V	1.87M	240kHz	174k	285kHz	147k
18V to 36V	1.2V	1µF, 50V, 1206	2.2µF, 50V, 1206	4 × 100µF, 6.3V, 1210	2.8V to 25V	953k	255kHz	162k	315kHz	130k
18V to 36V	1.5V	1µF, 50V, 1206	2.2µF, 50V, 1206	4 × 100µF, 6.3V, 1210	2.8V to 25V	549k	270kHz	154k	360kHz	113k
18V to 36V	1.8V	1µF, 50V, 1206	2.2µF, 50V, 1206	3 × 100µF, 6.3V, 1210	2.8V to 25V	383k	285kHz	147k	420kHz	95.3k
18V to 36V	2.5V	1µF, 50V, 1206	2.2µF, 50V, 1206	2 × 100µF, 6.3V, 1210	2.8V to 25V	226k	345kHz	118k	540kHz	71.5k
18V to 36V	3.3V	1µF, 50V, 1206	2.2µF, 50V, 1206	100µF, 6.3V, 1210	AUX	154k	425kHz	93.1k	675kHz	54.9k
18V to 36V	5V	1µF, 50V, 1206	1µF, 50V, 1206	47µF, 10V, 1210	AUX	93.1k	500kHz	76.8k	950kHz	36.5k
18V to 36V	8V	2.2µF, 50V, 1206	1µF, 50V, 1206	47µF, 16V, 1210	AUX	54.9k	700kHz	52.3k	1.45MHz	20.5k

Note: A bulk capacitor is required. Do not allow V_{IN} + BIAS above 56V.

APPLICATIONS INFORMATION

Frequency Selection

The LTM8033 uses a constant frequency PWM architecture that can be programmed to switch from 200kHz to 2.4MHz by using a resistor tied from the RT pin to ground. Table 2 provides a list of R_T resistor values and their resulting frequencies.

Table 2. Switching Frequency vs R_T Value

SWITCHING FREQUENCY (MHz)	R_T VALUE (kΩ)
0.2	215
0.3	137
0.4	100
0.5	76.8
0.6	63.4
0.7	52.3
0.8	44.2
0.9	38.3
1	34
1.2	25.5
1.4	21.5
1.6	17.8
1.8	14.7
2	12.1
2.2	9.76
2.4	8.25

Operating Frequency Trade-Offs

It is recommended that the user apply the optimal R_T value given in Table 1 for the input and output operating condition. System level or other considerations, however, may necessitate another operating frequency. While the LTM8033 is flexible enough to accommodate a wide range of operating frequencies, a haphazardly chosen one may result in undesirable operation under certain operating or fault conditions. A frequency that is too high can reduce efficiency, generate excessive heat or even damage the LTM8033 if the output is overloaded or short-circuited. A frequency that is too low can result in a final design that has too much output ripple or too large of an output capacitor.

BIAS Pin Considerations

The BIAS pin is used to provide drive power for the internal power switching stage and operate other internal circuitry. For proper operation, it must be powered by at least 2.8V. If the output voltage is programmed to 2.8V or higher, BIAS may be simply tied to V_{OUT}. If V_{OUT} is less than 2.8V, BIAS can be tied to V_{IN} or some other voltage source. If the BIAS pin voltage is too high, the efficiency of the LTM8033 may suffer. The optimum BIAS voltage is dependent upon many factors, such as load current, input voltage, output voltage and switching frequency, but 4V to 5V works well in many applications. In all cases, ensure that the maximum voltage at the BIAS pin is less than 25V and that the sum of V_{IN} and BIAS is less than 56V. If BIAS power is applied from a remote or noisy voltage source, it may be necessary to apply a decoupling capacitor locally to the pin.

Load Sharing

Two or more LTM8033 may be paralleled to produce higher currents. To do this, tie the V_{IN}, ADJ, V_{OUT} and SHARE pins of all the paralleled LTM8033 together. To ensure that paralleled modules start up together, the RUN/SS pins may be tied together as well. If the RUN/SS pins are not tied together, make sure that the same valued soft-start capacitors are used for each module. Current sharing can be improved by synchronizing the LTM8033s. An example of two LTM8033 configured for load sharing is given in the Typical Applications section.

Burst Mode Operation

To enhance efficiency at light loads, the LTM8033 automatically switches to Burst Mode operation which keeps the output capacitor charged to the proper voltage while minimizing the input quiescent current. During Burst Mode operation, the LTM8033 delivers single cycle bursts of current to the output capacitor followed by sleep periods where the output power is delivered to the load by the output capacitor. In addition, V_{IN} and BIAS quiescent currents are reduced to typically 30µA and 75µA respectively during the sleep time. As the load current decreases towards a

APPLICATIONS INFORMATION

no-load condition, the percentage of time that the LTM8033 operates in sleep mode increases and the average input current is greatly reduced, resulting in higher efficiency.

Burst Mode operation is enabled by tying SYNC to GND. To disable Burst Mode operation, tie SYNC to a stable voltage above 0.7V. Do not leave the SYNC pin floating.

Minimum Input Voltage

The LTM8033 is a step-down converter, so a minimum amount of headroom is required to keep the output in regulation. In addition, the input voltage required to turn on is higher than that required to run, and depends upon BIAS power whether RUN/SS is used. If BIAS is available before V_{OUT} ramps up, the minimum V_{IN} voltage to start may be reduced. As shown in the Typical Performance Characteristics section, the minimum input voltage to run a 3.3V output at light load is only about 3.6V, but, if RUN/SS is pulled up to V_{IN}, it takes 5.6V_{IN} to start. If the LTM8033 is enabled with the RUN/SS pin, the minimum voltage to start at light loads is lower, about 4.2V. Similar curves detailing this behavior of the LTM8033 for other outputs are also included in the Typical Performance Characteristics section.

Soft-Start

The RUN/SS pin can be used to soft-start the LTM8033, reducing the maximum input current during start-up. The RUN/SS pin is driven through an external RC filter to create a voltage ramp at this pin. Figure 2 shows the start-up and shutdown waveforms with the soft-start circuit. By choosing an appropriate RC time constant, the peak start-up current can be reduced to the current that is required to regulate the output, with no overshoot. Choose the value of the resistor so that it can supply at least 20µA when the RUN/SS pin reaches 2.5V.

Frequency Foldback

The LTM8033 is equipped with frequency foldback which acts to reduce the thermal and energy stress on the internal power elements during a short-circuit or output overload condition. If the LTM8033 detects that the output has fallen out of regulation, the switching frequency is reduced as a function of how far the output is below the target voltage. This in turn limits the amount of energy that can be delivered to the load under fault. During the start-up time, frequency foldback is also active to limit the energy delivered to the potentially large output capacitance of the load.

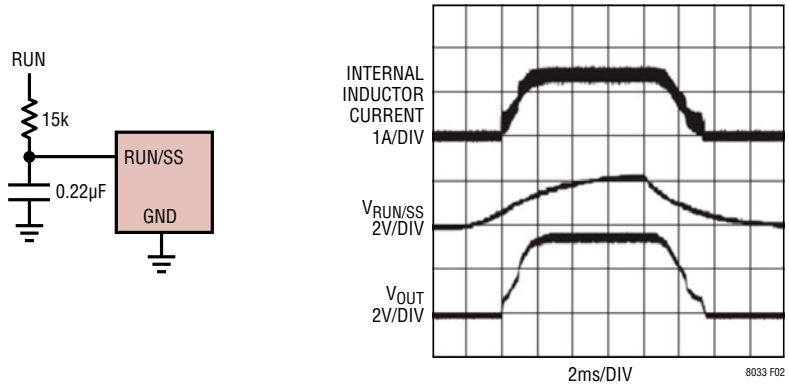


Figure 2. To Soft-Start the LTM8033, Add a Resistor and Capacitor to the RUN/SS Pin

APPLICATIONS INFORMATION

Synchronization

The internal oscillator of the LTM8033 can be synchronized by applying an external 250kHz to 2MHz clock to the SYNC pin. Do not leave this pin floating. Ground the SYNC pin if the synchronization function is not used. When synchronizing the LTM8033, select an R_T resistor value that corresponds to an operating frequency 20% lower than the intended synchronization frequency (see the Frequency Selection section).

In addition to synchronization, the SYNC pin controls Burst Mode behavior. If the SYNC pin is driven by an external clock, or pulled up above 0.7V, the LTM8033 will not enter Burst Mode operation, but will instead skip pulses to maintain regulation instead.

Shorted Input Protection

Care needs to be taken in systems where the output will be held high when the input to the LTM8033 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode OR-ed with the LTM8033's output. If the V_{IN} pin is allowed to float and the RUN/SS pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LTM8033's internal circuitry will pull its quiescent current through its internal power switch. This is fine if your system can tolerate a few milliamps in this state. If you ground the RUN/SS pin, the SW pin current will drop to essentially zero. However, if the V_{IN} pin is grounded while the output is held high, then parasitic diodes inside the LTM8033 can pull large currents from the output through the V_{IN} pin. Figure 3 shows a circuit that will run only when the input voltage is present and that protects against a shorted or reversed input.

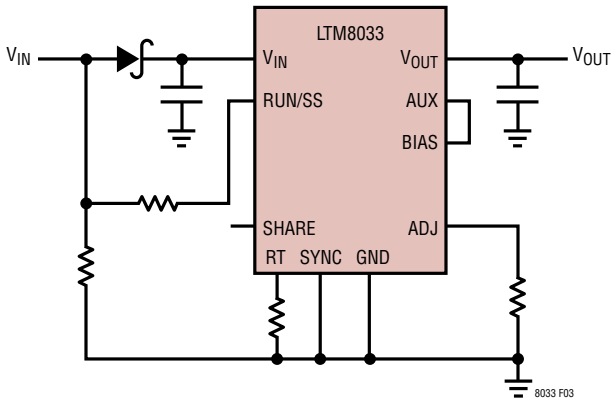


Figure 3. The Input Diode Prevents a Shorted Input from Discharging a Backup Battery Tied to the Output. It Also Protects the Circuit from a Reversed Input. The LTM8033 Runs Only When the Input is Present

APPLICATIONS INFORMATION

PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8033. The LTM8033 is nevertheless a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 4 for a suggested layout. Ensure that the grounding and heat sinking are acceptable.

A few rules to keep in mind are:

1. Place the R_{ADJ} and R_T resistors as close as possible to their respective pins.
2. Place the C_{IN} and C_{FIN} capacitors as close as possible to the V_{IN}, FIN and GND connections of the LTM8033. A haphazardly placed C_{FIN} capacitor may impair EMI performance.
3. Place the C_{OUT} capacitors as close as possible to the V_{OUT} and GND connection of the LTM8033.
4. Place the C_{IN}, C_{FIN} and C_{OUT} capacitors such that their ground currents flow directly adjacent or underneath the LTM8033.
5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8033.
6. Use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in Figure 4. The LTM8033 can benefit from the heat sinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

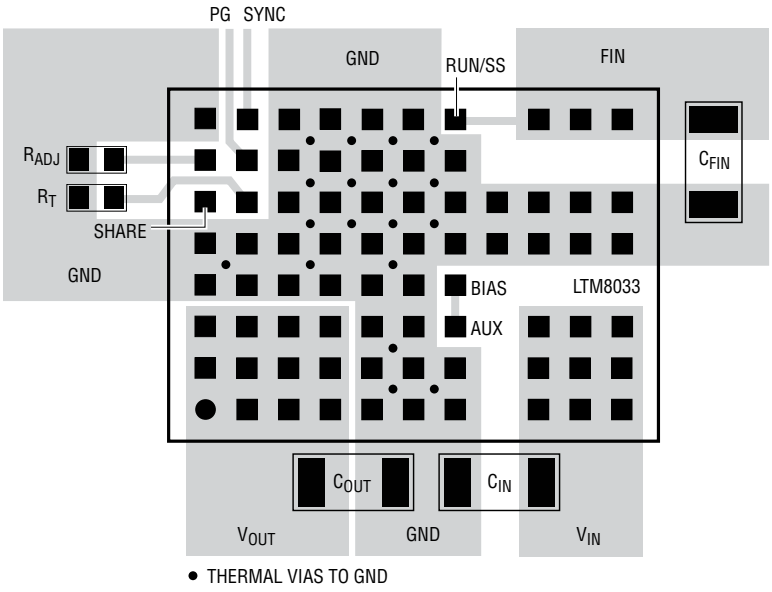


Figure 4. Layout Showing Suggested External Components, GND Plane and Thermal Vias

APPLICATIONS INFORMATION

Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM8033. However, these capacitors can cause problems if the LTM8033 is plugged into a live supply (see Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pin of the LTM8033 can ring to more than twice the nominal input voltage, possibly exceeding the LTM8033's rating and damaging the part. A similar phenomenon can occur inside the LTM8033 module, at the output of the integrated EMI filter (FIN), with the same potential of damaging the part. If the input supply is poorly controlled or the user will be plugging the LTM8033 into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series to V_{IN}, but the most popular method of controlling input voltage overshoot is adding an electrolytic bulk capacitor to the V_{IN} or FIN net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it can be a large component in the circuit.

Electromagnetic Compliance

The LTM8033 was evaluated by an independent nationally recognized test lab and found to be compliant with EN 55022 class B: 2006 by a wide margin. Sample graphs of the LTM8033's radiated EMC performance are given in the Typical Performance Characteristics section, while further data, operating conditions and test set-up are detailed in the electromagnetic compatibility test report, available on the Linear Technology website. Conducted emissions requirements may be met by adding an appropriate input power line filter. The proper implementation of this filter depends upon the system operating and performance conditions as a whole, of which the LTM8033 is typically only a component, so conducted emissions are not addressed at this level.

Thermal Considerations

The LTM8033 output current may need to be derated if it is required to operate in a high ambient temperature or deliver a large amount of continuous power. The amount of current derating is dependent upon the input voltage, output power and ambient temperature. The temperature rise curves given in the Typical Performance Characteristics section can be used as a guide. These curves were generated by an LTM8033 mounted to a 40cm^2 4-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

The thermal resistance numbers listed in the Pin Configuration are based on modeling the µModule package mounted on a test board specified per JESD51-9 "Test Boards for Area Array Surface Mount Package Thermal Measurements." The thermal coefficients provided in this page are based on JESD 51-12 "Guidelines for Reporting and Using Electronic Package Thermal Information."

For increased accuracy and fidelity to the actual application, many designers use FEA to predict thermal performance. To that end, the Pin Configuration typically gives four thermal coefficients:

- θ_{JA} – Thermal resistance from junction to ambient.
- $\theta_{JCBOTTOM}$ – Thermal resistance from junction to the bottom of the product case.
- θ_{JCTOP} – Thermal resistance from junction to top of the product case.
- θ_{JB} – Thermal resistance from junction to the printed circuit board.

APPLICATIONS INFORMATION

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD 51-12, and are quoted or paraphrased in the following:

- θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.
- $\theta_{JCBOTTOM}$ is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModule, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.
- θ_{JCTOP} is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCBOTTOM}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.
- θ_{JB} is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule and into the board, and is really the sum of the $\theta_{JCBOTTOM}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD 51-9.

The most appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all of the thermal resistances simultaneously. None of them can be individually used to accurately predict the thermal performance of the product, so it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature versus load graphs given in the LTM8033 data sheet.

A graphical representation of these thermal resistances is given in Figure 5.

The blue resistances are contained within the µModule, and the green are outside.

The die temperature of the LTM8033 must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8033. The bulk of the heat flow out of the LTM8033 is through the bottom of the module and the LGA pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please

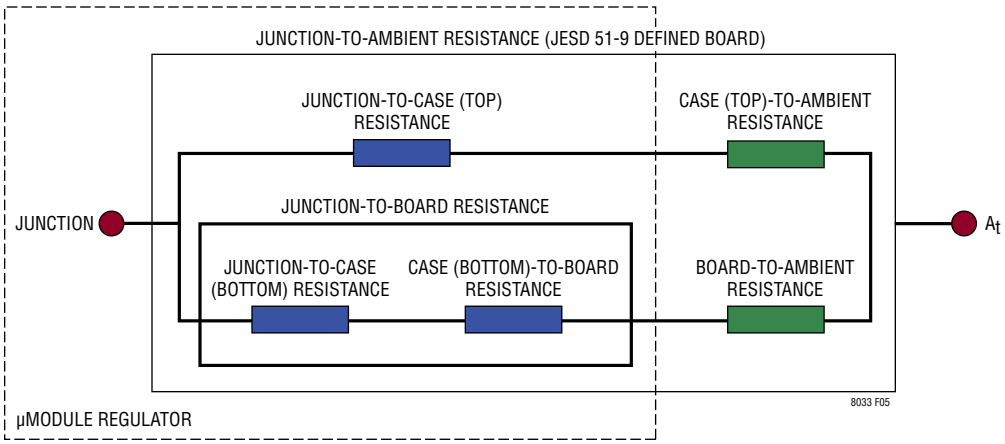


Figure 5

APPLICATIONS INFORMATION

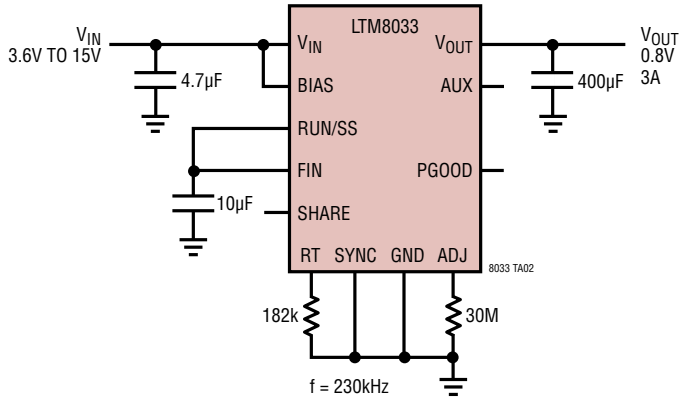
refer to the PCB Layout section for printed circuit board design suggestions.

The LTM8033 is equipped with a thermal shutdown that will inhibit power switching at high junction temperatures. The activation threshold of this function, however, is above 125°C to avoid interfering with normal operation. Thus, it follows that prolonged or repetitive operation under a condition in which the thermal shutdown activates necessarily means that the internal components are subjected to temperatures above the 125°C rating for prolonged or repetitive intervals, which may damage or impair the reliability of the device.

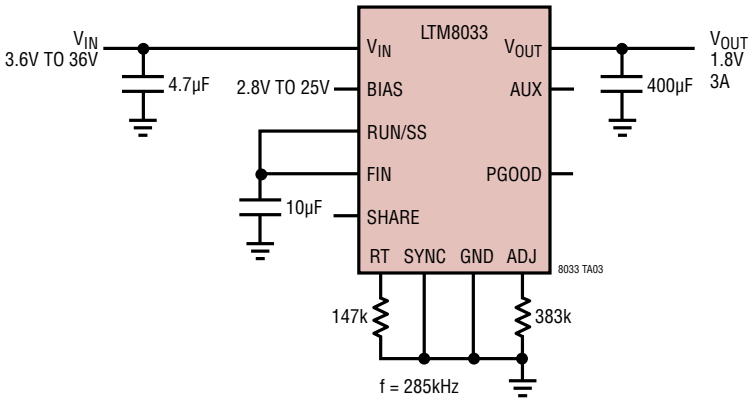
Finally, be aware that at high ambient temperatures the internal Schottky diode will have significant leakage current (see the Typical Performance Characteristics section) increasing the quiescent current of the LTM8033.

TYPICAL APPLICATIONS

0.8V Step-Down Converter



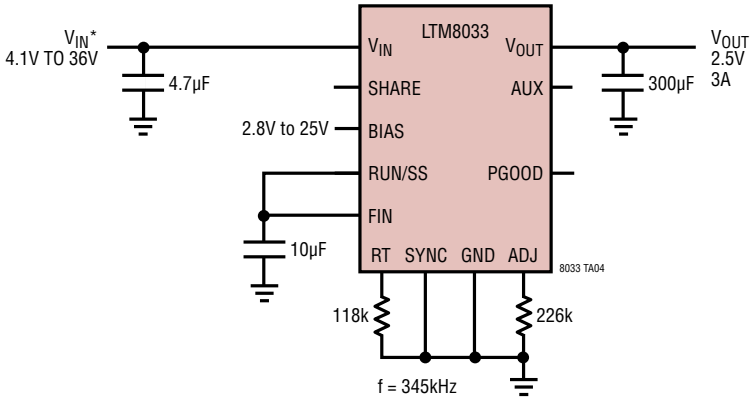
1.8V Step-Down Converter



NOTE: DO NOT ALLOW V_{IN} + BIAS TO BE GREATER THAN 56V.

TYPICAL APPLICATIONS

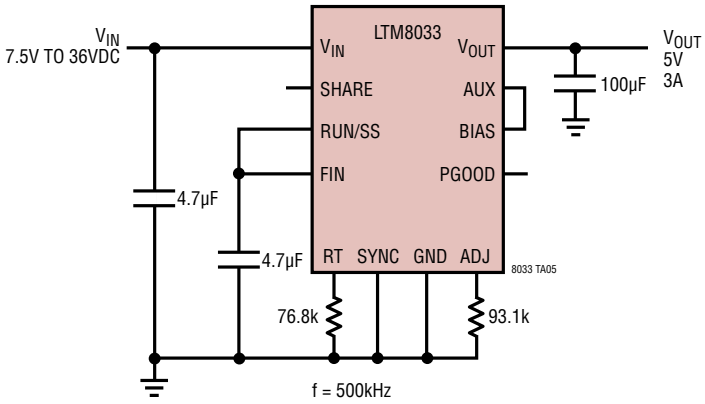
2.5V Step-Down Converter



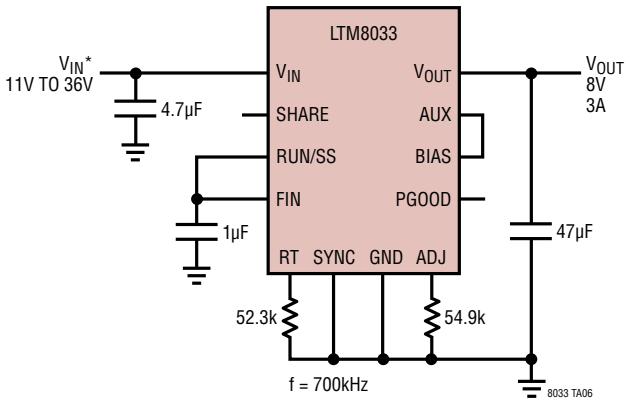
NOTE: DO NOT ALLOW V_{IN} + BIAS TO BE GREATER THAN 56V.

* RUNNING VOLTAGE RANGE. PLEASE REFER TO THE APPLICATIONS INFORMATION SECTION FOR START-UP DETAILS.

5V Step-Down Converter



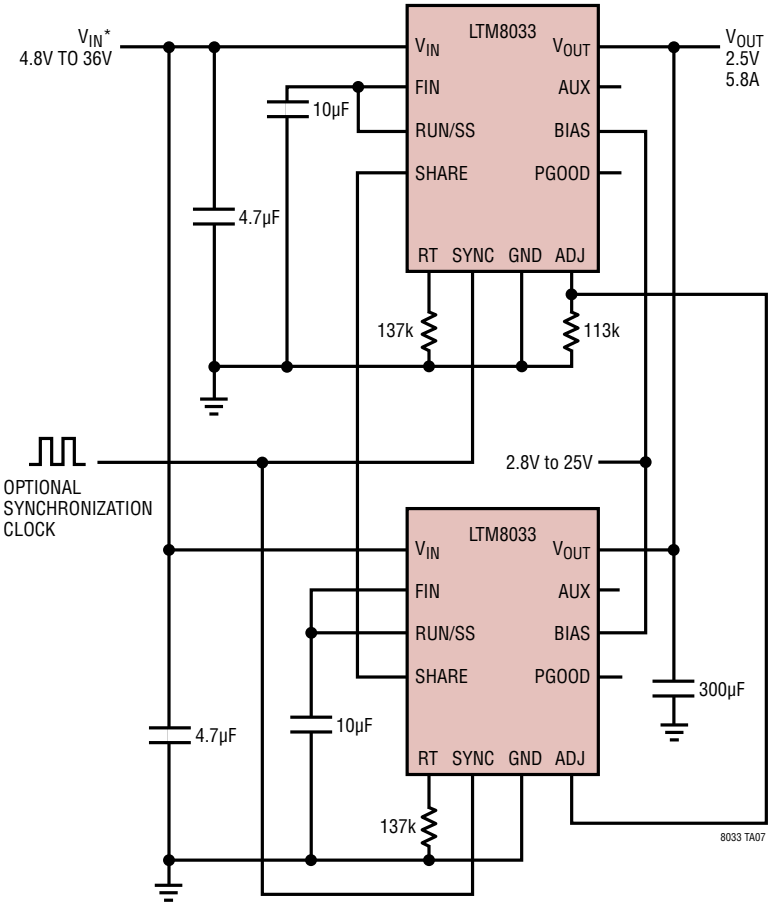
8V Step-Down Converter



* RUNNING VOLTAGE RANGE. PLEASE REFER TO THE APPLICATIONS INFORMATION SECTION FOR START-UP DETAILS.

TYPICAL APPLICATIONS

Current Sharing Two LTM8033 Parts



* RUNNING VOLTAGE RANGE. PLEASE REFER TO THE APPLICATIONS INFORMATION SECTION FOR START-UP DETAILS.

NOTE: SYNCHRONIZE THE TWO MODULES TO AVOID BEAT FREQUENCIES, IF NECESSARY. OTHERWISE, TIE EACH SYNC TO GND.

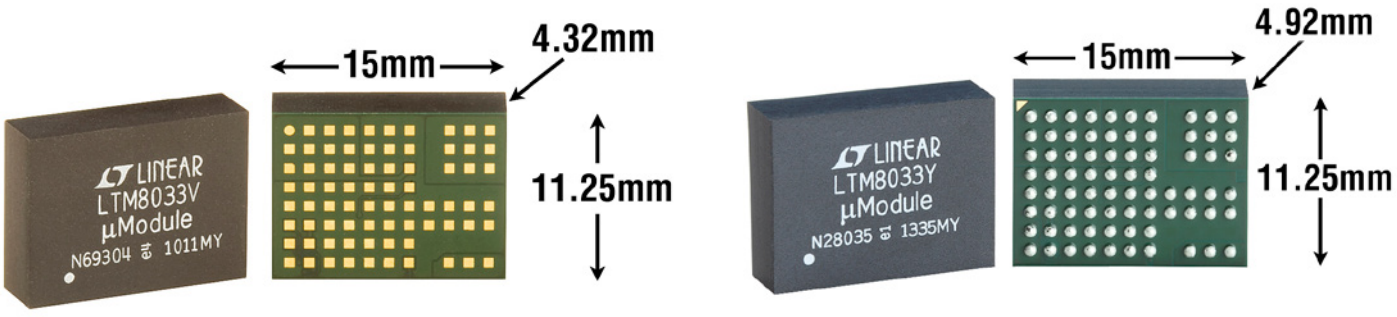
PACKAGE DESCRIPTION

Pin Assignment Table
(Arranged by Pin Number)

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A1	V_{OUT}	B1	V_{OUT}	C1	V_{OUT}	D1	V_{OUT}	E1	GND	F1	GND
A2	V_{OUT}	B2	V_{OUT}	C2	V_{OUT}	D2	V_{OUT}	E2	GND	F2	GND
A3	V_{OUT}	B3	V_{OUT}	C3	V_{OUT}	D3	V_{OUT}	E3	GND	F3	GND
A4	GND	B4	GND	C4	GND	D4	GND	E4	GND	F4	GND
A5	GND	B5	GND	C5	GND	D5	GND	E5	GND	F5	GND
A6	SHARE	B6	RT	C6	GND	D6	GND	E6	GND	F6	GND
A7	ADJ	B7	PGOOD	C7	GND	D7	GND	E7	GND	F7	GND
A8	GND	B8	SYNC	C8	GND	D8	GND	E8	GND	F8	GND

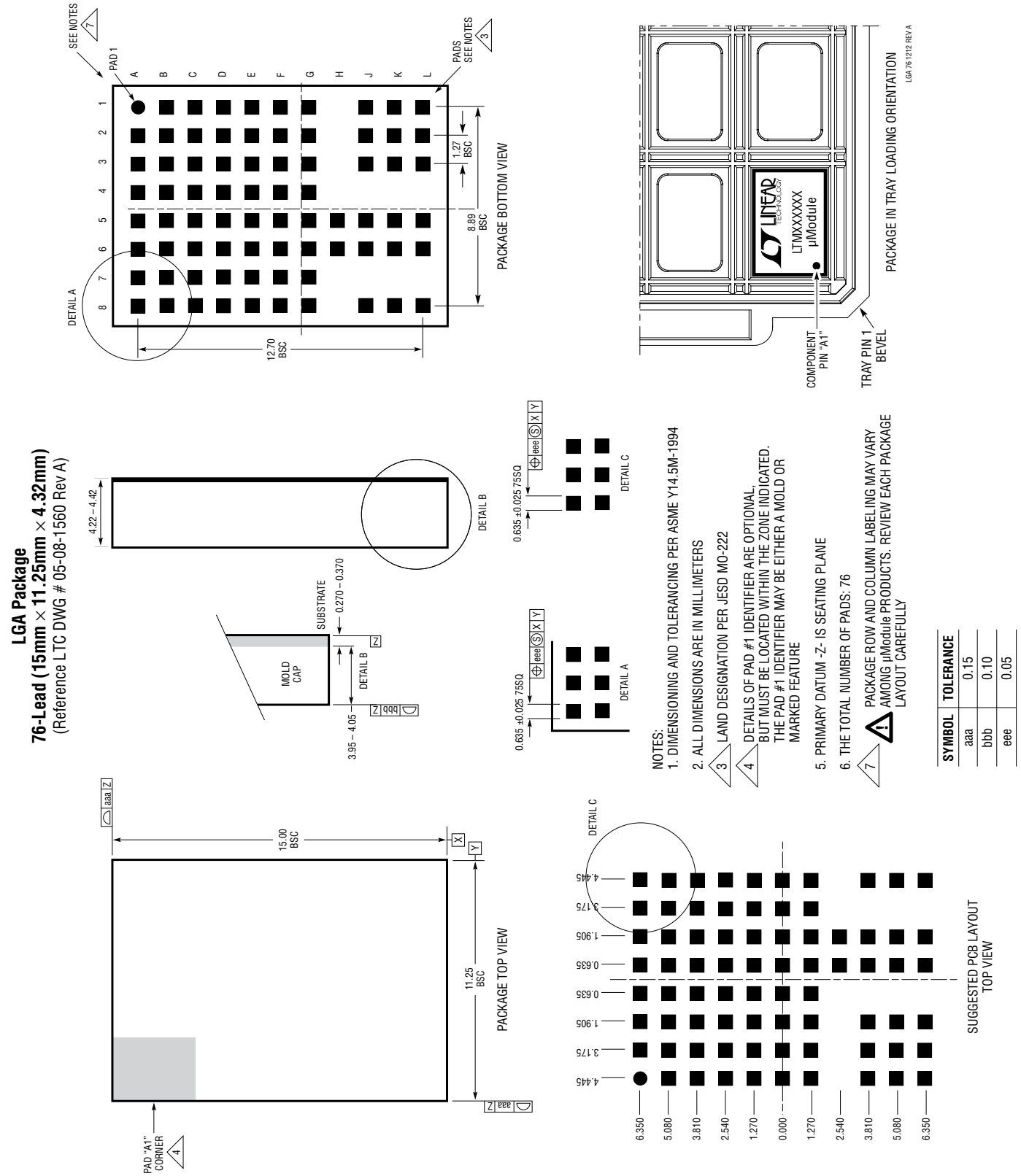
PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
G1	GND			J1	V_{IN}	K1	V_{IN}	L1	V_{IN}
G2	GND			J2	V_{IN}	K2	V_{IN}	L2	V_{IN}
G3	AUX			J3	V_{IN}	K3	V_{IN}	L3	V_{IN}
G4	BIAS								
G5	GND	H5	GND	J5	GND	K5	GND	L5	GND
G6	GND	H6	GND	J6	GND	K6	GND	L6	GND
G7	GND								
G8	RUN			J8	FIN	K8	FIN	L8	FIN

PACKAGE PHOTOGRAPHS



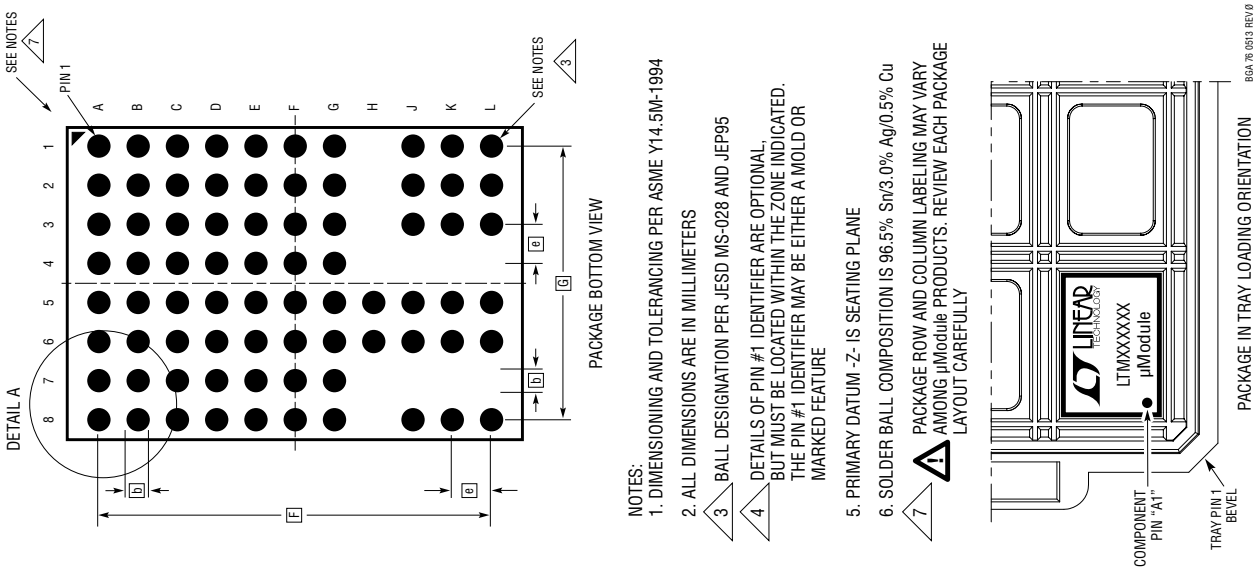
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

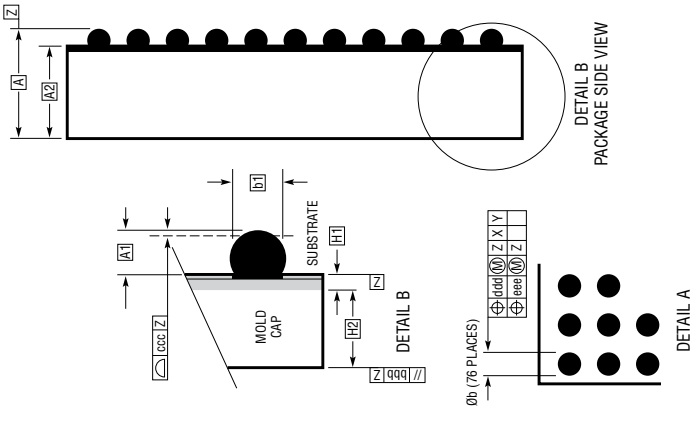


PACKAGE DESCRIPTION

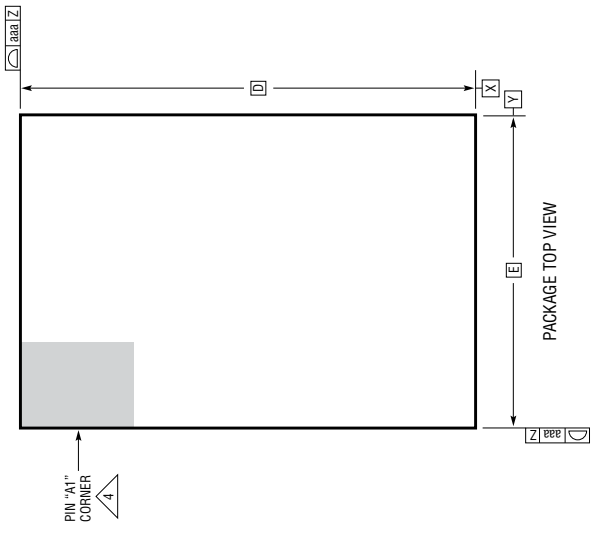
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

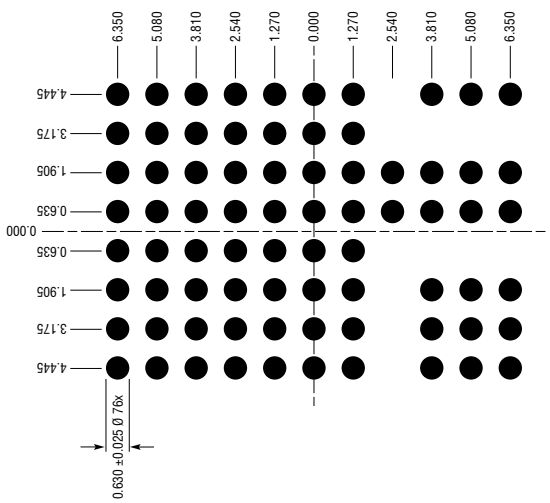


BGA Package
76-Lead (15mm × 11.25mm × 4.92mm)
(Reference LTC DWG # 05-08-1952 Rev Ø)



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.72	4.92	5.12	
A1	0.50	0.60	0.70	
A2	4.22	4.32	4.42	
b	0.60	0.75	0.90	
b1	0.60	0.63	0.66	
D		15.00		
E		11.25		
e		1.27		
F		12.70		
G		8.89		
H1	0.27	0.32	0.37	
H2	3.95	4.00	4.05	
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 76				





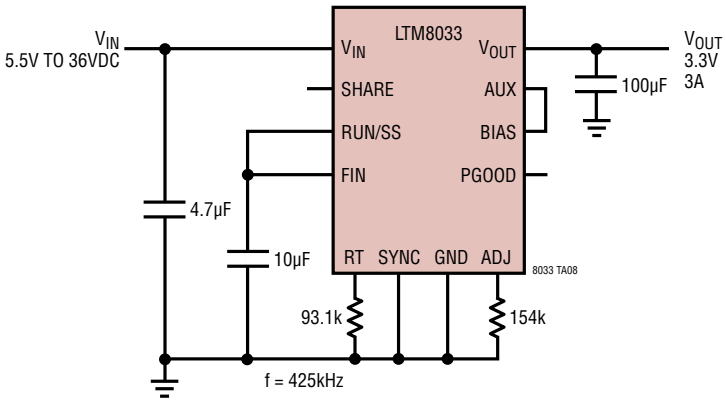
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	04/14	Add BGA package option	1, 2, 22, 24
B	09/14	BGA ball A1 was missing, corrected	2
		Changed quiescent current V_{IN} and BIAS from 20µA and 50µA to 30µA and 75µA, respectively	13

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

3.3V Step-Down Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM8031	Ultralow Noise EMC 1A µModule Regulator	EN55022 Class B Compliant, 3.6V ≤ V_{IN} ≤ 36V; 0.8V ≤ V_{OUT} ≤ 10V, 9mm × 15mm × 2.82mm LGA
LTM8032	Ultralow Noise EMC 2A µModule Regulator	EN55022 Class B Compliant, 3.6V ≤ V_{IN} ≤ 36V; 0.8V ≤ V_{OUT} ≤ 10V 9mm × 15mm × 2.82mm LGA and 9mm × 15mm × 3.42mm BGA
LTM4613	36V_{IN}, 8A EN55022 Class B Certified DC/DC Step-Down µModule Regulator	5V ≤ V_{IN} ≤ 36V, 3.3V ≤ V_{OUT} ≤ 15V, PLL Input, V_{OUT} Tracking and Margining, 15mm × 15mm × 4.32mm LGA
LTM4612	36V_{IN}, 5A EN55022 Class B Certified DC/DC Step-Down µModule Regulator	5V ≤ V_{IN} ≤ 36V, 3.3V ≤ V_{OUT} ≤ 15V, PLL Input, V_{OUT} Tracking and Margining, 15mm × 15mm × 2.82mm LGA
LTM4624	14V_{IN}, 4A Step-Down µModule Regulator in tiny 6.25mm × 6.25mm × 5.01mm BGA	4V ≤ V_{IN} ≤ 14V, 0.6V ≤ V_{OUT} ≤ 5.5V, V_{OUT} Tracking, PGOOD, Light Load Mode, Complete Solution in 1cm^2 (Single-Sided PCB)

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com/LTM8033
LT 0914 REV B • PRINTED IN USA
© LINEAR TECHNOLOGY CORPORATION 2010